

# S71GL-P Based MCPs

**Stacked Multi-Chip Product (MCP)**

**Flash Memory and RAM**

**128 Megabit (8 M x 16-bit) CMOS 3.0 Volt-only**

**Page Mode Flash Memory and**

**64 Megabit (4M x 16-bit) Pseudo Static RAM**

*Data Sheet (Advance Information)*

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# S71GL-P Based MCPs

## Stacked Multi-Chip Product (MCP)

### Flash Memory and RAM

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Page Mode Flash Memory and

64 Megabit (4M x 16-bit) Pseudo Static RAM



*Data Sheet (Advance Information)*

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## Distinctive Characteristics

### MCP Features

- Power supply voltage of 2.7 to 3.1 volt
- High performance
  - 100 ns access time (100 ns Flash, 70 ns pSRAM/SRAM)
  - 25 ns page read times

### ■ Packages

- 8 x 11.6 x 1.2 mm 84 ball FBGA (TLA084)

### ■ Operating Temperature

- –25°C to +85°C

## General Description

The S71GL-P product series consists of S29GL-P Flash memory with pSRAM combinations defined as:

|               |       | Flash Memory Density |
|---------------|-------|----------------------|
|               |       | 128 Mb               |
| pSRAM Density | 64 Mb | S71GL128PC0          |

For detailed specifications, please refer to the individual data sheets.

| Document           | Publication Identification Number (PID) |
|--------------------|-----------------------------------------|
| S29GL-P            | S29GL-P_00                              |
| 64 Mb pSRAM Type 7 | pSRAM_38                                |

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**Publication Number** S71GL-P\_00    **Revision** 03    **Issue Date** February 3, 2009

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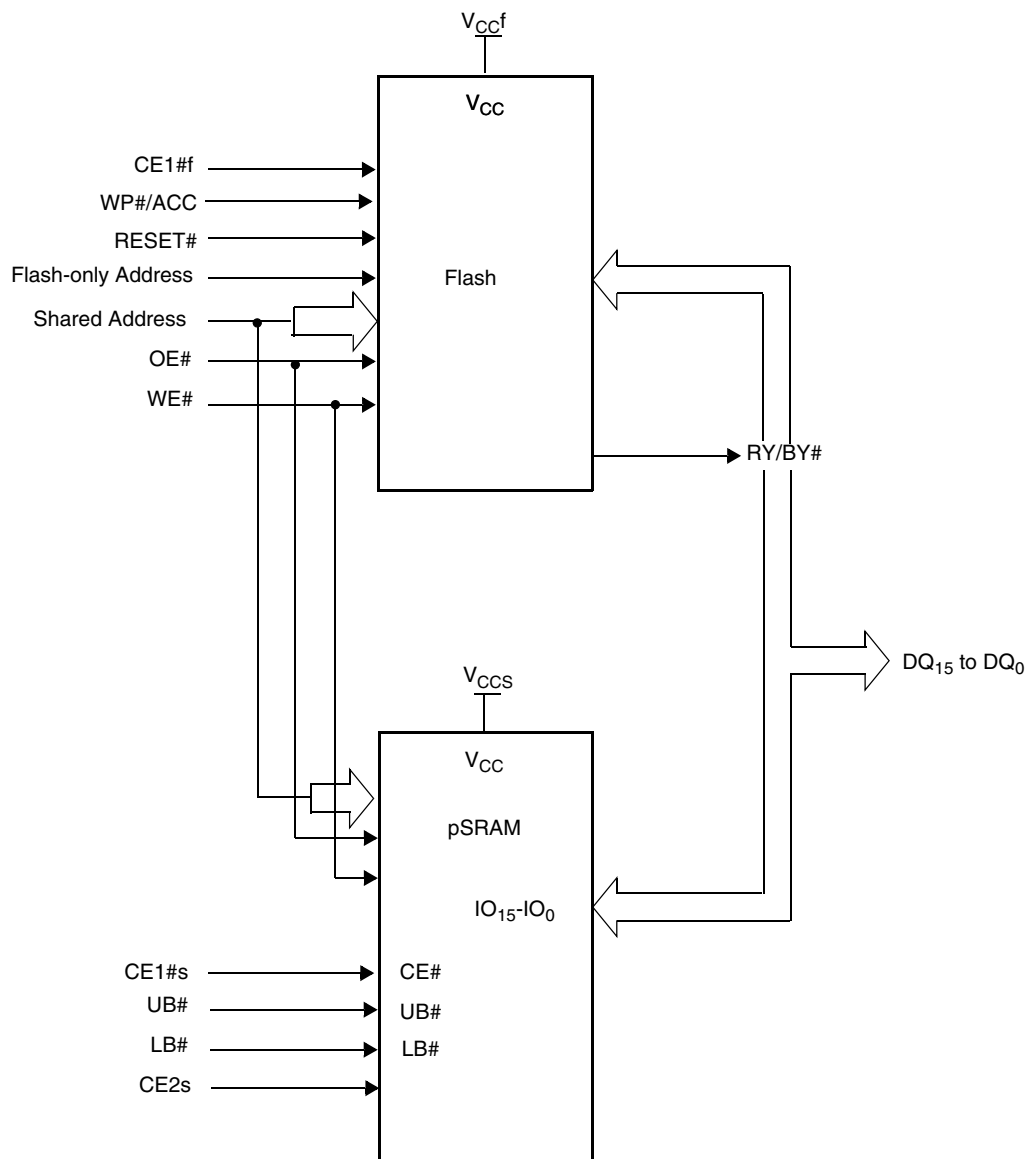
# 1. Product Selector Guide

## 1.1 128 Mb Flash Memory

| Device-Model# (Note) | Flash Access time (ns) | (p)SRAM density | (p)SRAM Access time (ns) | (p)SRAM type | Package | Sector Protect |
|----------------------|------------------------|-----------------|--------------------------|--------------|---------|----------------|
| S71GL128PC0-0Y       | 100                    | 64 Mb           | 70                       | pSRAM 7      | TSB084  | Low            |
| S71GL128PC0-1Y       |                        |                 |                          |              |         | High           |

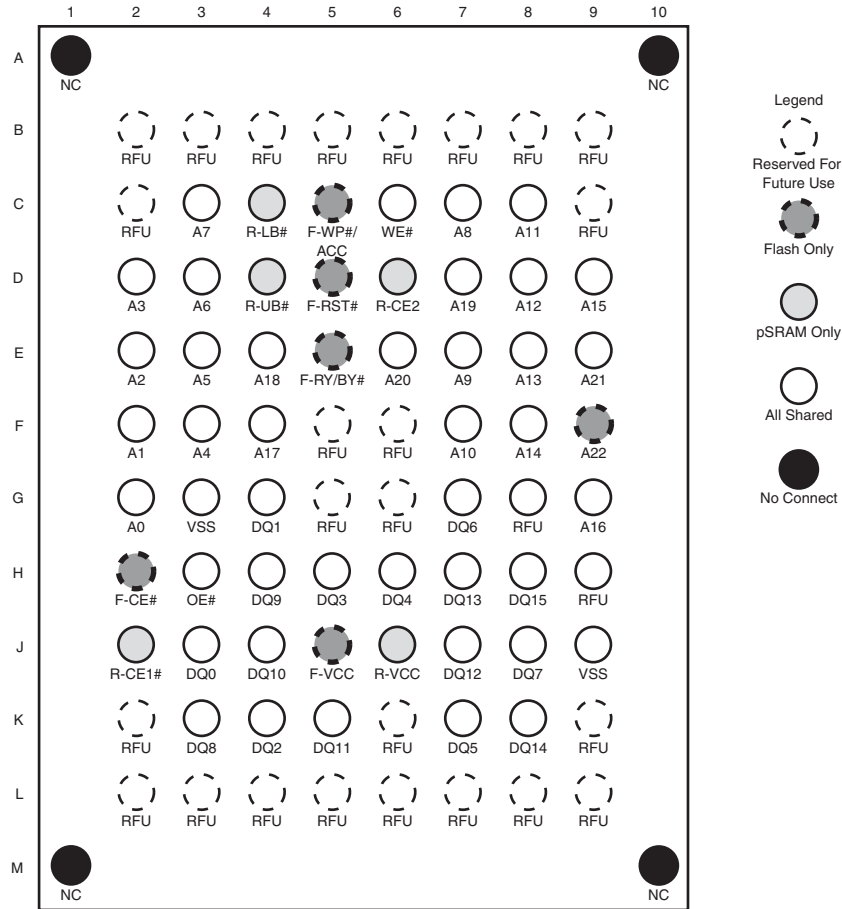
**Note**  
Please see the valid combinations table for the model# description.

## 2. MCP Block Diagram



### 3. Connection Diagram

**84-ball Fine-Pitch Ball Grid Array**  
(Top View, Balls Facing Down)



**Note**  
May be shared depending on density.

| MCP         | Flash-only Addresses | Shared Addresses |
|-------------|----------------------|------------------|
| S71GL128PC0 | A22                  | A21-A0           |

#### 3.1 Special Handling Instructions For FBGA Package

Special handling is required for Flash Memory products in FBGA packages.

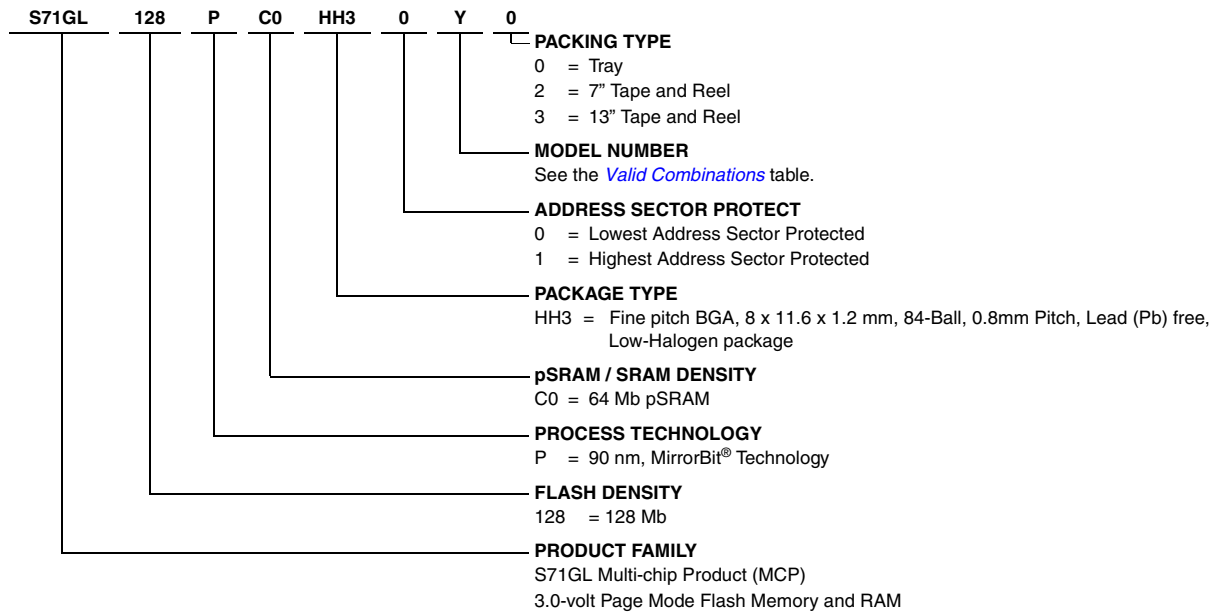
Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

## 4. Pin Description

| Pin              | Description                                                                                                                          |
|------------------|--------------------------------------------------------------------------------------------------------------------------------------|
| A22–A0           | 23 Address Inputs (Common and Flash only)                                                                                            |
| DQ15–DQ0         | 16 Data Inputs/Outputs (Common)                                                                                                      |
| CE1#f            | Chip Enable (Flash)                                                                                                                  |
| CE1#s            | Chip Enable 1 (pSRAM/SRAM)                                                                                                           |
| CE2s             | Chip Enable 2 (pSRAM/SRAM)                                                                                                           |
| OE#              | Output Enable (Common)                                                                                                               |
| WE#              | Write Enable (Common)                                                                                                                |
| RY/BY#           | Ready/Busy Output (Flash 1)                                                                                                          |
| UB#              | Upper Byte Control (pSRAM/SRAM)                                                                                                      |
| LB#              | Lower Byte Control (pSRAM/SRAM)                                                                                                      |
| RESET#           | Hardware Reset Pin, Active Low (Flash)                                                                                               |
| WP#/ACC          | Hardware Write Protect/Acceleration Pin (Flash)                                                                                      |
| V <sub>CCf</sub> | Flash 3.0 volt-only single power supply (see <a href="#">Product Selector Guide</a> for speed options and voltage supply tolerances) |
| V <sub>CCs</sub> | pSRAM/SRAM Power Supply                                                                                                              |
| V <sub>SS</sub>  | Device Ground (Common)                                                                                                               |
| NC               | Pin Not Connected Internally                                                                                                         |

## 5. Ordering Information

The order number is formed by a valid combinations of the following:



**Table 5.1** Valid Combinations

| S71GL128P Valid Combinations |                          |                                  |              | Speed Options (ns)/<br>Address Sector Protection | (p)SRAM Type/<br>Access Time<br>(ns) | Package<br>Marking |
|------------------------------|--------------------------|----------------------------------|--------------|--------------------------------------------------|--------------------------------------|--------------------|
| Base Ordering<br>Part Number | Package &<br>Temperature | Package Modifier/Model<br>Number | Packing Type |                                                  |                                      |                    |
| S71GL128PC0                  | HH3                      | 0Y                               | 0, 2, 3 (1)  | 100 / Low Protect                                | pSRAM9 / 70                          | TSB084             |
|                              |                          | 1Y                               |              | 100 / High Protect                               |                                      |                    |

**Note**

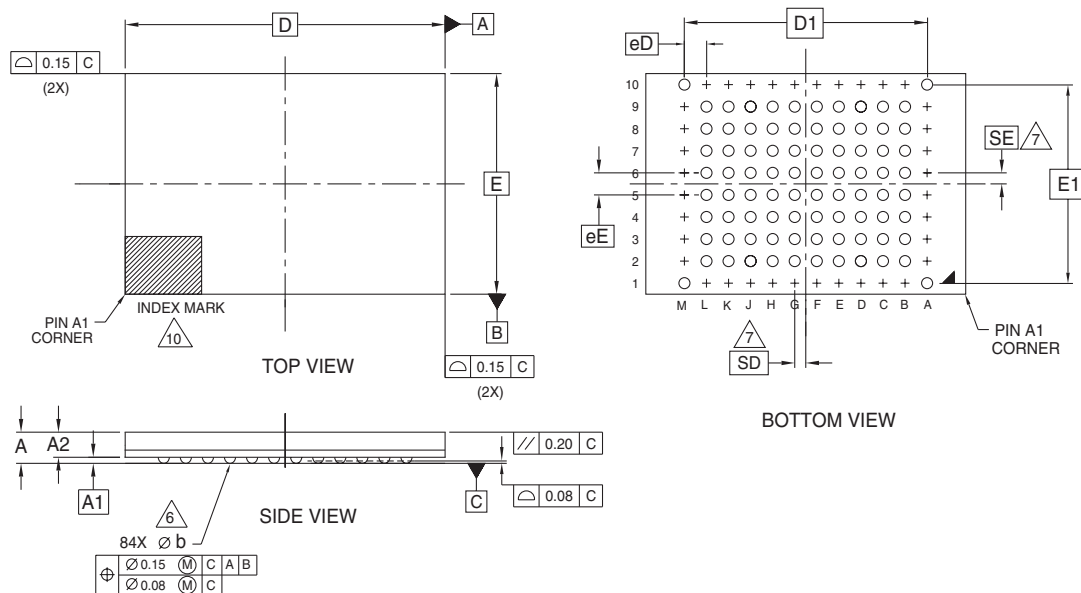
1. Type 0 is standard. Specify other options as required.

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

## 6. Physical Dimensions

### 6.1 TSB084—84-ball Fine-Pitch Ball Grid Array (FBGA) 11.6 x 8 mm Package



| PACKAGE | TSB 084                                                                                                                           |      |      | NOTE                     |
|---------|-----------------------------------------------------------------------------------------------------------------------------------|------|------|--------------------------|
| JEDEC   | N/A                                                                                                                               |      |      |                          |
| D x E   | 11.60 mm x 8.00 mm PACKAGE                                                                                                        |      |      |                          |
| SYMBOL  | MIN                                                                                                                               | NOM  | MAX  |                          |
| A       | ---                                                                                                                               | ---  | 1.20 | PROFILE                  |
| A1      | 0.17                                                                                                                              | ---  | ---  | BALL HEIGHT              |
| A2      | 0.81                                                                                                                              | ---  | 0.97 | BODY THICKNESS           |
| D       | 11.60 BSC.                                                                                                                        |      |      | BODY SIZE                |
| E       | 8.00 BSC.                                                                                                                         |      |      | BODY SIZE                |
| D1      | 8.80 BSC.                                                                                                                         |      |      | MATRIX FOOTPRINT         |
| E1      | 7.20 BSC.                                                                                                                         |      |      | MATRIX FOOTPRINT         |
| MD      | 12                                                                                                                                |      |      | MATRIX SIZE D DIRECTION  |
| ME      | 10                                                                                                                                |      |      | MATRIX SIZE E DIRECTION  |
| n       | 84                                                                                                                                |      |      | BALL COUNT               |
| φb      | 0.35                                                                                                                              | 0.40 | 0.45 | BALL DIAMETER            |
| eE      | 0.80 BSC                                                                                                                          |      |      | BALL PITCH               |
| eD      | 0.80 BSC                                                                                                                          |      |      | BALL PITCH               |
| SD / SE | 0.40 BSC                                                                                                                          |      |      | SOLDER BALL PLACEMENT    |
|         | A2,A3,A4,A5,A6,A7,A8,A9<br>B1,B10,C1,C10,D1,D10<br>E1,E10,F1,F10,G1,G10<br>H1,H10,J1,J10,K1,K10,L1,L10<br>M2,M3,M4,M5,M6,M7,M8,M9 |      |      | DEPOPULATED SOLDER BALLS |

NOTES:

- DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
- $\square$  REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.  
SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.  
n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- $\triangle$  DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- $\triangle$  SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
- WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.  
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE =  $\lfloor e/2 \rfloor$
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
- N/A
- $\triangle$  A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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## 7. Revision History

| Section                               | Description                                                  |
|---------------------------------------|--------------------------------------------------------------|
| <b>Revision 01 (May 5, 2008)</b>      |                                                              |
|                                       | Initial release.                                             |
| <b>Revision 02 (May 23, 2008)</b>     |                                                              |
| General Information                   | Updated 64 Mb pSRAM Type 7 Publication ID to psram_38        |
| <b>Revision 03 (February 3, 2009)</b> |                                                              |
| Product Selector Guide                | Changed flash density to 128 Mb<br>Changed package to TSB084 |
| Valid Combinations Table              | Changed S71GL064N to S71GL128P<br>Changed package to TSB084  |
| Physical Dimensions                   | Changed package to TSB084                                    |

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