6 4x Port Switch Serial RapidIO®

Product Brief
80KSW0006

1 Device Overview

The CPS-6Q, device number 80KSW0006, is a serial RapidIO switch whose functionality is central to routing packets for distribution among DSPs, processors, FPGAs, other switches, or any other sRIO-based devices. It may also be used in serial RapidIO backplane switching. The CPS-6Q supports serial RapidIO packet switching (unicast, multicast, and an optional broadcast) from any of its 16 input ports to any of its 16 output ports.

2 Features

- ***Interfaces - sRIO***
  - *24 bidirectional serial RapidIO (sRIO) lanes v 1.3*
  - *Port Speeds selectable: 3.125Gbps, 2.5Gbps, or 1.25Gbps*
  - *All lanes support short haul or long haul reach for each PHY speed*
  - *Configurable port count to up to 16 1x ports, 6 4x ports, or combinations of 1x and 4x ports*
  - *Two Enhanced Quad can be configured as individual 4 1x ports or 1 4X. Other Quad can be configured as 2 1x ports or 1 4x port.*
  - *Supports standard 4 levels of priority*
  - *Error management support*
- ***Interfaces - I^2C***
  - *Provides I^2C port for maintenance and error reporting*
  - *Master or Slave Operation*
  - *Master allows power-on configuration from external ROM*
  - *Master mode configuration with external image compressing and checksum*
- ***Performance***
  - *60 Gbps of peak switching bandwidth*
  - *Non-blocking data flow architecture within each sRIO priority*
  - *Very low latency for all packet length and load condition*
  - *Internal queuing buffer and retransmit buffer*
  - *Standard receiver based physical layer flow control*
- ***Features***
  - *Device configurable through any of sRIO ports, I^2C, or JTAG*
  - *Packet Trace/Mirror/Filter. Per-port line rate copy or filter of all packets matching user compare value. Supports security, sniffing, and diagnostics.*
  - *Supports up to 40 simultaneous multicast masks per port*
  - *Broadcast support*
  - *Configurable for Cut Through or Store And Forward data flow*
  - *Port Loopback Debug Feature*
  - *Software assisted error recovery, supporting hot swap*
  - *Ports may be individually turned off to reduce power*
  - *PMON counters for monitor and diagnostics. Per input port and output port counters.*
  - *Serdes physical diagnostic registers*
  - *Embedded PRBS generation and detection with programmable polinominals cover error rate under all conditions*
  - *0.13um technology*
  - *Low power dissipation*
  - **Package: FCBGA 676-ball grid array, 27mm x 27mm, 1.0mm ball pitch**

3 Block Diagram

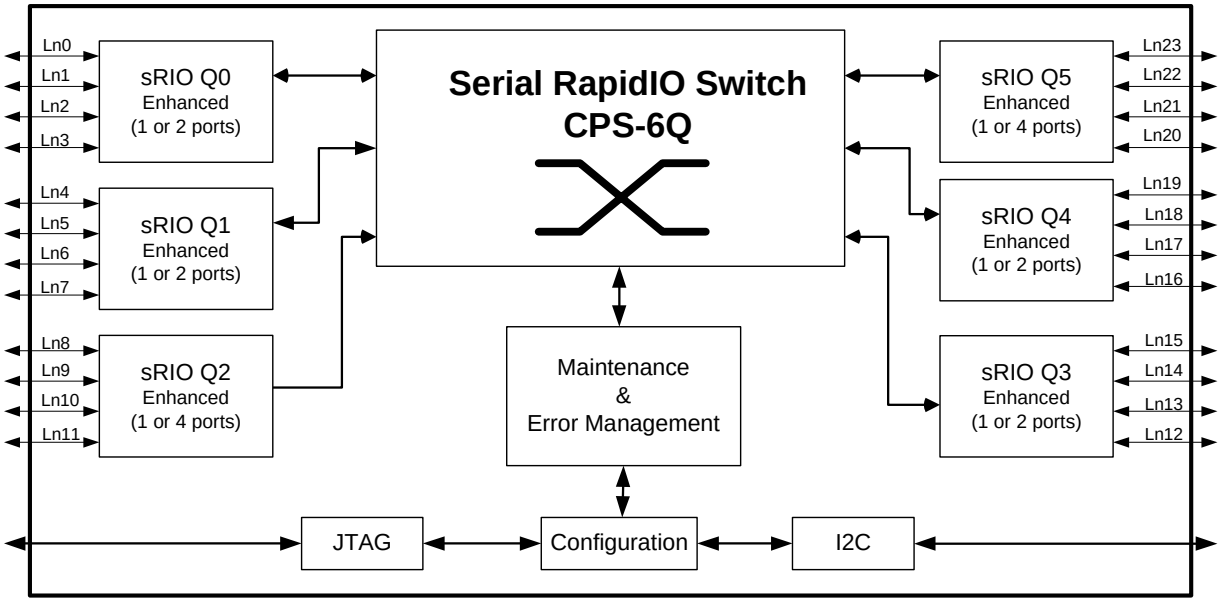

Figure 1 Block diagram

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4 Functional Overview

IDT's CPS-6Q is optimized for either board-level DSP/ASIC cluster applications or module-level distributed processing application. Up to 16 serial RapidIO ports fully meet the latest standard V1.3. The physical lanes may be configured to work at 3.125Gbps, 2.5Gbps or 1.25Gbps. All lanes independently work in short haul or long haul.

The CPS-6Q switch has a sustained 60Gbps bandwidth, supporting non-blocking within a priority.

The CPS-6Q offers full support for normal switching as well as enhanced functions:

1) Normal Switching

All packets are switched in accordance with standard serial RapidIO specifications, with packet destination IDs determining how the packet is routed.

Three major options exist within this category:

a. Multicast: If a Multicast ID is received, the CPS-6Q performs a multicast as defined by the device's configurable sRIO multicast mask registers. Also optional for broadcast.
b. Unicast: All other operations are performed as specified in sRIO.
c. Maintenance packets: As specified in sRIO.

2) Enhanced Functions

Enhanced features are provided for support of system debug. These features which are optional for the user consist of two major functions:

a. Packet Trace: The Packet Trace feature provides at-speed checking of the first 160 bits (header plus a portion of any payload) of every incoming packet against user-defined comparison register values. The trace feature is available on all serial RapidIO ports, each acting independently from one another. If the trace feature is enabled for a given port, every incoming packet is checked for a match against up to 4 comparison registers. In the event of a match, either of two possible user defined actions may take place:
   i) not only does the packet route normally through the switch to its appropriate destination port, but this same packet is replicated and sent to a "trace port." The trace port itself may be any of the standard serial RapidIO ports. The port used for the trace port is defined by the user through simple register configuration.
   ii) the packet is dropped.

   If there is no match, the packets route normally through the switch with no action taken.

   The Packet Trace feature can be used during system bring-up and prototyping to identify particular packet types of interest to the user. It might be used in security applications, where packets must be checked for either correct or incorrect tags in either of the header or payload. Identified (match) packets are then routed to the trace port for receipt by a host processor, which can perform an intervention at the software level.
b. Port Loopback: The CPS-6Q offers internal loopback for each port that may be used for system debug of the high speed sRIO ports. By enabling loopback on a given port, packets sent to the port's receiver are immediately looped back at the physical layer to the transmitter - bypassing the higher logical or transport layers.
c. Broadcast: Each multicast mask can be configured so that the source port is included among the destination ports of that multicast operation.

The CPS-6Q can be programmed through any one or combination of sRIO, I^2C, or JTAG. Note that any sRIO port may be used for programming. It can also configure itself on power-up by reading directly from ROM over I^2C in master mode.

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5 Applications

Central Switch Based Wireless Processing

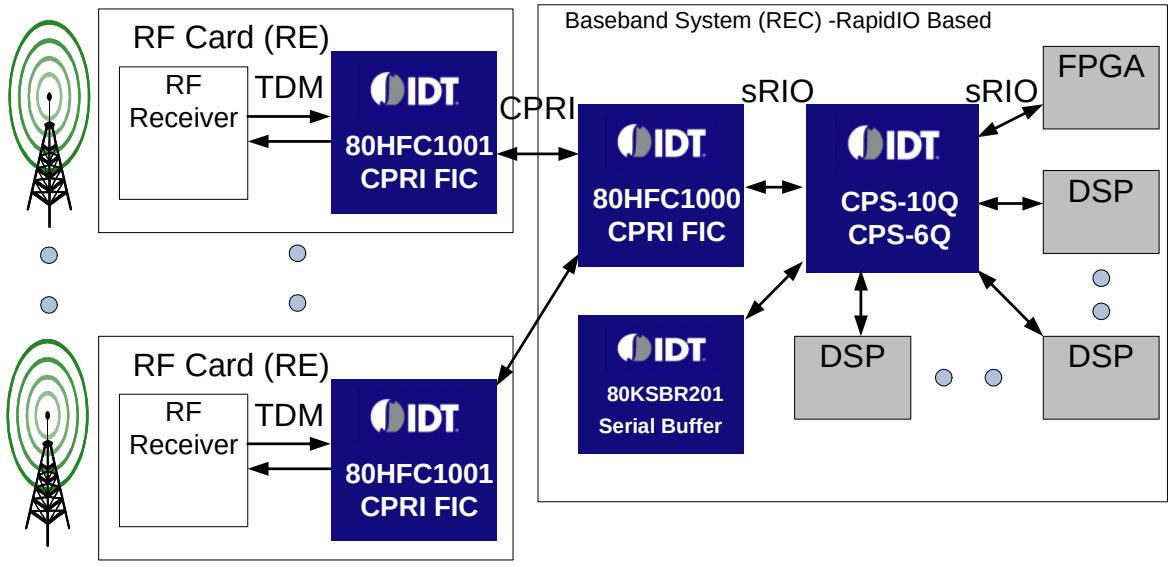

Figure 2 Application Overview

Note: The CPS-6Q provides direct support for backplane connections using the serial RapidIO standard. The addition of an appropriate bridge (e.g., CPRI ↔ sRIO) allows for further backplane flexibility, accommodating designs based on a wide range of standards such as CPRI, OBSAI, GbE or PCIe.

In a macro wireless station, a switch-based raw data combination and distribution architecture is widely adopted. Switch based architecture provides high flexibility and high resource efficiency. The raw data from the Radio Unit is distributed to one or more processing cards by unicast or multicast. Aggregating raw data from processing cards to a buffer-less chain can be done by a fast non-blocking switch.

Media Gateway and General Processing

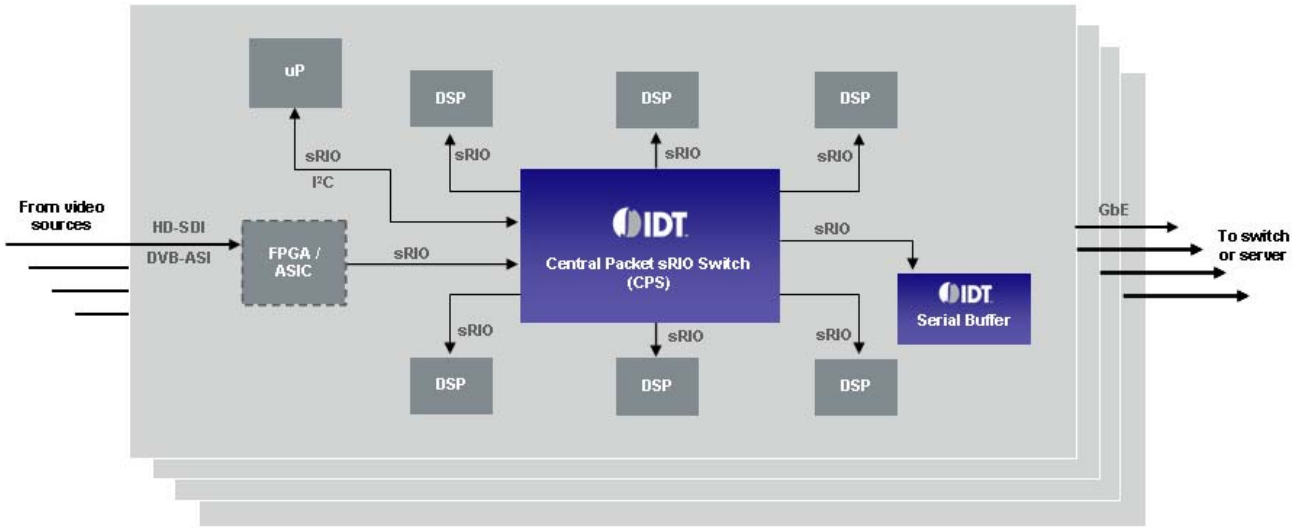

Figure 3 Application Overview

Note: The CPS-6Q provides direct support for backplane connections using the serial RapidIO standard.

Though SAR and RTP is usually processed by NP/Processor, but DSP is more efficient for TDM conversion and compression. A low jitter switch enables the full using of DSP processing power. Priority support, fast switching, and multicasting will differentiate class of traffic to provide QoS.

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