Serial RapidIO™ Pre-Processing Switch for DSP Clusters

Product Brief
80KSW0001

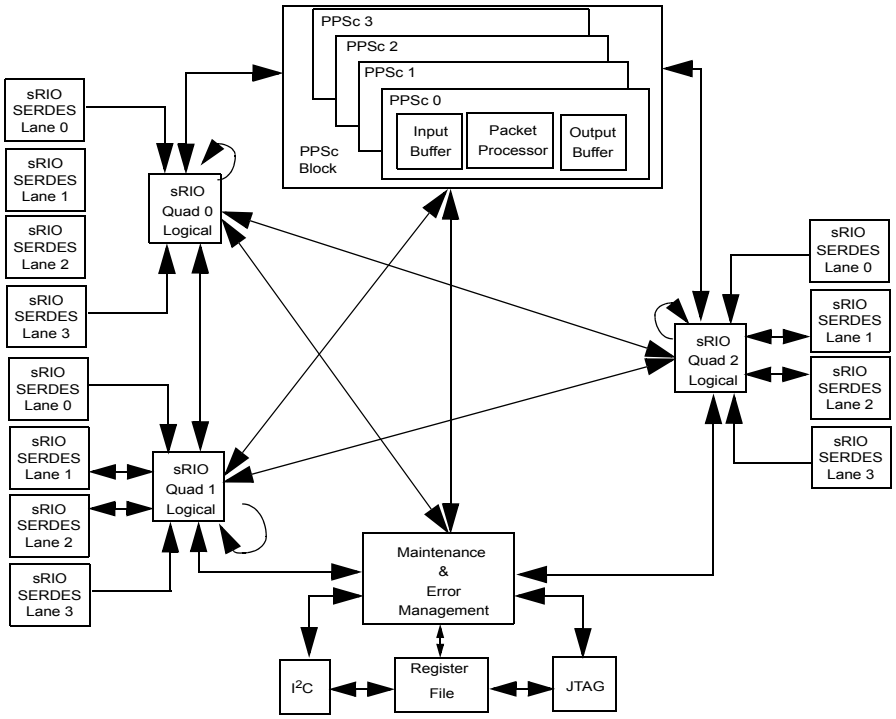
1 Device Overview

The 80KSW0001 is a member of IDT's serial RapidIO™ Pre-Processing Switch (PPS) family of devices. The PPS is designed to be a central component to DSP cluster architectures. It supports true serial RapidIO™ packet switching (unicast, multicast, or broadcast) from any input to any output port. The PPS accelerates baseband processing in support of a variety of wireless standards. The 80KSW0001 can also optionally perform a variety of data processing on the payload of sample packets to accelerate the subsequent algorithmic operations of a receiving processor (DSP, CRP, FPGA). The special processing capabilities may also be used for media gateways, video imaging such as that in medical equipment or high-end surveillance, or similar signal processing-intensive applications.

2 Features

- ***Interfaces - sRIO***
  - 12 Serial RapidIO (sRIO) v 1.3 full duplex lanes
  - Lane Rates selectable; 3.125Gbps, 2.5Gbps, or 1.25Gbps
  - Short- or Long-haul reach for each lane at all rates
  - 2 Configurations: a) 10 Ports (IDT70K2000 compatible) b) 12 ports (compatibility possible with new configuration software)
  - sRIO Multicast support (10 simultaneous masks)
  - Support for 4 sRIO priorities
  - *Port Loopback Debug Feature*
  - *Software assisted error recovery, supporting hot swap*
- ***Interfaces - I^2C***
  - One I^2C port for configuration and error reporting
- ***Switch***
  - 30 Gbps peak throughput (max throughput for all ports)
- ***4 Independent Packet Processing Scenarios (PPSc)***
  - *Each PPSc offers 24 Gbps peak input bandwidth, 24 Gbps peak processing throughput, 10 Gbps peak unicast output, 24 Gbps peak multicast with decoded packets*
- ***DMA Support***
  - Resultant output data may be segmented into up to 8 smaller output data (SWRITE only)
  - Automatic 34-bit target memory address generation per sRIO packet
- ***Packet Trace***
  - Each Port provides the ability to match the first 160 bits of any packet against up to 4 programmable values as comparison criteria to copy the packet to a programmable output trace port
- ***FIR Filtering***
  - Each PPSc supports the ability to perform 2.5 GMACs per second, and an aggregate of 9.9 GMACs
- ***Synchronization***
  - Packet alignment and deskew capabilities in support of time-based domains
- ***Full JTAG Boundary Scan Support (IEEE1149.1 & 1149.6)***
- ***2 Package Options:***
  - FCBGA 676-ball grid array, 27 mm x 27mm, 1.0mm ball pitch
  - FCBGA 324-ball grid array, 19mm x 19mm, 1.0mm ball pitch

3 Block Diagram



DSC 5697

(continued on next page)

- ***2 Group Packet Processing Scenarios***
  - 2 Group Scenarios each of which can address up to 4 Individual PPScs
  - Allows multiple types of processing and output ports for the same data packet
- ***Within Sample Processing***
  - Sign Extension or Deletion, Endian Change
  - Number of bits per sample is user programmable
  - Support for I/Q- or I-only Sample Formats
- ***Within Packet Processing***
  - Complete remapping of each input packet sample into any location in the resultant output packet
  - Multiple input packets may be concatenated into a single resultant output packet
  - SWRITE (type 6) and Message Passing (type 11) packets re-formed for Packet Processor Output Packets
  - Incoming packet header information will be used in the resultant packet
- ***Summation Across Ports (Type 6 & 11 packets)***
  - Supports CDMA / WCDMA downstream summing requirement
  - Samples from any input ports may be summed to give one sample ouput, which is placed in any location of the resultant packet
  - Summing of each I or Q sub-sample from up to 12 separate ports
  - Dynamic Range or Saturation of result to 4-32 bit range

4 Functional Overview

IDT's 80KSW0001 is optimized for DSP cluster applications at board level. It may have a backplane interface which can connect to a backplane switch or directly to multiple RF cards. On the line card side it can also connect to multiple ports. It can support up to 12 ports which are configurable as line card, or backplane ports. It operates as an end-point free (switch) device in an sRIO network.

The user may program the 80KSW0001 to direct incoming packets with a given destination ID to a packet processor. Here the unprocessed data samples in their payload will be pre-processed. Input packets packets with other destination IDs are switched as defined by the transport layer sRIO specification. The packet manipulation in the 80KSW0001 is transparent to the sRIO protocol.

The 80KSW0001 receives the packets from up to 12 unique ports. Depending on the device ID field within a received packet, two functions can be performed by the device:

1) **Packet Processing**: If DestID in the sRIO transport layer targets one of the Packet Processing Scenario (PPSc) addresses specified in the routing tables, the 80KSW0001 terminates the sRIO packet and implements the sample preprocessing.

   The sample preprocessing operations are defined in Packet Processing Scenarios. There are a total of 4 individual PPScs in the 80KSW0001. There are also 2 Group PPScs (GPPSc), each of which may be linked to 4 individual PPScs.

2) **Switching**: All other addresses are treated as regular sRIO destination addresses, and packets are switched accordingly.

   Also three major options exist within this category:
   a. Multicast:If a Multicast ID is received, the 80KSW0001 performs a multicast as defined by the device's configurable sRIO multicast mask registers.
   b. Unicast: All other operations are performed as specified in sRIO.
   c. Maintenance packets: As specified in sRIO.

The core of the Pre-Processing Switch are the Packet Processing Scenarios. The PPScs perform a variety of data manipulations on the payload of the sample packets. The intent is to make the data payload more efficient for the receiving device (DSP, FPGA, CRP) . Thus it is pre-processed to accelerate the subsequent algorithmic operations of the receiving processor. Please refer to the User's Manual for full functional details of the processing capabilities of the PPScs.

The payload manipulations defined in the User's Manual are completely configurable through use of the device's configuration registers. Each PPSc is functionally independent from all other PPScs. Thus, one scenario might be used for data formatting and multicasting only on a WCDMA upstream datapath while another scenario might be aligning, synchronizing, and summing packets from multiple input ports (coming from multiple DSPs or baseband boards), and multicasting these to multiple antennas on the downstream. Packets are targeted to a given PPSc via its destID field.

Data manipulation options include (among others):

- **MSB / LSB bit reversal - independent for both I and Q subsamples**
- **Interleaving**

- **I and Q subsample re-ordering (which comes first)**
- **Change of endianness**
- **Summing of samples across packets from multiple ports**
  - *summing options (truncate, roll-over)*
- **Signed and unsigned arithmetic**
- **Real Finite Impulse Response filtering with configurable Multiply and Accumulate (MAC) block**

The resultant samples may be fully re-ordered. The resultant samples are then re-packetized for transmission out those port(s) specified by user. The user may select “multiple packet mode” which allows a resultant payload destined to a given output port(s) to be split up across multiple individual packets prior to transmission. The destination address of the resultant packets may be controlled as well. The result is a seamless dump of the modified data into the processing device’s memory in a format it may readily use for computation.

The 80KSW0001’s 2 GPPScs may be used to direct incoming packets to up to 4 different PPScs, simultaneously. Thus, a given incoming packet destined to a GPPSc (again, dictated by the packet’s destID), are sent to multiple PPScs. The number and which PPScs are used is programmable by user. By utilizing the GPPScs, a given data stream may have several types of processing performed and transferred to the same or multiple output ports.

The 80KSW0001 can be programmed through a CPU or a DSP connected to one of the sRIO ports of the device or with a CPU connected to an I^2C or JTAG bus. This option is added to allow the user to use a conventional CPU instead of a sRIO interface.

The packets received from packet processing or switching are sent to re-transmit buffers, which are 16 maximum sized packets deep - four for each of the sRIO defined 4 priorities. The 4 levels of priority apply as defined in Rapid IO at each output port to packets which arrive from the device’s internal switch resource or from any of its PPScs.

The Packet Processing Module can reach a peak input bandwidth of 24 Gbps, which is the line rate for 12 ports in 1x configuration, each at 2 Gbps. Peak processing throughput per PPSc is 24 Gbps, while peak output is 10 Gbps to a given port and 24 Gbps when multicast is used. Each PPSc is programmed via the PPSc registers. Re-programming each PPSc dynamically is possible, and does not affect the operation of all other PPScs, but does incur a pause on the affected PPSc.

The sRIO Switch has a peak throughput of 30 Gbps, and switches dynamically in accordance with the packet headers.

Each sRIO port provides a packet trace capability. For any packet received by a port, a comparison between the first 160 bits and up to four configurable values can be performed. A match against any of these parameters will result in a copy of the packet and a route of the packet to a configurable ouput port. This feature can be used as a tactical function to track user data or in a debug environment to test how specific packets are moving through the platform.