

## Device Overview

The 89HPES16NT2 is a member of the IDT PRECISE™ family of PCI Express® switching solutions offering the next-generation I/O interconnect standard. The PES16NT2 is a 16-lane, 2-port peripheral chip that provides high-performance switching and non-transparent bridging (NTB) functions between a PCIe® upstream port and an NTB downstream port. The PES16NT2 is a part of the IDT PCIe System Interconnect Products and is intended to be used with IDT PCIe System Interconnect Switches. Together, the chipset targets multi-host and intelligent I/O applications such as communications, storage, and blade servers where inter-domain communication is required.

## Features

- ◆ **High Performance PCI Express Switch**
  - Sixteen PCI Express lanes (2.5Gbps), two switch ports
  - Delivers 64 Gbps (8 GBps) of aggregate switching capacity
  - Low latency cut-through switch architecture
  - Support for Max Payload size up to 2048 bytes
  - Supports one virtual channel and eight traffic classes
  - PCI Express Base specification Revision 1.0a compliant
- ◆ **Flexible Architecture with Numerous Configuration Options**
  - Supports automatic per port link width negotiation (x8, x4, x2, or x1)
  - Static lane reversal on all ports
  - Automatic polarity inversion on all lanes

- Supports locked transactions, allowing use with legacy software
- Ability to load device configuration from serial EEPROM
- Ability to control device via SMBus
- ◆ **Non-Transparent Port**
  - Crosslink support on NTB port
  - Four mapping windows supported
    - Each may be configured as a 32-bit memory or I/O window
    - May be paired to form a 64-bit memory window
  - Interprocessor communication
    - Thirty-two inbound and outbound doorbells
    - Four inbound and outbound message registers
    - Two shared scratchpad registers
  - Allows up to sixteen masters to communicate through the non-transparent port
  - No limit on the number of supported outstanding transactions through the non-transparent bridge
  - Completely symmetric non-transparent bridge operation allows similar/same configuration software to be run
  - Supports direct connection to a transparent or non-transparent port of another switch
- ◆ **Highly Integrated Solution**
  - Requires no external components
  - Incorporates on-chip internal memory for packet buffering and queueing
  - Integrates sixteen 2.5 Gbps embedded full duplex SerDes, 8B/10B encoder/decoder (no separate transceivers needed)

## Block Diagram

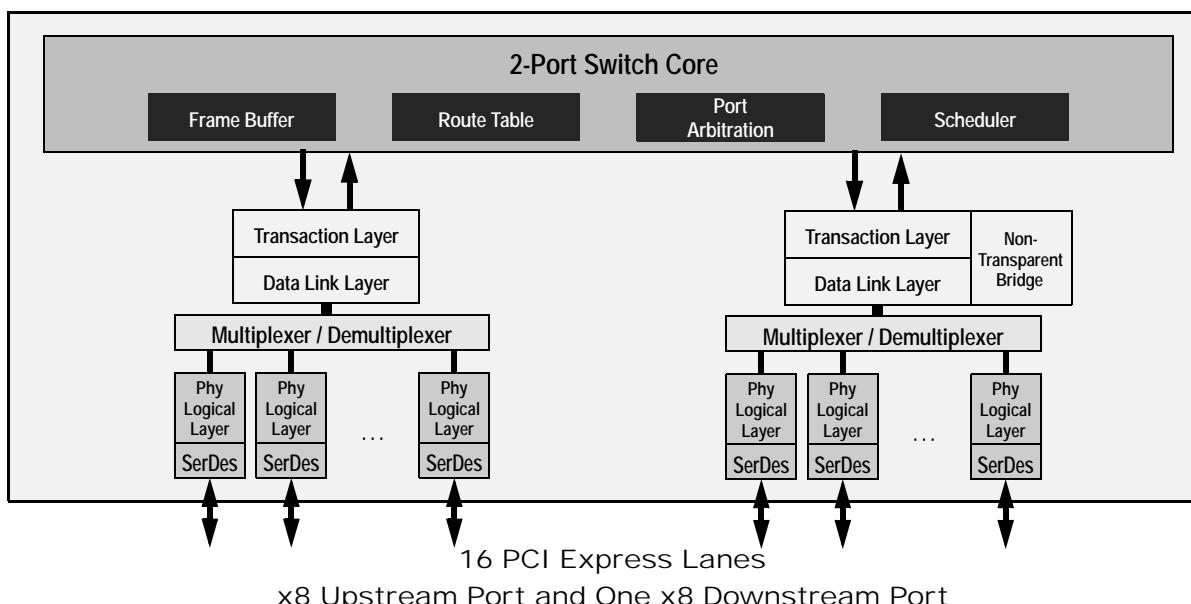


Figure 1 Internal Block Diagram

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- ◆ Reliability, Availability, and Serviceability (RAS) Features
  - Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)
  - Supports ECRC pass-through
  - Supports Hot-Swap
- ◆ Power Management
  - Supports PCI Power Management Interface specification, Revision 1.1 (PCI-PM)
  - Unused SerDes are disabled
- ◆ Testability and Debug Features
  - Built in SerDes Pseudo-Random Bit Stream (PRBS) generator
  - Ability to read and write any internal register via the SMBus
  - Ability to bypass link training and force any link into any mode
  - Provides statistics and performance counters
- ◆ Two SMBus Interfaces
  - Slave interface provides full access to all software-visible registers by an external SMBus master
  - Master interface provides connection for an optional serial EEPROM used for initialization
  - Master and slave interfaces may be tied together so the switch can act as both master and slave
- ◆ Eight General Purpose Input/Output pins
- ◆ Packaged in a 23mm x 23mm 484-ball BCG with 1mm ball spacing

## Product Description

Utilizing standard PCI Express interconnect, the PES16NT2 provides the most efficient high-performance I/O connectivity solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. With support for non-transparent bridging, the PES16NT2 is part of the IDT PCIe System Interconnect Products that target multi-host and intelligent I/O applications requiring inter-domain communication. The PES16NT2 provides 64 Gbps (8 GBps) of aggregated, full-duplex switching capacity through 16 integrated serial lanes, using proven and robust IDT technology. Each lane provides 2.5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification 1.0a.

The PES16NT2 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link, and Transaction layers in compliance with PCI Express Base specification Revision 1.0a. The PES16NT2 can operate either as a store and forward or cut-through switch depending on the packet size and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management.

## Switch Configuration

The PES16NT2 is a two port switch that contains sixteen PCI Express lanes. Each of the two ports is statically allocated eight lanes with ports labeled as A and C. Port A is the upstream port and port C is the non-transparent downstream port.

During link training, link width is automatically negotiated. Each PES16NT2 port is capable of independently negotiating to a x8, x4, x2, or x1 width. Thus, the PES16NT2 may be used in virtually any two port switch configuration (e.g., {x8, x8}, {x4, x4}, {x4, x2}, etc.). The PES16NT2 supports static lane reversal. For example, lane reversal for upstream port A may be configured by asserting the PCI Express Port A Lane Reverse (PEALREV) input signal or through serial EEPROM or SMBus initialization. Lane reversal for port C may be enabled via a configuration space register, serial EEPROM, or the SMBus.

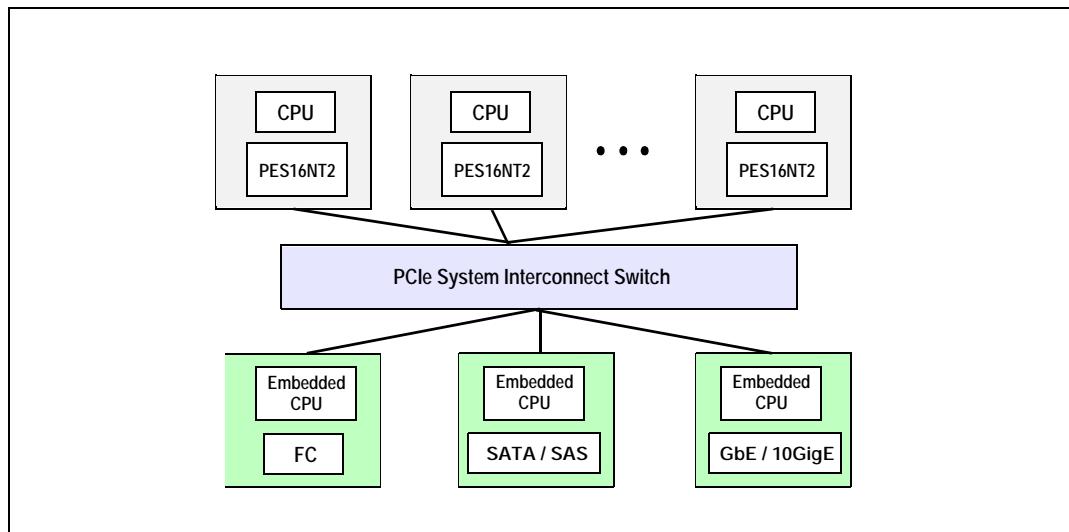


Figure 2 PCIe System Interconnect Architecture Block Diagram

## Pin Description

The following tables list the functions of the pins provided on the PES16NT2. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an "N" are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Signal	Type	Name/Description
PEALREV	I	PCI Express Port A Lane Reverse. When this bit is asserted, the lanes of PCI Express Port A are reversed. This value may be overridden by modifying the value of the PALREV bit in the PA_SWCTL register.
PEARP[7:0] PEARN[7:0]	I	PCI Express Port A Serial Data Receive. Differential PCI Express receive pairs for port A.
PEATP[7:0] PEATN[7:0]	O	PCI Express Port A Serial Data Transmit. Differential PCI Express transmit pairs for port A
PECLREV	I	PCI Express Port C Lane Reverse. When this bit is asserted, the lanes of PCI Express Port C are reversed. This value may be overridden by modifying the value of the PCLREV bit in the PA_SWCTL register.
PECRP[7:0] PECRN[7:0]	I	PCI Express Port C Serial Data Receive. Differential PCI Express receive pairs for port C.
PECTP[7:0] PECTN[7:0]	O	PCI Express Port C Serial Data Transmit. Differential PCI Express transmit pairs for port C
PEREFCLKP[1:0] PEREFCLKN[1:0]	I	PCI Express Reference Clock. Differential reference clock pair input. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic and on-chip SerDes. The frequency of the differential reference clock is determined by the REFCLKM signal.
REFCLKM	I	PCI Express Reference Clock Mode Select. These signals select the frequency of the reference clock input. 0x0 - 100 MHz 0x1 - 125 MHz

Table 1 PCI Express Interface Pins

Signal	Type	Name/Description
MSMBADDR[4:1]	I	<b>Master SMBus Address.</b> These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded.
MSMBCLK	I/O	<b>Master SMBus Clock.</b> This bidirectional signal is used to synchronize transfers on the master SMBus. It is active and generating the clock only when the EEPROM is being accessed.
MSMBDAT	I/O	<b>Master SMBus Data.</b> This bidirectional signal is used for data on the master SMBus.
SSMBADDR[5,3:1]	I	<b>Slave SMBus Address.</b> These pins determine the SMBus address to which the slave SMBus interface responds.
SSMBCLK	I/O	<b>Slave SMBus Clock.</b> This bidirectional signal is used to synchronize transfers on the slave SMBus.
SSMBDAT	I/O	<b>Slave SMBus Data.</b> This bidirectional signal is used for data on the slave SMBus.

Table 2 SMBus Interface Pins

Signal	Type	Name/Description
GPIO[0]	I/O	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin.
GPIO[1]	I/O	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. Alternate function pin name: PECRSTN Alternate function pin type: Output Alternate function: Reset output for downstream port C
GPIO[2]	I/O	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. Alternate function pin name: PALINKUPN Alternate function pin type: Output Alternate function: Port A link up status output
GPIO[3]	I/O	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin.
GPIO[4]	I/O	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCLINKUPN Alternate function pin type: Output Alternate function: Port C link up status output
GPIO[5]	I/O	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. Alternate function pin name: FAILOVERP Alternate function pin type: Input Alternate function: NTB upstream port failover
GPIO[6]	I/O	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin.
GPIO[7]	I/O	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin.

Table 3 General Purpose I/O Pins

Signal	Type	Name/Description
CCLKDS	I	<b>Common Clock Downstream.</b> When the CCLKDS pin is asserted, it indicates that a common clock is being used between the downstream device and the downstream port.
CCLKUS	I	<b>Common Clock Upstream.</b> When the CCLKUS pin is asserted, it indicates that a common clock is being used between the upstream device and the upstream port.
MSMBSSMODE	I	<b>Master SMBus Slow Mode.</b> The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 KHz. This value may not be overridden.
PENTBRSTN	I	<b>Non-Transparent Bridge Reset.</b> Assertion of this signal indicates a reset on the external side of the non-transparent bridge. This signal is only used when the switch mode selects a non-transparent mode and has no effect otherwise.
PERSTN	I	<b>Fundamental Reset.</b> Assertion of this signal resets all logic inside the PES16NT2 and initiates a PCI Express fundamental reset.
RSTHALT	I	<b>Reset Halt.</b> When this signal is asserted during a PCI Express fundamental reset, the PES16NT2 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the PA_SWCTL register by an SMBus master.
SWMODE[3:0]	I	<b>Switch Mode.</b> These configuration pins determine the PES16NT2 switch operating mode. 0x0 - Transparent mode 0x1 - Transparent mode with serial EEPROM initialization 0x2 - Non-transparent mode 0x3 - Non-transparent mode with serial EEPROM initialization 0x4 - Non-transparent failover mode 0x5 - Non-transparent failover mode with serial EEPROM initialization 0x6 through 0xF - Reserved

Table 4 System Pins

Signal	Type	Name/Description
JTAG_TCK	I	<b>JTAG Clock.</b> This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	<b>JTAG Data Input.</b> This is the serial data input to the boundary scan logic or JTAG Controller.

Table 5 Test Pins (Part 1 of 2)

Signal	Type	Name/Description
JTAG_TDO	O	<b>JTAG Data Output.</b> This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	<b>JTAG Mode.</b> The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.
JTAG_TRST_N	I	<b>JTAG Reset.</b> This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 5 Test Pins (Part 2 of 2)

Signal	Type	Name/Description
V <sub>DDCORE</sub>	I	Core V <sub>DD</sub> . Power supply for core logic.
V <sub>DDIO</sub>	I	I/O V <sub>DD</sub> . LVTTI I/O buffer power supply.
V <sub>DDPE</sub>	I	PCI Express Digital Power. PCI Express digital power used by the digital power of the SerDes.
V <sub>DDAPE</sub>	I	PCI Express Analog Power. PCI Express analog power used by the PLL and bias generator.
V <sub>TTP</sub> E	I	PCI Express Termination Power.
V <sub>SS</sub>	I	Ground.

Table 6 Power and Ground Pins

## Pin Characteristics

**Note:** Some input pads of the PES16NT2 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any input pin left floating can cause a slight increase in power consumption.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes
PCI Express Interface	PEALREV	I	LVTTL	Input	pull-down	
	PEARN[7:0]	I	CML	Serial link		
	PEARP[7:0]	I				
	PEATN[7:0]	O				
	PEATP[7:0]	O				
	PECLREV	I	LVTTL	Input	pull-down	
	PECRN[7:0]	I	CML	Serial link		
	PECRP[7:0]	I				
	PECTN[7:0]	O				
	PECTP[7:0]	O				
	PEREFCLKN[1:0]	I	LVPECL/ CML	Diff. Clock Input		Refer to Table 8
	PEREFCLKP[1:0]	I				
	REFCLKM	I	LVTTL	Input	pull-down	
SMBus	MSMBADDR[4:1]	I	LVTTL	Input	pull-up	
	MSMBCLK	I/O		STI		
	MSMBDAT	I/O				
	SSMBADDR[5:3:1]	I		Input	pull-up	
	SSMBCLK	I/O		STI		
	SSMBDAT	I/O				
General Purpose I/O	GPIO[7:0]	I/O	LVTTL	Input, High Drive	pull-up	
System Pins	CCLKDS	I	LVTTL	Input	pull-up	
	CCLKUS	I			pull-up	
	MSMBSMODE	I			pull-down	
	PENTBRSTN	I				
	PERSTN	I				
	RSTHALT	I			pull-down	
	SWMODE[3:0]	I			pull-up	
JTAG	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDI	I			pull-up	
	JTAG_TDO	O		Low Drive		
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I			pull-up	External pull-down

Table 7 Pin Characteristics

# Logic Diagram — PES16NT2

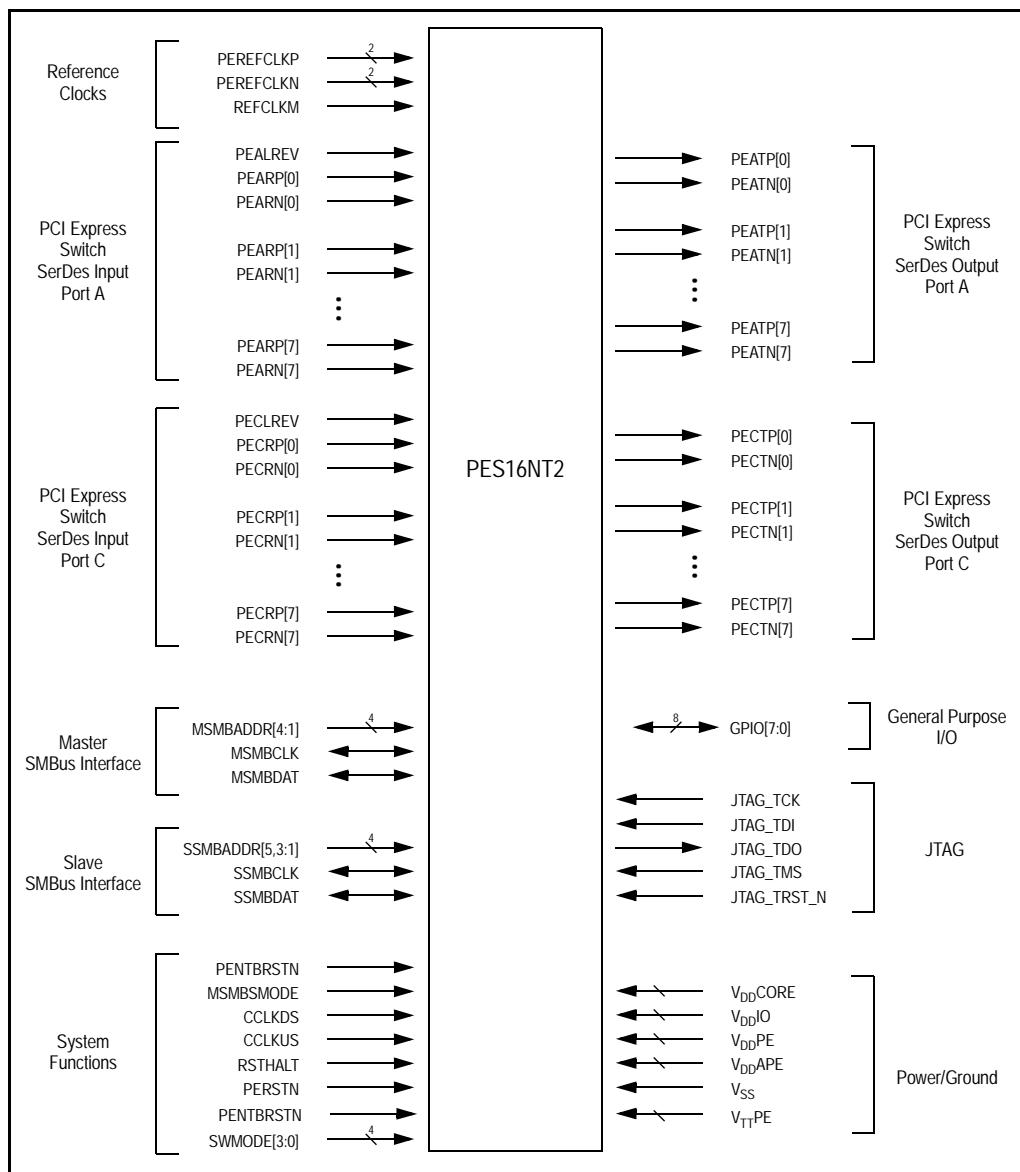


Figure 3 PES16NT2 Logic Diagram

Advance Information

## System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 12 and 13.

Parameter	Description	Min	Typical	Max	Unit
Refclk <sub>FREQ</sub>	Input reference clock frequency range	100		125 <sup>1</sup>	MHz
Refclk <sub>DC</sub> <sup>2</sup>	Duty cycle of input clock	40	50	60	%
T <sub>R</sub> , T <sub>F</sub>	Rise/Fall time of input clocks			0.2*RCUI	RCUI <sup>3</sup>
V <sub>SW</sub>	Differential input voltage swing <sup>4</sup>	0.6		1.6	V
T <sub>jitter</sub>	Input clock jitter (cycle-to-cycle)			125	ps
R <sub>T</sub>	Termination Resistor		110		Ohms

Table 8 Input Clock Requirements

1. The input clock frequency will be either 100 or 125 MHz depending on signal REFCLKM.

2. Ckln must be AC coupled. Use 0.01 — 0.1  $\mu$ F ceramic capacitors.

3. RCUI (Reference Clock Unit Interval) refers to the reference clock period.

4. AC coupling required.

## AC Timing Characteristics

Parameter	Description	Min <sup>1</sup>	Typical <sup>1</sup>	Max <sup>1</sup>	Units
<b>PCIe Transmit</b>					
UI	Unit Interval	399.88	400	400.12	ps
T <sub>TX-EYE</sub>	Minimum Tx Eye Width	0.7	.9		UI
T <sub>TX-EYE-MEDIAN-to-MAX-JITTER</sub>	Maximum time between the jitter median and maximum deviation from the median			0.15	UI
T <sub>TX-RISE</sub> , T <sub>TX-FALL</sub>	D+ / D- Tx output rise/fall time	50	90		ps
T <sub>TX-IDLE-MIN</sub>	Minimum time in idle	50			UI
T <sub>TX-IDLE-SET-TO-IDLE</sub>	Maximum time to transition to a valid Idle after sending an Idle ordered set			20	UI
T <sub>TX-IDLE-TO-DIFF-DATA</sub>	Maximum time to transition from valid idle to diff data			20	UI
T <sub>TX-SKEW</sub>	Transmitter data skew between any 2 lanes		500	1300	ps
<b>PCIe Receive</b>					
UI	Unit Interval	399.88	400	400.12	ps
T <sub>RX-EYE</sub> (with jitter)	Minimum Receiver Eye Width (jitter tolerance)	0.4			UI

Table 9 PCIe AC Timing Characteristics (Part 1 of 2)

Parameter	Description	Min <sup>1</sup>	Typical <sup>1</sup>	Max <sup>1</sup>	Units
T <sub>RX-EYE-MEDIUM TO MAX JITTER</sub>	Max time between jitter median & max deviation			0.3	UI
T <sub>RX-IDLE-DET-DIFF-ENTER TIME</sub>	Unexpected Idle Enter Detect Threshold Integration Time			10	ms
T <sub>RX-SKEW</sub>	Lane to lane input skew			20	ns

Table 9 PCIe AC Timing Characteristics (Part 2 of 2)

<sup>1</sup>. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.1

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
<b>GPIO</b>						
GPIO[7:0] <sup>1</sup>	T <sub>pw_13b</sub> <sup>2</sup>	None	50	—	ns	

Table 10 GPIO AC Timing Characteristics

<sup>1</sup>. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.

<sup>2</sup>. The values for this symbol were determined by calculation, not by testing.

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
<b>JTAG</b>						
JTAG_TCK	T <sub>per_16a</sub>	none	50.0	—	ns	See Figure 4.
	T <sub>high_16a</sub> , T <sub>low_16a</sub>		10.0	25.0	ns	
JTAG_TMS <sup>1</sup> , JTAG_TDI	T <sub>su_16b</sub>	JTAG_TCK rising	2.4	—	ns	
	T <sub>hd_16b</sub>		1.0	—	ns	
JTAG_TDO	T <sub>do_16c</sub>	JTAG_TCK falling	—	20	ns	
	T <sub>dz_16c</sub> <sup>2</sup>		—	20	ns	
JTAG_TRST_N	T <sub>pw_16d</sub> <sup>2</sup>	none	25.0	—	ns	

Table 11 JTAG AC Timing Characteristics

<sup>1</sup>. The JTAG specification, IEEE 1149.1, recommends that JTAG\_TMS should be held at 1 while the signal applied at JTAG\_TRST\_N changes from 0 to 1. Otherwise, a race may occur if JTAG\_TRST\_N is deasserted (going from low to high) on a rising edge of JTAG\_TCK when JTAG\_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

<sup>2</sup>. The values for this symbol were determined by calculation, not by testing.

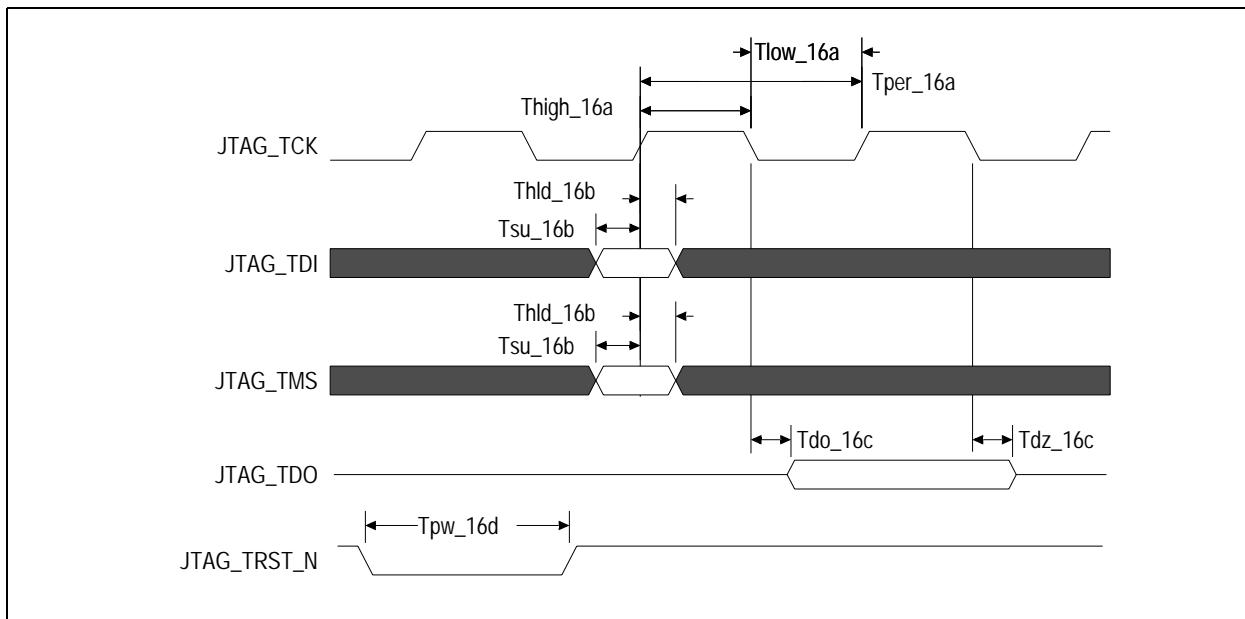


Figure 4 JTAG AC Timing Waveform

## Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
$V_{DDCORE}$	Internal logic supply	0.9	1.0	1.1	V
$V_{DDI/O}$	I/O supply except for SerDes LVPECL/CML	3.0	3.3	3.6	V
$V_{DDPE}$	PCI Express Digital Power	0.9	1.0	1.1	V
$V_{DDAPE}$	PCI Express Analog Power	0.9	1.0	1.1	V
$V_{TTP}$	PCI Express Serial Data Transmit Termination Voltage	1.425	1.5	1.575	V
$V_{SS}$	Common ground	0	0	0	V

Table 12 PES16NT2 Operating Voltages

## Power-Up Sequence

This section describes the sequence in which various voltages must be applied to the part during power-up to ensure proper functionality. For the PES16NT2, the power-up sequence must be as follows:

1.  $V_{DDI/O}$  — 3.3V
2.  $V_{DDCore}$ ,  $V_{DDPE}$ ,  $V_{DDAPE}$  — 1.0V
3.  $V_{TTP}$  — 1.5V

When powering up, each voltage level must ramp and stabilize prior to applying the next voltage in the sequence to ensure internal latch-up issues are avoided. There are no maximum time limitations in ramping to valid power levels. The power-down sequence must be in the reverse order of the power-up sequence.

## Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient

Table 13 PES16NT2 Operating Temperatures

## Power Consumption

Typical power is measured under the following conditions: 25°C Ambient, 35% total link usage on all ports, typical voltages defined in Table 14.

Maximum power is measured under the following conditions: 70°C Ambient, 85% total link usage on all ports, maximum voltages defined in Table 14.

All power measurements assume that the part is mounted on a 10 layer printed circuit board with 0 LFM airflow.

Number of Connected Lanes: Port-A/Port-C	Core (Watts) (1.0V supply)		PCIe Digital (Watts) (1.0V supply)		PCIe Analog (Watts) (1.0V supply)		PCIe Termination (Watts) (1.5V supply)		I/O (Watts) (3.3V supply)		Total (Watts)	
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max
8/8	472	546	697	905	266	345	354	440	1	3	1.97	
	0.47	0.60	0.70	1.00	0.27	0.38	0.53	0.69	0.003	0.01		

Table 14 PES16NT2 Power Consumption

## DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 12.

Note: See Table 7, Pin Characteristics, for a complete I/O listing.

I/O Type	Parameter	Description	Min <sup>1</sup>	Typ <sup>1</sup>	Max <sup>1</sup>	Unit	Conditions
Serial Link	PCIe Transmit						
	$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	800		1200	mV	
	$V_{TX-DE-RATIO}$	De-emphasized differential output voltage	-3		-4	dB	
	$V_{TX-DC-CM}$	DC Common mode voltage	-0.1	1	3.7	V	
	$V_{TX-CM-ACP}$	RMS AC peak common mode output voltage			20	mV	
	$V_{TX-CM-DC-active-idle-delta}$	Abs delta of DC common mode voltage between L0 and idle			100	mV	
	$V_{TX-CM-DC-line-delta}$	Abs delta of DC common mode voltage between D+ and D-			25	mV	
Serial Link (cont.)	$V_{TX-RCV-Detect}$	Voltage change during receiver detection			600	mV	
	$RL_{TX-DIFF}$	Transmitter Differential Return loss	12			dB	
	$RL_{TX-CM}$	Transmitter Common Mode Return loss	6			dB	
	$Z_{TX-DEFF-DC}$	DC Differential TX impedance	80	100	120	$\Omega$	
	$Z_{OSE}$	Single ended TX Impedance	40	50	60	$\Omega$	
	Transmitter Eye Diagram	TX Eye Height (De-emphasized bits)	505	650		mV	
	Transmitter Eye Diagram	TX Eye Height (Transition bits)	800	950		mV	
PCIe Receive							
	$V_{RX-DIFFp-p}$	Differential input voltage (peak-to-peak)	175		1200	mV	
	$V_{RX-CM-AC}$	Receiver common-mode voltage for AC coupling			150	mV	
	$RL_{RX-DIFF}$	Receiver Differential Return Loss	15			dB	
	$RL_{RX-CM}$	Receiver Common Mode Return Loss	6			dB	
	$Z_{RX-DIFF-DC}$	Differential input impedance (DC)	80	100	120	$\Omega$	
	$Z_{RX-COMM-DC}$	Single-ended input impedance	40	50	60	$\Omega$	
	$Z_{RX-COMM-HIGH-Z-DC}$	Powered down input common mode impedance (DC)	200k	350k		$\Omega$	
	$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65		175	mV	
PCIe REFCLK							
	$C_{IN}$	Input Capacitance	1.5	—		pF	

Table 15 DC Electrical Characteristics (Part 1 of 2)

I/O Type	Parameter	Description	Min <sup>1</sup>	Typ <sup>1</sup>	Max <sup>1</sup>	Unit	Conditions
<b>Other I/Os</b>							
LOW Drive Output	I <sub>OL</sub>		—	2.5	—	mA	V <sub>OL</sub> = 0.4v
	I <sub>OH</sub>		—	-5.5	—	mA	V <sub>OH</sub> = 1.5V
High Drive Output	I <sub>OL</sub>		—	12.0	—	mA	V <sub>OL</sub> = 0.4v
	I <sub>OH</sub>		—	-20.0	—	mA	V <sub>OH</sub> = 1.5V
Schmitt Trigger Input (STI)	V <sub>IL</sub>		-0.3	—	0.8	V	—
	V <sub>IH</sub>		2.0	—	V <sub>DDIO</sub> + 0.5	V	—
Input	V <sub>IL</sub>		-0.3	—	0.8	V	—
	V <sub>IH</sub>		2.0	—	V <sub>DDIO</sub> + 0.5	V	—
Capacitance	C <sub>IN</sub>		—	—	8.5	pF	—
Leakage	Inputs		—	—	± 10	µA	V <sub>DDIO</sub> (max)
	I/O <sub>LEAK W/o Pull-ups/downs</sub>		—	—	± 10	µA	V <sub>DDIO</sub> (max)
	I/O <sub>LEAK WITH Pull-ups/downs</sub>		—	—	± 80	µA	V <sub>DDIO</sub> (max)

Table 15 DC Electrical Characteristics (Part 2 of 2)

<sup>1</sup>. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.0a.

## Package Pinout — 484-BGA Signal Pinout for PES16NT2

The following table lists the pin numbers and signal names for the PES16NT2 device.

Advance Information

Pin	Function	Alt									
A1	V <sub>SS</sub>		B13	PEATN03		D3	V <sub>SS</sub>		E15	V <sub>TT</sub> PE	
A2	V <sub>SS</sub>		B14	V <sub>SS</sub>		D4	PEARN07		E16	V <sub>DD</sub> PE	
A3	V <sub>DD</sub> CORE		B15	PEATP02		D5	V <sub>SS</sub>		E17	V <sub>SS</sub>	
A4	V <sub>SS</sub>		B16	V <sub>SS</sub>		D6	PEARP06		E18	V <sub>SS</sub>	
A5	PEATN07		B17	PEATN01		D7	V <sub>TT</sub> PE		E19	PECRN07	
A6	V <sub>SS</sub>		B18	V <sub>SS</sub>		D8	PEARN05		E20	PECRP07	
A7	PEATN06		B19	PEATP00		D9	V <sub>TT</sub> PE		E21	V <sub>SS</sub>	
A8	V <sub>SS</sub>		B20	V <sub>SS</sub>		D10	PEARP04		E22	V <sub>SS</sub>	
A9	PEATN05		B21	V <sub>SS</sub>		D11	V <sub>DD</sub> PE		F1	V <sub>SS</sub>	
A10	V <sub>SS</sub>		B22	V <sub>SS</sub>		D12	PEARP03		F2	V <sub>SS</sub>	
A11	PEATN04		C1	V <sub>DD</sub> CORE		D13	V <sub>SS</sub>		F3	V <sub>DD</sub> CORE	
A12	V <sub>SS</sub>		C2	V <sub>DD</sub> CORE		D14	PEARN02		F4	V <sub>SS</sub>	
A13	PEATP03		C3	V <sub>DD</sub> CORE		D15	V <sub>SS</sub>		F5	V <sub>SS</sub>	
A14	V <sub>SS</sub>		C4	PEARP07		D16	PEARP01		F6	V <sub>DD</sub> IO	
A15	PEATN02		C5	V <sub>SS</sub>		D17	V <sub>SS</sub>		F7	V <sub>SS</sub>	
A16	V <sub>SS</sub>		C6	PEARN06		D18	PEARN00		F8	V <sub>DD</sub> PE	
A17	PEATP01		C7	V <sub>SS</sub>		D19	V <sub>SS</sub>		F9	V <sub>DD</sub> APE	
A18	V <sub>SS</sub>		C8	PEARP05		D20	V <sub>SS</sub>		F10	V <sub>DD</sub> APE	
A19	PEATN00		C9	V <sub>SS</sub>		D21	PECTP07		F11	V <sub>DD</sub> PE	
A20	V <sub>SS</sub>		C10	PEARN04		D22	PECTN07		F12	V <sub>DD</sub> PE	
A21	V <sub>SS</sub>		C11	V <sub>SS</sub>		E1	V <sub>DD</sub> CORE		F13	V <sub>DD</sub> APE	
A22	V <sub>SS</sub>		C12	PEARN03		E2	V <sub>DD</sub> CORE		F14	V <sub>DD</sub> APE	
B1	V <sub>SS</sub>		C13	V <sub>TT</sub> PE		E3	V <sub>SS</sub>		F15	V <sub>DD</sub> PE	
B2	V <sub>SS</sub>		C14	PEARP02		E4	V <sub>DD</sub> CORE		F16	V <sub>SS</sub>	
B3	V <sub>DD</sub> CORE		C15	V <sub>TT</sub> PE		E5	V <sub>SS</sub>		F17	V <sub>SS</sub>	
B4	V <sub>SS</sub>		C16	PEARN01		E6	V <sub>SS</sub>		F18	V <sub>DD</sub> PE	
B5	PEATP07		C17	V <sub>SS</sub>		E7	V <sub>TT</sub> PE		F19	V <sub>SS</sub>	
B6	V <sub>SS</sub>		C18	PEARP00		E8	V <sub>DD</sub> PE		F20	V <sub>SS</sub>	
B7	PEATP06		C19	V <sub>SS</sub>		E9	V <sub>DD</sub> APE		F21	PECTP06	
B8	V <sub>SS</sub>		C20	V <sub>DD</sub> CORE		E10	V <sub>TT</sub> PE		F22	PECTN06	
B9	PEATP05		C21	V <sub>DD</sub> CORE		E11	V <sub>SS</sub>		G1	V <sub>DD</sub> CORE	
B10	V <sub>SS</sub>		C22	V <sub>DD</sub> CORE		E12	V <sub>DD</sub> PE		G2	V <sub>DD</sub> CORE	
B11	PEATP04		D1	V <sub>SS</sub>		E13	V <sub>TT</sub> PE		G3	V <sub>SS</sub>	
B12	V <sub>SS</sub>		D2	V <sub>SS</sub>		E14	V <sub>SS</sub>		G4	V <sub>DD</sub> CORE	

Table 16 PES16NT2 484-pin Signal Pin-Out (Part 1 of 4)

Pin	Function	Alt									
G5	V <sub>SS</sub>		H20	V <sub>SS</sub>		K13	V <sub>DD</sub> CORE		M6	V <sub>DD</sub> CORE	
G6	V <sub>SS</sub>		H21	PECTP05		K14	V <sub>SS</sub>		M7	V <sub>SS</sub>	
G7	V <sub>DD</sub> IO		H22	PECTN05		K15	V <sub>DD</sub> CORE		M8	V <sub>SS</sub>	
G8	V <sub>SS</sub>		J1	V <sub>SS</sub>		K16	V <sub>SS</sub>		M9	V <sub>DD</sub> CORE	
G9	V <sub>SS</sub>		J2	V <sub>DD</sub> CORE		K17	V <sub>DD</sub> APE		M10	V <sub>SS</sub>	
G10	V <sub>SS</sub>		J3	V <sub>SS</sub>		K18	V <sub>SS</sub>		M11	V <sub>DD</sub> CORE	
G11	V <sub>DD</sub> IO		J4	V <sub>DD</sub> CORE		K19	V <sub>TT</sub> PE		M12	V <sub>SS</sub>	
G12	V <sub>SS</sub>		J5	V <sub>SS</sub>		K20	V <sub>TT</sub> PE		M13	V <sub>DD</sub> CORE	
G13	V <sub>SS</sub>		J6	V <sub>DD</sub> IO		K21	PECTN04		M14	V <sub>SS</sub>	
G14	V <sub>DD</sub> APE		J7	V <sub>SS</sub>		K22	PECTP04		M15	V <sub>DD</sub> CORE	
G15	V <sub>SS</sub>		J8	V <sub>DD</sub> CORE		L1	V <sub>SS</sub>		M16	V <sub>SS</sub>	
G16	V <sub>DD</sub> IO		J9	V <sub>SS</sub>		L2	V <sub>DD</sub> CORE		M17	V <sub>DD</sub> CORE	
G17	V <sub>DD</sub> IO		J10	V <sub>DD</sub> CORE		L3	V <sub>SS</sub>		M18	V <sub>SS</sub>	
G18	V <sub>SS</sub>		J11	V <sub>SS</sub>		L4	V <sub>DD</sub> CORE		M19	V <sub>SS</sub>	
G19	PECRP06		J12	V <sub>DD</sub> CORE		L5	V <sub>SS</sub>		M20	V <sub>SS</sub>	
G20	PECRN06		J13	V <sub>SS</sub>		L6	V <sub>DD</sub> IO		M21	PECTP03	
G21	V <sub>SS</sub>		J14	V <sub>DD</sub> CORE		L7	V <sub>SS</sub>		M22	PECTN03	
G22	V <sub>SS</sub>		J15	V <sub>SS</sub>		L8	V <sub>DD</sub> CORE		N1	V <sub>SS</sub>	
H1	V <sub>SS</sub>		J16	V <sub>DD</sub> APE		L9	V <sub>SS</sub>		N2	V <sub>SS</sub>	
H2	V <sub>SS</sub>		J17	V <sub>SS</sub>		L10	V <sub>DD</sub> CORE		N3	V <sub>DD</sub> CORE	
H3	V <sub>DD</sub> CORE		J18	V <sub>DD</sub> APE		L11	V <sub>SS</sub>		N4	V <sub>DD</sub> CORE	
H4	V <sub>SS</sub>		J19	PECRN05		L12	V <sub>DD</sub> CORE		N5	V <sub>DD</sub> APE	
H5	V <sub>SS</sub>		J20	PECRP05		L13	V <sub>SS</sub>		N6	V <sub>DD</sub> APE	
H6	V <sub>DD</sub> CORE		J21	V <sub>SS</sub>		L14	V <sub>DD</sub> CORE		N7	V <sub>SS</sub>	
H7	V <sub>SS</sub>		J22	V <sub>SS</sub>		L15	V <sub>SS</sub>		N8	V <sub>DD</sub> CORE	
H8	V <sub>DD</sub> CORE		K1	V <sub>SS</sub>		L16	V <sub>SS</sub>		N9	V <sub>SS</sub>	
H9	V <sub>SS</sub>		K2	V <sub>SS</sub>		L17	V <sub>DD</sub> PE		N10	V <sub>DD</sub> CORE	
H10	V <sub>DD</sub> CORE		K3	V <sub>DD</sub> CORE		L18	V <sub>DD</sub> PE		N11	V <sub>SS</sub>	
H11	V <sub>SS</sub>		K4	V <sub>SS</sub>		L19	PECRN04		N12	V <sub>DD</sub> CORE	
H12	V <sub>SS</sub>		K5	V <sub>SS</sub>		L20	PECRP04		N13	V <sub>SS</sub>	
H13	V <sub>DD</sub> CORE		K6	V <sub>DD</sub> CORE		L21	V <sub>SS</sub>		N14	V <sub>DD</sub> CORE	
H14	V <sub>SS</sub>		K7	V <sub>SS</sub>		L22	V <sub>SS</sub>		N15	V <sub>SS</sub>	
H15	V <sub>DD</sub> CORE		K8	V <sub>SS</sub>		M1	V <sub>SS</sub>		N16	V <sub>SS</sub>	
H16	V <sub>SS</sub>		K9	V <sub>DD</sub> CORE		M2	V <sub>SS</sub>		N17	V <sub>DD</sub> APE	
H17	V <sub>DD</sub> PE		K10	V <sub>SS</sub>		M3	V <sub>SS</sub>		N18	V <sub>DD</sub> APE	
H18	V <sub>TT</sub> PE		K11	V <sub>DD</sub> CORE		M4	V <sub>SS</sub>		N19	PECRP03	
H19	V <sub>TT</sub> PE		K12	V <sub>SS</sub>		M5	V <sub>SS</sub>		N20	PECRN03	

Table 16 PES16NT2 484-pin Signal Pin-Out (Part 2 of 4)

Pin	Function	Alt									
N21	V <sub>TT</sub> PE		R14	V <sub>SS</sub>		U7	V <sub>SS</sub>		V22	PECTN00	
N22	V <sub>TT</sub> PE		R15	V <sub>SS</sub>		U8	V <sub>SS</sub>		W1	V <sub>SS</sub>	
P1	PEREFCLKP0		R16	V <sub>SS</sub>		U9	V <sub>SS</sub>		W2	V <sub>DD</sub> CORE	
P2	PEREFCLKN0		R17	V <sub>DD</sub> APE		U10	V <sub>SS</sub>		W3	V <sub>SS</sub>	
P3	V <sub>SS</sub>		R18	V <sub>DD</sub> APE		U11	V <sub>SS</sub>		W4	V <sub>DD</sub> CORE	
P4	V <sub>SS</sub>		R19	PECRN02		U12	V <sub>SS</sub>		W5	V <sub>SS</sub>	
P5	V <sub>SS</sub>		R20	PECRP02		U13	V <sub>SS</sub>		W6	V <sub>DD</sub> IO	
P6	V <sub>DD</sub> IO		R21	V <sub>SS</sub>		U14	V <sub>SS</sub>		W7	V <sub>SS</sub>	
P7	V <sub>SS</sub>		R22	V <sub>SS</sub>		U15	V <sub>SS</sub>		W8	V <sub>DD</sub> IO	
P8	V <sub>SS</sub>		T1	V <sub>SS</sub>		U16	V <sub>DD</sub> CORE		W9	V <sub>DD</sub> CORE	
P9	V <sub>DD</sub> CORE		T2	V <sub>SS</sub>		U17	V <sub>DD</sub> CORE		W10	V <sub>SS</sub>	
P10	V <sub>SS</sub>		T3	V <sub>SS</sub>		U18	V <sub>DD</sub> CORE		W11	V <sub>DD</sub> IO	
P11	V <sub>DD</sub> CORE		T4	V <sub>SS</sub>		U19	PECRP01		W12	V <sub>SS</sub>	
P12	V <sub>SS</sub>		T5	V <sub>SS</sub>		U20	PECRN01		W13	V <sub>SS</sub>	
P13	V <sub>DD</sub> CORE		T6	V <sub>DD</sub> IO		U21	V <sub>DD</sub> PE		W14	V <sub>DD</sub> IO	
P14	V <sub>SS</sub>		T7	V <sub>DD</sub> IO		U22	V <sub>TT</sub> PE		W15	V <sub>SS</sub>	
P15	V <sub>DD</sub> CORE		T8	V <sub>DD</sub> IO		V1	V <sub>DD</sub> CORE		W16	V <sub>DD</sub> IO	
P16	V <sub>SS</sub>		T9	V <sub>DD</sub> CORE		V2	V <sub>SS</sub>		W17	V <sub>SS</sub>	
P17	V <sub>DD</sub> PE		T10	V <sub>DD</sub> IO		V3	V <sub>DD</sub> CORE		W18	V <sub>SS</sub>	
P18	V <sub>DD</sub> PE		T11	V <sub>DD</sub> CORE		V4	V <sub>SS</sub>		W19	PECRN00	
P19	V <sub>SS</sub>		T12	V <sub>DD</sub> CORE		V5	V <sub>SS</sub>		W20	PECRP00	
P20	V <sub>SS</sub>		T13	V <sub>DD</sub> IO		V6	V <sub>SS</sub>		W21	V <sub>SS</sub>	
P21	PECTP02		T14	V <sub>DD</sub> IO		V7	V <sub>DD</sub> CORE		W22	V <sub>SS</sub>	
P22	PECTN02		T15	V <sub>DD</sub> CORE		V8	V <sub>SS</sub>		Y1	V <sub>DD</sub> CORE	
R1	V <sub>SS</sub>		T16	V <sub>DD</sub> IO		V9	V <sub>SS</sub>		Y2	V <sub>SS</sub>	
R2	V <sub>SS</sub>		T17	V <sub>DD</sub> IO		V10	V <sub>DD</sub> CORE		Y3	V <sub>DD</sub> CORE	
R3	V <sub>DD</sub> CORE		T18	V <sub>SS</sub>		V11	V <sub>SS</sub>		Y4	V <sub>DD</sub> CORE	
R4	V <sub>DD</sub> CORE		T19	V <sub>SS</sub>		V12	V <sub>DD</sub> CORE		Y5	JTAG_TDO	
R5	V <sub>SS</sub>		T20	V <sub>DD</sub> APE		V13	V <sub>SS</sub>		Y6	MSMBADDR_1	
R6	V <sub>DD</sub> CORE		T21	PECTP01		V14	V <sub>DD</sub> CORE		Y7	MSMBADDR_4	
R7	V <sub>SS</sub>		T22	PECTN01		V15	V <sub>SS</sub>		Y8	SSMBADDR_1	
R8	V <sub>SS</sub>		U1	V <sub>SS</sub>		V16	V <sub>DD</sub> CORE		Y9	SSMBADDR_5	
R9	V <sub>SS</sub>		U2	V <sub>SS</sub>		V17	V <sub>SS</sub>		Y10	CCLKUS	
R10	V <sub>SS</sub>		U3	V <sub>SS</sub>		V18	V <sub>DD</sub> CORE		Y11	CCLKDS	
R11	V <sub>SS</sub>		U4	V <sub>DD</sub> CORE		V19	V <sub>DD</sub> PE		Y12	PEALREV	
R12	V <sub>SS</sub>		U5	V <sub>SS</sub>		V20	V <sub>TT</sub> PE		Y13	SWMODE_1	
R13	V <sub>SS</sub>		U6	V <sub>SS</sub>		V21	PECTP00		Y14	PECLREV	

Table 16 PES16NT2 484-pin Signal Pin-Out (Part 3 of 4)

Advance Information

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
Y15	RSTHALT		AA6	JTAG_TRST_N		AA19	REFCLKM		AB10	SSMBCLK	
Y16	GPIO_02	1	AA7	MSMBADDR_3		AA20	V <sub>DDCORE</sub>		AB11	V <sub>SS</sub>	
Y17	GPIO_05	1	AA8	MSMBDAT		AA21	V <sub>SS</sub>		AB12	V <sub>SS</sub>	
Y18	MSMBSMODE		AA9	SSMBADDR_3		AA22	V <sub>SS</sub>		AB13	V <sub>SS</sub>	
Y19	V <sub>SS</sub>		AA10	SSMBDAT		AB1	V <sub>SS</sub>		AB14	SWMODE_2	
Y20	V <sub>SS</sub>		AA11	V <sub>SS</sub>		AB2	V <sub>SS</sub>		AB15	PERSTN	
Y21	PEREFCLKP1		AA12	V <sub>DDCORE</sub>		AB3	V <sub>SS</sub>		AB16	GPIO_00	
Y22	PEREFCLKN1		AA13	SWMODE_0		AB4	V <sub>SS</sub>		AB17	GPIO_03	
AA1	V <sub>SS</sub>		AA14	SWMODE_3		AB5	JTAG_TCK		AB18	GPIO_06	
AA2	V <sub>SS</sub>		AA15	PENTBRSTN		AB6	JTAG_TMS		AB19	V <sub>SS</sub>	
AA3	V <sub>DDCORE</sub>		AA16	GPIO_01	1	AB7	MSMBADDR_2		AB20	V <sub>SS</sub>	
AA4	V <sub>DDCORE</sub>		AA17	GPIO_04	1	AB8	SSMBCLK		AB21	V <sub>SS</sub>	
AA5	JTAG_TDI		AA18	GPIO_07		AB9	SSMBADDR_2		AB22	V <sub>SS</sub>	

Table 16 PES16NT2 484-pin Signal Pin-Out (Part 4 of 4)

### Alternate Signal Functions

Pin	GPIO	Alternate
AA16	GPIO_1	PECRSTN
Y16	GPIO_2	PALINKUPN
AA17	GPIO_4	PCLINKUPN
Y17	GPIO_5	FAILOVERP

Table 17 PES16NT2 Alternate Signal Functions

## Power Pins

$V_{DDCore}$	$V_{DDCore}$	$V_{DDCore}$	$V_{DDCore}$	$V_{DDIO}$	$V_{DDPE}$	$V_{DDAPE}$	$V_{TTPE}$
A3	J2	M13	U16	F6	D11	E9	C13
B3	J4	M15	U17	G7	E8	F9	C15
C1	J8	M17	U18	G11	E12	F10	D7
C2	J10	N3	V1	G16	E16	F13	D9
C3	J12	N4	V3	G17	F8	F14	E7
C20	J14	N8	V7	J6	F11	G14	E10
C21	K3	N10	V10	L6	F12	J16	E13
C22	K6	N12	V12	P6	F15	J18	E15
E1	K9	N14	V14	T6	F18	K17	H18
E2	K11	P9	V16	T7	H17	N5	H19
E4	K13	P11	V18	T8	L17	N6	K19
F3	K15	P13	W2	T10	L18	N17	K20
G1	L2	P15	W4	T13	P17	N18	N21
G2	L4	R3	W9	T14	P18	R17	N22
G4	L8	R4	Y1	T16	U21	R18	U22
H3	L10	R6	Y3	T17	V19	T20	V20
H6	L12	T9	Y4	W6			
H8	L14	T11	AA3	W8			
H10	M6	T12	AA4	W11			
H13	M9	T15	AA12	W14			
H15	M11	U4	AA20	W16			

Table 18 PES16TN2 Power Pins

## Ground Pins

| $V_{SS}$ |
|----------|----------|----------|----------|----------|----------|----------|
| A1       | D2       | G13      | K10      | N9       | T3       | W10      |
| A2       | D3       | G15      | K12      | N11      | T4       | W12      |
| A4       | D5       | G18      | K14      | N13      | T5       | W13      |
| A6       | D13      | G21      | K16      | N15      | T18      | W15      |
| A8       | D15      | G22      | K18      | N16      | T19      | W17      |
| A10      | D17      | H1       | L1       | P3       | U1       | W18      |
| A12      | D19      | H2       | L3       | P4       | U2       | W21      |
| A14      | D20      | H4       | L5       | P5       | U3       | W22      |
| A16      | E3       | H5       | L7       | P7       | U5       | Y2       |
| A18      | E5       | H7       | L9       | P8       | U6       | Y19      |
| A20      | E6       | H9       | L11      | P10      | U7       | Y20      |
| A21      | E11      | H11      | L13      | P12      | U8       | AA1      |
| A22      | E14      | H12      | L15      | P14      | U9       | AA2      |
| B1       | E17      | H14      | L16      | P16      | U10      | AA11     |
| B2       | E18      | H16      | L21      | P19      | U11      | AA21     |
| B4       | E21      | H20      | L22      | P20      | U12      | AA22     |
| B6       | E22      | J1       | M1       | R1       | U13      | AB1      |
| B8       | F1       | J3       | M2       | R2       | U14      | AB2      |
| B10      | F2       | J5       | M3       | R5       | U15      | AB3      |
| B12      | F4       | J7       | M4       | R7       | V2       | AB4      |
| B14      | F5       | J9       | M5       | R8       | V4       | AB11     |
| B16      | F7       | J11      | M7       | R9       | V5       | AB12     |
| B18      | F16      | J13      | M8       | R10      | V6       | AB13     |
| B20      | F17      | J15      | M10      | R11      | V8       | AB19     |
| B21      | F19      | J17      | M12      | R12      | V9       | AB20     |
| B22      | F20      | J21      | M14      | R13      | V11      | AB21     |
| C5       | G3       | J22      | M16      | R14      | V13      | AB22     |
| C7       | G5       | K1       | M18      | R15      | V15      |          |
| C9       | G6       | K2       | M19      | R16      | V17      |          |
| C11      | G8       | K4       | M20      | R21      | W1       |          |
| C17      | G9       | K5       | N1       | R22      | W3       |          |
| C19      | G10      | K7       | N2       | T1       | W5       |          |
| D1       | G12      | K8       | N7       | T2       | W7       |          |

Table 19 PES16NT2 Ground Pins

## Signals Listed Alphabetically

Signal Name	I/O Type	Location	Signal Category
CCLKDS	I	Y11	System
CCLKUS	I	Y10	
GPIO_00	I/O	AB16	General Purpose Input/Output
GPIO_01	I/O	AA16	
GPIO_02	I/O	Y16	
GPIO_03	I/O	AB17	
GPIO_04	I/O	AA17	
GPIO_05	I/O	Y17	
GPIO_06	I/O	AB18	
GPIO_07	I/O	AA18	
JTAG_TCK	I	AB05	JTAG
JTAG_TDI	I	AA05	
JTAG_TDO	O	Y5	
JTAG_TMS	I	AB6	
JTAG_TRST_N	I	AA6	
MSMBADDR_1	I	Y6	SMBus
MSMBADDR_2	I	AB7	
MSMBADDR_3	I	AA7	
MSMBADDR_4	I	Y7	
MSMBCLK	I/O	AB8	PCI Express
MSMBDAT	I/O	AA8	
MSMBSMODE	I	Y18	
PEALREV	I	Y12	
PEARN00	I	D18	
PEARN01	I	C16	
PEARN02	I	D14	
PEARN03	I	C12	
PEARN04	I	C10	
PEARN05	I	D8	
PEARN06	I	C6	
PEARN07	I	D4	
PEARP00	I	C18	
PEARP01	I	D16	
PEARP02	I	C14	

Table 20 89PES16NT2 Alphabetical Signal List (Part 1 of 4)

Signal Name	I/O Type	Location	Signal Category
PEARP03	I	D12	PCI Express (cont.)
PEARP04	I	D10	
PEARP05	I	C8	
PEARP06	I	D6	
PEARP07	I	C4	
PEATN00	O	A19	
PEATN01	O	B17	
PEATN02	O	A15	
PEATN03	O	B13	
PEATN04	O	A11	
PEATN05	O	A9	
PEATN06	O	A7	
PEATN07	O	A5	
PEATP00	O	B19	
PEATP01	O	A17	
PEATP02	O	B15	
PEATP03	O	A13	
PEATP04	O	B11	
PEATP05	O	B9	
PEATP06	O	B7	
PEATP07	O	B5	
PECLREV	I	Y14	PCI Express (cont.)
PECRN00	I	W19	
PECRN01	I	U20	
PECRN02	I	R19	
PECRN03	I	N20	
PECRN04	I	L19	
PECRN05	I	J19	
PECRN06	I	G20	
PECRN07	I	E19	
PECRP00	I	W20	
PECRP01	I	U19	
PECRP02	I	R20	
PECRP03	I	N19	
PECRP04	I	L20	
PECRP05	I	J20	

Table 20 89PES16NT2 Alphabetical Signal List (Part 2 of 4)

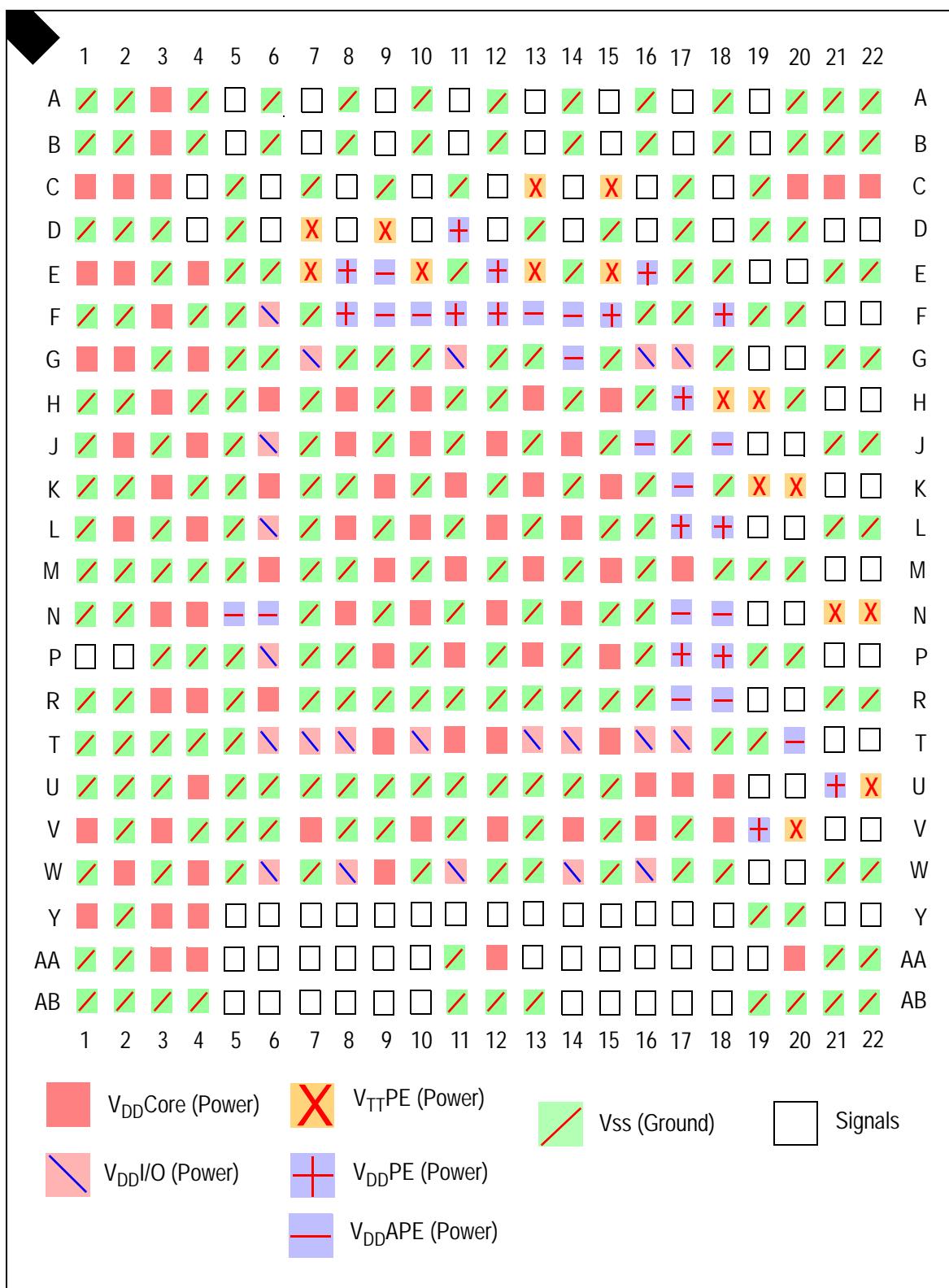
Signal Name	I/O Type	Location	Signal Category
PECRP06	I	G19	PCI Express (cont.)
PECRP07	I	E20	
PECTN00	O	V22	
PECTN01	O	T22	
PECTN02	O	P22	
PECTN03	O	M22	
PECTN04	O	K21	
PECTN05	O	H22	
PECTN06	O	F22	
PECTN07	O	D22	
PECTP00	O	V21	
PECTP01	O	T21	
PECTP02	O	P21	
PECTP03	O	M21	
PECTP04	O	K22	
PECTP05	O	H21	
PECTP06	O	F21	
PECTP07	O	D21	
PENTBRSTN	I	AA15	System
PEREFCLKN0	I	P2	PCI Express
PEREFCLKN1	I	Y22	
PEREFCLKP0	I	P1	
PEREFCLKP1	I	Y21	
PERSTN	I	AB15	
REFCLKM	I	AA19	PCI Express
RSTHALT	I	Y15	System
SSMBADDR_1	I	Y8	SMBus
SSMBADDR_2	I	AB9	
SSMBADDR_3	I	AA9	
SSMBADDR_5	I	Y9	
SSMBCLK	I/O	AB10	
SSMBDAT	I/O	AA10	

Table 20 89PES16NT2 Alphabetical Signal List (Part 3 of 4)

Signal Name	I/O Type	Location	Signal Category	
SWMODE_0	I	AA13	System	
SWMODE_1	I	Y13		
SWMODE_2	I	AB14		
SWMODE_3	I	AA14		
V <sub>DD</sub> CORE, V <sub>DD</sub> APE, V <sub>DD</sub> IO, V <sub>DD</sub> PE, V <sub>TT</sub> PE	See Table 18 for a listing of power pins.			
V <sub>SS</sub>	See Table 19 for a listing of ground pins.			

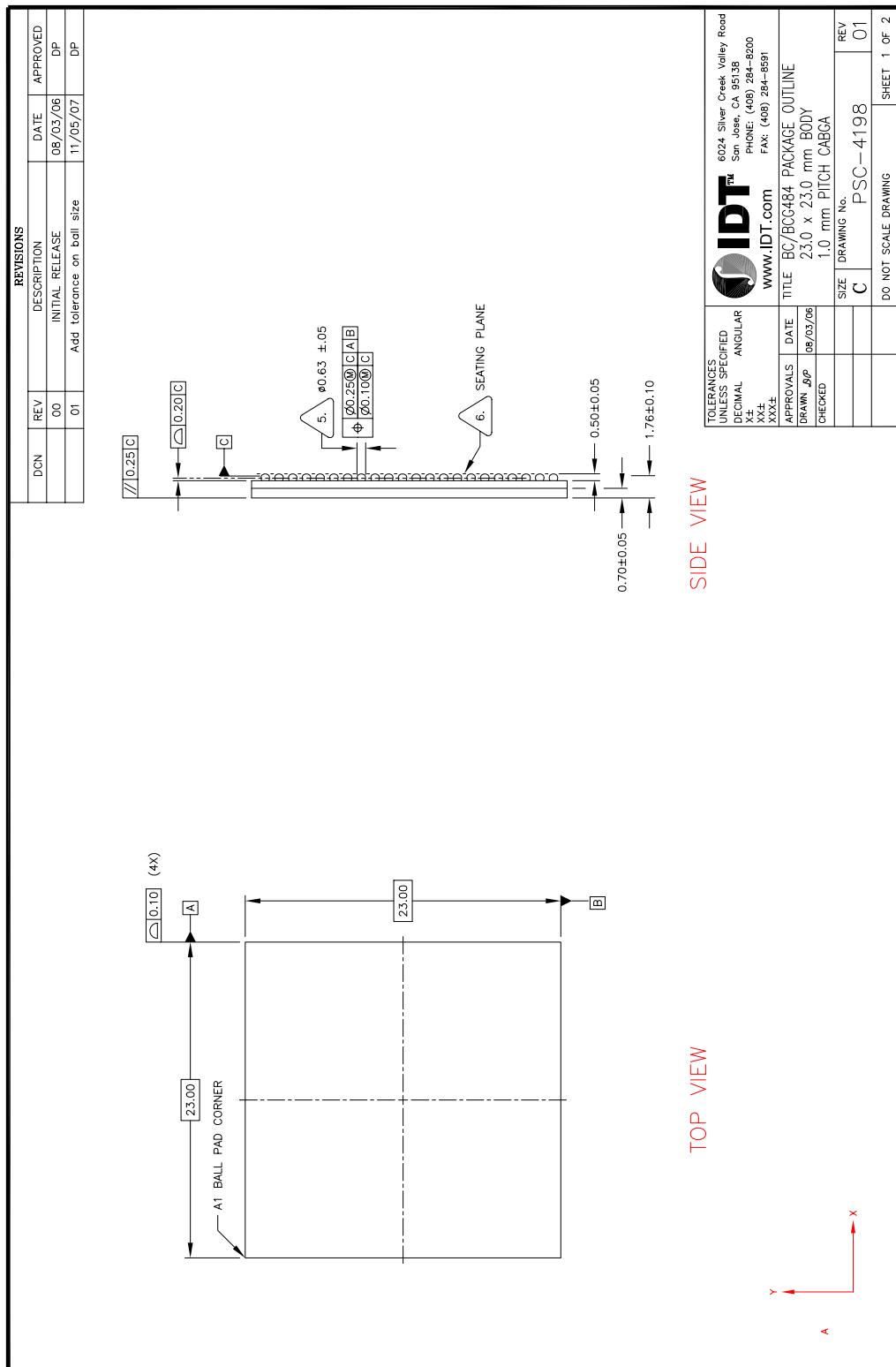
Table 20 89PES16NT2 Alphabetical Signal List (Part 4 of 4)

## PES16NT2 Pinout — Top View



Advance Information

## PES16NT2 Package Drawing — 484-Pin BC484/BCG484



Advance Information

## PES16NT2 Package Drawing — Page Two

REVISIONS			
DCN	REV	DESCRIPTION	DATE APPROVED
	00	INITIAL RELEASE	08/03/06 DP
	01	Add tolerance on ball size	11/05/07 DP

A1 BALL PAD CORNER

22 20 18 16 14 12 10 8 6 4 2 1

1.00

(0.01)

(1.00)

(1.00) ← → (1.00)

A B C D E F G H J K L M N P R T U V Y AA AB

**BOTTOM VIEW**

484 SOLDER BALLS

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.
2. THE BASIC SOLDER BALL GRID PITCH IS 1.00mm.
3. THE MAXIMUM SOLDER BALL MATRIX SIZE IS 22 X 22.
4. THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS IS 484.
5. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. "A1" ID CORNER MUST BE IDENTIFIED. IDENTIFICATION MAY BE BY MEANS OF CHAMFER, METALLIZED OR INK MARK, INDENTATION OR OTHER FEATURE OF THE PACKAGE BODY.
8. THIS DRAWING CONFORMS TO THE JEDEC REGISTERED OUTLINE MS-034/A, VARIATION AAG-1 EXCEPT FOR A1, b, AND ~~aaa~~ DIMENSIONS.

TOLERANCES UNLESS SPECIFIED DECIMAL X± XX± XXX±	ANGULAR	DRAWN <i>As Is</i>	TITLE BC/BCG44 PACKAGE OUTLINE	6024 Silver Creek Valley Road San Jose CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591 <a href="http://www.IDT.com">www.IDT.com</a>
APPROVALS	DATE	08/03/06	SIZE 1.0 mm PITCH CABA	REV 01
CHECKED			DO NOT SCALE DRAWING	SHEET 2 OF 2

Advance Information

## Revision History

March 15, 2007: Initial publication of Advanced data sheet.

March 26, 2007: Revised pin list.

April 11, 2007: In Table 2, revised description of MSMBCLK.

June 1, 2007: Revised pins in Tables 16, 18, and 19 and in pinout graphic.

June 19, 2007: In Tables 16 and 20, changed the names of PEREFCLKN[2/1] to PEREFCLKN[1/0] and PEREFCLKP[2/1] to PEREFCLKP[1/0].

June 28, 2007: In the Features section, deleted reference to Hot-plug IO expander.

November 1, 2007: Changed package drawing to reflect correct ball/package dimensions.

November 6, 2007: Updated package drawing with solder ball tolerance added.

November 12, 2007: Updated SWMODE[3:0] field to include Transparent mode.

November 14, 2007: Added new parameter, Termination Resistor, to Table 8, Input Clock Requirements.

January 2, 2008: Added values to Table 14, Power Consumption.

January 14, 2008: Revised Typical values in Table 14, Power Consumption.

## Ordering Information

NN	A	AAA	NNAAN	AA	AA	A	Legend
Product Family	Operating Voltage	Device Family	Product Detail	Revision ID	Package	Temp Range	A = Alpha Character N = Numeric Character
						Blank	Commercial Temperature (0°C to +70°C Ambient)
					BC	BC484 484-ball CABGA	
					BCG	BCG484 484-ball CABGA, Green	
					ZA	Silicon revision	
					16NT2	16-lane, 2-port Non-Transparent	
					PES	PCI Express Switch	
					H	1.0V +/- 0.1V Core Voltage	
					89	Serial Switching Product	

### Valid Combinations

- 89HPES16NT2ZABC      484-ball CABGA package, Commercial Temperature  
 89HPES16NT2ZABCG      484-ball Green CABGA package, Commercial Temperature

Advance Information



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