



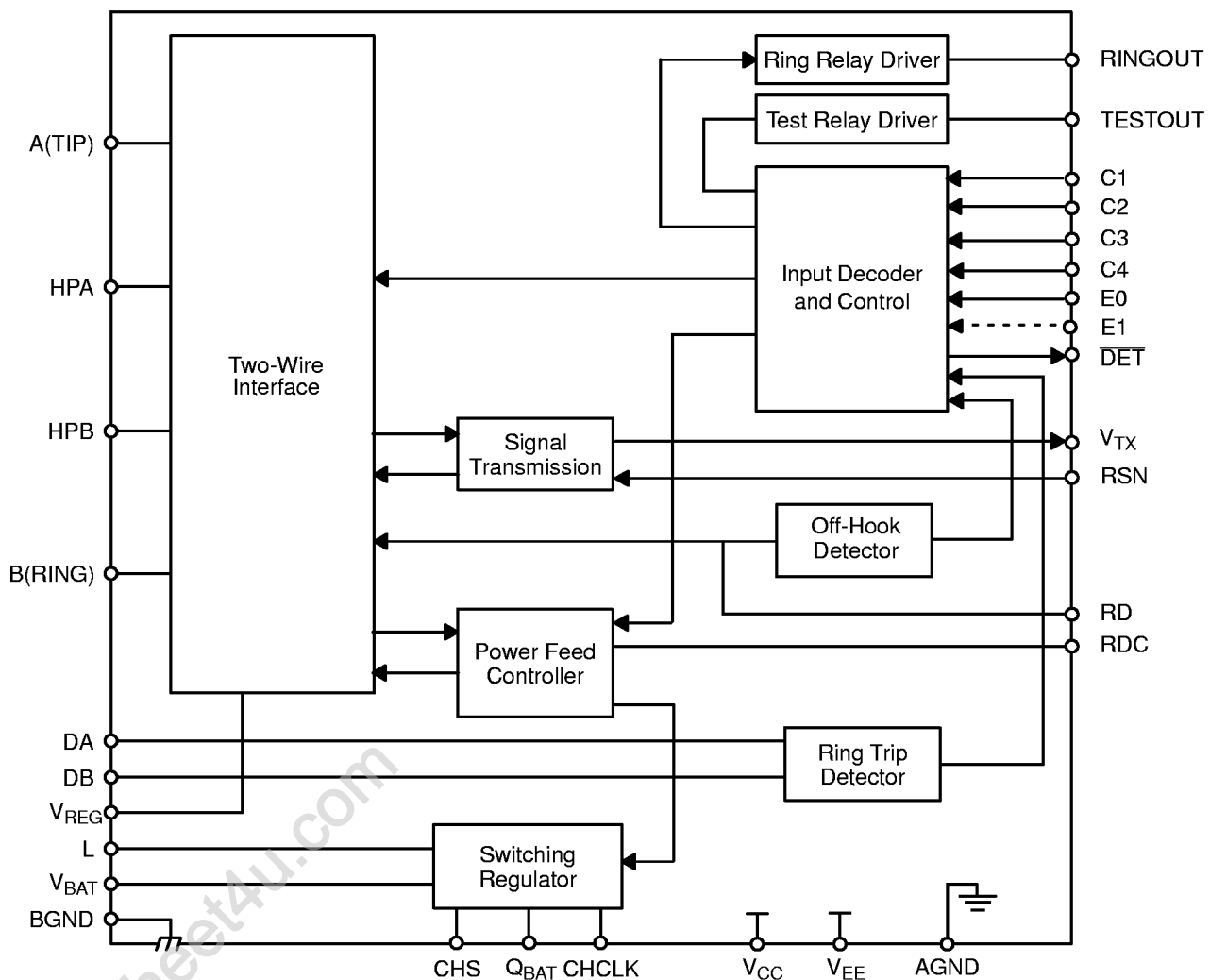
# Am79533I/Am79534I

## Subscriber Line Interface Circuit

### DISTINCTIVE CHARACTERISTICS

- Programmable constant current feed
- Programmable loop detect threshold
- Performs polarity reversal
- Tip open state for ground start lines
- Line feed characteristics independent of battery variations
- On-chip switching regulator for low power dissipation
- Two-wire impedance set by single external impedance
- On-hook transmission

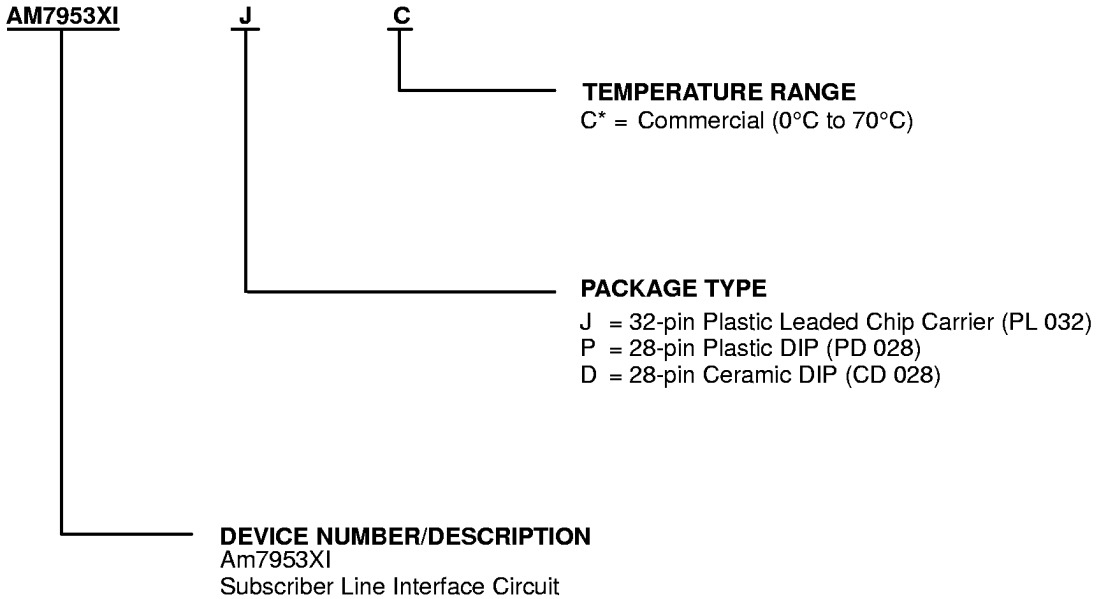
### BLOCK DIAGRAM



**ORDERING INFORMATION**

**Standard Products**

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
AM7953XI	DC, JC, PC

**Valid Combinations**

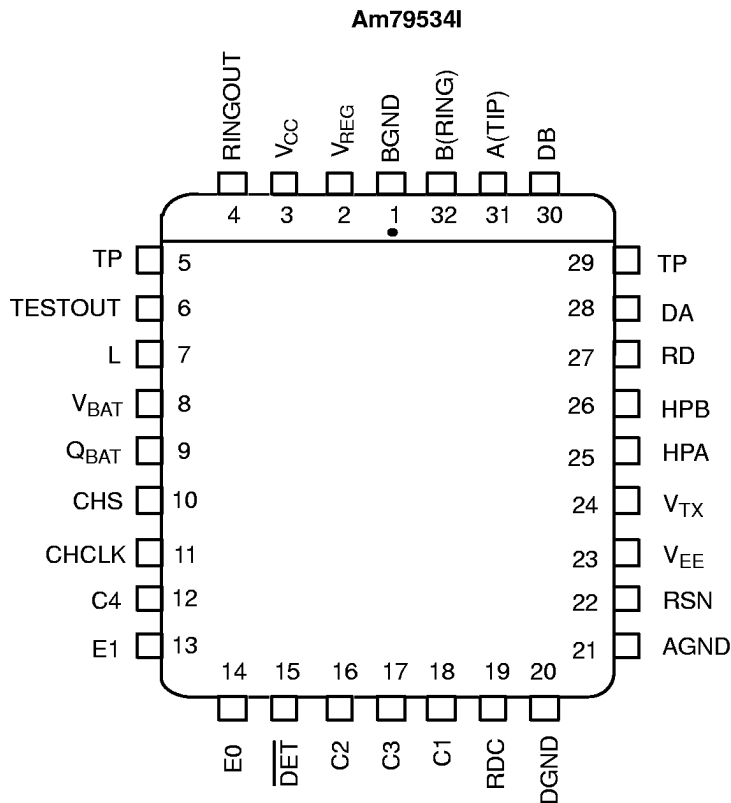
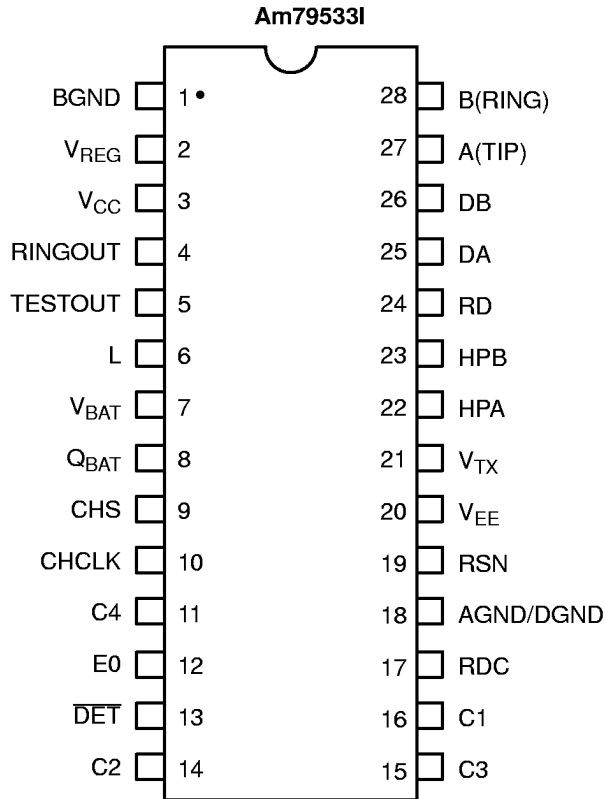
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

**Note:**

\* Specifications in this data sheet are guaranteed by testing from 0°C to +70°C. Performance from -40°C to +85°C is guaranteed by characterization and periodic sampling of production units..

# CONNECTION DIAGRAM

## Top View



**Note:**

Pin 1 is marked for orientation.

## PIN DESCRIPTION

### AGND/DGND

(Ground)

Analog and Digital ground.

*Note:* Analog and digital ground are connected internally to a single pin.

### A(TIP)

(Output)

Output of A(TIP) power amplifier.

### BGND

(Ground)

Battery (power) ground.

### B(RING)

(Output)

Output of B(RING) power amplifier.

### C3–C1

Decoder (Inputs)

TTL compatible. C3 is MSB and C1 is LSB.

### C4

Test Relay Driver Command (Input)

TTL compatible. A logic High enables the driver.

### CHCLK

Chopper Clock (Input)

Input to switching regulator (TTL compatible).  
Frequency = 256 kHz (Nominal).

### CHS

Chopper Stabilization (Input)

Connection for external stabilization components.

### DA

Ring Trip Negative (Input)

Negative input to ring trip comparator.

### DB

Ring Trip Positive (Input)

Positive input to ring trip comparator.

### DET

Detector (Output)

When enabled, a logic Low indicates that the selected detector is tripped. The detector is selected by the logic inputs (C3–C1, E0, and E1). The output is open-collector with a built-in pull-up resistor.

### E0

Read Enable (Input)

A logic High enables  $\overline{\text{DET}}$ . A logic Low disables  $\overline{\text{DET}}$ .

### E1

Ground Key Enable (Input)

When E0 is High, E1 = High connects the ground-key detector to  $\overline{\text{DET}}$ , and E1 = Low connects the off-hook or ring trip detector to  $\overline{\text{DET}}$ .

### HPA

A(TIP) side of high-pass filter capacitor.

### HPB

B(RING) side of high-pass filter capacitor.

### L

Switching Regulator Power Transistor (Output)

Connection point for filter inductor and anode of catch diode. This pin will have up to 60 volts of pulse waveform on it and must be isolated from sensitive circuits. Extreme care must be taken to keep the diode connections short because of the high currents and high di/dt.

### Q<sub>BAT</sub>

Quiet Battery

Filtered battery supply for the signal processing circuits.

### RD

Detect Resistor Pin

Threshold modification and filter point for the off-hook detector.

### RDC

DC Feed Resistor Pin

Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN). The sign of  $V_{\text{RDC}}$  is minus for normal polarity and plus for reverse polarity. The magnitude is typically 2.5 V.

### RINGOUT

Ring Relay Driver (Output)

Sourcing from  $V_{\text{CC}}$  with internal diode to Q<sub>BAT</sub>.

### RSN

Receive Summing Node (Input)

The metallic current (both AC and DC) between A(TIP) and B(RING) is equal to 1000 times the current into this pin. The networks that program receive gain, two-wire impedance, and feed current all connect to this node.

**TESTOUT****Test Relay Driver (Output)**

Sourcing from  $V_{CC}$  with internal diode to  $Q_{BAT}$ .

 **$V_{BAT}$** 

Battery supply.

 **$V_{CC}$** 

+5-V power supply.

 **$V_{EE}$** 

-5-V power supply.

 **$V_{REG}$** **Regulated Voltage (Input)**

Provides negative power supply for power amplifiers, connection point for inductor, filter capacitor and chopper stabilization.

 **$V_{TX}$** **Transmit Audio (Output)**

This output is a unity gain version of the A(TIP) and B(RING) metallic voltage. The other end of the two-wire input impedance programming network connects here.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature .....	-55°C to +150°C
Ambient temperature, operating .....	0°C to +70°C
V <sub>CC</sub> with respect to AGND/DGND .....	-0.4 V to +7 V
V <sub>EE</sub> with respect to AGND/DGND .....	+0.4 V to -7 V
V <sub>BAT</sub> with respect to AGND/DGND ..	+0.4 V to -70 V
AGND/DGND with respect to BGND .....	+1 V to -3 V
A(TIP) or B(RING) to BGND:	
Continuous .....	-70 V to +1.0 V
10 ms (F = 0.1 Hz) .....	-70 V to +5 V
1 μs (F = 0.1 Hz) .....	-90 V to +10 V
250 ns (F = 0.1 Hz) .....	-120 V to +15 V
Current from A(TIP) or B(RING) .....	±150 mA
Voltage on RINGOUT .....	V <sub>BAT</sub> to V <sub>CC</sub>
Voltage on TESTOUT .....	V <sub>BAT</sub> to V <sub>CC</sub>
Current through relay drivers or internal driver catch diodes .....	60 mA
Voltage on ring trip inputs DA and DB ...	V <sub>BAT</sub> to 0 V
Current into ring trip inputs .....	±10 mA
Peak current into regulator switch (L pin) .....	150 mA
Switcher transient peak off voltage on L pin ...	+1.0 V
Voltage on chopper stabilization pin CHS .....	V <sub>BAT</sub> to 0 V
C1, C2, C3, C4, E0, E1, CHCLK, to AGND/DGND .....	-0.4 V to V <sub>CC</sub> +0.4 V
Maximum power dissipation, T <sub>A</sub> = 70°C (See note):	
In 28-pin ceramic DIP .....	1.5 W
In 28-pin plastic DIP .....	1.0 W

**Note:** Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never be exposed to this temperature. Operation above 145°C junction temperature may degrade device reliability. See SLIC Packaging Considerations section for more information.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

## OPERATING RANGES

### Commercial (C) Devices

Ambient Temperature .....	0°C to +70°C*
V <sub>CC</sub> .....	4.75 V to 5.25 V
V <sub>EE</sub> .....	-4.75 V to -5.25 V
V <sub>BAT</sub> .....	-40.5 V to -58 V
AGND .....	0 V
BGND with respect to AGND/DGND .....	-100 mV to +100 mV
Load resistance on V <sub>TX</sub> to ground ...	10 kΩ minimum

*Operating Ranges define those limits between which the functionality of the device is guaranteed.*

\* Specifications in this data sheet are guaranteed by testing from 0°C to +70°C. Performance from -40°C to +85°C is guaranteed by characterization and periodic sampling of production units.

**ELECTRICAL CHARACTERISTICS (See Note 1)**

Description	Test Conditions	Final			Unit	Note
		Min	Typ	Max		
Analog ( $V_{TX}$ ) output impedance			3		$\Omega$	
Analog ( $V_{TX}$ ) output offset	0°C to +70°C -40°C to +85°C	-35 -40		+35 +40	mV	5
Analog (RSN) input impedance	300 Hz to 3.4 kHz		1	20	$\Omega$	
Longitudinal impedance at A or B				35		
Overload level $Z_{2WIN} = 600 \Omega$ to $900 \Omega$	4-wire	-2.2		+2.2	Vpk	2
	2-wire	-2.2		+2.2		
<b>Transmission Performance, 2-Wire Impedance</b>						
Two-wire return loss (See Test Circuit D)	300 Hz to 500 Hz	26			dB	5
	500 Hz to 2500 Hz	26				
	2500 Hz to 3400 Hz	20				
<b>Longitudinal Balance (2-Wire and 4-Wire, See Test Circuit C)</b>						
Longitudinal to metallic L-T, L-4 $R_L = 600 \Omega$	300 Hz to 3400 Hz	48			dB	
Longitudinal signal generation 4-L	300 Hz to 800 Hz	40			dB	
Longitudinal current capability per wire	Active state		25		mArms	
	OHT state		18			
<b>Insertion Loss (2-Wire to 4-Wire and 4-Wire to 2-Wire, See Test Circuits A and B)</b>						
Gain accuracy	0 dBm, 1 kHz 0°C to +70°C	-0.15		+0.15	dB	5
	0 dBm, 1 kHz -40°C to +85°C	-0.20		+0.20	dB	
Variation with frequency	300 Hz to 3400 Hz Relative to 1 kHz 0°C to +70°C	-0.1		+0.1	dB	5
	-40°C to +85°C	-0.15		+0.15	dB	
Gain tracking	+7 dBm to -55 dBm -4 dBm Reference 0°C to +70°C	-0.1		+0.1	dB	5
	-40°C to +85°C	-0.15		+0.15	dB	
<b>Balance Return Signal (4-Wire to 4-Wire, See Test Circuit B)</b>						
Gain accuracy	0 dBm, 1 kHz 0°C to +70°C	-0.15		+0.15	dB	5
	0 dBm, 1 kHz -40°C to +85°C	-0.20		+0.20	dB	
Variation with frequency	300 Hz to 3400 Hz Relative to 1 kHz 0°C to +70°C	-0.1		+0.1	dB	5
	-40°C to +85°C	-0.15		+0.15	dB	
Gain tracking	+7 dBm to -55 dBm -4 dBm Reference 0°C to +70°C	-0.1		+0.1	dB	5
	-40°C to +85°C	-0.15		+0.15	dB	
Group delay	F = 1 kHz		5.3		$\mu$ s	
<b>Total Harmonic Distortion (2-Wire to 4-Wire or 4-Wire to 2-Wire, See Test Circuits A and B)</b>						
Total harmonic distortion	0 dBm, 300 Hz to 3400 Hz		-64	-50	dB	
	+6 dBm, 300 Hz to 3400 Hz		-55	-40	dB	

**ELECTRICAL CHARACTERISTICS (continued)**

Description	Test Conditions	Final			Unit	Note
		Min	Typ	Max		
<b>Idle Channel Noise</b>						
C-message weighted noise	2-wire			+15	dBrnc	5, 7
	4-wire			+15		5, 7
Psophometric weighted noise	2-wire			-75	dBmp	
	4-wire			-75		
<b>Single Frequency Out-of-Band Noise (See Test Circuit E)</b>						
Metallic	4 kHz to 9 kHz		-76		dBm	4, 5, 8
	9 kHz to 1 MHz		-76			4, 5, 8
	256 kHz and harmonics		-57		dBm	4,5
Longitudinal	1 kHz to 15 kHz		-70		dBm	4, 5, 8
	Above 15 kHz		-85			4, 5, 8
	256 kHz and harmonics		-57		dBm	4, 5
<b>DC Feed Currents (See Figure 1) <math>V_{BAT} = -48 V</math></b>						
Active mode loop current accuracy	$I_{LOOP}$ (nominal) = 33 mA, $R_L = 600 \Omega$	-8		+8	%	
Active mode loop current	$R_L = 1240 \Omega$	30			mA	
OHT mode	$R_L = 600 \Omega$	14.5	16.5	18.5	mA	
Tip open mode	$R_L = 600 \Omega$			1.0		
Disconnect mode	$R_L = 0 \Omega$			1.0		
<b>Power Dissipation <math>V_{BAT} = -48 V</math></b>						
On-hook open circuit			40	120	mW	
On-hook OHT mode			150	250		
On-hook active mode			210	400		
Off-hook OHT mode	$R_L = 600 \Omega$		400	750		
Off-hook active mode	$R_L = 600 \Omega$		550	1000		
<b>Supply Current</b>						
$V_{CC}$ On-hook supply current	Open circuit mode		3	4.5	mA	
	OHT mode		6	10		
	Active mode		7.5	12		
$V_{EE}$ On-hook supply current	Open circuit mode		1.0	2.3		
	OHT mode		2.2	3.5		
	Active mode		2.7	6.0		
$V_{BAT}$ On-hook supply current	Open circuit mode		0.4	1.0		
	OHT mode		3.0	5.0		
	Active mode		4.0	6.0		



**ELECTRICAL CHARACTERISTICS (continued)**

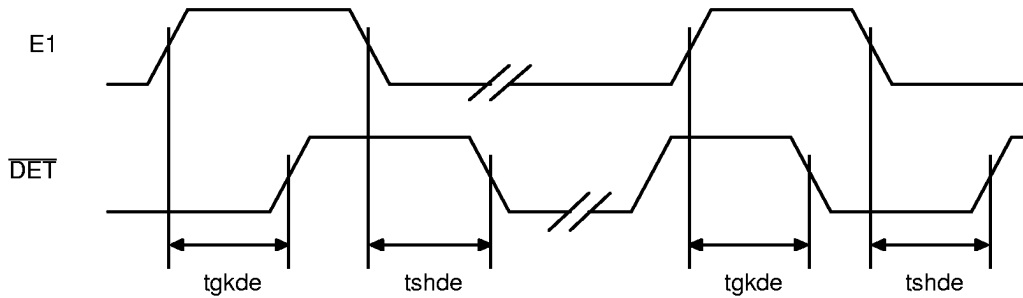
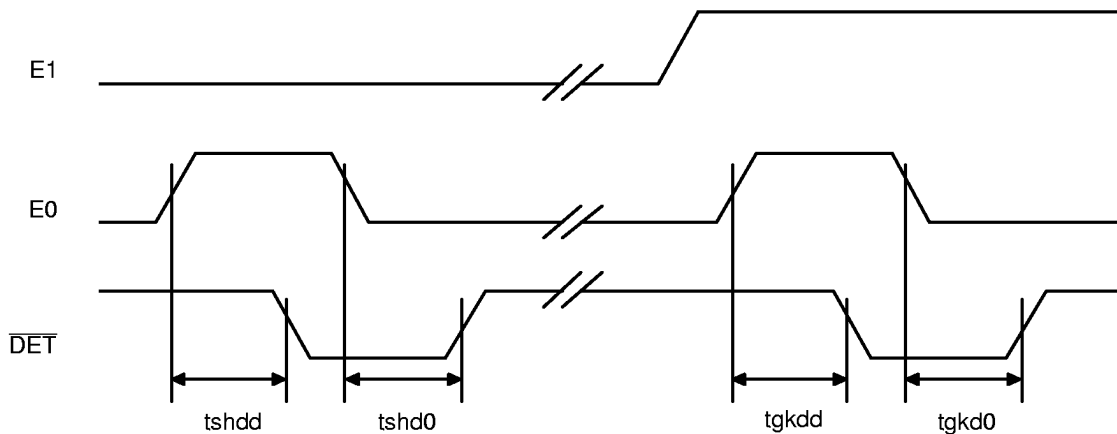
Description	Test Conditions	Final			Unit	Note
		Min	Typ	Max		
<b>Power Supply Rejection Ratio (Vripple = 50 mVrms)</b>						
V <sub>CC</sub>	40 Hz to 3400 Hz	20	35		dBm	6, 7
	3.4 kHz to 50 kHz	20	30			
V <sub>EE</sub>	40 Hz to 3400 Hz	20	30			
	3.4 kHz to 50 kHz	15	25			
V <sub>BAT</sub>	40 Hz to 3400 Hz	27	30			
	3.4 kHz to 50 kHz	20	30			
<b>Off-Hook Detector</b>						
Current threshold	I <sub>DET</sub> = 365 / R <sub>D</sub> ; I <sub>DET</sub> = 7.14 mA	-20		+20	%	
<b>Ring Trip Detector Inputs</b>						
Bias current		-25	4		μA	
Offset voltage	Source resistance = 0 to 200K	-50	0	+50	mV	
<b>Logic Inputs (C1, C2, C3, C4, E0, E1, and CHCLK)</b>						
Input High voltage		2.0			V	
Input Low voltage				0.8		
Input High current	All inputs except E1	-75		40	μA	
Input High current	Input E1	-75		45	μA	
Input Low current		-0.4	-0.2		mA	
<b>Logic Output (DET)</b>						
Output Low voltage	I <sub>OUT</sub> = 0.8 mA			0.4	V	
Output High voltage	I <sub>OUT</sub> = -0.1 mA	2.4				

**Table 1. SLIC Decoding**

State	C3 C2 C1	Two-Wire Status	DET Output	
			E0 = 1 E1 = 0	E0 = 1 E1 = 1
0	0 0 0	Open circuit	Ring trip	Ring trip
1	0 0 1	Ringing	Ring trip	Ring trip
2	0 1 0	Active	Loop det.	Ground key
3	0 1 1	On-hook TX (OHT)	Loop det.	Ground key
4	1 0 0	Tip open	Loop det.	—
5	1 0 1	Reserved	Loop det.	—
6	1 1 0	Active polarity reversal	Loop det.	Ground key
7	1 1 1	OHT polarity reversal	Loop det.	Ground key

**SWITCHING CHARACTERISTICS**
**Am79533I/Am79534I**

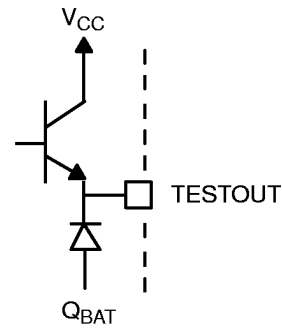
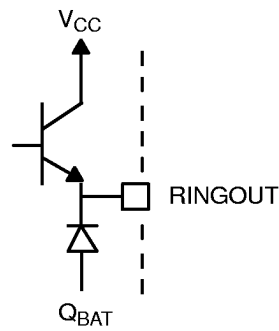
Symbol	Parameter	Test Conditions	Temperature Range	Min	Typ	Max	Unit	Note
tgkde	E1 Low to $\overline{\text{DET}}$ High (E0 = 1)	Ground key detect mode $R_L$ open, $R_G$ connected (See Figure H)	0°C to +70°C			3.8	$\mu\text{s}$	5
			-40°C to +85°C			4.0		5
tgkdd	E0 High to $\overline{\text{DET}}$ Low (E1 = 0)		0°C to +70°C			1.1		5
			-40°C to +85°C			1.6		5
tgkd0	E0 Low to $\overline{\text{DET}}$ High (E1 = 0)		0°C to +70°C			3.8		5
			-40°C to +85°C			4.0		5
tshde	E1 High to $\overline{\text{DET}}$ Low (E0 = 1)	Switch hook detect mode $R_L = 600 \Omega$ , $R_G$ open (See Figure G)	0°C to +70°C			1.2	$\mu\text{s}$	5
			-40°C to +85°C			1.7		5
tshdd	E0 High to $\overline{\text{DET}}$ Low (E1 = 1)		0°C to +70°C			3.8		5
			-40°C to +85°C			4.0		5
tshd0	E0 Low to $\overline{\text{DET}}$ High (E1 = 1)		0°C to +70°C			1.1		5
			-40°C to +85°C			1.6		5
			0°C to +70°C			3.8		5
			-40°C to +85°C			4.0		5

**SWITCHING WAVEFORMS**
**Am79533I/Am79534I**
**E1 to  $\overline{\text{DET}}$** 

**E0 to  $\overline{\text{DET}}$** 

**Note:**

All delays measured at 1.4-V level.

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## RELAY DRIVER SPECIFICATIONS



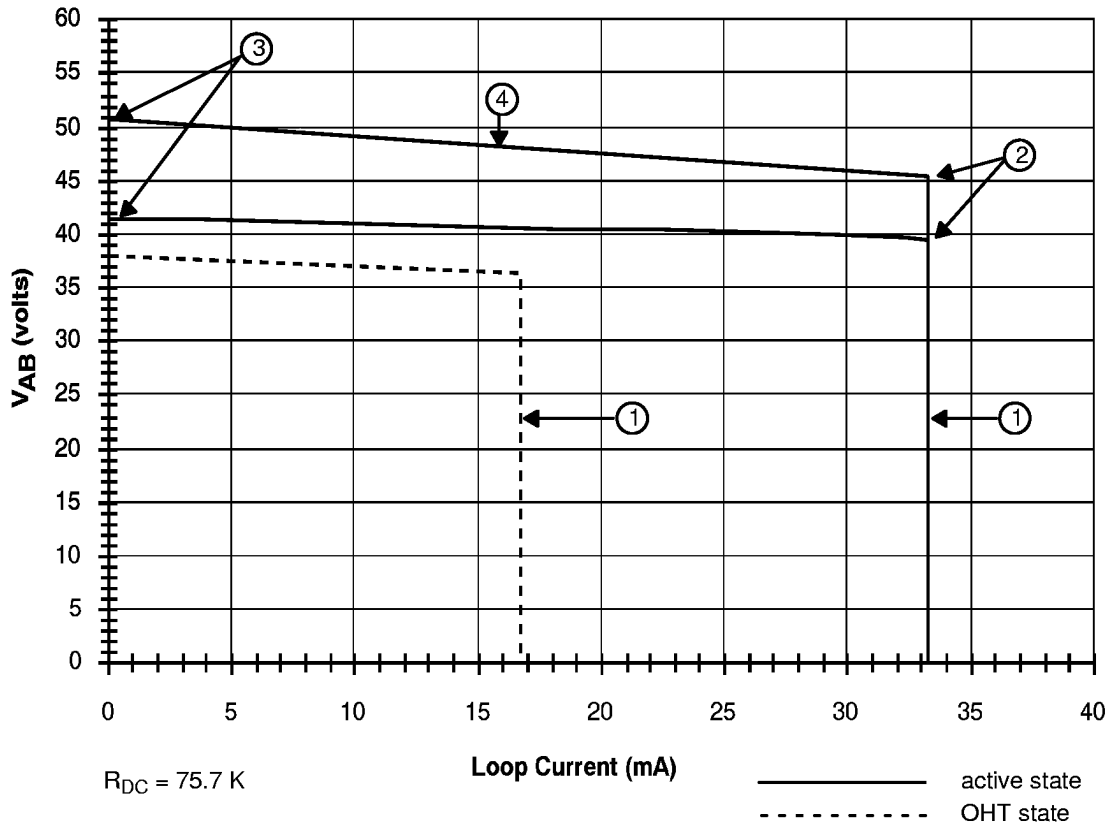
Description	Test Conditions	Min	Typ	Max	Unit	Note
<b>Relay Driver Outputs (RINGOUT, TESTOUT)</b>						
On voltage	50-mA source	$V_{CC}-2$			V	
Off leakage			0.5	100	$\mu$ A	
Clamp voltage	50-mA sink	$Q_{BAT}-2$	$Q_{BAT}-1.3$		V	

**Notes:**

- Unless otherwise noted, test conditions are:  $V_{BAT} = -48$  V,  $V_{CC} = +5$  V,  $V_{EE} = -5$  V,  $R_L = 600 \Omega$ ,  $C_{HP} = 0.22 \mu$ F,  $R_{DC1} = 37.4$ K,  $R_{DC2} = 38.3$ K,  $C_{DC} = 0.1 \mu$ F,  $R_d = 51.1$ K, No fuse resistors, Two-Wire AC output impedance programming impedance ( $Z_T$ ) = 600K resistive, Receive input summing impedance ( $Z_{RX}$ ) = 300 K resistive. (See Table 1 for component formulas.)
- Overload level is defined when THD = 1%.
- Balance return signal is the signal generated at  $V_{TX}$  by  $V_{RX}$ . This spec assumes that the two-wire AC load impedance matches the impedance programmed by  $Z_T$ .
- These tests are performed with a longitudinal impedance of 90  $\Omega$  and metallic impedance of 300  $\Omega$  for frequencies below 12 kHz and 135  $\Omega$  for frequencies greater than 12 kHz. These tests are extremely sensitive to circuit board layout. Please refer to application notes for details.
- Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.
- This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.
- When the SLIC is in the Anti-sat 2 operating region, this parameter will be degraded. The exact degradation will depend on system design. The Anti-sat 2 region occurs at high loop resistances when  $|V_{BAT}| - |V_{AX} - V_{BX}|$  is less than approximately 15 V.
- Fundamental and harmonics from 256-kHz switch regulator chopper are not included.

**Table 2. User-Programmable Components**

$Z_T = 1000 (Z_{2WIN} - 2R_F)$	<p>Where <math>Z_T</math> is connected between the <math>V_{TX}</math> and RSN pins. The fuse resistors are <math>R_F</math> and <math>Z_{2WIN}</math> is the desired 2-wire AC input impedance. When computing <math>Z_T</math>, any external stray capacitance between <math>V_{TX}</math> and RSN must be taken into account.</p>
$Z_{RX} = \frac{1}{2Z_T}$	<p>Where <math>Z_{RX}</math> is connected from <math>V_{RX}</math> to the RSN pin, <math>Z_T</math> is defined above. This equation sets the receive gain to 0 dB when the SLIC is terminated with an impedance equal to <math>Z_{2WIN}</math>.</p>
$R_{DC1} + R_{DC2} = \frac{2500}{I_{FEED}}$ $C_{DC} = 1.5 \text{ ms} \cdot \frac{R_{DC1} + R_{DC2}}{R_{DC1} \cdot R_{DC2}}$	<p>Where <math>R_{DC1}</math>, <math>R_{DC2}</math>, and <math>C_{DC}</math> form the network connected to the RDC pin. <math>R_{DC1}</math> and <math>R_{DC2}</math> are approximately equal.</p>
$R_D = \frac{365}{I_T}, \quad C_D = \frac{0.5 \text{ ms}}{R_D}$	<p>Where <math>R_D</math> and <math>C_D</math> form the network connected from RD to -5 V and <math>I_T</math> is the threshold current between on-hook and off-hook.</p>

**Notes:**

## 1. Constant current region:

$$\text{active state, } I_L = \frac{2500}{R_{DC}}$$

$$\text{OHT state, } I_L = \frac{1}{2} \cdot \frac{2500}{R_{DC}}$$

## 2. Anti-sat cut-in:

$$V_{AB} = 1.067 |V_{BAT}| - 13.57, \quad |V_{BAT}| \leq 55.7 \text{ V}$$

$$V_{AB} = 45.81 \text{ V}, \quad |V_{BAT}| > 55.7 \text{ V}$$

## 3. Open-circuit voltage (active state):

$$V_{AB} = 1.067 |V_{BAT}| - 11.78, \quad |V_{BAT}| \leq 58.9 \text{ V}$$

$$V_{AB} = 51.1 \text{ V}, \quad |V_{BAT}| > 58.9 \text{ V}$$

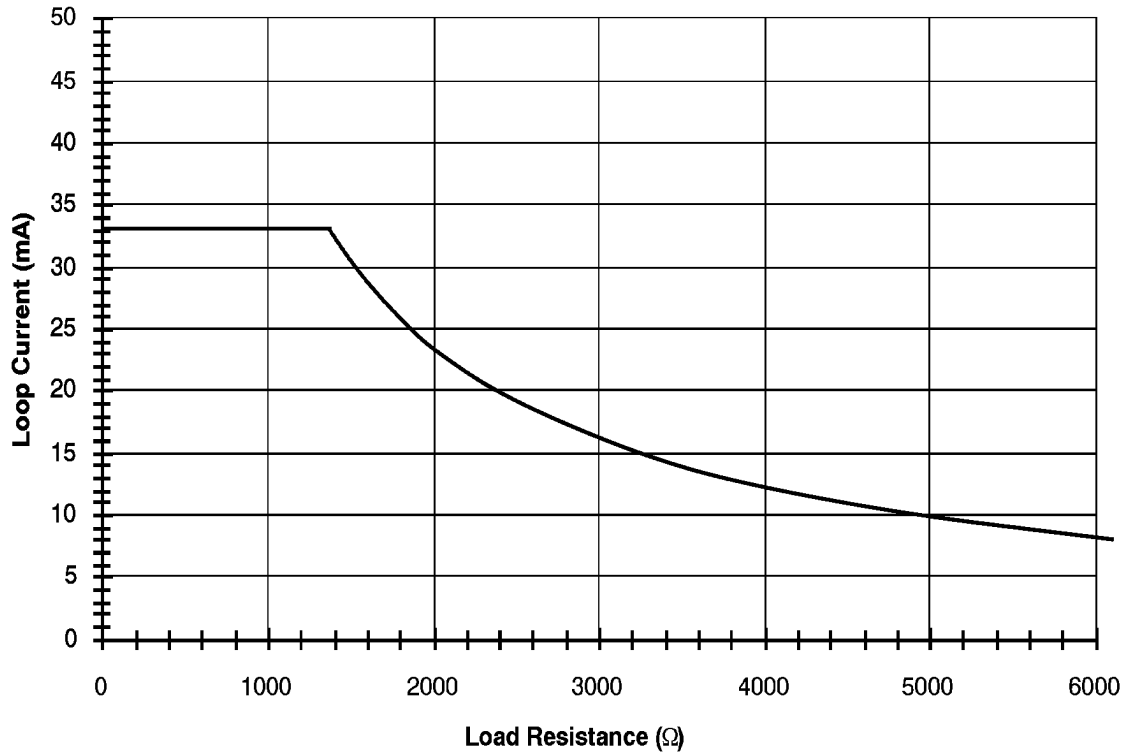
## 4. Anti-sat -1 region:

$$V_{AB} = 51.1 - I_L \frac{R_{DC}}{470.4}$$

## Anti-sat -2 region:

$$V_{AB} = 1.067 |V_{BAT}| - 11.78 - I_L \frac{R_{DC}}{1385}$$

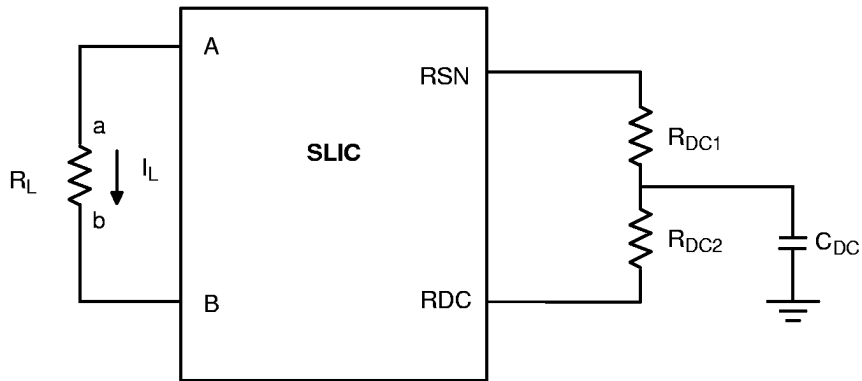
a.  $V_A - V_B$  ( $V_{AB}$ ) Voltage vs Loop Current (Typical)



$V_{BAT} = 64.0 \text{ V}$

$R_{DC} = 75.7 \text{ K}$

b. Loop Current vs Load Resistance (Typical)



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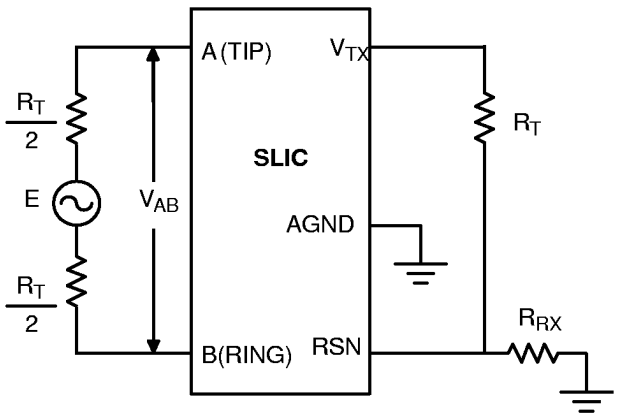
c. Feed Programming

**Note:**

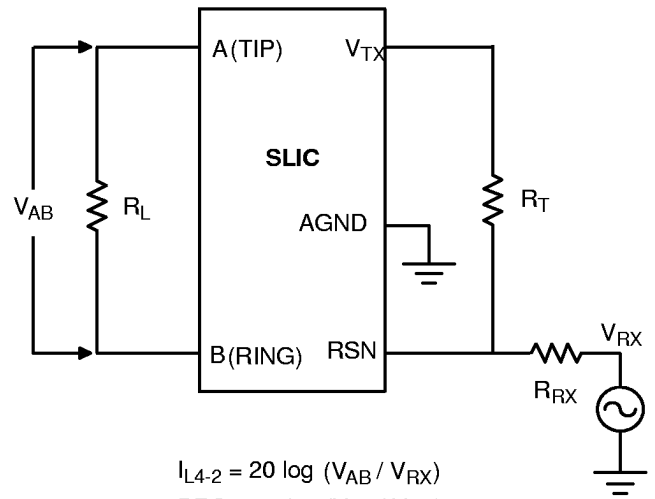
Current programmed by  $R_{DC1}$  and  $R_{DC2}$ .

Figure 1. DC Feed Characteristics

TEST CIRCUITS



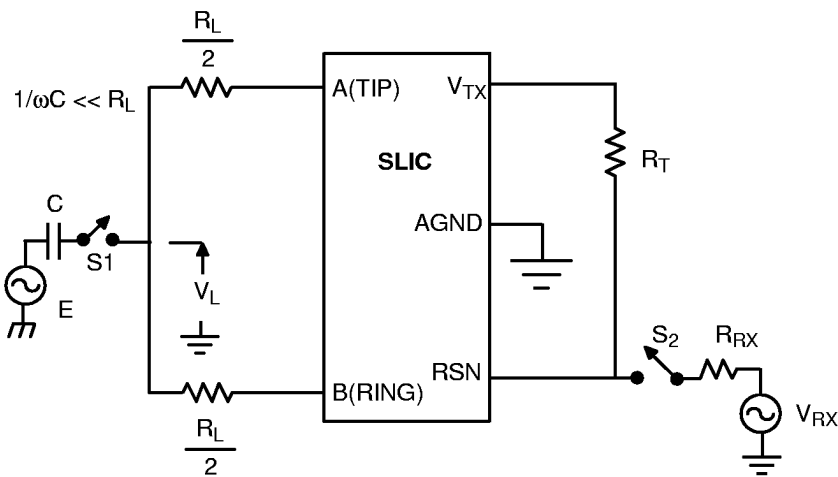
$I_{L2-4} = 20 \log (V_{TX} / V_{AB})$  TC004440



$I_{L4-2} = 20 \log (V_{AB} / V_{RX})$   
 $BRS = 20 \log (V_{TX} / V_{RX})$  TC004480

A. Two-to-Four-Wire Insertion Loss

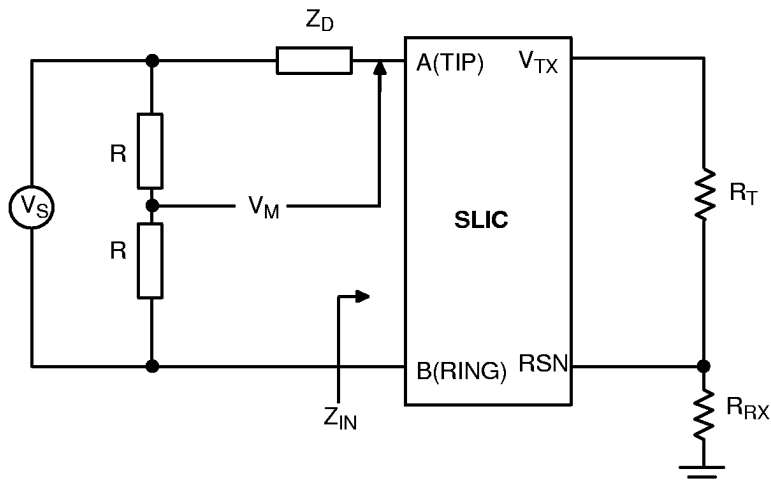
B. Four-to-Two-Wire Insertion Loss and Balance Return Signal



S1 Closed, S2 Open  
 L-T Long. Bal. =  $20 \log (V_{AB} / E)$   
 L-4 Long. Rej. =  $20 \log (V_{TX} / E)$   
 S2 Closed, S1 Open:  
 4-L Long. Sig. Gen. =  $20 \log (V_L / V_{RX})$

TC004470

C. Longitudinal Balance (IEEE)



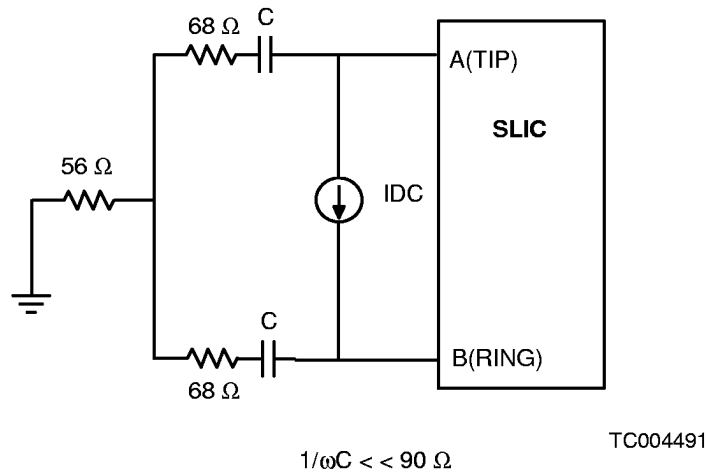
**Note:**  
 $Z_D$  is the desired impedance (e.g., the characteristic impedance of the line).

$R_L = 20 \log (2 V_M / V_S)$

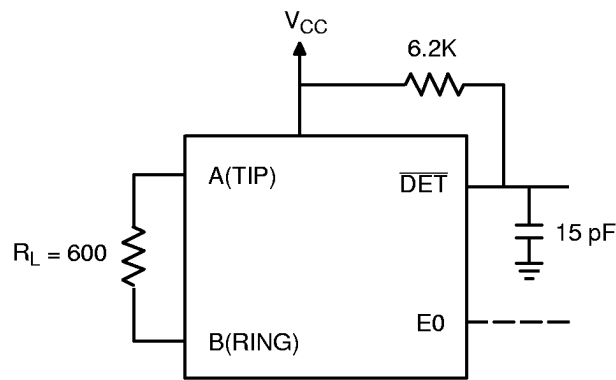
TC004501

D. Two-Wire Return Loss Test Circuit

TEST CIRCUITS (continued)



E. Single Frequency Noise



F. Loop Detect Switching