PRELIMINARY

Am79C864A

Physical Layer Controller With Scrambler (PLC-S)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Implements FDDI PHY layer protocol for ISO standard (FDDI) 9314-1**
- **Implements ANSI standard Stream Cipher Scrambling/Descrambling**
- **Hardware Physical Connection Management (PCM) support**
- **Performs Physical Connection insertion and removal**
- **On-chip Link Error Monitor (LEM) and Link Confidence Test (LCT)**
- **Line state detection**
- **Repeat filter**
- **Elasticity buffer and smoother functions**
- **4B/5B encoding/decoding**
- **Full duplex operation**
- **Data framing**
- **Built-in Self Test**

GENERAL DESCRIPTION

The Physical Layer Controller with Scrambler (PLC-S) is a CMOS device which along with Physical Data Transmitter (PDT) and Physical Data Receiver (PDR) implements the Physical Layer Protocol (PHY) and portions of the Station Management (SMT) of the ANSI Fiber Distributed Data Interface (FDDI) standard. The PLC-S, PDT and PDR are collectively known as the AmPHY. PHY functions performed by the PLC-S include framing of data on symbol pair boundaries, the elasticity buffer function, the smoothing function, 4B/5B encoding and decoding of symbols, line state detection, the repeat filter function, and Stream Cipher Scrambling/Descrambling. SMT functions performed include Physical Connection Management (PCM), Physical Connection insertion and removal and Link Error Monitor.

The PLC-S chip receives symbol-wide (5 bits) data along with a 25 MHz recovered clock from the PDR chip and searches for a JK symbol pair (also known as Starting Delimiter). It uses the starting delimiter to establish byte boundaries (i.e. to frame the data).

Framed data is then sent to the Elasticity Buffer which serves to compensate for the frequency difference between the recovered clock and the local clock. Data output by the Elasticity Buffer is checked by the Smoother and when necessary, Idle symbols are inserted between frames to maintain a minimum number of Idle symbols in the interframe gap.

The data is then decoded and sent to the Media Access Control (MAC) chip. The data is byte-wide (10 bits) and is clocked by a 12.5 MHz local clock.

The PLC-S receives byte-wide data from the MAC at 12.5 million bytes per second, encodes the data and sends out symbol-wide data at 25 million symbols per second to PDT chip. In the transmit path, there is a Repeat Filter to detect corrupted symbols and convert them into the specified pattern of Halt and Idle symbols. The Repeat Filter in each PLC-S chip converts the last byte of a frame fragment into Idle symbols and thus eventually removing fragments from the ring.

The PLC-S device includes a Stream Cipher Scrambler/Descrambler as prescribed in the ANSI TP-PMD standard for transmission over twisted-pair cable. For copper-based designs, the scrambler/descrambler may be enabled either through software or hardware. For fiber-based designs, the scrambler/descrambler is disabled by default. For a detailed description of the ANSI-compliant copper FDDI system using the PLC-S device, refer to AMD PID #18258A, *Implementing FDDI over Copper; The ANSI X3T9.5 Standard*.

The PCM initializes the connection of neighboring PHYs and manages the PHY signaling. PCM consists of the PCM state machine, which determines the timing and state requirements for PCM, and the PCM Pseudo Code, which provides the information to be communicated to the neighboring PCM and specifies the connection policies. The PLC-S chip contains the PCM State Machine, while the PCM Pseudo Code is controlled by software. The PCM State Machine communicates with other PCMs using a bit signaling mechanism whereby certain line states are received and transmitted. The PCM also makes use of the Link Error Monitor in the

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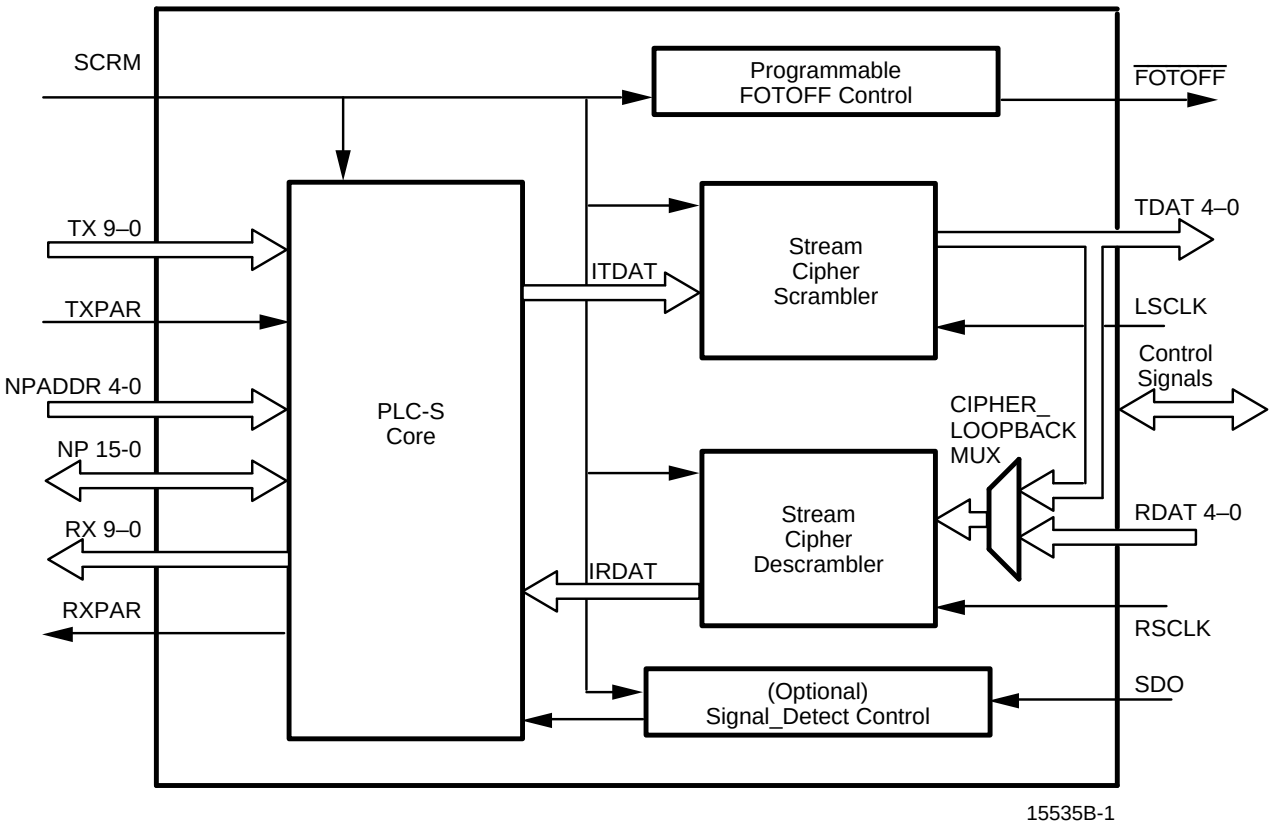
PLC-S chip during Link Confidence Test and after the link has been formed, to detect a noisy link. The PLC-S contains a Line State Machine for detecting received line states and a Data Stream Generator for transmitting the various line states. The PLC-S also contains a state machine called Physical Connection Insertion (PCI) which is used in Physical Connection insertion and removal. It performs the necessary ring scrubbing and data path switching.

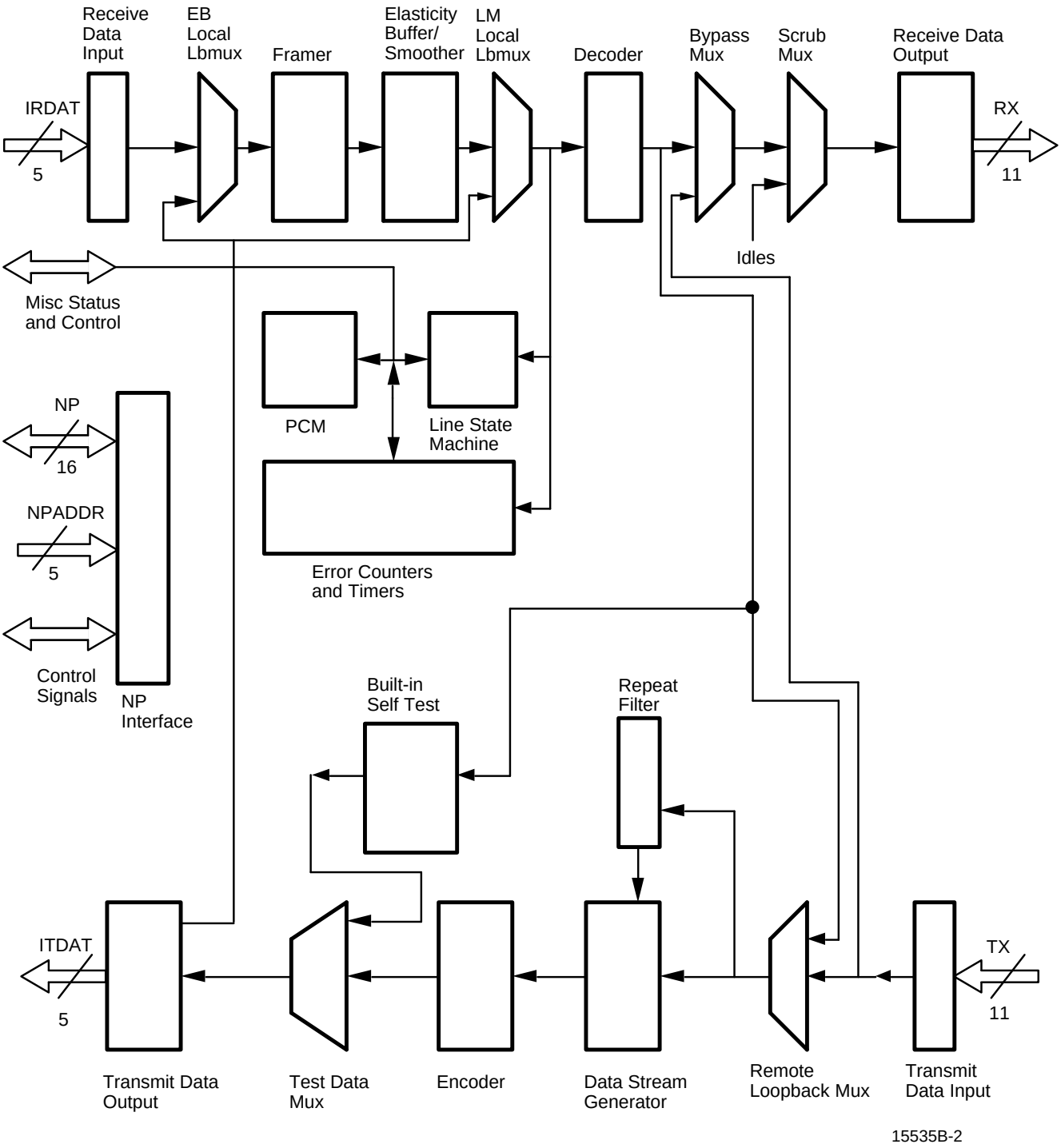
The Node Processor Interface in the PLC-S consists of several control and status registers. The PLC-S also contains error and special event counters, Built In Self Test (BIST) logic, Boundary Scan logic, and several data loopback multiplexers so that internal data paths may be reconfigured for test purposes.

PLC-S BLOCK DIAGRAM



See next page for the PLC-S Core block diagram

PLC-S CORE BLOCK DIAGRAM



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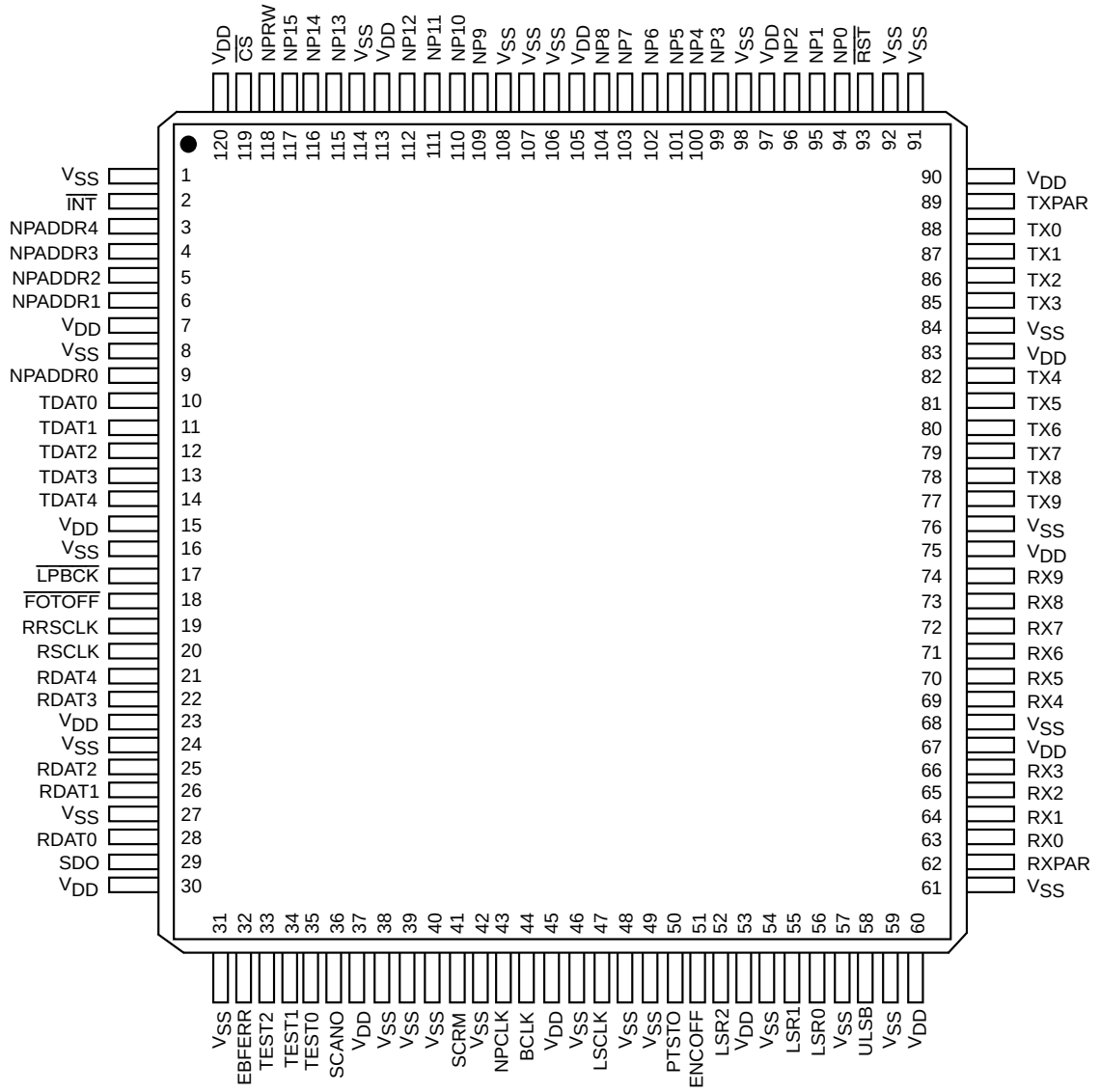
CONNECTION DIAGRAM
120-Pin PQR (Top View)



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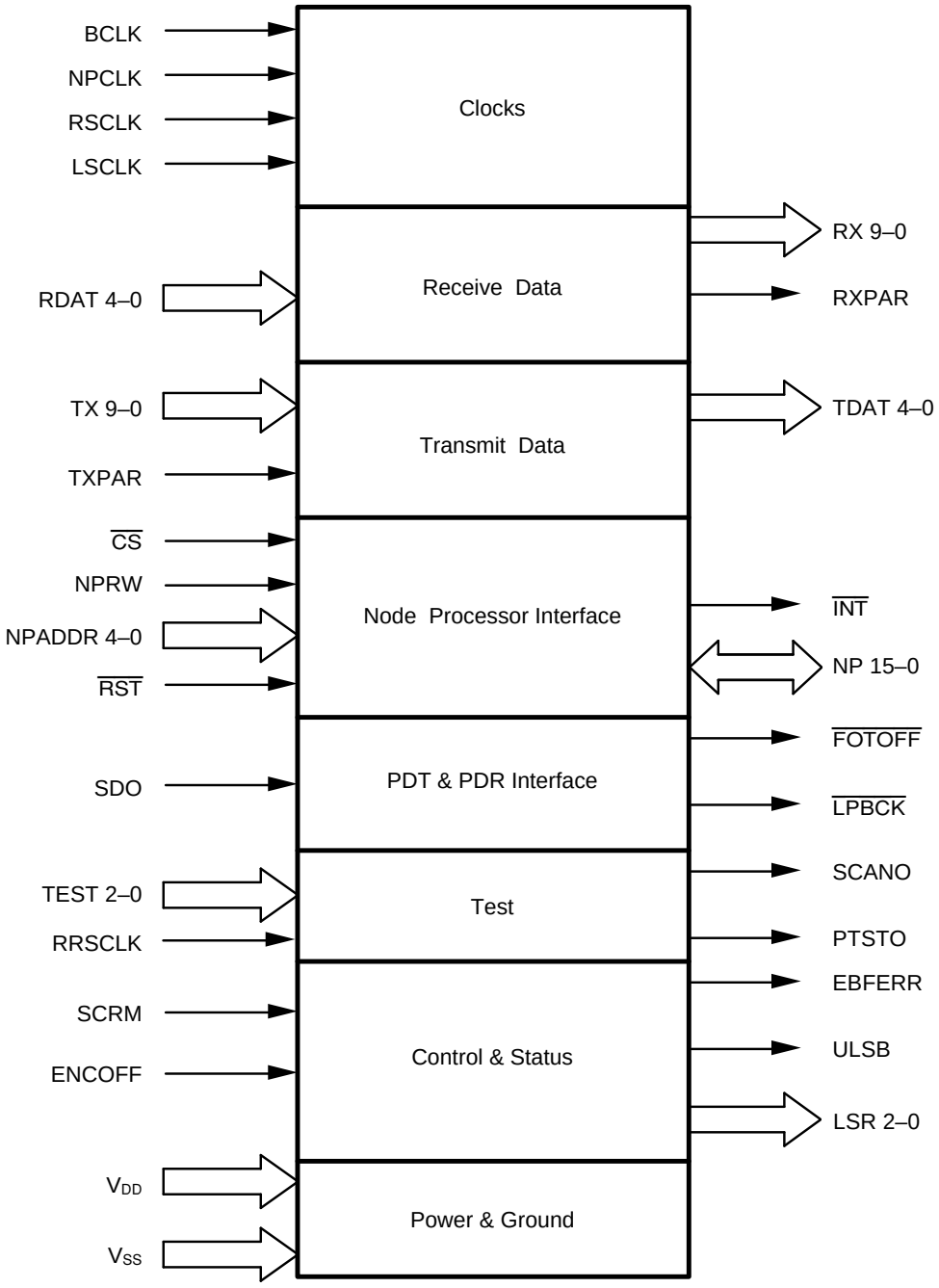
PQFP PIN DESIGNATIONS

Listed by Pin Number

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
1	V_{SS}	31	V_{SS}	61	V_{SS}	91	V_{SS}
2	$\overline{INT}$	32	EBFERR	62	RXPAR	92	V_{SS}
3	NPADDR4	33	TEST2	63	RX0	93	$\overline{RST}$
4	NPADDR3	34	TEST1	64	RX1	94	NP0
5	NPADDR2	35	TEST0	65	RX2	95	NP1
6	NPADDR1	36	SCANO	66	RX3	96	NP2
7	V_{DD}	37	V_{DD}	67	V_{DD}	97	V_{DD}
8	V_{SS}	38	V_{SS}	68	V_{SS}	98	V_{SS}
9	NPADDR0	39	V_{SS}	69	RX4	99	NP3
10	TDAT0	40	V_{SS}	70	RX5	100	NP4
11	TDAT1	41	SCRM	71	RX6	101	NP5
12	TDAT2	42	V_{SS}	72	RX7	102	NP6
13	TDAT3	43	NPCLK	73	RX8	103	NP7
14	TDAT4	44	BCLK	74	RX9	104	NP8
15	V_{DD}	45	V_{DD}	75	V_{DD}	105	V_{DD}
16	V_{SS}	46	V_{SS}	76	V_{SS}	106	V_{SS}
17	$\overline{LPBCK}$	47	LSCLK	77	TX9	107	V_{SS}
18	$\overline{FOTOFF}$	48	V_{SS}	78	TX8	108	V_{SS}
19	RRSCLK	49	V_{SS}	79	TX7	109	NP9
20	RSCLK	50	PTSTO	80	TX6	110	NP10
21	RDAT4	51	ENCOFF	81	TX5	111	NP11
22	RDAT3	52	LSR2	82	TX4	112	NP12
23	V_{DD}	53	V_{DD}	83	V_{DD}	113	V_{DD}
24	V_{SS}	54	V_{SS}	84	V_{SS}	114	V_{SS}
25	RDAT2	55	LSR1	85	TX3	115	NP13
26	RDAT1	56	LSR0	86	TX2	116	NP14
27	V_{SS}	57	V_{SS}	87	TX1	117	NP15
28	RDAT0	58	ULSB	88	TX0	118	NPRW
29	SDO	59	V_{SS}	89	TXPAR	119	$\overline{CS}$
30	V_{DD}	60	V_{DD}	90	V_{DD}	120	V_{DD}

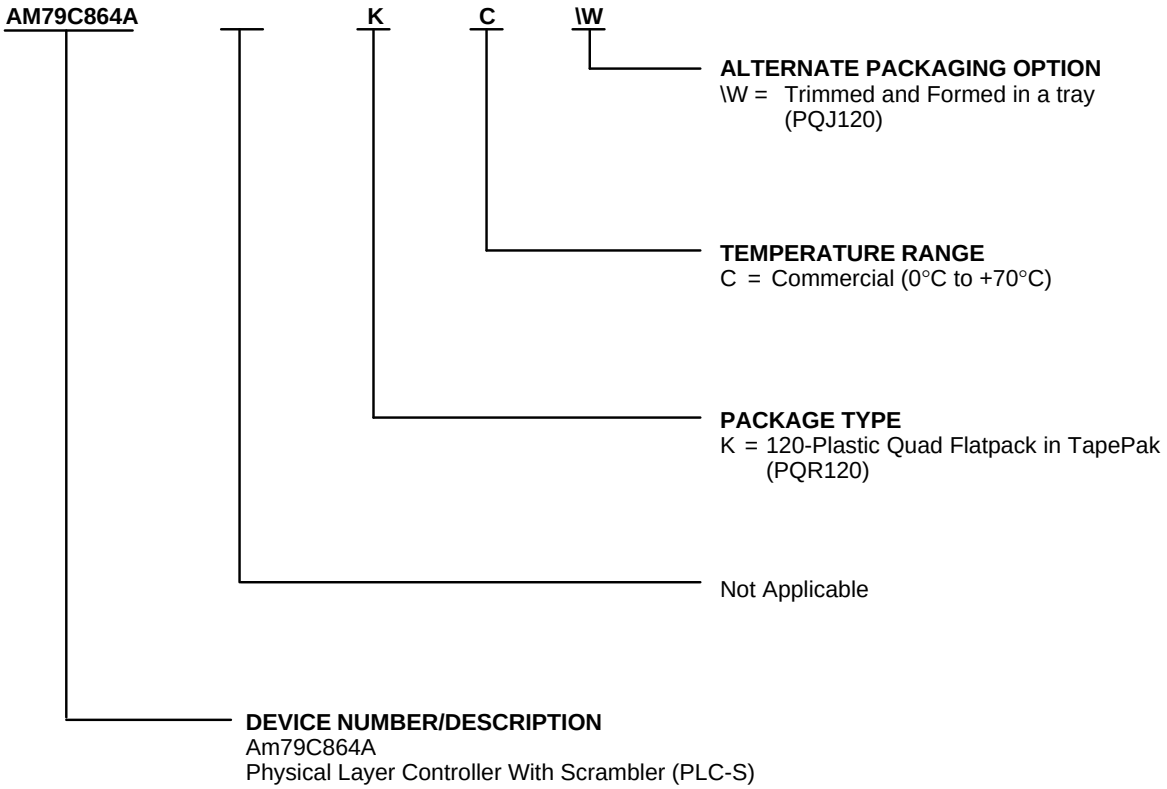
LOGIC SYMBOL



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM79C864A	KC, KC\W

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PIN DESCRIPTION

Clock Signals

BCLK
Byte Clock (Input)

BCLK is a 12.5 MHz clock. It is used by the PLC-S to clock most internal operations, clock RX 9–0 to the MAC device and, along with LSCLK, latch TX 9–0 from the MAC device.

NPCLK
Node Processor Clock (Input)

NPCLK is used to latch Node Processor inputs, run the Node Processor Interface state machine, and clock output signals to the Node Processor. It is distinct from the BCLK for test and diagnostic purposes only. For normal operations, the BCLK and NPCLK pins MUST be tied together.

RSCLK
Recovered Symbol Clock (Input)

RSCLK is a 25 MHz clock. It is recovered from the data sent to the Physical Data Receiver (PDR) by the upstream station in the ring. It is used to latch RDAT 4–0 from the PDR device. It is also used for clocking the Framer and the Elasticity Buffer input controller.

LSCLK
Local Symbol Clock (Input)

LSCLK is a 25 MHz clock. It is used by the PLC-S to clock TDAT 4–0 to the Physical Data Transmitter (PDT) and, along with BCLK, to latch TX 9–0 from the MAC device.

Receive Data Signals

RX 9–0
Receive Data Bus (Output)

RX 9–0 is a ten bit output bus used to transfer symbol pairs from the PLC-S to a MAC device, or to another PLC-S. The ten bits are clocked to the MAC device on the rising edge of BCLK. RX 9–5 contain the most significant symbol and RX 4–0 contain the least significant symbol of the framed byte. Bit 9 is the upper control bit and bit 4 is the lower control bit.

RXPAR
Receive Data Parity bit (Output)

RXPAR is an output signal used to enhance error detection on the RX bus. If there is an odd number of ones on RX 9–0 then RXPAR will be one, and if there is an even number of ones on RX 9–0 then RXPAR will be zero (even parity). When the PLC-S is in Bypass mode (that is when the data output on RX 9–0 is the data input on TX 9–0) RXPAR is not calculated and is just the value input on TXPAR.

RDAT 4–0
Receive Data Bus (Input)

RDAT 4–0 is a five bit input bus used to transfer data from the PDR device to the PLC-S. Data is latched by the PLC-S on the rising edge of RSCLK.

Transmit Data Signals

TDAT 4–0
Physical Transmit Data Bus (Output)

TDAT 4–0 is a five bit output bus used to transfer symbols from the PLC-S to the PDT. The symbols are clocked to the PDT on the rising edge of LSCLK.

TX 9–0
Transmit Data Bus (Input)

TX 9–0 is a ten bit input bus used to transfer symbol pairs from a MAC device, or from another PLC-S, to the PLC-S. The ten bits are latched by the PLC-S on the falling edge of LSCLK. Bits 9–5 of the bus contain the first symbol to be transmitted on the fiber and bits 4–0 contain the second symbol. Bit 9 is the upper control bit and bit 4 is the lower control bit.

TXPAR
Transmit Data Parity bit (Input)

TXPAR is an input signal used to implement even parity on the TX bus. If there is an odd number of ones on TX 9–0 then TXPAR should be one and if there is an even number of ones on TX 9–0 then TXPAR should be zero.

Node Processor Interface Signals

$\overline{\text{INT}}$
Interrupt (Output, Active Low)

The $\overline{\text{INT}}$ signal indicates an interrupt request from the PLC-S. This signal is active until cleared by reading the INTR_EVENT register at address 17 (hex).

$\overline{\text{CS}}$
Chip Select (Input, Active Low)

$\overline{\text{CS}}$ selects the PLC-S for the current bus cycle.

NPADDR 4–0
Node Processor Address Bus (Input)

The NPADDR 4–0 bus is a five bit input bus used to select one of the registers in the PLC-S for a read or write cycle.

NP 15–0
Node Processor Data Bus (Input/Output, Three State)

The NP 15–0 bus is a sixteen bit bi-directional, three-state data bus used to exchange data between the PLC-S and the Node Processor.

NPRW
Node Processor Read/Write (Input)

The NPRW signal indicates whether the current bus cycle is a read (NPRW = 1) or a write (NPRW = 0) cycle.

$\overline{\text{RST}}$
Reset (Input, Active Low, Asynchronous)

The $\overline{\text{RST}}$ signal provides a means of initializing the PLC-S on power up. When asserted, the Reset causes the following:

- The various state machines are initialized: LSM-NOT ACTIVE, PCM-OFF, PCI-REMOVED, Repeat Filter on REPEAT, Node Processor Interface-NOT ACTIVE.
- All writable registers are cleared and all registers that are cleared on a read are cleared.
- Built-in Self Test – OFF
- The Fiber Optic Transmitter Off ($\overline{\text{FOTOFF}}$) signal is asserted, Quiet Symbols are transmitted on TDAT, and TX is looped back onto RX.

Once $\overline{\text{RST}}$ is asserted low, it must remain asserted for at least twenty NPCLK cycles. When it is deasserted the PLC-S is ready to begin its normal operation.

Assertion and deassertion are asynchronous. A warm reset (assertion of $\overline{\text{RST}}$ after the device is in operation) will cause device outputs to be unpredictable until the device is initialized.

PDT and PDR Interface Signals

$\overline{\text{LPBCK}}$
Loopback (Output, Active Low)

The $\overline{\text{LPBCK}}$ signal controls the receive multiplexer in the PDR device. If LPBCK= 0, the MUX selects its input from the PDT. If LPBCK = 1, the MUX selects its input from the Fiber Optic Receiver.

$\overline{\text{FOTOFF}}$
Fiber Optic Transmitter Off (Output, Active Low)

The $\overline{\text{FOTOFF}}$ signal, when asserted, causes the PDT to transmit Quiet symbols. This signal is asserted whenever:

- The FOT_OFF bit, LOOPBACK bit, EB_LOC_LOOP bit, LM_LOC_LOOP bit in the PLC_CNTRL_A register (or) CIPHER_LPBCK bit in PLC_CNTRL_C register is set.
- The MAINT_LS field in the PLC_CNTRL_B register equal Transmit QUIET and the PCM is in the MAINT state and FOTOFF assertion timer expires, if enabled.
- The Physical Connection Management logic has set LS_REQUEST = Transmit QUIET Line State and FOTOFF assertion timer expires, if enabled.
- Built-in Self Test is active.

SDO
Signal Detect (Input, Active High)

The SDO signal is output by the PDR to indicate whether the Fiber Optic Receiver is detecting an optical signal above its threshold. The inverted value of this signal is held in the PLC_STATUS_A register, and the LSDO bit in the INTR_EVENT register is set when SDO is asserted.

Test Signals

PTSTO
Parametric Test Output (Output)

This is an internal parametric test output signal. This pin should be left unconnected.

SCANO
Scan Output (Output)

The SCANO signal is used as an output of the scan chain when the PLC-S is in Boundary Scan Serial Test Mode.

TEST 2–0
PLC-S Test Mode (Input)

The three TEST 2–0 input pins are used to select between normal operating mode and three different test modes. The different operating modes are as follows:

TEST 2–0	Mode of Device Operation
0 0 0	Normal Operating Mode
0 1 X	Normal Operating Mode
0 0 1	Factory Test Mode (Counter Segmentation Test)
1 0 Scan Input	Boundary Scan Serial Test Mode
1 1 0	Boundary Scan Parallel Test Mode
1 1 1	All output pins except PTSTO are High Impedance

RRSCLK
Reserved (Input)

This pin should be connected to VSS.

Control and Status Signals

EBFERR
Elasticity Buffer Error (Output, Active High)

EBFERR indicates when an overflow or underflow condition occurs in the Elasticity Buffer.

ENCOFF
Encoder Off (Input, Active High)

The ENCOFF signal turns off the encoding and decoding function of the PLC-S. This allows for the transmission of any symbol, including invalid symbols for diagnostic purposes.

LSR 2–0
Line State Register (Output)

The LSR 2–0 signals directly output the LINE_ST field of the PLC_STATUS_A register to ring test and monitor equipment.

LSR 2–0	Description
000	Noise Line State (NLS)
001	Active Line State (ALS)
010	Undefined
011	Idle Line State (ILS4 – achieved after 4 Idle symbols)
100	Quiet Line State (QLS)
101	Master Line State (MLS)
110	Halt Line State (HLS)
111	Idle Line State (ILS16 – achieved after 16 Idle symbols)

ULSB
Unknown Line State (Output)

The ULSB signal directly outputs the UNKN_LINE_ST bit of the PLC_STATUS_A register to ring test and monitor equipment.

SCRM
Scrambler Enable (Input)

This pin when held high will enable the Stream Cipher Scrambling/Descrambling function. If this pin is held low, then bit 0 of PLC_CNTRL_C Register determines if Stream Cipher Scrambling/Descrambling function is enabled.

Power and Ground

V_{DD}
Power (Inputs)

The V_{DD} pins supply +5 V to the device.

V_{SS}
Ground (Input)

The V_{SS} pins ground the device.

FUNCTIONAL DESCRIPTION

Node Processor Interface (NPI)

The Node Processor Interface serves as the interface between an external Node Processor and the PLC-S. The interface is a general purpose synchronous interface.

The Node Processor Interface is controlled by the NPCLK. In normal operation this clock is tied to the BCLK. All signals of the NPI must be synchronous with the NPCLK, that is the signals must be stable a setup time before and a hold time after a rising edge of the NPCLK. Figure 1 illustrates the NPI state machine.

Read Cycle

A read cycle is used by the Node Processor to read data from a PLC-S register. Normally the PLC-S is unaffected by a read, although the INTR_EVENT, VIOL_SYM_CTR, MIN_IDLE_CTR, and LINK_ERR_CTR registers are cleared when read.

A read cycle of one of the PLC-S registers is initiated by the assertion of the $\overline{CS}$ signal which is sampled by the rising edge of NPCLK. Once the $\overline{CS}$ signal is asserted the NPADDR bus and NPRW signals are sampled. The NPRW signal should be high for a read and low for a write. At least one half NPCLK cycle after this edge, the PLC-S will begin to drive the NP bus to allow the chip driving the bus in the previous read or write cycle time to tri-state the NP bus.

After the next rising edge of NPCLK (the second rising edge after the assertion of $\overline{CS}$), the data on the NP bus will be valid. It will remain valid until the second rising edge of NPCLK after the deassertion of $\overline{CS}$. The PLC-S will tri-state the NP bus within 1/2 NPCLK cycle after this clock edge.

The timing described above will allow a read cycle every 2 NPCLK periods. However, if the Node Processor needs to extend the read cycle and have the NP bus valid longer than one clock cycle, it can delay the deassertion of the $\overline{CS}$ signal. For a minimum length read cycle (2 NPCLK periods), the Node Processor must deassert $\overline{CS}$ a setup time before the second rising edge of NPCLK following the assertion of $\overline{CS}$. If $\overline{CS}$ remains asserted for a hold time after the second rising edge of NPCLK, again with respect to $\overline{CS}$ being asserted, the PLC-S will continue to drive the NP bus with valid data for two more rising edges of the NPCLK. When $\overline{CS}$ is kept asserted beyond the initial read cycle, the read cycle extends by two NPCLK periods. The $\overline{CS}$ signal is sampled on the second and each subsequent rising edge of NPCLK after the initial assertion of $\overline{CS}$. The Node Processor can indefinitely extend the read cycle by maintaining the assertion of the $\overline{CS}$ signal. The Node Processor must deassert and then assert the $\overline{CS}$ signal for each unique read access.

Write Cycle

A write cycle is used by the Node Processor to write data into a PLC-S control register. The Node Processor is normally allowed to write to any read-write or write-only register at any time except to the following registers XMIT_VECTOR, VECTOR_LENGTH, TPC_LOAD_VALUE, and TNE_LOAD_VALUE due to special operating conditions imposed by the PLC-S in their usage. If the Node Processor attempts a write on a read-only register or the special registers mentioned above at a wrong time, the PLC-S sets the NP_ERR bit in the INTR EVENT register. The PLC-S will not modify the contents of the register accessed.

The write cycle is very similar to the read cycle. The principal differences are as follows:

- The NPRW signal must be low while $\overline{CS}$ is asserted
- The data to be written must be valid on the second rising edge of NPCLK after $\overline{CS}$ is asserted

The Node Processor must tri-state the NP bus within one half NPCLK period after the second rising edge after the deassertion of $\overline{CS}$. Thus, by delaying the deassertion of the $\overline{CS}$ signal, the Node Processor can extend the write cycle and the time it has to tri-state the NP bus. The deassertion of the $\overline{CS}$ signal has no effect on the PLC-S during a write cycle. The PLC-S will not attempt to write to a selected register more than once until the $\overline{CS}$ signal has been deasserted. Thus, to accomplish back to back writes, the Node Processor must deassert the $\overline{CS}$ signal before attempting the second write.

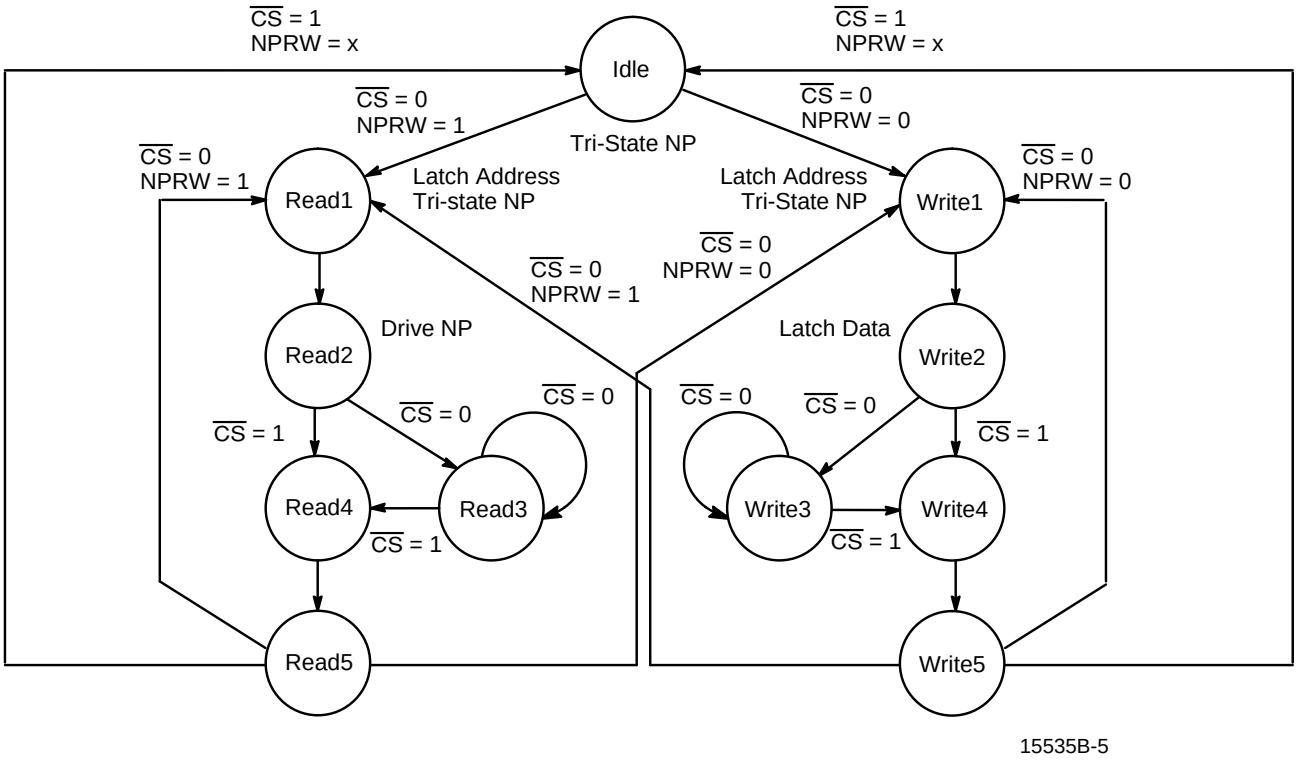


Figure 1. Node Processor Interface State Machine

Registers

The PLC-S contains twenty-six 16 bit registers addressed from 00 to 1A (hex). These registers are listed in Table 1.

Table 1. PLC-S Registers

Address (hex)	Name	Type
00	PLC_CNTRL_A	read/write
01	PLC_CNTRL_B	read/write
02	INTR_MASK	read/write
03	XMIT_VECTOR	read/write (Note 1)
04	VECTOR_LENGTH	read/write (Note 1)
05	LE_THRESHOLD	read/write
06	C_MIN	read/write
07	TL_MIN	read/write
08	TB_MIN	read/write
09	T_OUT	read/write
0A	PLC_CNTRL_C	read/write
0B	LC_LENGTH	read/write
0C	T_SCRUB	read/write
0D	NS_MAX	read/write
0E	TPC_LOAD_VALUE	write only (Note 2)
0F	TNE_LOAD_VALUE	write only (Note 3)
10	PLC_STATUS_A	read only
11	PLC_STATUS_B	read only
12	TPC	read only
13	TNE	read only
14	CLK_DIV	read only
15	BIST_SIGNATURE	read only
16	RCV_VECTOR	read only
17	INTR_EVENT	read only (Note 4)
18	VIOL_SYM_CTR	read only (Note 4)
19	MIN_IDLE_CTR	read only (Note 4)
1A	LINK_ERR_CTR	read only (Note 4)

Notes:

1. *Writable only when the PCM_SIGNALING bit in the PLC_STATUS_B register is not set.*
2. *Writable only when the PCM is in the MAINT state.*
3. *Writable only when the PCM is in the MAINT state and the NOISE_TIMER bit in the PLC_CONTROL_A register is not set.*
4. *Register cleared on read.*

PLC-S Control and Status Registers

The control and status information for the PLC-S is contained in four registers.

PLC-S Control Register A (PLC_CNTRL_A)

PLC_CNTRL_A has address 00 (hex). It is readable and writable. All bits of this register are cleared with the assertion of $\overline{\text{RST}}$. PLC_CNTRL_A is used for the following functions:

- Timer configuration
- Specification of PCM MAINT state options
- Counter interrupt frequency
- PLC-S data path configuration
- Execution of PLC-S Built In Self Test

Note that several bits of this register can only be written if the PCM is in the OFF or MAINT state. If this register is written when the PCM is in any other state these bits will remain unchanged.

The PLC_CNTRL_A register bit assignments are listed in Table 2.

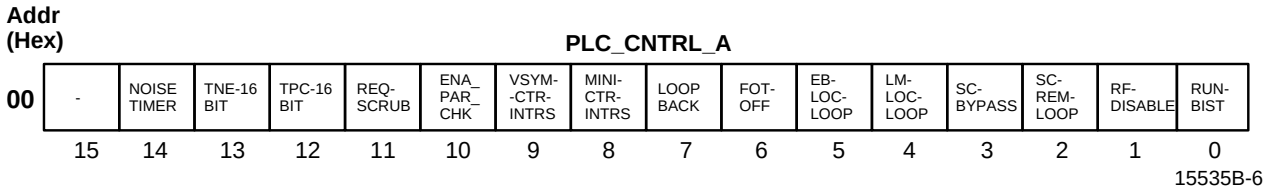


Table 2. PLC_CNTRL_A

Bit	Name	Definition
15		Reserved
14	NOISE_TIMER	The NOISE_TIMER bit allows the noise timing function of the PCM to be used when the PCM is in the MAINT state. This function causes the TNE Timer to be loaded with the value in the NS_MAX register whenever the Line State Machine transitions from Idle Line State to Noise Line State, Active Line State or Unknown Line State. If the timer expires before Idle Line State is recognized, the TNE_EXPIRED bit in the INTR_EVENT register is set.
13	TNE_16BIT	When TNE_16BIT is set it causes the TNE Timer to operate as a 16 bit timer. In this mode the 2 bits of the TNE Clock Divider are bypassed and the TNE Timer is incremented every 80 ns. TNE_16BIT can only be written if the PCM is in the OFF or MAINT state.
12	TPC_16BIT	When TPC_16BIT is set it causes the TPC Timer to operate as a 16 bit timer. In this mode the 8 bits of the TPC Clock Divider are bypassed and the TPC Timer is incremented every 80 ns. TPC_16BIT can only be written if the PCM is in the OFF or MAINT state.
11	REQ_SCRUB	The REQ_SCRUB bit allows limited access to the scrub capability of the PLC-S chip. If the PCM is in the MAINT state or if the CONFIG_CNTRL bit in the PLC_CNTRL_B register is set then the REQ_ SCRUB bit controls the Scrub MUX. If REQ_SCRUB is set then Idle symbols are sourced at the RX 9–0 output port. The output at the TDAT 4–0 output port is controlled separately by the MAINT_LS field in the PLC_CNTRL_B register. This bit may be written at any time, but only takes effect when the PCM is in the MAINT state or if the CONFIG_CNTRL bit in the PLC_CNTRL_B register is set.
10	ENA_PAR_CHK	If this bit is set, then parity checking takes place on TX9–0 lines. If reset, then parity checking is disabled. *Note: PLC-S supports even parity.*
09	VSYM_CTR_INTRS	The VSYM_CTR_INTRS bit controls when the VSYM_CTR interrupt bit in the INTR_EVENT register is asserted. When VSYM_CTR_INTRS is set, the interrupt is generated only when the VIOL_SYM_CTR overflows (reaches 256). When VSYM_CTR_INTRS is cleared, the interrupt is generated every time the VIOL_SYM_CTR is incremented (whenever a violation symbol is detected).
08	MINI_CTR_INTRS	The MINI_CTR_INTRS bit partially controls when the MINI_CTR interrupt bit in the INTR_EVENT register is asserted. When MINI_CTR_INTRS is set, the interrupt is generated when the Minimum Idle Gap Counter portion of MIN_IDLE_CTR overflows (reaches16). When MINI_CTR_INTRS is cleared, the interrupt is generated every time the counter is incremented (whenever a minimum length Idle gap is detected). Note that this bit does not affect interrupts caused by the Idle Counter Minimum Detector portion of MIN_IDLE_CTR.
07	LOOPBACK	When LOOPBACK is set, it causes the $\overline{\text{LPBCK}}$ output pin to be asserted low. This, in turn, causes data to be looped back from the output of the PDT chip to the input of the PDR chip.

Table 2. PLC_CNTRL_A (continued)

Bit	Name	Definition
06	FOT_OFF	The setting of this bit will cause the assertion of the $\overline{\text{FOTOFF}}$ output pin of the PLC-S. Read PLC_CNTRL_C register description for behavior of this signal when scrambling/ descrambling is enabled.
05	EB_LOC_LOOP	When EB_LOC_LOOP is set, a loopback path is set up in the PLC-S chip just prior to the framer. Data from the PLC-S transit path are looped back to the input of the Framer. This loopback path is also set up when the PLC-S is executing its Built In Self Test. Note that this bit also controls which clock the Framer and Elasticity Buffer use. When it is not set, the Recovered Byte Clock is derived from the RSCLK input pin, and when it is set, the BCLK is used. Thus, when this bit gets set, a clock glitch could be created which could cause receive data to be indeterminate for a clock cycle, spurious interrupts, and unknown values in the event counters. EB_LOC_LOOP can only be written if the PCM is in the OFF or MAINT state.
04	LM_LOC_LOOP	When LM_LOC_LOOP is set a loopback path is set up in the PLC-S chip such that data from TX 9–0 are passed through the PLC-S transmit path and looped back to the input of the receive path just after the Elasticity Buffer at the LM Local Loopback MUX. This loopback path differs from EB_LOC_LOOP in that the Framer and Elasticity Buffer are bypassed. LM_LOC_LOOP can only be written if the PCM is in the OFF or MAINT state.
03	SC_BYPASS	The SC_BYPASS bit provides limited control over the PLC-S's data path by providing a physical bypass of the PLC-S. If the PCM is in the MAINT state or if the CONFIG_CNTRL bit in the PLC_CNTRL_B register is set, then the SC_BYPASS bit controls the Bypass MUX. If both SC_BYPASS and REQ_ SCRUB are asserted then RX 9–0 is driven with Idle symbols. If SC_BYPASS is asserted and REQ_SCRUB cleared, then RX 9–0 is driven by the data entering the PLC-S at the TX 9–0 input. Otherwise, RX 9–0 is driven by the data entering the PLC-S at the RDAT 4–0 input. This bit may be written at any time, but only takes effect when the PCM is in its MAINT state or if the CONFIG_CNTRL bit in the PLC_CNTRL_B register is set.
		SC_BYPASS / **REQ_SCRUB** / **RX 9–0** SET / SET / IDLE SET / RESET / TX 9–0 RESET / RESET / RDAT 4–0 RESET / SET / RDAT 4–0
02	SC_REM_LOOP	When SC_REM_LOOP is set, a remote loopback path is set up inside the PLC-S where symbols from the receive data path are looped back onto the transmit data path, traversing all of both paths except for the receive data output latch and the transmit data input latch. If the PCM is in the MAINT state or if the CONFIG_CNTRL bit in the PLC_CNTRL_B register is set, then the SC_REM_LOOP bit controls the Remote Loopback MUX. This loopback is used by the PCM to control the configuration and can be used to monitor the ring or otherwise control configuration during normal operation. This bit only has effect if the EB_LOC_LOOP, LM_LOC_LOOP and CIPHER_LPBCK bits are not set. This bit may be written at any time, but only takes effect when the PCM is in the MAINT state or if the CONFIG_CNTRL bit in the PLC_CNTRL_B register is set.
01	RF_DISABLE	When RF_DISABLE is set, it disables the Repeat Filter state machine in the PLC-S.
00	RUN_BIST	When RUN_BIST is set, it causes the PLC-S to begin running its Built In Self Test. The completion of BIST is indicated via an interrupt. BIST can be stopped before completion by clearing this bit. Once BIST has completed, this bit must be cleared and set again before BIST will restart. For more detail, refer to pages 30 and 42 . Reset PLC-S before setting this bit.

PLC-S Control Register B (PLC_CNTRL_B)

PLC_CNTRL_B has address 01 (hex). It is readable and writeable. All bits of this register are cleared with the assertion of $\overline{RST}$. PLC_CNTRL_B contains signals and requests to direct the process of physical connection management. It is also used to control the Line State Match interrupt.

The PLC_CNTRL_B register bit assignments are listed in Table 3.

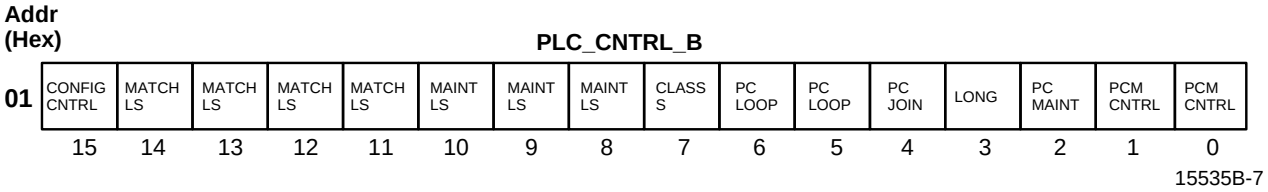


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Table 3. PLC_CNTRL_B

Bit	Name	Definition
15	CONFIG_CNTRL	The CONFIG_CNTRL bit allows control over the Scrub, Bypass, and Remote Loopback datapath MUXes while the PCM is in normal operation. If this bit is set, then the REQ_SCRUB, SC_BYPASS, and SC_REM_LOOP bits in the PLC_CNTRL_A register will have effect regardless of the state of the PCM. If this bit is not set then the REQ_SCRUB, SC_BYPASS and SC_REM_LOOP bits will only have effect if the PCM is in the MAINT state.
14–11	MATCH_LS	The MATCH_LS field specifies line states to be compared with the currently detected line state (as defined by LINE_ST in the PLC_STATUS_A register). When a match occurs, the LS_MATCH interrupt bit in the INTR_EVENT register is asserted. Each bit of MATCH_LS corresponds to a line state. If more than one bit is set, the interrupt is signalled if any of the line states match the current line state. If no bits are set, the interrupt is signalled on any change in the LINE_ST field or the UNKN_LINE_ST bit. It is defined as follows:
		MATCH_LS — **Description** 0000 — Interrupt on any change in LINE_ST or UNKN_LINE_ST 1XXX — Interrupt on Quiet Line State X1XX — Interrupt on Master Line State XX1X — Interrupt on Halt Line State XXX1 — Interrupt on Idle Line State
		In the above table, "X" means don't care. Also Idle Line State refers to ILS16, which is signalled only after sixteen Idle symbols (eight Idle bytes) have been received.
10–8	MAINT_LS	The MAINT_LS field defines the line state the PCM will source while in the MAINT state. The PCM enters the MAINT state from the OFF state if the PC_MAINT bit is asserted. It is further defined as follows:
		MAINT_LS — **Description** 000 — Transmit QUIET Line State 001 — Transmit IDLE Line State 010 — Transmit HALT Line State 011 — Transmit MASTER Line State 100 — Transmit QUIET Line State 101 — Transmit QUIET Line State 110 — Transmit PDR (Transmit PHY_DATA request)—the symbol stream at TX 9–0 is transmitted 111 — Transmit QUIET Line State

Table 3. PLC_CNTRL_B (continued)

Bit	Name	Definition
07	CLASS_S	When CLASS_S is set, signifying that the PHY is a single attach station, the station will not be bypassed before the PCM gets to the ACTIVE state. Note that this bit has effect when the PCM is in normal operation. When the PCM is in the MAINT state, the REQ_SCRUB and SC_BYPASS bits in the PLC_CNTRL_A register control the bypass operation. This bit can only be changed when the PCM is in the OFF state. If this bit is written when the PCM is in any other state, the change will be ignored.
06–05	PC_LOOP	PC_LOOP controls the loopback used in the Link Confidence Test (LCT). When it is set to a value other than zero and the PCM is in the NEXT state, the PCM will perform the LCT in one of three ways. The following table describes the action taken according to the value of the two bits:
		PC_LOOP — **Description** 00 — No LCT is performed 01 — The PCM asserts Transmit PDR. This assumes that Protocol Data Units (PDUs) will be input at TX(9–0). 10 — The PCM asserts Transmit Idle. This causes the PLC-S to source Idle symbols. 11 — The PCM asserts Transmit PDR and sets up a remote loopback path in the PLC-S.
		PC_LOOP should only be written after the PCM_CODE interrupt has been generated. If the PCM is not in the NEXT state, or if PCM_SIGNALING is set, then any value written to this field will be ignored. Once PC_LOOP has been written, it must be cleared and then written again to perform another LCT.
04	PC_JOIN	When PC_JOIN is set and the PCM is in the NEXT state, the PCM will transition to the JOIN state and the PCM join sequence will be started. PC_JOIN should only be written after the PCM_CODE interrupt has been generated. If the PCM is not in the NEXT state or if PCM_SIGNALING is set, then any value written to this field will be ignored. After this bit is set, it must be cleared and then set again to cause another transition from the NEXT state to the JOIN state. Note that if PC_JOIN is set after the LCT has been started but before it has completed, then the LCT will be aborted and the PCM join sequence started.
03	LONG	When LONG is set, the PCM will perform a long LCT; that is, it will continue the test until the processor issues a PC_SIGNAL (i.e., a write to XMIT_VECTOR register), PC_JOIN, or other command. Otherwise it will perform a LCT, that is, it will stop the test after the length of time indicated in the LC_LENGTH register. In either case LCT will stop whenever Master Line State or Halt Line State is detected, indicating that the neighboring station has completed its LCT and has started signaling.
02	PC_MAINT	When PC_MAINT is set, the PCM state machine transitions to the MAINT state if it is currently in the OFF state. If the PCM is not in the OFF state when this bit is written, and subsequently transitions to the OFF state, it will immediately transition to the MAINT state.

Table 3. PLC_CNTRL_B (continued)

<table>
<tr><th>Bit</th><th>Name</th><th>Definition</th></tr>
<tr><td>01–00</td><td>PCM_CNTRL</td><td>PCM_CNTRL controls the PCM state machine. When set to a value other than zero, it will cause the PCM to immediately make a transition to the BREAK, TRACE or OFF state. The transition to the BREAK or OFF state will occur regardless of the state the PCM is in at the time. The transition to the TRACE state will only be made if the PCM is in the ACTIVE state, otherwise PCM_CNTRL will be ignored. The following table describes the action taken according to the value of the two bits:
<table>
<tr><th>PCM_CNTRL</th><th>Description</th></tr>
<tr><td>00</td><td>The PCM state is not affected</td></tr>
<tr><td>01</td><td>The PCM goes to the BREAK state (PC_Start)</td></tr>
<tr><td>10</td><td>The PCM goes to the TRACE state (PC_Trace)</td></tr>
<tr><td>11</td><td>The PCM goes to the OFF state (PC_Stop)</td></tr>
</table>
After a PC_Start (PCM_CNTRL=01) has been issued and before another one can be issued, PCM_CNTRL must first be written with zero and then written with the PC_Start value again. Note that if the PCM goes to the BREAK state for a reason other than writing PCM_CNTRL (e.g. QLS is received, or a timeout occurs), the PCM will not go to the CONNECT state and will remain in the BREAK state until PCM_CNTRL is written with the PC_Start value. If the PCI is in the INSERTED state when PC_Start or PC_Stop is issued, scrubbing will be performed. If the PCI is in the INSERT_SCRUB or REMOVE_SCRUB state when PC_Start or PC_Stop is issued, the scrubbing will be completed before the PCM enters the BREAK or OFF state.</td></tr>
</table>

PLC-S Control Register C (PLC_CNTRL_C)

PLC_CNTRL_C has address OA (hex). It is readable and writeable. Bits 1 through 15 are cleared with the assertion of $\overline{RST}$. Bit 0 (CIPHER_ENABLE) assumes the same value as SCRM after $\overline{RST}$ is asserted.

The PLC_CNTRL_C register bit assignments are listed in Table 4.

PLC_CNTRL_C

Addr (Hex) 0A	RESERVED	SDOFF_ TIMER	SDOFF_ TIMER	SDON_ TIMER	SDON_ TIMER	FOTOFF_ CTRL	FOTOFF_ CTRL	SDON_ ENABLE	SDOFF_ ENABLE	RESERVED	CIPHER_ LPBCK	CIPHER_ ENABLE
	15 14	13	12	11	10	9	8	7	6	5 4 3 2	1	0

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Table 4. PLC_CNTRL_C

Bit	Name	Definition
15–14	RESERVED	These two bits are reserved for diagnostic purposes and must be 0 for normal operation.
13–12	SDOFF_TIMER	These two bits are used to select the timing values shown for deasserting Signal_Detect ENABLE bit is set and scrambler/descrambler is enabled either (by SCRM or CIPHER_ ENABLE) 00=0.76 µs 01=1.32 µs 10=2.52 µs 11=5.12 µs
11–10	SDON_TIMER	These two bits are used to select the timing values shown for asserting Signal_Detect if SDON_ ENABLE bit is set and scrambler/descrambler is enabled either by hardware or software. 00=0.84 µs 01=1.32 µs 10=2.52 µs 11=5.12 µs
9–8	FOTOFF _CTRL	These two bits are used to control the assertion of FOTOFF signal of PLC-S if scrambler/ descrambler is enabled either (by SCRM or CIPHER_ENABLE). The following timing delays are with respect to the time from which PLC-S output scrambled Quiet symbols on TDAT lines. 00=Timer is bypassed (i.e., FOTOFF is asserted at the same time when scrambled Quiet symbols are output on TDAT lines) 01=30 µs delay 10=50 µs delay 11=FOTOFF is never asserted
7	SDON_ENABLE	If this bit is set and scrambler/descrambler is enabled (by SCRM or CIPHER_ENABLE), then SDON_TIMER bits (11–10) will determine the delay for asserting the Signal_Detect signal. During this time, the descrambler is allowed to acquire synchronization of its input stream.
6	SDOFF_ENABLE	If this bit is set and scrambler/descrambler is enabled (bySCRM or CIPHER_ENABLE), then SDOFF_TIMER bits (13–12) will determine the delay for deasserting the Signal_Detect signal.
5–2	RESERVED	Bits 5–2 are reserved and should be set to 0.
1	CIPHER_LPBCK	If this bit is set, then the output of the scrambler is looped back to the input of the descrambler (within PLC-S).
0	CIPHER_ENABLE	This bit is used to enable and disable the scrambler/descrambler function if SCRM (pin #41) is not asserted. If SCRM is asserted, this bit is automatically set to 1. If SCRM is not asserted, the value of this bit is determined by software. The default state (SCRM not asserted) is 0.

PLC-S Status Register A (PLC_STATUS_A)

PLC_STATUS_A has address 10 (hex). It is read-only. It is used to report status information to the Node Processor about the Line State Machine (LSM).

The PLC_STATUS_A register bit assignments are listed in Table 5.

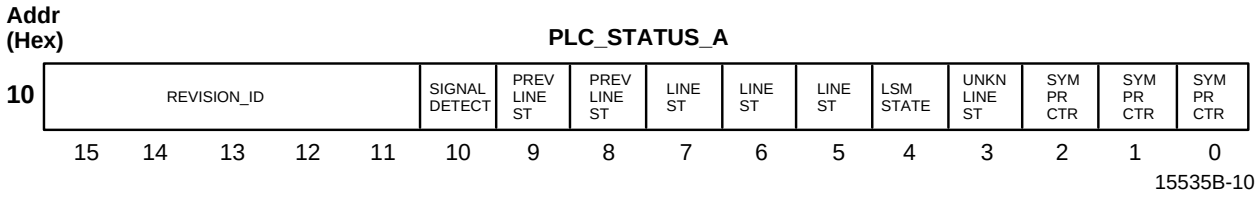

Table 5. PLC_STATUS_A

Bit	Name	Definition
15–11	REVISION_ID	These bits give the revision identification. For Am79864A (PLC-S), these bits equal '11111'. For Am79C864 (PLC), these bits equal '00000'.
10	SIGNAL_DETECT	This bit, when set, indicates that signal detect is deasserted. If SDO equals zero, then SIGNAL_DETECT is one; if SDO equals one, then SIGNAL_DETECT is zero.
09–08	PREV_LINE_ST	This field contains the value of the previous line state whenever line state changes from Quiet Line State, Master Line State, Halt Line State or Idle Line State (ILS16, where ILS16 is achieved after 16 idle symbols) to another line state. When the line state changes from anything else, this field will not be updated. It is further defined as follows:
		PREV_LINE_ST — **Description**
		00 — Quiet Line State (QLS)
		01 — Master Line State (MLS)
		10 — Halt Line State (HLS)
		11 — Idle Line State (ILS16 – achieved after 16 Idle symbols)
07–05	LINE_ST	This field contains the most recently recognized Line State by the LSM. LINE_ST is further defined as follows:
		LINE_ST — **Description**
		000 — Noise Line State (NLS)
		001 — Active Line State (ALS)
		010 — Undefined
		011 — Idle Line State (ILS4 – achieved after 4 Idle symbols)
		100 — Quiet Line State (QLS)
		101 — Master Line State (MLS)
		110 — Halt Line State (HLS)
		111 — Idle Line State (ILS16 – achieved after 16 Idle symbols)
04	LSM_STATE	This field contains the state bit of the LSM state machine.
03	UNKN_LINE_ST	This bit is the Unknown Line State Bit from the LSM. Since a minimum of sixteen symbols is required to satisfy the entry conditions of a line state (four symbols in the case of Idle Line State), the LSM uses this bit to indicate it is attempting to recognize a new line state. This bit is set to a one when the line state is unknown and reset to a zero when known.
02–00	SYM_PR_CTR	This field contains the LSM Symbol Pair Counter. When the count reaches seven, indicating eight consecutive like symbol pairs, then Current Line State is set with the new line state and the Unknown Line State Bit is reset. Note that Idle Line State (ILS4) is reached after just two Idle symbol pairs.

PLC-S Status Register B (PLC_STATUS_B)

PLC_STATUS_B has address 11 (hex). It is read-only. It contains signals and status from the Repeat Filter and Physical Connection Management state machine (PCM).

The PLC_STATUS_B register bit assignments are listed in Table 6.

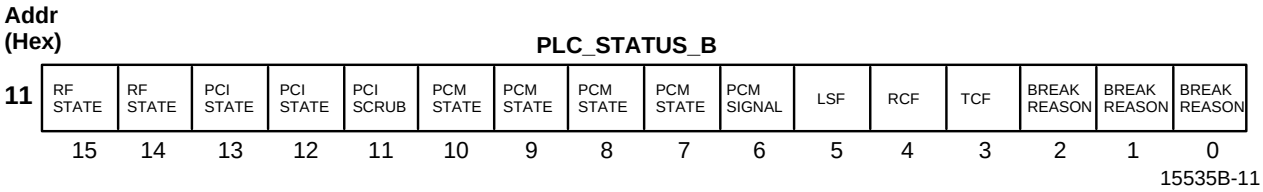

Table 6. PLC_STATUS_B

Bit	Name	Definition	
15–14	RF_STATE	This field contains the state bits of the Repeat Filter state machine. The states are defined as follows:	
		RF_STATE	**Name**
		00	REPEAT
		01	IDLE
		10	HALT1
		11	HALT2
13–12	PCI_STATE	This field contains the state bits of the Physical Connection Insertion state machine. The states are defined as follows:	
		PCI_STATE	**Name**
		00	REMOVED
		01	INSERT_SCRUB
		10	REMOVE_SCRUB
		11	INSERTED
11	PCI_SCRUB	The PCI_SCRUB flag indicates that the scrubbing function is being executed, that is Idle symbol pairs are being sourced on the RX output pins.	
10–07	PCM_STATE	This field contains the state bits of the Physical Connection Management state machine. The states are defined as follows:	
		PCM_STATE	**Name**
		0000	PC0 (OFF)
		0001	PC1 (BREAK)
		0010	PC2 (TRACE)
		0011	PC3 (CONNECT)
		0100	PC4 (NEXT)
		0101	PC5 (SIGNAL)
		0110	PC6 (JOIN)
		0111	PC7 (VERIFY)
		1000	PC8 (ACTIVE)
		1001	PC9 (MAINT)
		1010–1111	Reserved

Table 6. PLC_STATUS_B (continued)

Bit	Name	Definition
06	PCM_SIGNALING	PCM_SIGNALING is a flag from the PCM indicating that the XMIT_VECTOR register has been written. The XMIT_VECTOR and VECTOR_LENGTH registers cannot be written when this flag is set.
05	LSF	The Line State Flag is used by the PCM to indicate that a given line state has been received since entering the current state. It is cleared on every change of PCM state.
04	RCF	The Receive Code Flag is used by the PCM to indicate that the Receive Pseudo Code has started execution. This flag is used to prevent the Receive Pseudo Code from being started multiple times while in the NEXT state.
03	TCF	The Transmit Code Flag is used by the PCM to indicate that the Transmit Pseudo Code has started execution. This flag is used to prevent the Transmit Pseudo Code from being started multiple times while in the NEXT state.
02–00	BREAK_REASON	This field indicates the reason for the PCM state machine's last transition to the BREAK state. It is defined as follows:

BREAK_REASON	Description
000	The PCM state machine has not gone to the BREAK state.
001	PC_Start issued
010	TPC Timer expired after T_OUT
011	TNE Timer expired after NS_MAX
100	Quiet Line State detected
101	Idle Line State detected
110	Halt Line State detected
111	Reserved

Physical Connection Management (PCM) Timers

The PCM contains two timers, TPC and TNE. Both timers have a clock divider circuit to reduce the frequency at which they are clocked.

TPC Timer

The TPC Timer is a 16-bit timer. In normal operation it is read-only by the Node Processor. TPC is read at address 12 (hex). When the PCM is in the MAINT state a value can be written to TPC by writing TPC_LOAD_VALUE at address 0E. The TPC Timer is incremented by the output of an 8-bit clock divider circuit. It is incremented every 20.48 µs (2^8 times 80 ns). The value in the TPC Clock Divider is contained in bits 7 through 0 of the CLK_DIV register at address 14 (hex).

The TPC Timer is used while the PCM is attempting to establish a physical connection with a neighboring PCM. It is used to ensure that state transitions proceed at the desired rate.

The timer is loaded with a two's complement value and counts up until it reaches zero. In normal operation the timer is loaded by the PCM from the TPC Timing Parameter Registers, which contain the two's complement of the time value in 20.48 µs units. At the same time the TPC Timer is loaded, the TPC Clock Divider is loaded with zero.

When the PCM is in the MAINT state, the TPC Timer can be loaded directly from the Node Processor. The Node Processor accomplishes this by writing a 16-bit value which is loaded into the timer (the TPC Clock Divider is loaded with zero). The value written is the two's complement of the time in 20.48 µs units. If the PCM is not in the MAINT state when a write is attempted to the TPC timer, the NP_ERR bit in the INTR_EVENT register will be set and the timer will not be loaded.

The timer may also be used in 16-bit mode, where the TPC Clock Divider is bypassed and the timer is incremented every 80 ns when in operation. In this mode the value loaded into the timer is the two's complement of the time remaining in 80 ns units. This feature, controlled by the TPC_16BIT bit in the PLC_CNTRL_A register, is intended for test purposes, where it is desirable to run the timer for only short periods of time.

TNE Timer

The TNE Timer is a 16-bit timer. In normal operation it is read-only by the Node Processor. TNE is read at address 13 (hex). When the PCM is in the MAINT state and the NOISE_TIMER bit in the PLC_CNTRL_A register is not set, a value can be written to TNE by writing TNE_LOAD_VALUE at address 0F. The TNE Timer is incremented by the output of a 2-bit clock divider circuit. It is incremented every 0.32 µs (2^2 times 80 ns).

The value in the TNE Clock Divider is contained in bits 9 and 8 of the CLK_DIV at address 14 (hex).

The TNE Timer is used to time the length of (potential) noise events while the PCM is in the ACTIVE state. The TNE Timer is started whenever the Line State Machine transitions from Idle Line State to Noise Line State, Active Line State, or Unknown Line State. If the timer expires before the LSM recognizes Idle Line State again, the PCM transitions to the BREAK state.

The timer is loaded with a two's complement value and counts up until it reaches zero. In normal operation the timer is loaded by the PCM from the NS_MAX Timing Parameter Register, which contains the two's complement of the time value in 0.32 μs units, whenever the LSM leaves Idle Line State. At the same time the TNE Timer is loaded, the TNE Clock Divider is loaded with zero.

When the PCM is in the MAINT state the TNE timer can be loaded directly from the Node Processor. The Node Processor accomplishes this by writing a 16-bit value which is loaded into the timer (the TNE Clock Divider is loaded with zero). The value written is the two's complement of the time in 0.32 μs units. If the PCM is not in the MAINT state when a write is attempted to the TNE timer, the NP_ERR bit in the INTR_EVENT register will be set and the timer will not be loaded.

Note that through use of the NOISE_TIMER bit in the PLC_CNTRL_A register, the TNE Timer can be used to time noise duration when the PCM is in the MAINT state without the timer having to be explicitly loaded by the Node Processor. The Node Processor should not attempt to load the TNE Timer when the NOISE_TIMER bit in the PLC_CNTRL_A is set. If this condition is violated the NP_ERR bit in the INTR_EVENT register will be set and the timer will not be loaded.

The timer may also be used in 16-bit mode, where the TNE Clock Divider is bypassed and the timer is incremented every 80 ns when in operation. In this mode the value loaded into the timer is the two's complement of the time remaining in 80 ns units. This feature, controlled by the TNE_16BIT bit in the PLC_CNTRL_A register, is intended for test purposes, where it is desirable to run the timer for only short periods of time.

Physical Connection Management Timing Parameters

The PCM uses a number of different timing parameters while forming a physical connection. The parameters are programmable and must be written by the node processor. The registers are readable at any time. The parameters are 16 bits in length and are loaded into the TPC Timer. They hold the two's complement of the time in 20.48 μs (2^8 times 80 ns) units. They have a maximum value of about 1.34 seconds (2^{16} times 20.48 μs). When the TPC Timer is in 16-bit mode the timing parameters are the two's complement of the time in 80 ns units and can have a maximum value of about 5.24 ms (2^{16} times 80 ns).

In addition to the TPC Timing Parameters, there is one timing parameter used by the TNE Timer. Unlike the TPC Timing Parameters, NS_MAX holds the two's complement of the time in 0.32 μs (2^2 times 80 ns) units. It can have a maximum value of about 20.97 ms (2^{16} times 0.32 μs). When the TNE Timer is in 16-bit mode, NS_MAX is the two's complement of the time in 80 ns units and can have a maximum value of about 5.24 ms (2^{16} times 80 ns).

Table 7 summarizes the PCM timing parameters.

Minimum Connect State Time Register (C_Min)

The Minimum Connect State Time (C_Min) register has address 06 (hex). It has a recommended value of 1.6 ms (FFB2 hex in 2's complement). This is the minimum time required to remain in the Connect State to assure that the other end has recognized HALT Line State.

Minimum Line State Transmit Time Register (TL_Min)

The Minimum Line State Transmit Time Register (TL_Min) has address 07 (hex). It has a recommended value of 0.03 ms (FFFE hex in 2's complement). This is the minimum time required to transmit a Line State before advancing to the next PCM state.

Minimum Break Time Register (TB_MIN)

The Minimum Break Time (TB_MIN) register has address 08 (hex). It has a recommended value of 5 ms (FF10 hex in 2's complement). When PCM performs a break (in state BREAK), the break shall be of adequate length to allow time for a response to be seen on the inbound physical link. This time allows for the possibility of a bypass failure mode in this or a neighboring station that could cause four PHYs to be connected in a loop and produce an invalid response to the break. The minimum break time guarantees that in this case the response to the break will propagate around the loop and be seen on the inbound link.

Signaling Timeout Register (T_OUT)

The Signaling Timeout (T_OUT) register has address 09 (hex). It has a recommended value of 100 ms (ECED hex in 2's complement). A response from a neighboring PCM must be received by T_OUT. When a response is expected and no transition is made in T_OUT time, a transition is made to the BREAK state.

Link Confidence Test Time Register (LC_LENGTH)

The Link Confidence Test (LCT) Time register (LC_LENGTH) has address 0B (hex). This register specifies the time duration of the LCT and limits the duration of loopback to prevent deadlock. It has a recommended value of 50 ms (F676 hex in 2's complement)

for the short LCT. For medium LCT, it has a recommended value of 500 ms (A0A2 hex in 2's complement).

Scrub Time Register (T_SCRUB)

The Scrub Time (T_SCRUB) register has address 0C (hex). It has a recommended value of 3.5 ms. T_SCRUB is the same as the MAC TVX time. Its use is described in the Physical Connection Insertion Process functional description.

Noise Time Register (NS_MAX)

The Noise Time (NS_MAX) register has address 0D (hex). It has a recommended value of 2 ms. NS_MAX is the maximum length of time that noise is tolerated before a connection is broken down.

Table 7 summarizes the recommended values for the timing parameter registers. Also shown is the 2's complement, hexadecimal equivalent of the recommended value and the timer used for the parameter.

Table 7. Summary of PCM Timing Parameters

Parameter	Recommended Value (ms)	Register Value (2's comp/hex)	Timer	Address (hex)
C_MIN	1.6	FFB2	TPC	06
TL_MIN	0.03	FFFE	TPC	07
TB_MIN	5	FF10	TPC	08
T_OUT	100	ECED	TPC	09
LC_LENGTH	50	F676	TPC	0B
LC_LENGTH	500	A0A2	TPC	0B
T_SCRUB	3.5	FF6D	TPC	0C
NS_MAX	2	E796	TNE	0D

Physical Connection Management Bit Signaling Registers

The PLC-S contains three registers used by the PCM to perform bit signaling. Bit signaling is the mechanism the PCM uses to transfer information to the PCM in the neighboring station.

Transmit Vector Register (XMIT_VECTOR)

The Transmit Vector register has address 03 (hex). It is readable and writable. All bits of the register are cleared with the assertion of $\overline{RST}$. The PCM_SIGNALING bit must not be asserted in order to write to this register. If PCM_SIGNALING is asserted when a write is attempted, the register will not be written and the NP_ERR bit in the INTR_EVENT register will be set. This register is readable at any time.

The Transmit Vector consists of from one to sixteen bits of data to be transmitted to the neighboring PCM. Bits are transmitted one at a time by the bit signaling mechanism. A one bit is represented by the transmission of Halt Line State and a zero bit by Master Line State. Bit 0 of this register is the first bit to be transmitted, then bit 1, etc., up to the number of bits specified in the VECTOR_LENGTH register.

Writing this register causes PCM_SIGNALING to be asserted. Therefore, the VECTOR_LENGTH register must be initialized before this register is written.

Transmit Vector Length Register (VECTOR_LENGTH)

The Transmit Vector Length register has address 04 (hex). It is readable and writable. All bits of the register are cleared with the assertion of $\overline{RST}$. The PCM_SIGNALING bit must not be asserted in order to write to this register. If PCM_SIGNALING is asserted when a write is attempted, the register will not be written and the NP_ERR bit in the INTR_EVENT register will be set. This register is readable at any time.

Bits 15 through 4 of this register are unused. Any value written to these bits will be ignored. These bits will always be read as zeros.

Bits 3 through 0 of this register contain the number of bits in the XMIT_VECTOR register to transmit. The value in this field (0 to 15) is actually one less than the number of bits to transmit (1 to 16).

Receive Vector Register (RCV_VECTOR)

The Receive Vector register has address 16 (hex). It is read-only.

The Receive Vector consists of from one to sixteen bits of data received from the neighboring PCM. Bits are received at the same time bits are being transmitted. As bit n is being transmitted from the Transmit Vector, bit n is received and placed in the Receive Vector register. If Halt Line State is received, then bit n is a one, and if Master Line State is received then bit n is a zero. Bit 0 of this register is the first bit received, then bit 1, etc., up to the number of bits specified in the VECTOR_LENGTH register.

Although this register is readable at any time, if PCM_SIGNALING bit is asserted when this register is read the data may be incomplete.

Event Counters

The PLC-S contains three event counter registers and one threshold value register (used for gathering information about errors occurring on its associated physical link and for monitoring Idle symbol gaps between packets).

Violation Symbol Counter (VIOL_SYM_CTR)

The Violation Symbol Counter has address 18 (hex). It is read-only and is cleared whenever it is read as well as when $\overline{RST}$ is asserted. The high order 8 bits of the register will always be read as zeros. The low order 8 bits will contain the counter value. The VSYM_CTR bit in the

INTR_EVENT register is set whenever the counter increments or whenever the counter overflows (reaches 256), depending on the setting of the VSYM_CTR_INTRS bit in the PLC_CNTRL_A register. When the counter overflows it wraps to zero and continues to count.

The Violation Symbol Counter is incremented whenever the 4B/5B decoder in the PLC-S decodes a violation symbol. See the Decoder description for the symbols considered to be violation symbols by the Decoder. They are represented as a "V" in Table 15.

Minimum Idle Counter (MIN_IDLE_CTR)

The Minimum Idle Counter has address 19 (hex). It is read-only and is cleared whenever it is read as well as when $\overline{RST}$ is asserted. The high order 9 bits of the register will always be read as zeros.

Bits 6 through 4 of the counter contain the value in the Idle Counter Minimum Detector. This is the minimum number of inter-packet Idle symbol pairs seen since the counter was last reset. It gets reset to 7. Whenever the value changes to a lower value, the MINI_CTR bit in the INTR_EVENT register is set. The Idle symbol pair count definitions are given in Table 8.

Table 8. Idle Counter Minimum Detector

MIN_IDLE_CTR 6–4	Idle Symbol Pair Count
100	7 or more
101	6
111	5
110	4
010	3
011	2
001	1
000	0

Bits 3 through 0 of the counter contain the value in the Minimum Idle Gap Counter. This is the number of times the minimum number of inter-packet Idles has been seen since the last reset. It gets reset to 1. The MINI_CTR bit in the INTR_EVENT register is set whenever the counter increments or whenever the counter overflows (reaches 16), depending on the setting of the MINI_CTR_INTRS bit in the PLC_CNTRL_A register. When the counter overflows, it remains at 16. The minimum Idle occurrence count definitions are given in Table 9.

Table 9. Minimum Idle Gap Counter

MIN_IDLE_CTR 3–0	Minimum Idle Occurrence Count
0000	1
1000	2
1100	3
0100	4
0101	5
0111	6
1111	7
1110	8
1010	9
0010	10
0011	11
0001	12
1001	13
1101	14
0110	15
1011	16

Link Error Event Counter (LINK_ERR_CTR)

The Link Error Event Counter has address 1A (hex). It is read-only and is cleared whenever it is read as well as when $\overline{RST}$ is asserted. It is an 8-bit counter contained in bits 7 through 0 of the register. Bits 15 through 8 of the register will always be read as zeros. The LE_CTR bit in the INTR_EVENT register is set whenever the counter reaches the value contained in the LE_THRESHOLD register. The counter will continue to count past this point. When the counter overflows (reaches 256), it wraps to zero and continues to count.

The Link Error Event Counter is part of the Link Error Monitor (LEM) and is implemented in the PLC-S. The LEM monitors Bit Error Rate (BER) of an active link and detects and isolates physical links having an inadequate BER, e.g. due to a marginal link quality, link degradation or connector unplugging.

In addition to the counter, the PLC-S also contains logic to detect link error events. Link error events are defined in Table 12.

Link Error Event Threshold Register (LE_THRESHOLD)

The Link Error Event Threshold register has address 05 (hex). It is readable and writeable and is cleared on the assertion of $\overline{RST}$. Bits 7 through 0 of this register contain a value that controls when the LE_CTR bit in the INTR_EVENT register is set. Whenever the value in the LINK_ERR_CTR reaches the value contained in this register the LE_CTR bit will be set. Bits 15 through 8 are ignored and will always be read as zeros.

Interrupt Registers

The PLC-S has two interrupt registers which correspond bit-for-bit. One of the registers contains bits set by interrupt events and the other a mask which enables or disables the assertion of the $\overline{INT}$ pin due to a corresponding interrupt event.

Interrupt Event Register (INTR_EVENT)

The Interrupt Event Register (INTR_EVENT) has address 17 (hex). It is read-only and is cleared whenever it is read, as well as when $\overline{RST}$ is asserted. It is used by the PLC-S to report events to the node processor. Individual bits are set by the PLC-S for the particular event occurrences. When an interrupt is generated (via the $\overline{INT}$ pin), the node processor should read this register to identify the source(s) of the interrupt.

Note that while the RUN_BIST bit in the PLC_CNTRL_A register is set, all interrupts are masked (prevented from asserting the $\overline{INT}$ pin) except BIST_DONE. Since this is the only interrupt that can occur in this situation, BIST_DONE need not occupy a bit in the INTR_EVENT register. The interrupt is cleared by clearing the RUN_BIST bit in the PLC_CNTRL_A register.

The INTR_EVENT register bit assignments are listed in Table 10.

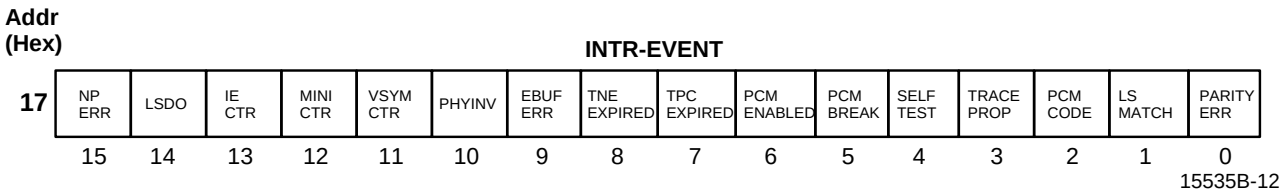

Table 10. INTR_EVENT Register

Bit	Name	Definition
15	NP_ERR	An event indicating that the Node Processor has requested a read or write to an invalid register. This case includes a write to a read-only register (such as this one), a read of a write-only register, a write to a XMIT_VECTOR or VECTOR_LENGTH register when PCM_SIGNALLING is set, a write to the TPC Timer register while the PCM is not in the MAINT state, and a write to the TNE Timer register while the PCM is not in the MAINT state or NOISE_TIMER is set.
14	LSDO	This bit is set whenever SD0 pin is asserted.
13	LE_CTR	An event indicating that the Link Error Event Counter has reached the value contained in the LE_THRESHOLD register.
12	MINI_CTR	Indicates that either of two events has occurred in the MIN_IDLE_CTR: the Idle Counter Minimum Detector has changed to a lower value; or, the Minimum Idle Gap Counter has incremented or overflowed, depending on the MINI_CTR_INTRS bit in the PLC_CNTRL_A register.
11	VSYM_CTR	An event indicating that a Violation Symbol Counter has incremented or overflowed, depending on the VSYM_CTR_INTRS bit in the PLC_CNTRL_A register.
10	PHYINV	An event indicating that the Physical Layer Invalid signal has been asserted.
09	EBUF_ERR	An event indicating that the Elasticity Buffer has detected an overflow or underflow.
08	TNE_EXPIRED	An event indicating that the TNE Timer has expired, i.e. reached zero.
07	TPC_EXPIRED	An event indicating that the TPC Timer has expired, i.e. reached zero.
06	PCM_ENABLED	An event indicating the PCM has asserted SC_JOIN, has completed scrubbing, and is in the ACTIVE state.
05	PCM_BREAK	An event indicating the PCM has entered the BREAK state.
04	SELF_TEST	An event indicating Quiet or Halt Line State has been received while the PCM is in the TRACE state.
03	TRACE_PROP	An event indicating that Master Line State has been received while the PCM is in the ACTIVE or TRACE state.
02	PCM_CODE	An event indicating the PCM has completed transmitting the last bit in the vector written to the XMIT_VECTOR register and has received the corresponding bit of the RCV_VECTOR, or that the Link Confidence Test has completed. In the case where signalling has completed, PCM_CODE will not be set until the RCF flag has been set again.
01	LS_MATCH	An event indicating that the line state detected equals the line state in the MATCH_LS field of the PLC_CNTRL_B register.
00	PARITY_ERR	An event indicating that a parity error has been detected on the TX 9–0 input pins. This bit will not be set if ENA_PAR_CHK bit in PLC_CNTRL_A register is cleared.

Interrupt Mask Register (INTR_MASK)

The Interrupt Mask Register (INTR_MASK) has address 02 (hex). It is readable and writeable. It allows the disabling of interrupts caused by specific events. The INTR_MASK contains a bit that corresponds to each bit of the INTR_EVENT register that, when clear, prohibits that condition from causing an interrupt to the node processor. For each set bit, the setting of the corresponding bit in the INTR_EVENT will generate an interrupt to the node processor via the $\overline{INT}$ pin of the PLC-S. Note however, that the operation of a bit in the INTR_EVENT remains unchanged by the state of the corresponding bit in the INTR_MASK. All bits of this register are cleared with the assertion of $\overline{RST}$.

Addr (Hex) **INTR-MASK**

02	NP ERR	LSDO	IE CTR	MINI CTR	VSYM CTR	PHYINV	EBUF ERR	TNE EXPIRED	TPC EXPIRED	PCM ENABLED	PCM BREAK	SELF TEST	TRACE PROP	PCM CODE	LS MATCH	PARITY ERR
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Built In Self Test Register

In addition to a bit in the PLC_CNTRL_A register and a bit in the INTR_EVENT register, Built In Self Test requires one register.

Built In Self Test Signature Register (BIST_SIGNATURE)

The Built In Self Test Signature register (BIST_SIGNATURE) has address 15 (hex). It is a 16 bit, read-only register that contains the resultant signature after execution of the chip's self test. After BIST has been completed (signaled by the $\overline{INT}$ pin being asserted), this register should be read and its contents compared against the known good signature for the PLC-S to determine whether the chip has passed its self test. The value of the BIST signature is 5B6B (hex).

Framer

The Framer accepts five bit wide parallel data as well as the recovered clock from the Physical Data Receiver (PDR) chip. Generally, data received by the Framer is not framed into proper FDDI symbols. The Framer is used to align the incoming data to form proper symbols before the data is passed onto the Elasticity Buffer. A starting delimiter that is used at the beginning of each frame is detected by the Framer and used to determine proper symbol boundaries for the data. The Framer has been designed such that the starting delimiter (the JK symbol pair) can be detected independent of previous framing.

Elasticity Buffer

The purpose of the Elasticity Buffer is to perform the necessary buffering in order to allow the passing of data between different FDDI stations with independent station clocks. The Elasticity Buffer consists of an 80-bit buffer and some control circuitry. The buffer is used to compensate for the differences in the transmit and receive clock frequencies in the station. Data is clocked into the buffer by the recovered byte clock and clocked out of the buffer by the byte clock. The recovered clock is also used to drive all the input circuitry including the input controller and the local input pointer. The byte clock is used to drive the output circuitry including the output pointer, the output controller, the overflow/underflow detection circuitry and the output buffer. Note that the Elasticity Buffer uses a different version of the byte clock than the rest of the PLC-S chip. This version is generated on chip from LSCLK.

Smoother Operation

The Smoother resides in the Elasticity Buffer. The main purpose of the Smoother is to add and delete Idle symbols into the data stream when the Smoother detects an inadequate or a surplus number of Idles between frames.

The Smoother function is necessary because the Elasticity Buffer may delete symbols from the preamble of a frame. If multiple PHY Elasticity Buffers delete symbols from the same preamble, then the number of Idle symbols in that preamble can reach a value resulting in a loss of that frame. This may happen because according to the ANSI PHY document,

- An Elasticity Buffer is not required to recenter on preambles shorter than four symbols
- MAC is not required to repeat frames with preambles shorter than two symbols
- MAC is not required to copy frames with preambles shorter than twelve symbols

The Smoother absorbs surplus symbols from longer preambles and redistributes them into shorter preambles. The smoothing function is capable of inserting additional preamble symbols into repeated preambles shorter than fourteen symbols. The Smoother attempts to maintain 7 Idle bytes (or 14 Idle symbols) between frames. If there are less than 7 Idle bytes the smoother may inject Idle bytes onto the data path. If there are more than 7 Idle bytes in the preamble the Smoother may delete at least one Idle byte of the longer preamble.

Line State Machine (LSM)

In the FDDI network, a special group of symbols called Line State Symbols (Q – Quiet, H – Halt, I – Idle) are transmitted to establish the physical connection between neighboring stations. These Line State Symbols are unique in that they may be recognized independently of symbol boundaries.

The LSM constantly monitors symbol pairs coming from the Elasticity Buffer. The current symbols pair is encoded (ENC_CSP) and compared to the encoded value of the previous symbol pair (ENC_PSP). The symbol pairs are counted by the Symbol Pair Counter (SYM_PR_CTR – bits 2–0 in the PLC_STATUS_A Register) until a Line State is reached. Once a Line State is reached the SYM_PR_CTR is stopped, the new line state (LINE_ST – bits 7–5 in the PLC_STATUS_A Register) is stored and the UNKN_LINE_ST bit is reset to zero. Upon receiving the first symbol pair that is not identical to the previous symbol pair (and is not a JK or noise symbol pair) the SYM_PR_CTR is started and UNKN_LINE_ST is set to 1 until conditions for the next Line State are met.

The recognition of these Line States is reported to the PCM, which uses this information for insertion and removal of the station from the ring, ring recovery and maintenance. A change in the value of LINE_ST is reported to the Node Processor by means of an interrupt which can be enabled or disabled by setting the MATCH_LS bits in the PLC_CNTRL_B register.

The LSM is reset into the NOT_ACTIVE state with LINE_ST = NLS, UNKN_LINE_ST = 0, SYM_PR_CTR = 000 and PREV_LINE_ST = QLS.

The function of the LSM State Machine is described in Table 11.

Table 11. LSM State Descriptions

State	Description
LSM0	This is the NOT ACTIVE state. The LSM is in this state whenever LINE_ST equals anything other than ALS. A transition to LSM1 will occur whenever ENC_CSP = JK.
LSM1	This is the ACTIVE state. The LSM will stay in this state only if ENC_CSP = JK, DATA, or II (if ENC_CPS = I I then only if ENC_PSP not = I I). Anything else will cause a transition to LSM0.

Link Error Monitor (LEM)

The Link Error Monitor provides an indication of the inbound link quality to the Physical Connection Management entity. The PCM uses this information to determine if the Link Confidence Test passes to establish a new connection. Once a link is active the PCM continually runs a Link Error Monitor test to detect and isolate links having an inadequate bit error rate.

The LEM hardware consists of a detector, accumulator and threshold element. The detector is a state machine which constantly monitors incoming symbol pairs on the receive path. When Link Error Events are detected they are counted by the 8-bit Link Error Event Counter (LINK_ERR_CTR). When the LINK_ERR_CTR matches the count written to the Link Error Event Threshold Register (LE_THRESHOLD) the LE_CTR bit in the INTR_EVENT register is set.

A Link Error Event is defined in Table 12 below. Note that a number following an H or V symbol indicates the value of that symbol's encoding. For instance, H2 is the symbol "00010", V5 is the symbol "00101", etc.

Table 12. LEM Error Events

Noise Events	Exceptions
Transition from Idle Line State to Noise Line State or Unknown Line State	When the symbol pair which causes the transition is followed by: QQ, QH, HQ, or HH
When in Active Line State, detection of the symbol pair: XV', V"X, J ~K, ~JK, or I D where: V' = H1, H2, H8, H16, V3, V5, V6, V12, or J V" = H1, H2, H8, H16, V3, V5, V6, V12, or K D = n, R, S, or T X = don't care ~K = not K; ~J = not J	None
When in Active Line State, detection of the symbol pair: I I followed by D X I I followed by I D	None
Other transitions from Active Line State to Noise Line State or Unknown Line State	When the symbol pair H4 H4 which causes the transition is followed by: H4 Q, Q H4, I I, H4 I, or JK

Physical Connection Management (PCM)

Connection Management (CMT) defines the operation of Physical Layer (PHY) insertion and removal, and the connection of PHY entities to the Media Access Control (MAC) entities. Physical Connection Management (PCM) is a subset of CMT. Fundamental to this task is the management of a connection between two physical attachments (PHYs) in adjacent stations. It is the job of the PCM state machines in both stations to cooperate in forming a connection between the two PHYs within the rules established by the Connection Management.

The FDDI SMT ANSI Standard defines the following types of physical attachment:

A. Dual ring PHY entity connected to Primary Ring In, Secondary Ring Out

B. Dual ring PHY entity connected to Secondary Ring In, Primary Ring Out

M. Concentrator PHY entity type “Master” to provide connection within the concentrator tree

S. Single attachment PHY entity type “Slave”, intended to be attached to a PHY of type M within a concentrator tree.

Figure 2 illustrates different connection types.

CMT defines the type of physical connection between two physical attachments. PCM consists of two entities; the PCM State Machine and the PCM Pseudo Code. The PLC-S chip implements the state machine, while the pseudo code is implemented in SMT software. SMT software decides the acceptability of connections and communicates it to the neighboring PHY.

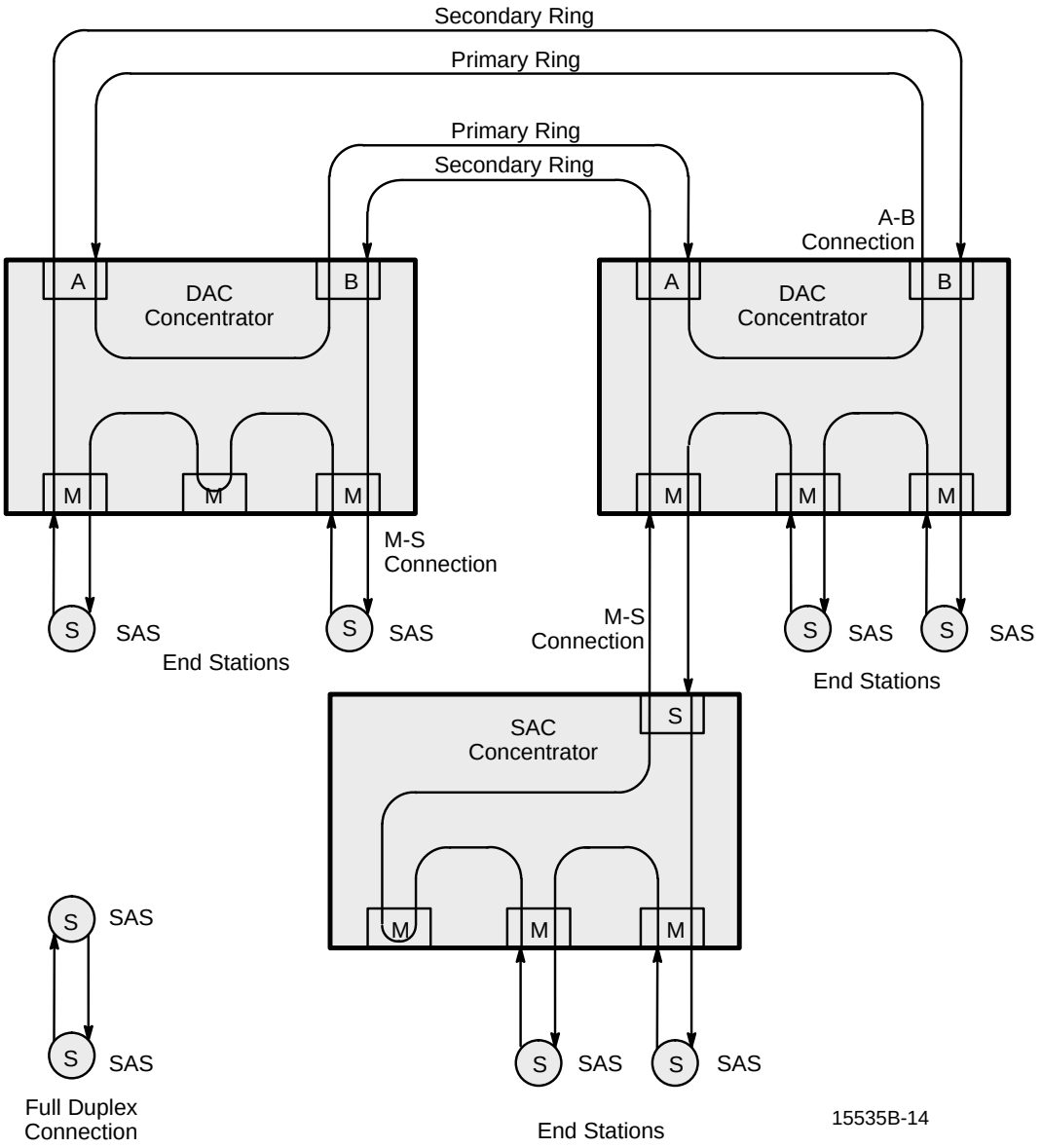


Figure 2. Illustrations of Connection Types

The Physical Connection Insertion (PCI) State Machine works in conjunction with the PCM State Machine. It controls ring scrubbing and the insertion and removal of a station on the ring.

PCM Operation

The PLC-S implements the PCM state machine as specified in the ANSI FDDI SMT standard. By only allowing a specific set of connection types, CMT secures a deterministic ring topology, independent of the sequence of station power on, etc. The primary purpose for the PCM is to enforce these allowable connections. The local PCM announces its attachment type to the remote PCM and listens for the type of attachment from the remote PCM. If they are compatible, the local PCM accepts the connection, reporting the type of connection to the station configurator. Once the connection type has been established, the two PCMs share in testing the pair of physical links between them. If this is successful, the link can then be configured into the ring. The bit signaling protocol is implemented in a fashion which reduces the software processing overhead considerably while at the same time allow enough flexibility to change the actual pseudo code.

PCM State Machine

The PCM State machine implements the connection sequence for establishing the physical connection into the ring. The state machine is as described in the SMT document. The PCM state machine uses various timers whose expiration values are programmable by the various time registers. The time registers that are relevant to the PCM state machine are the Minimum Connect State (C_Min), Minimum Line State Transmit Time (TL_MIN) Minimum Break (TB_Min), Signalling timeout (T_Out), Link Confidence Test (LC_Length)and Noise time (NS_Max). The current state of PCM is readable through the PLC_Status_B Register.

The PCM State machine is started by PC_Start signal from the node processor as indicated by PCM_CNTRL bits of PLC_CNTRL_B. The PCM State machine can be brought to the OFF state (Stop connection) also by programming PCM_CNTRL bits of PLC_CNTRL_B.

PCM flags that are readable by the Node Processor through the status register of PLC-S include Line State Flag (LSF), Receive Code Flag (RCF) and Transmit Code Flag (TCF).

Once the connection is established and the ring is scrubbed, PCM indicates the event through the PCM enabled bit of the INTR_EVENT register.

The function of the PCM State Machine is described in Table 13.

Pseudo Code Bit Signaling (PCS)

As a part of the PCM process, before the connection is established, a sequence of bits are communicated through the physical link. These bits as defined in the standard convey the following information:

- Normal or Escape Sequence (escape sequence is not defined by the standard)
- The type of Physical connection (Slave, Master, Peer A or Peer B)
- The acceptance of the connection
- The length of the Link Confidence Test (LCT): short, medium, long or extended
- MAC for LCT
- LCT Pass/Fail
- MAC Loopback
- MAC output connected to this PHY

The above information is conveyed in the first 10 bits of the standard pseudo code bit signalling sequence. If more bits are needed, more information up to a maximum of 16 bits can be sent through this process.

The normal operation of the PCM is as follows. When the PCM is in the OFF state, all the parameter registers and the configuration registers are loaded with the appropriate values. The PC_Start is written into the PLC_CNTRL_B register. The VECTOR_LENGTH register is then written with value n-1 (n = the number of bits to be transmitted). Next, the XMIT_VECTOR register is written with the bit pattern which is to be transmitted. The PCM then transitions through the BREAK, CONNECT and NEXT states. ***Note:*** *The VECTOR_LENGTH and XMIT_VECTOR register has to be written after PC_STart and before TB_MIN timer expires.* It then transitions back and forth between the NEXT and the SIGNAL states until all the bits in the XMIT_VECTOR register are transmitted. It causes Master Line State to be sourced to signal a zero bit and Halt Line State to be sourced to signal a one bit. While it transmits all the bits it also receives the corresponding bits from the remote station and forms a Receive Vector which is stored in the RCV_VECTOR register. When all the bits are transmitted the PCM_CODE Interrupt bit is set. The Node Processor can then read the RCV_VECTOR register. (***Note****: The PCM is still in the NEXT state).*

If for any reason (other than PC_Start) the PCM state machine transitions to the BREAK state, then a PC_Start has to be issued before the connection process can begin again. This is to allow the VECTOR_LENGTH and the XMIT_VECTOR to be re-initialized. Also, any transition to the BREAK state sets the PCM_BREAK interrupt and writes the reason for the transition in the BREAK_REASON field in the PLC_STATUS_B register.

Typically, three bits are written into the XMIT_VECTOR register in the beginning. After they are received, the received bits are read by the node processor to know the connection type. Then the node processor decides if the

connection is acceptable and flags the next bit. On receipt of the corresponding bit from the neighbor, the node processor decides the length of the Link Confidence Test and communicates it through the next two bits. On receipt of the corresponding bits from the neighbor, the node processor communicates if it wants to perform LCT through the MAC. After receipt of corresponding bit from the neighbor, the LCT is performed. If the length of the LCT is longer, then the node processor will set the LONG bit in the PLC_CNTRL_B register. If LONG bit is set, the node processor has to issue a PC_SIGNAL command to progress the sequence and communicate the status of LCT in the next bit.

On receipt of the corresponding bit from the neighbor, the MAC LOOPBACK bit is sent. On receipt of MAC LOOPBACK bit from the neighbor, the MAC LOOPBACK is performed based on the bit information. Once the MAC LOOPBACK is finished, the last bit is communicated indicating if the MAC output is going to be connected to this PHY.

After the LCT is completed (i.e. after LC_LENGTH, or after Halt or Master Line State is received) the PCM_CODE interrupt is set. If the Node Processor decides to transmit more signaling bits it should load the VECTOR_LENGTH with a new value of n and then the XMIT_VECTOR register with the bit pattern to be transmitted. The PCM again starts transmitting these bits and alternates between NEXT and SIGNAL states until all bits are transmitted upon which the PCM_CODE interrupt is set again.

This sequence continues until all the bits are transmitted and the Node Processor writes PC_JOIN in the PLC_CNTRL_B register. The PCM then leaves the NEXT state and enters the JOIN state. Setting these bits has no effect when the PCM is not in the NEXT state or when the PCM_SIGNALING bit is set. However, if this bit is set even though LCT is not finished yet, then LCT will be aborted and the PCM join sequence will be initiated.

Noise Detection Mechanism

The TNE Timer in the PCM times the period between the receptions of the Idle Line State. This timer is loaded with the NS_MAX parameter when Line State Machine leaves the Idle Line State. The TNE Timer keeps counting the Noise until Idle Line State is again detected. While in the ACTIVE state if this timer expires then the PCM will break the link and transition to the BREAK state. In the ACTIVE state the TNE Timer starts counting noise only after LSF is set. If PC_Trace is set and the TNE Timer expires in the same cycle then the transition to the TRACE state is taken. This timer is ignored in all the PCM states except the ACTIVE state.

Noise in MAINT State

If the NOISE_TIMER bit in the PLC_CNTRL_A register is not set, then the Node Processor can write the TNE Timer if the PCM is in MAINT state. If the NOISE_TIMER bit is set, then the TNE Timer is used in the MAINT state to time the Noise as described above. If the TNE Timer expires, then the TNE_EXPIRED bit in the INTR_EVENT register is set.

Operation in TRACE State

In the ACTIVE state if Trace Propagation (i.e., receipt of Master Line State) is detected then the TRACE_PROP interrupt is set. In the ACTIVE state if PC_Trace is received and a transition is made to the TRACE state then the station remains inserted, Master Line State is sourced on the TDAT(4–0) port, and no scrubbing is performed. Again in this state if Master Line State is detected, the TRACE_PROP interrupt is set. If Quiet Line State or Halt Line State is detected, then the SELF_TEST interrupt is set.

Table 13. PCM State Description

State	Description
PC0(OFF)	The PCM enters the OFF state whenever the $\overline{RST}$ pin is asserted or whenever the PCM_CNTRL field of the PLC_CNTRL_B register is set to 11 (PC_Stop). The PCM stays in this state until PC_Start is issued or the PC_MAINT bit is set.
PC1(BREAK)	This is the entry point in the start of a PCM connection. The PCM enters this state when PC_Start is issued, or while it is in the process of forming a connection when any of various error conditions occur (such as receipt of Quiet Line State, a timeout, etc.).
PC2(TRACE)	The TRACE state is issued to localize a stuck Beacon condition. It is entered when PC_Trace is issued while the PCM is in the ACTIVE state.
PC3(CONNECT)	This state is used to synchronize the ends of the connection for the signaling sequence. It is entered from the BREAK state.
PC4(NEXT)	This state is used to separate the signaling performed in the SIGNAL state and to perform the Link Confidence Test. It is entered from the CONNECT state or SIGNAL state.
PC5(SIGNAL)	In this state individual bits of information are communicated across the connection by transmitting either Halt symbols or alternating Halt and Quiet symbols (Master Line State). The PCM transmits and receives bits of information at the same time. This state is entered from the NEXT state.
PC6(JOIN)	This state is the first of three states that leads to an active connection. It is entered from the NEXT state.
PC7(VERIFY)	This state is the second state in the path to the ACTIVE state. It will not be reached by a connection that is not synchronized.
PC8(ACTIVE)	The ACTIVE state is the state where the PHY has been incorporated into the ring. It is entered from the VERIFY state.
PC9(MAINT)	This state is used to override the normal PCM operation for test purposes or so that the PCM operation may be done completely in software. In this state the data path configuration and the transmit data stream are controlled by the Node Processor.

PCI Operation

The PCI State Machine works in conjunction with the PCM state machine to control the data paths of the PLC-S on the MAC side (the RX 9–0 and TX 9–0 paths).

There are three primary functions of the PCI state machine:

- Provide a bypass path between TX 9–0 and RX 9–0
- Provide a scrubbing function upon the insertion and removal of a station from the ring
- Provide a direct path between the PDT/PDR and the MAC

The operation of the PCI state machine depends on whether the CLASS_S bit in the PLC_CNTRL_B register is set and whether the PCM state machine is in the MAINT state.

PCI Operation for Non-Class S Type Station

After a reset the PCI state machine will be in the REMOVED state. If the station is not of type Class S, then the PLC-S will be in the bypass mode where the data input on TX 9–0 is directly output on RX 9–0.

When the PCM state machine enters the ACTIVE state and asserts the SC_JOIN Flag, the PCI state machine enters the INSERT_SCRUB state and Idle symbol pairs are sourced on RX 9–0. At the same time, the PCM state machine causes Idle symbols to be output on TDAT 4–0.

The PCI state machine remains in the INSERT_SCRUB state for T_SCRUB length of time, after which it enters the INSERTED state. Upon entering the INSERTED state, the PCM_ENABLED interrupt is asserted. In this state, a direct path exists from TX 9–0 to TDAT 4–0.

If for some reason the connection is broken and the PCI state machine enters the REMOVE_SCRUB state, Idle symbol pairs are sourced on RX 9–0. Because the PCM state machine is in the BREAK state, Quiet symbols are sourced on TDAT 4–0. While scrubbing is being performed, the PCM state machine will not re–start the connection process. The PCI state machine remains in the REMOVE_SCRUB state for T_SCRUB length of time and then enters the REMOVED state.

Note that if the connection is broken while the PCI state machine is in the INSERT_SCRUB state, scrubbing will

continue for T_SCRUB length of time and then enter the REMOVED state.

PCI Operation for Class S Type Station

For a Class S type station, the PCI Operation is same as above with one exception. Normally, for a Non-Class S type station, PCI will be in REMOVED state at reset, but for a Class S type station, PCI will be in the INSERTED state. Thus, before entering INSERT_SCRUB or after leaving REMOVE_SCRUB, rather than putting the PLC-S in the bypass mode, PHY_INVALID is output on RX 9–0.

PCI Operation in MAINT State

When the PCM state machine is in the MAINT state, the PCI state machine does not control the above functions. In this state all the data paths are under the control of software. Software controls the data paths via several control bits in the PLC_CNTRL_A register. Software can also override the PCI functions when the PCM state machine is not in the MAINT state by setting the CONFIG_CNTRL bit in the PLC_CNTRL_B register.

PCI State Machine

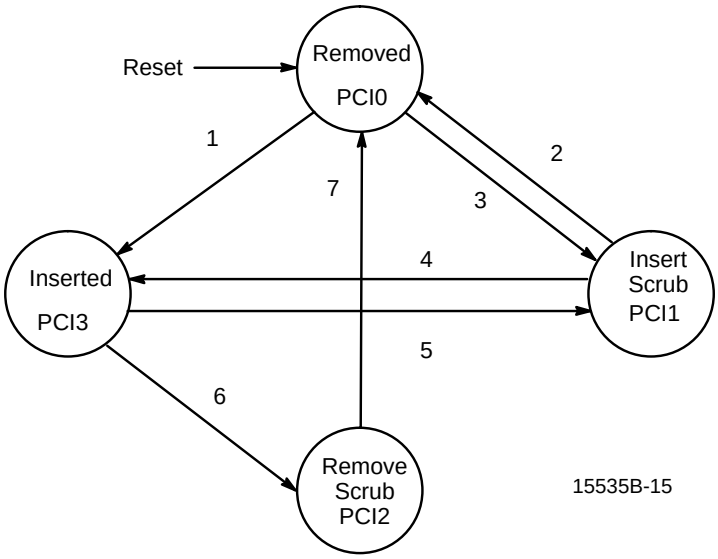
The function of the PCI State Machine is described in Table 14 and Figure 3.

Table 14. PCI State Description

State	Description
PCI0 (REMOVED)	In this state the PCI causes PLC-S to be bypassed. A transition is made to INSERT_SCRUB when SET_SC_JOIN signal is asserted. A transition is made to INSERTED if CLASS_S or PCM_MAINT is set.
PCI1 (INSERT SCRUB)	In this state scrubbing is performed. A transition is made to INSERTED after T_SCRUB length of time.
PCI2 (REMOVE SCRUB)	In this state scrubbing is performed. A transition is made to REMOVED (or to INSERTED if CLASS_S is set) after T_SCRUB length of time.
PCI3 (INSERTED)	In this state scrubbing has completed and the data paths exists between the PDT/PDR and the MAC. A transition is made to the REMOVE_SCRUB state if the START_SCRUBBING signal is asserted. A transition is made to the INSERT_SCRUB state if the SET_SC_JOIN signal is asserted (will only occur if CLASS_S is set).

Note:

User cannot disable PCI.



Notes:

1. *Class = S or PCM_MAINT*
2. *Not (SC_ JOIN and not START_SCRUBBING)*
3. *SET_SC_ JOIN*
4. *TPC > T_SCRUB and (SC_JOIN and not START_SCRUBBING)*
5. *SET_SC_ JOIN*
6. *Not SET_SC_JOIN and START_SCRUBBING*
7. *TPC > T_SCRUB*

Signals on PCI State Machine:

SC_JOIN:

This signal is output by the PCM state machine and indicates that is has reached the ACTIVE state and scrubbing may be started.

SET_SC_JOIN:

This signal is output by the PCM state machine and is asserted during the clock cycle before SC_JOIN is asserted.

CLASS_S:

This bit in the PLC_CNTRL_B register, when set, indicates that the station is of type CLASS_S.

START_SCRUBBING:

This signal is asserted by the PCM state machine when the station has joined the ring (SC_JOIN is asserted) and a Break condition occurs. It causes the PCI state machine to enter the REMOVE_SCRUB state.

PCM_MAINT:

This signal indicates that the PCM state machine is in the MAINT state.

Figure 3. PCI State Machine

Decoder

The Decoder performs the 4B/5B decoding of received data symbols. The five bits of data from the Elasticity Buffer are decoded into four bits of data and one control bit, with the high order bit being the control bit. The decoded symbol pairs are then sent to the MAC. Although the Decoder operates on symbol pairs, each symbol is decoded independently of the other.

Until the PCM has completed establishing a connection for the physical link, the PHY_INVALID symbol is output by the Decoder. Whether the output of the decoder or the data on TX 9–0 is output on RX 9–0 is dependent on the CLASS_S bit in the PLC_CNTRL_B register. In addition, a Violation symbol (V) shall be generated when an input error condition has been detected, such as an Elasticity Buffer error (buffer overflow or underflow). PHY_INVALID takes precedence over Violation, so if an Elasticity Buffer error occurs while the Current Line State is Quiet, Halt, Master, or Noise then PHY_INVALID (1F in hex) is given to MAC.

The symbol decoding is shown in Table 15.

Table 15. 4B/5B Decoding of Data

Symbol	Encoded Input	Decoded Output
Q	00000	1 0000
I	11111	1 0111
H	00100	1 0100
J	11000	1 1100
K	10001	1 0011
T	01101	1 1101
R	00111	1 0001
S	11001	1 1001
H	00001	1 0100
H	00010	1 0100
V	00011	1 1000
V	00101	1 1000
V	00110	1 1000
H	01000	1 0100
V	01100	1 1000
H	10000	1 0100
0	11110	0 0000
1	01001	0 0001
2	10100	0 0010
3	10101	0 0011
4	01010	0 0100
5	01011	0 0101
6	01110	0 0110
7	01111	0 0111
8	10010	0 1000
9	10011	0 1001
A	10110	0 1010
B	10111	0 1011
C	11010	0 1100
D	11011	0 1101
E	11100	0 1110
F	11101	0 1111

Table 16. 4B/5B Encoding of Data

Symbol	Data Input	Encoded Output
Q	1 0000	00000
I	1 0111	11111
H	1 0100	00100
J	1 1100	11000
K	1 0011	10001
T	1 1101	01101
R	1 0001	00111
S	1 1001	11001
INV	1 1110	11111
INV	1 0010	11111
INV	1 0101	11111
INV	1 0110	11111
INV	1 1111	11111
INV	1 1000	11111
INV	1 1010	11111
INV	1 1011	11111
0	0 0000	11110
1	0 0001	01001
2	0 0010	10100
3	0 0011	10101
4	0 0100	01010
5	0 0101	01011
6	0 0110	01110
7	0 0111	01111
8	0 1000	10010
9	0 1001	10011
A	0 1010	10110
B	0 1011	10111
C	0 1100	11010
D	0 1101	11011
E	0 1110	11100
F	0 1111	11101

Encoder

The Encoder performs the 4B/5B encoding of data symbols to be transmitted over the physical medium. The four bits of data and one control bit from the MAC are encoded into a unique five bit symbol which is sent to the PDT. Although the Encoder operates on symbol pairs, each symbol is encoded independently of the other.

The symbol encoding is defined in Table 16.

STREAM CIPHER SCRAMBLER

Background

A popular implementation of FDDI is the replacement of fiber with unshielded twisted pair wire (UTP). When a digital signal is transmitted over copper wire it radiates radio frequency (rf) energy. FDDI encoded data has repetitive patterns which result in peaks in the rf spectrum

large enough to keep the system from being approved by regulatory agencies such as the FCC.

The peaks in the radiated signal can be reduced significantly by scrambling the transmitted signal. Scramblers add the output of a random generator to the data signal. The resulting signal has fewer repetitive data patterns. Thus the occurrence and amplitude of peaks in the frequency spectrum, of the transmitted signal, are greatly reduced and the probability of a systems approval by regulatory agencies, such as the FCC, is increased.

The scrambled data is descrambled, at the receiver, by adding it to the output of another random generator. The receiver's random generator has the same function as the transmitter's random generator. Because the random generators are the same and anything exclusive-ORed with itself is zero, the output of the descrambler is the original data signal.

Data ⊕ A = S_Data S_Data ⊕ B = D_Data

A = B Therefore

A ⊕ B = 0 and

Data ⊕ A ⊕ B = D_Data = Data

where Data = Original Data

S_Data = Scrambled Data

D_Data = Unscrambled Data

A = Transmitter Random Generator

B = Receiver Descrambler

⊕ = Exclusive-OR Function

For proper operation, the random generator in the descrambler must be synchronized to the random generator in the scrambler, i.e., the random generators must be in the same state with respect to the data. Because the random generators operate independently of each other, they require synchronizing circuitry.

The descrambler synchronizes itself to the scrambler by utilizing the following relationship.

H[n] = S_Data[n] ⊕ S_Data[n-j] ⊕ S_Data[n-i] = Data[n]

where H[n] = a hypothesis bit

j and i are bit delays

This relationship is true when Data[n-J] = Data[n-K]. The requirements for a correct H(n) are approximated during the FDDI line states ILS, QLS, HLS and MLS. When a line state is detected, the corresponding correct data can be deduced. The proper setting for the random generator can be derived from Data and S_Data.

If A ⊕ Data = S_Data then Data ⊕ S_Data = A

The X3T9 committee has chosen $X^{11} + X^9$ as the random generator function. This can be represented as a shift register with the eleventh and ninth bits fed back to the input of the first bit via an exclusive OR gate (Figure 4). For this polynomial, j equals eleven and i equals nine. Table 17 shows the line state bits and the corresponding H bits.

Table 17. Line States

Line State	Data	H
QLS	00000000000	00000000000
ILS	11111111111	11111111111
HLS	00100001000	01110011100
MLS	00100000000	01110000000

The following rules apply to the descrambler. When a line state is not detected, the input to the random generator is bit 11 exclusive-ORed with bit 9. Data is S_Data exclusive-ORed with the random generator output. When a line state is detected, Data is derived from H in accordance with Table 17. The input to the random generator is Data exclusive ORed with S_Data.

Scrambler

A functional diagram of the scrambler is shown in Figure 4. It combines the output of a random generator ($X^{11} + X^9$) with FDDI-encoded data via an XOR gate.

Descrambler

The descrambler (Figure 5) combines the output of a random generator with the scrambled data to produce an exact copy of the original unscrambled data. The random generator has the same function as the random generator in the scrambler ($X^{11} + X^9$).

The descrambler has a state-synchronizer to set the descrambler-random generator to the same state as the scrambler-random generator. The state-synchronizer is enabled by SCRM_RSYNC, which is from the PLC-S decoder. When SCRM_RSYNC is true, the decoder has not detected a valid FDDI signal. The state-synchronizer attempts to set the random generator. If SCRM_RSYNC is false, the data is valid and the random generator is assumed to be synchronized to the scrambler and will remain synchronized.

The state-synchronizer monitors the scrambled data for one of the patterns in Table 17. When there is a match, the output data is set to the corresponding value. The random generator's input is the deduced output XORed with the scrambled data input, which corresponds to the scrambler's random generator. When there is not a match, the output data is the scrambled data XORed with the random generator's output. The random generator is open loop.

Using the Stream Cipher Scrambler

The system has access to the scrambler and descrambler through a pin and a register. Pin 41 (SCRM) and bit 0 (CIPHER_ENABLE) of PLC_CNTRL_C enable the scrambler. SCRM and CIPHER_ENABLE are ORed together so either one HIGH overrides the other (Table 18). Pin 41 is a ground pin on previous versions of the PLC; therefore if the PLC-S is to be used in the fiber mode, it can be inserted in a previously manufactured board without any changes.

Table 18. Stream Cipher Enable

SCRM	Cipher Enable	Scrambler
LOW	LOW	Disabled
LOW	HIGH	Enabled
HIGH	LOW	Enabled
HIGH	HIGH	Enabled

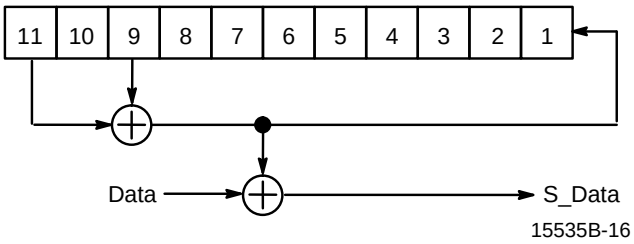


Figure 4. Stream Cipher Scrambler

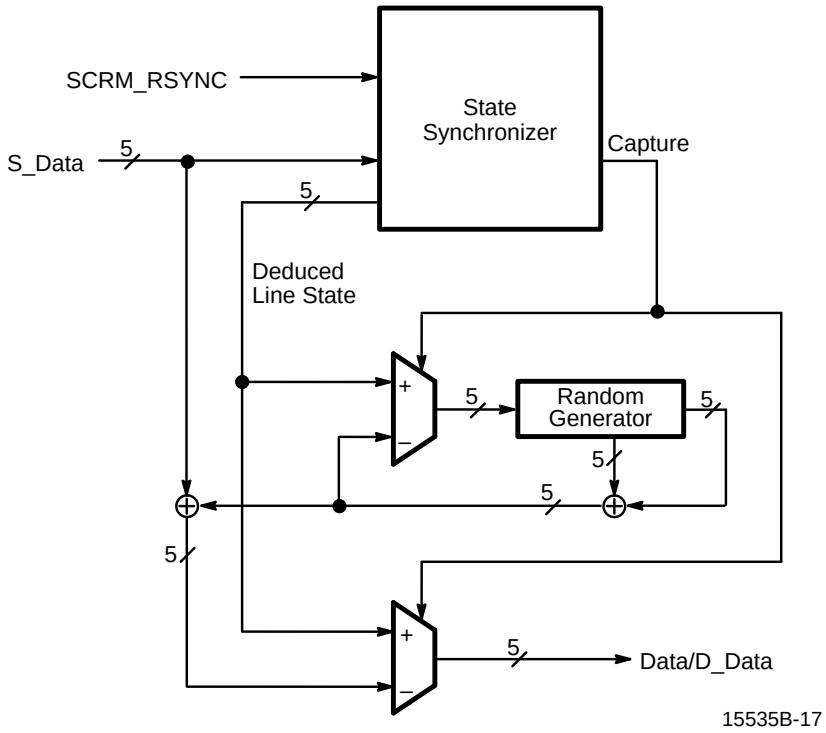


Figure 5. Stream Cipher Descrambler

Repeat Filter

The main function of the Repeat Filter is to prevent the propagation of code violations and invalid line states from the inbound link to the outbound link. This function is not required if a MAC layer is present in the station configuration (since MAC will not propagate invalid line states and code violations). But certain station configurations consist of only PHY layer entities (such as the path of the secondary ring inside a station with just one MAC in the primary ring). In such cases, a PHY layer implementation is expected to provide the Repeat Filter function.

The Repeat Filter in the PLC-S filters the symbol stream at the output of the Remote Loopback MUX. Invalid line states are not allowed to propagate through a station; they will be turned into an Idle symbol stream. Also, if the repeat filter detects a corrupted frame, it truncates the frame by transmitting four Halt symbols and then Idle symbols until a JK symbol pair is seen. The Halt symbols will cause the next MAC entity in the logical ring to count the frame as a lost frame.

Another function of the Repeat Filter is called the GOBBLE_BYTE function. When the Repeat Filter

detects a fragment, i.e., a frame in which Idle symbols appears before the ending delimiter, then it changes the previous symbol pair to Idles. After passing through Repeat Filters in other stations, the fragment will eventually be completely converted to Idles.

The PLC-S includes the symbol pair wide implementation of the Repeat Filter as defined in the FDDI PHY document.

Data Stream Generator

The Data Stream Generator block uses a multiplexer for the purpose of generating a symbol pair at the request of the PCM via an internal signal bus LS_REQ (or external through control when the PCM is in the MAINT state by using the MAINT_LS bits in the PLC_CNTRL_B register), the Repeat Filter via an internal signal RF-CNTRL (1_0), or transmitting the symbol pair from TX 9–0. The DATA_STRM(9–0) is an internal bus that comes from the Data Stream Generator to the encoder block.

The Data Stream Generator also latches the data each BCLK cycle. This is done for the GOBBLE_BYTE function of the Repeat Filter (see above) which requires that the data be delayed for one clock cycle.

Data Path Muxes

The Receive Data Path and Transmit Data Path of the PLC-S include six multiplexers (MUXes) for the purpose of altering the normal flow of data through the chip (see chip block diagram). Reasons for altering the data paths are for physical connection insertion and removal and for testing and diagnostics. All receive and transmit data paths internal to the PLC-S are ten bits (two symbols) wide.

EB Local Loopback Mux

In normal operating mode, the EB Local Loopback MUX puts the data held in the Receive Data Input latch to the input of Framer.

When the EB_LOC_LOOP bit in the PLC_CNTRL_A register is set or when the built-in self test is running, the MUX loops back the data in the Transmit Data Output latch onto the receive data path just after the Receive Data Input latch (i.e., to the input of Framer). This creates a path whereby data from a MAC device can traverse the entire transmit and receive data paths of the PLC-SS (excluding the scrambler and the descrambler) and be returned to the MAC device. The built-in self test uses this loopback along with the Remote Loopback to create a loop which covers all of the transmit data path and receive data path.

Cipher Loopback MUX

In normal operating mode, the Cipher Lookback MUX puts the data from PDR to the input of the descrambler block of PLC-SS and the data from the scrambler block of PLC-SS to PDT.

When the CIPHER_LPBCK bit in the PLC_CNTRL_C register is set, the MUX loops back the output of the descrambler to the input of the scrambler. This creates a path whereby data from a MAC device can traverse the entire transmit and receive data paths of the PLC-SS (including the scrambler and the descrambler) and be returned to the MAC device.

LM Local Loopback MUX

In normal operating mode, the LM Local Loopback MUX puts the output of Elasticity buffer/smoother block to the input of Decoder block.

When the LM_LOC_LOOP bit in the PLC_CNTRL_A register is set or when the built-in self test is running, the MUX loops back the data in the Transmit Data Output latch onto the receive data path just after the Elasticity buffer. This differs from the EB_LOC_LOOP in that the Framer and Elasticity Buffer are bypassed.

Bypass MUX

In normal operating mode, the Bypass MUX sends the data output by the Decoder to the Receive Data Output latch.

When the SC_BYPASS bit in the PLC_CNTRL_A register is set while the PCM is in the MAINT state, or when the CONFIG_CNTRL bit is set in the PLC_CNTRL_B register, or when the PCI is in the REMOVED, INSERT_SCRUB, or REMOVE_SCRUB state, the output of the BYPASS MUX is put to the Transmit Data Input Latch onto the receive data path. On reset this BYPASS_MUX will be in effect and will put the Transmit Data Input Latch onto the receive data path.

Remote Loopback MUX

In normal operating mode, the Remote Loopback MUX puts the data held in the Transmit Data Input latch onto the transmit data path of the PLC-SS.

When the SC_REM_LOOP bit is set (and EB_LOC_LOOP, LM_LOC_LOOP and CIPHER_LPBCK bits are not set) or when the BIST is running, this MUX loops back the data from the Decoder onto the transmit data path and is latched at this point. This creates a path whereby data from the PDR can traverse the entire receive and transmit data paths of the PLC-S and be transmitted by PDT. BIST uses this loopback along with the Local Loopback to create a loop which also covers all of the receive data path and the transmit data path.

Scrub MUX

The Scrub MUX selects its input from either constant Idle symbol pairs or the output of the BYPASS_MUX.

When the REQ_SCRUB bit in the PLC_CNTRL_A register is set while the PCM is in the MAINT state, or when CONFIG_CNTRL bits is set in the PLC_CNTRL_B

register, the PCI is in the INSERT_SCRUB or REMOVE_SCRUB state, the output of the Scrub MUX is Idle symbols. Otherwise transmit data from the BYPASS_MUX is placed on the Receive Data Output Latch.

This MUX is used when the PLC-S operates in a Concentrator. When a port in a Concentrator is connecting to an end station, Idle symbols are output on RX 9–0 so as to scrub the ring before the station starts putting data onto the ring. When a port in a Concentrator is not connected to another station, the port is bypassed by routing TX back out on RX.

Test Data MUX

In normal operating mode the Test Data MUX sends the data output by the Encoder to the Transmit Data Output Latch.

When the built-in self test is running the Test Data MUX selects the input from the BIST block. This is how BIST inserts pseudo-random test data into the loop it forms with the transmit and receive data paths. This point was chosen to inject test data because it was desired to avoid sending the test data through the Repeat Filter and the Data Stream Generator. Since both of these logic blocks act as filters, coverage of stuck-at faults in other parts of the chip would be reduced if data from these blocks rather than random test data were used.

Data Input/Output

The PLC-S contains four ports for receiving and transmitting network data: Receive Data Input, Receive Data Output, Transmit Data Input, and Transmit Data Output. The signal timing for these ports is detailed in the Switching Characteristics and Switching Waveforms chapters of this document.

Receive Data Input

RDAT is a five-bit (symbol wide) data bus going from the PDR chip to the PLC-S. RSCLK is also input from the PDR chip and is divided by two to get a recovered byte clock. RDAT is latched on each rising and falling edge of the recovered byte clock. Following the rising edge of the recovered byte clock, the five bits (symbol) just latched, plus the five bits (symbol) latched by the previous falling edge recovered byte clock edge, are used internally in the PLC-S. All data paths inside the PLC-S are 10 bits (two symbols) wide.

Receive Data Output

RX is a ten-bit (symbol pair wide) data bus going from the PLC-S to the a MAC device in a Single Attachment Station (SAS). In the case of a Concentrator or a Dual Attachment Station (DAS), RX may also go to another PLC-S. Data is latched inside the PLC-S on each rising edge of BCLK and is available to the MAC device shortly after this clock edge.

Transmit Data Input

TX is a ten-bit (symbol pair wide) data bus going from the MAC device (or in a Concentrator/DAS, from another PLC to the PLC-S. The data is latched by the falling edge of LSCLK that precedes the rising edge of BCLK. Then it is latched again by that rising edge of BCLK. Assuming no skew between LSCLK and BCLK, this effectively adds a one half LSCLK period to the hold time provided on TX. Any amount by which BCLK trails LSCLK will subtract from the hold time provided.

Transmit Data Output

TDAT is a five-bit (symbol wide) data bus going from the PLC-S to the PDT. The ten bit wide internal data bus is latched initially by the PLC-S by each rising edge of BCLK. Bits nine through five are sent on the rising edge of LSCLK following the rising edge of BCLK. Bits four through zero are then sent on the rising edge of LSCLK following the falling edge of BCLK. Data are available to the PDT shortly after each rising edge of LSCLK.

Built In Self Test (BIST)

The Built In Self Test block contains logic to run the PLC-S Built In Self Test and also contains control logic for the chip's Counter Segmentation Test Mode and Boundary Scan Test Mode.

BIST Operation

The bulk of the PLC-S data path and state machine logic is tested by BIST. It remains passive during normal chip operation. Under test mode, BIST tests the chip, and returns a signature which verifies the functioning of the chip's logic with a high degree of certainty. Since BIST sits right on the silicon with the rest of the chip, it has the advantage of the optimum observability location: inside the chip.

BIST tests the PLC-S by circulating pseudo random data throughout the chip. The various subcircuits within the chip are observed as they respond to these data, and a signature based upon their behavior is generated. This signature may be checked against the known correct signature, to verify the functioning of the chip. A single fault in the chip, as long as it is covered by BIST, will cause a different signature to be generated.

The majority of the logic blocks of the PLC-S sit directly on the chip's data path. These blocks are easily tested by placing pseudo random vectors, generated by the Linear Feedback Shift Register (LSFR), on the data paths, and observing the behavior of the blocks with the Signature Generator.

With this method, data from LFSR are input by the Transmit Data Output latch lines via the Test Data Mux (see Block Diagram on page 2). The test data are looped back onto the receive data path via the EB Local Loopback MUX. The test data traverse the entire receive data

path and are fed back to the Signature Generator. The test data are input to the transmit data path via the Remote Loopback MUX. The test data are fed back to the Signature Generator before the transmit data path because the Repeat Filter, Data Stream Generator, and Encoder act as filters which would reduce the fault coverage provided by the test data. Fault coverage is obtained for the Repeat Filter, Data Stream Generator, and Encoder by separate signals fed to the Signature Generator.

The state machines, while somewhat attached to the data path, are more control oriented, and are not likely to respond well to random vectors on the data paths. The LEM, LSM, PCM, PCI, and RF state machines are tested using scan logic. Under test mode, the state registers of the state machines, and their control bits in the registers of the NPI are linked together to form a scan chain. The output of the scan chain drives a bit in the Signature Generator.

BIST is activated with the assertion of the RUN-BIST bit in the PLC_CNTRL_A register. Upon activation, the data path, LFSR, and Signature Generator are initialized, and the latches in the scan chain are placed in scan mode. After initialization, the LFSR and Signature Generator are enabled, and the test proceeds.

When BIST has completed, the signature is frozen, and may be read through the Node Processor Interface. End of test occurs when a value of zero is reached in the LFSR. Using a 16 bit LFSR clocked by the 80 ns BCLK it will take approximately 5.24 ms to circulate 65535 test patterns through the chip. An interrupt to the node processor after RUN_BIST has been asserted, signifies the completion of the PLC-S self test. This interrupt is cleared by clearing the RUN_BIST bit in the PLC_CNTRL_A register (NOT by reading the INTR_EVENT register). BIST is aborted if the RUN_BIST bit is cleared by writing a zero in the RUN_BIST bit in the PLC_CNTRL_A register before BIST completes.

Counter Segmentation Test Mode

The counters (including all timers) in the PLC-S are designed in such a way, that under Counter Segmentation Test Mode, they break apart into several 4 bit counters. For example, in Counter Segmentation Test Mode, a 16-bit counter becomes four 4-bit counters. These 4-bit counters in parallel, allow the counters to be tested in $2^4 = 16$ cycles, as opposed to $2^{16} = 65536$ cycles for a 16-bit counter.

Since counter test requires the ability to control the BCLK, this test is not intended for any board level tests or diagnostics. This is a factory test only.

Boundary Scan Test Mode

In Boundary Scan Test Mode, most of the chip input and output latches are linked together to form a scan chain. While this complements BIST, which does not test these latches, the main purpose of this test mode is for board testing. In this mode the I/O latches of the various chips on the board are linked into a large scan chain. By serially shifting data into the scan chain (Boundary Scan Serial Test Mode), then clocking the data in parallel (Normal or Boundary Scan Parallel Test Mode) and then serially shifting the data out, the I/O latches and interconnections between the various chips can be tested.

The order of pins in the scan chain is shown in Table 19. The pin TEST 0 is the scan chain input and the pin SCANO is the scan chain output. The pins $\overline{\text{RST}}$, LSCLK, BCLK, NPCLK, RSCLK, RRSCLK, EBFERR, $\overline{\text{LPBCK}}$, SCRM, SDO, LSR 2–0, ULSB, ENCOFF, TEST 2–0, PTSTO, NPADDR 4–0, $\overline{\text{INT}}$, $\overline{\text{CS}}$, and NPRW are not included in the scan chain. Note that only the output portion of the NP 15–0 bus is in the scan chain. BCLK is used for clocking.

Table 19. Boundary Scan Chain Order

Pin	Type
RDAT0 to RDAT4	Input to Input
FOTOFF	Output
TDAT4 to TDAT0	Output to Output
TX0 to TX9	Input to Input
TXPAR	Input
RXPAR	Output
RX9 to RX0	Output to Output
NP 15 to NP 0	Output to Output

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C
Ambient Temperature . . . . . 0°C to 70°C
Supply Voltage Referenced to V_{SS} . . –0.3 V to +7 V
DC Voltage applied to any
Pin Referenced to V_{SS} . . . . . –0.5 to V_{DD} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Temperature (T_A) . . . . . 0°C to +70°C
Supply Voltage, V_{DD} . . . . . +5 V +/– 5%

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{DD} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4 mA	2.4		V
I_{OZ}	Output Leakage Current (Note 1)	0.4 V < V_{OUT} < V_{DD}	–10	10	µA
I_{IX}	Input Leakage Current (Note 2)	0 V < V_{IN} < V_{DD}	–10	10	µA

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
I_{DD}	Power Supply Current (Note 3)	V_{CC} = Max f(BCLK, NPCLK) = 12.5 MHz f(LSCLK, RSCLK) = 25 MHz		125	mA

Notes:

1. *I_{OZ} applies to all three-state output pins and bidirectional pins.*
2. *I_{IX} applies to all input-only pins.*
3. *V_{IL} = 0.0 V and V_{IH} = 3.0 V for I_{DD} test.*

CAPACITANCE (See Note 4)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
C_{IN}	Input pins			10	pF
$C_{I/O}$	Bidirectional pins (Note 5)			10	pF

Notes:

4. *Pin capacitance is characterized at a frequency of 1 MHz, but is not 100% tested.*
5. *Bidirectional and output pins are designed to drive a 50 pF capacitive load.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

Parameter Symbol	Parameter Description	Min	Max	Unit
1	BCLK Period	80		ns
2	BCLK Pulse Width Low	38	42	ns
3	BCLK Pulse Width High	38	42	ns
4	NPCLK Period	80		ns
5	NPCLK Pulse Width Low	38	42	ns
6	NPCLK Pulse Width High	38	42	ns
7	LSCLK Period	40		ns
8	LSCLK Pulse Width Low	15		ns
9	LSCLK Pulse Width High	15		ns
10	RSCLK Period	40		ns
11	RSCLK Pulse Width Low	15		ns
12	RSCLK Pulse Width High	10		ns
13	LSCLK to BCLK Skew	2	8	ns
14	$\overline{CS}$ Setup Time	10		ns
15	$\overline{CS}$ Hold Time	10		ns
16	NPRW, NPADDR Setup Time	5		ns
17	NPRW, NPADDR Hold Time	20		ns
18	NP Driven to High Impedence		30	ns
19	NP Driven	2		ns
20	NP Valid		30	ns
21	NP Invalid	2		ns
22	NP Setup Time	30		ns
23	NP Hold Time	20		ns
24	$\overline{INT}$ Asserted		40	ns
25	$\overline{INT}$ Deasserted		40	ns
26	RX, RXPAR Valid		25	ns
27	RX, RXPAR Invalid	3		ns
28	TX, TXPAR Setup Time	10		ns
29	TX, TXPAR Hold Time	5		ns
30	RDAT Setup Time	5		ns
31	RDAT Hold Time	8		ns
32	$\overline{LPRCK}$ $\overline{FOTOFF}$, SCAN0, LSR, ULSB, EBFERR Valid		25	ns
33	$\overline{LRRCK}$, FOTOFF, SCAN0, LSR ULSB, EBFFRR Invalid	2		ns
34	SDO Setup Time	5		ns
35	SDO Hold Time	15		ns
36	TDAT Valid		25	ns
37	TDAT Invalid	3		ns
38	TEST 2-0 Setup Time	15		ns
39	TEST 2-0 Hold Time	15		ns
40	ENCOFF Setup Time	15		ns
41	ENCOFF Hold Time	10		ns
42	$\overline{RST}$ Pulse Width	20 BCLK Periods		ns

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

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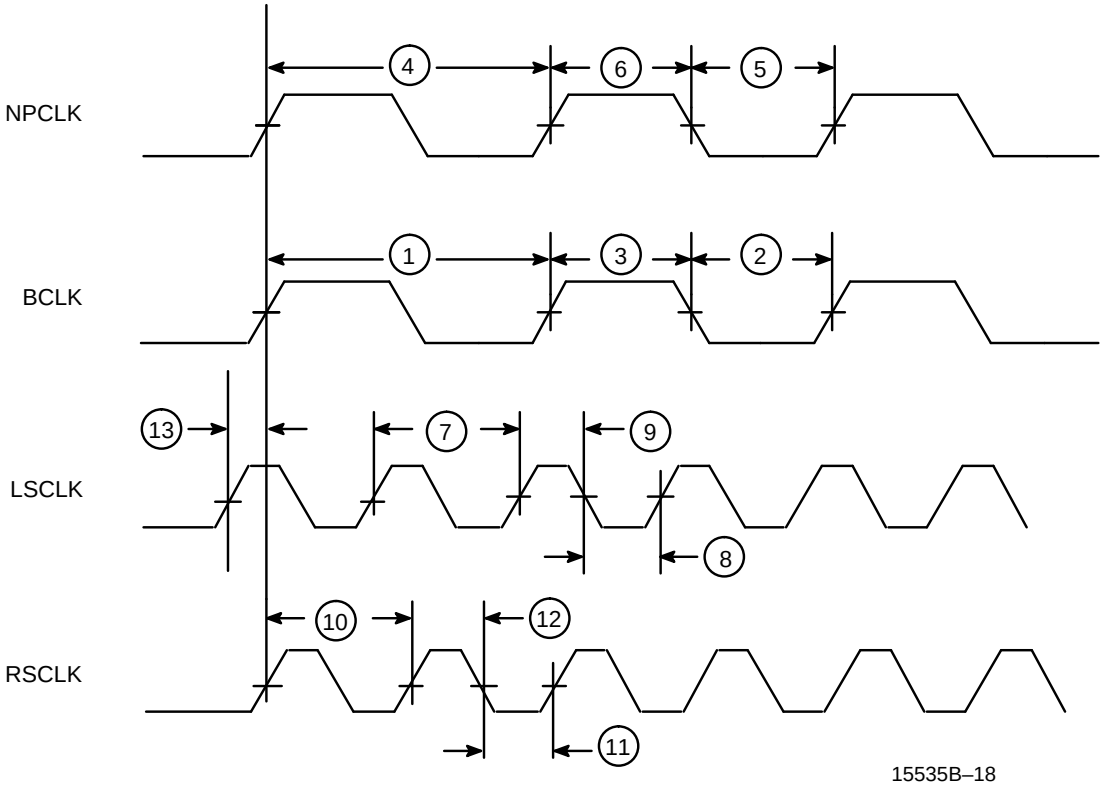
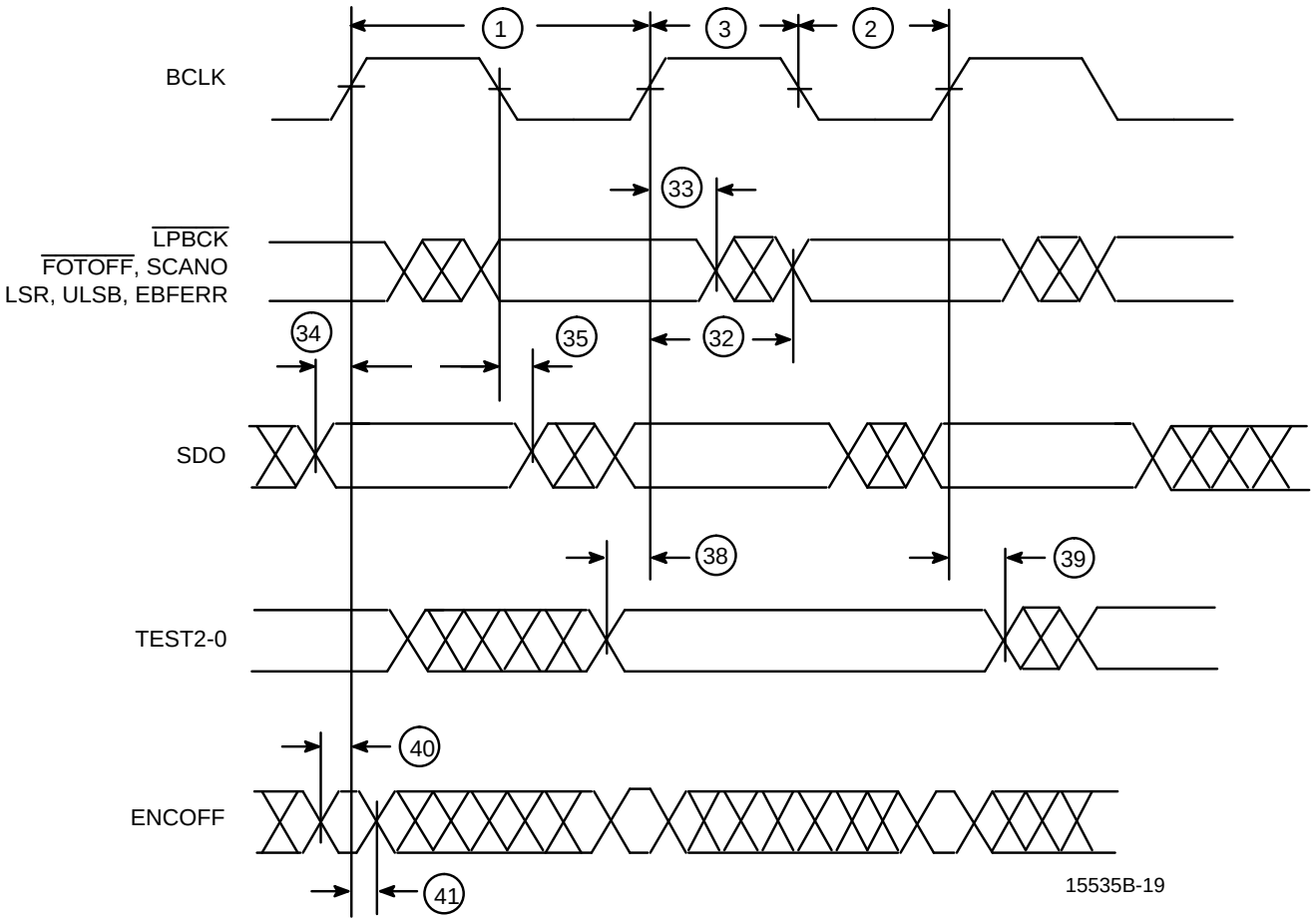
SWITCHING WAVEFORMS



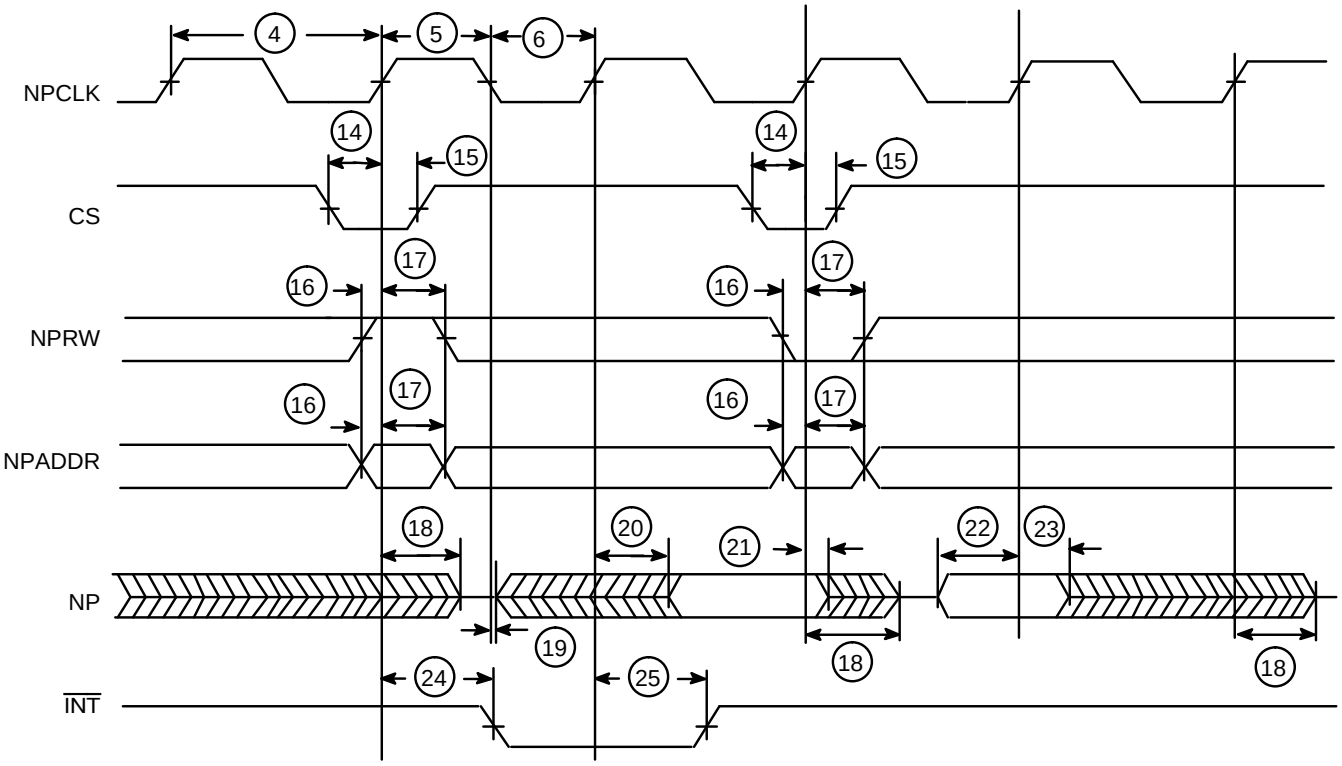
PLC-S Clock Timing Parameters

SWITCHING WAVEFORMS



PLC-S Misc Signals Timing Diagram

SWITCHING WAVEFORMS



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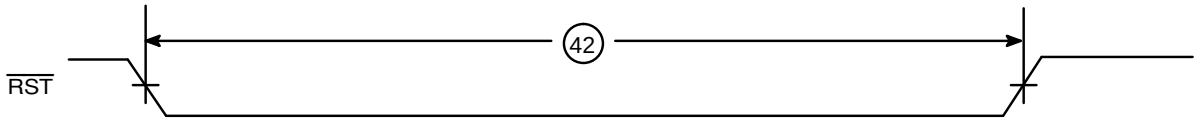
Node Processor Interface Timing Diagram



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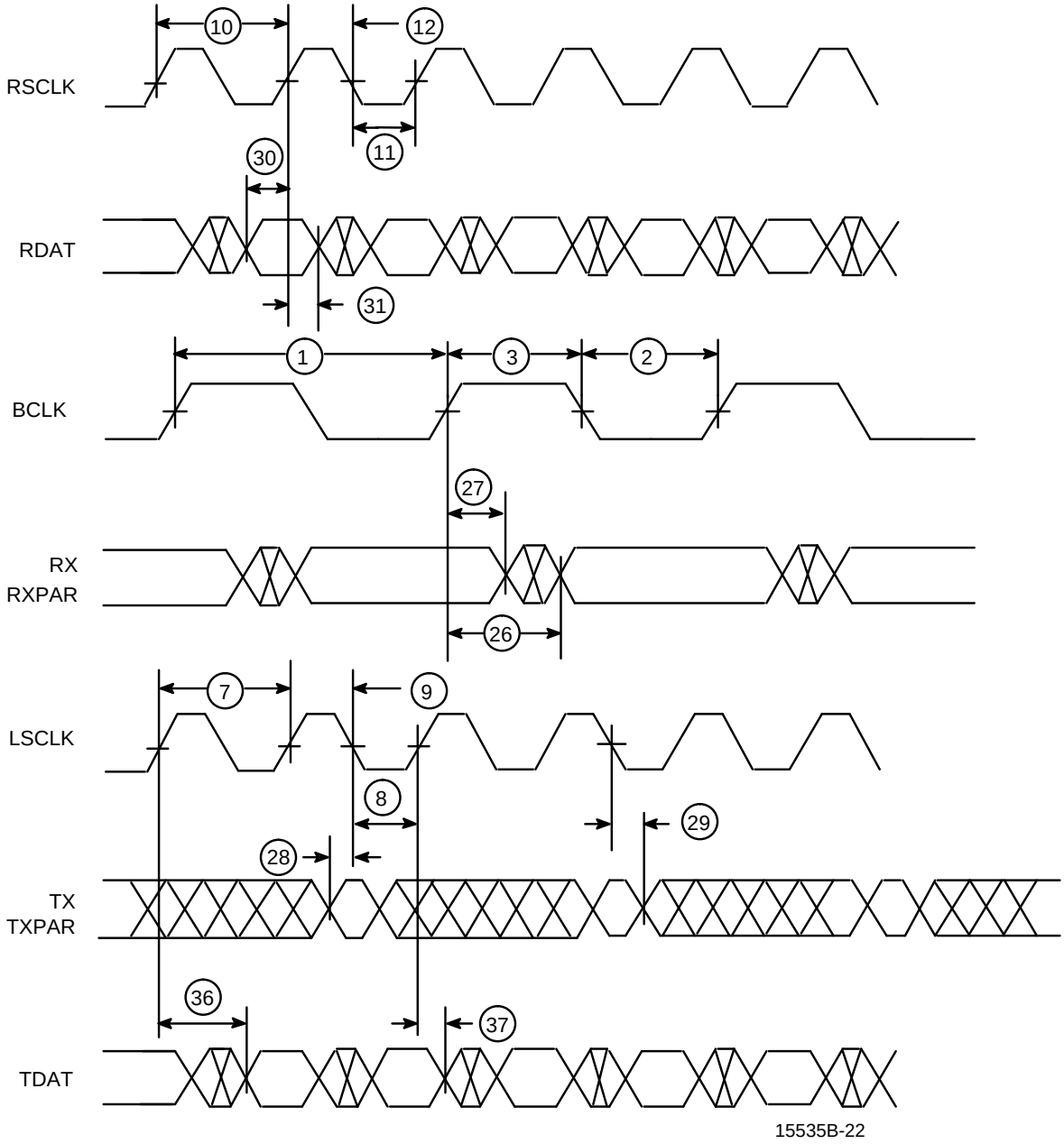
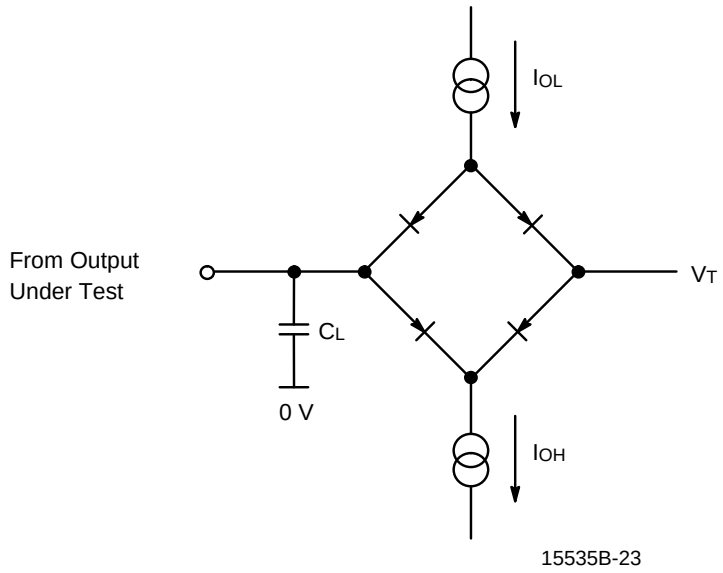
PLC-S Reset Timing Parameters

SWITCHING WAVEFORMS



PLC-S Data Interface Timing Diagram

SWITCHING TEST CIRCUIT

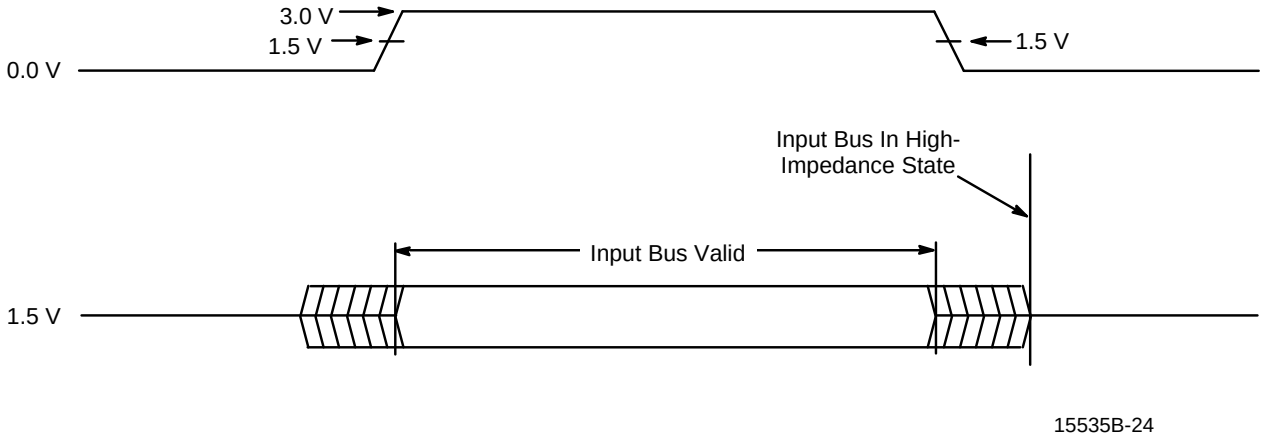


Note:

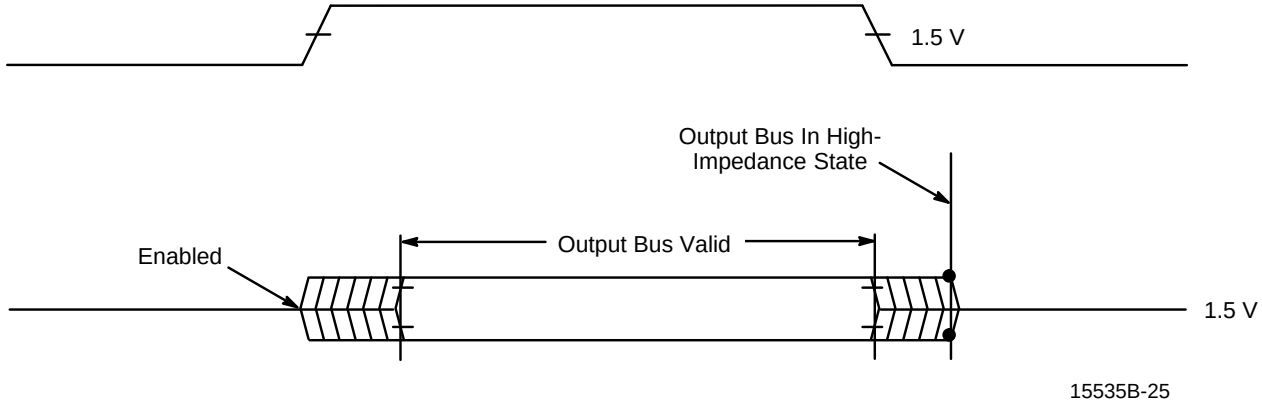
C_L = 50 pF for all bidirectional or output pins.

Standard Test Load

SWITCHING TEST WAVEFORMS



Input Waveform Test Points



Output Waveform Test Points