PRELIMINARY

Am79C850

SUPERNET® 3

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Compliant with the ANSI X3T9.5/ISO 9314 specification**
  - — 100 Mbps data rate
  - — Timed token-passing protocol
  - — Ring topology
- **Complete memory management**
  - — Supports 256K bytes of local frame buffer memory
  - — Supports buffer memory bandwidths of 200 Mbps and 400 Mbps
  - — Tag-Mode: minimum latency/highest performance buffer memory management, ideal for adapter card designs
- **ANSI-compliant TP-PMD Stream Cipher Scrambling/Descrambling**
- **Full duplex operation: 200 Mbps continuous data rate**
- **Supports both fiber optic and copper twisted-pair media**
- **Diagnostic features**
  - — Built in Self Test (BIST) in Address Filter, Physical Layer Controller with Scrambler
- **Hardware Physical Connection Management support**
- **Low power consumption—reduction of more than 25% from SUPERNET 2 solution**

FUNCTIONAL OVERVIEW

SUPERNET 3 is a 208-pin CMOS integration of FDDI MAC, PHY, Address Filter, and clock generation and recovery functions. It is the third generation FDDI offering from AMD which integrates the SUPERNET 2 family of chips into a single-chip solution. **Refer to the SUPERNET 2 data book (PID 15502C) for basic feature descriptions.**

The SUPERNET 3 is backward compatible to the SUPERNET 2 Tag Mode of operation in which the SUPERNET 3 buffer memory interface logic maintains the buffer memory as multiple FIFOs.

The SUPERNET 3 provides DMA channels, arbitrates access to the network buffer memory, and controls the data path between the buffer memory and the medium. The MAC also implements the timed-token protocol and receive/transmit control as specified for the Media Access Control (MAC) sublayer of the ISO standard 9314-2 for FDDI. The Physical Layer functions defined by the ISO 9314-1 are performed by the SUPERNET 3. SUPERNET 3 implements on-chip digital clock recovery and transmit functions for fiber. To support copper media, the PHY-PMD interface is maintained and an external module can be implemented in the same footprint as the fiber optic transceiver to perform the MLT-3 encoding/decoding and equalization. SUPERNET 3 integrates the scrambler and descrambler functions for transmissions over copper media.

SUPERNET 3 FEATURES UPDATE

The basic feature description for SUPERNET 3 is provided in the SUPERNET 2 data book. The enhanced features are as listed below:

- This is a CMOS integration of the redesigned FORMAC Plus, an enhanced PLC, a 32-entry address filter (AF, which is based on a Content Addressable Memory, or CAM, core), and a CMOS PDX core for clock and data recovery.
- A 32-entry, extensible and fully maskable AF allows additional individual and group addresses to be supported.
- The physical data transmitter and receiver (PDX) circuits are also embedded on-chip using proprietary digital clock-recovery technology.
- For the purposes of implementing copper PMD, the scrambler/descrambler functions are embedded within the chip.
- The Buffer Memory interface has been modified to support slower SRAM's (35 ns) without affecting backward compatibility with SUPERNET 2.
- SUPERNET 3 supports the FDDI single attachment station (SAS) but is capable of supporting a dual attachment station (DAS)

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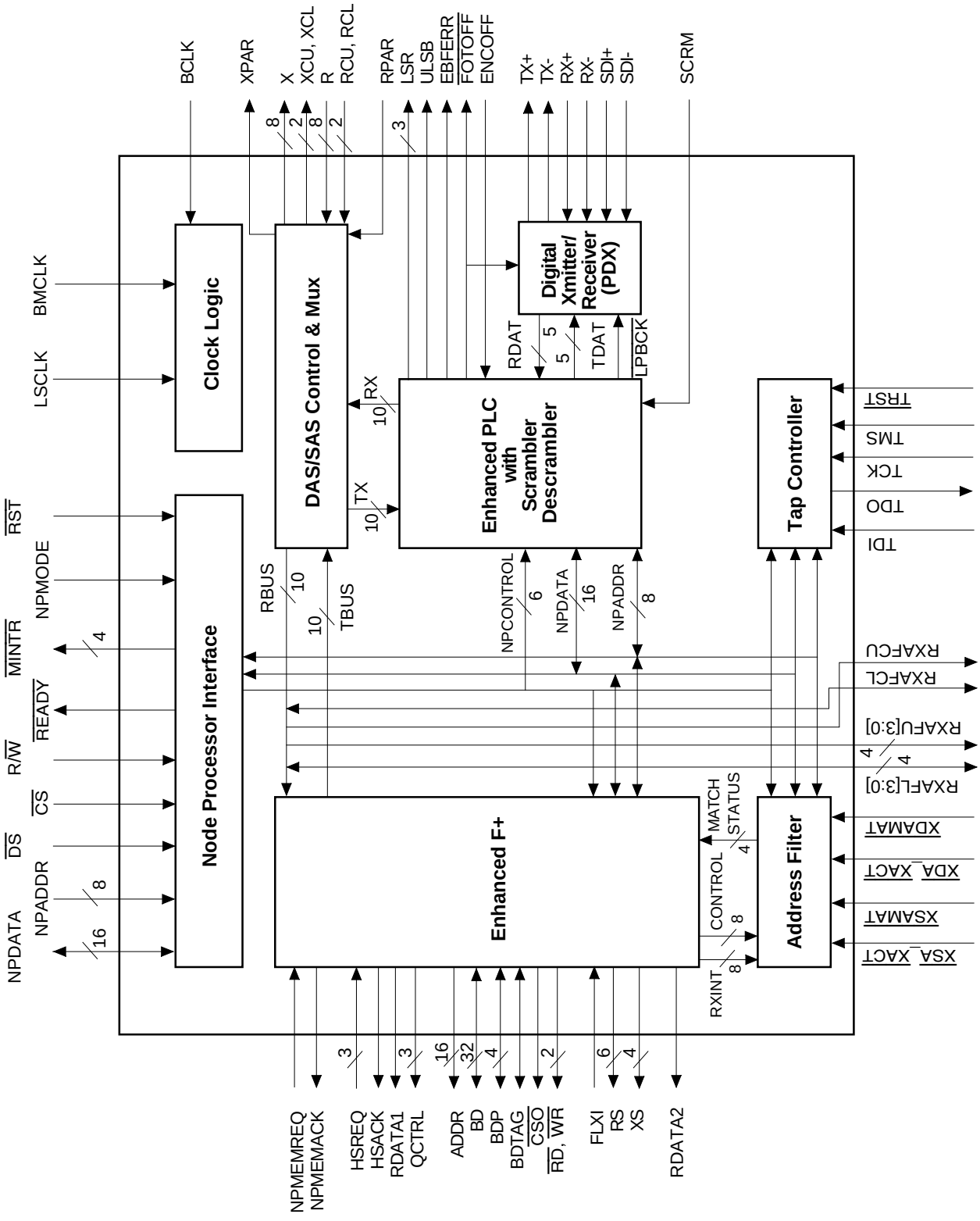
configurations with an external physical layer controller.

- SUPERNET 3 has a Test Access Port and Boundary Scan Architecture, IEEE1149.1.
- SUPERNET 3 provides Built-in Self Test (BIST) features for the Address Filter, and PLC-S.
- All registers are readable and writable by the Node Processor. All reserved bits shall be read back as zero except where noted.
- The Receive Status (RS) pins are expanded from 5 to 6 pins to support enhanced status reporting.
- The Transmit Status (XS) pins are expanded from 3 to 4 pins to support enhanced status reporting.
- Enhanced frame reception is possible by splitting the receive queue.
- Modified TAG Mode of operation for easy conversion from NON-TAG SUPERNET 2 to SUPERNET 3.
- All SUPERNET 3 registers will be initialized with a default value on reset.
- The A, C indicator setting has been modified. It is now possible to control the setting of the A, C indicators independent of the mode of operation (online, online special mode, and external loopback mode).
- Maskable ‘vectored-interrupts’ are provided. It is now possible to detect the event causing the interrupt in the SUPERNET 3 in two cycles by reading the vector register which gives the vector of the status register followed by a read of the appropriate status register.
- An additional mode register (MDREG3) is provided. Setting the bits in this mode register enables the additional SUPERNET 3 features.

BLOCK DIAGRAM



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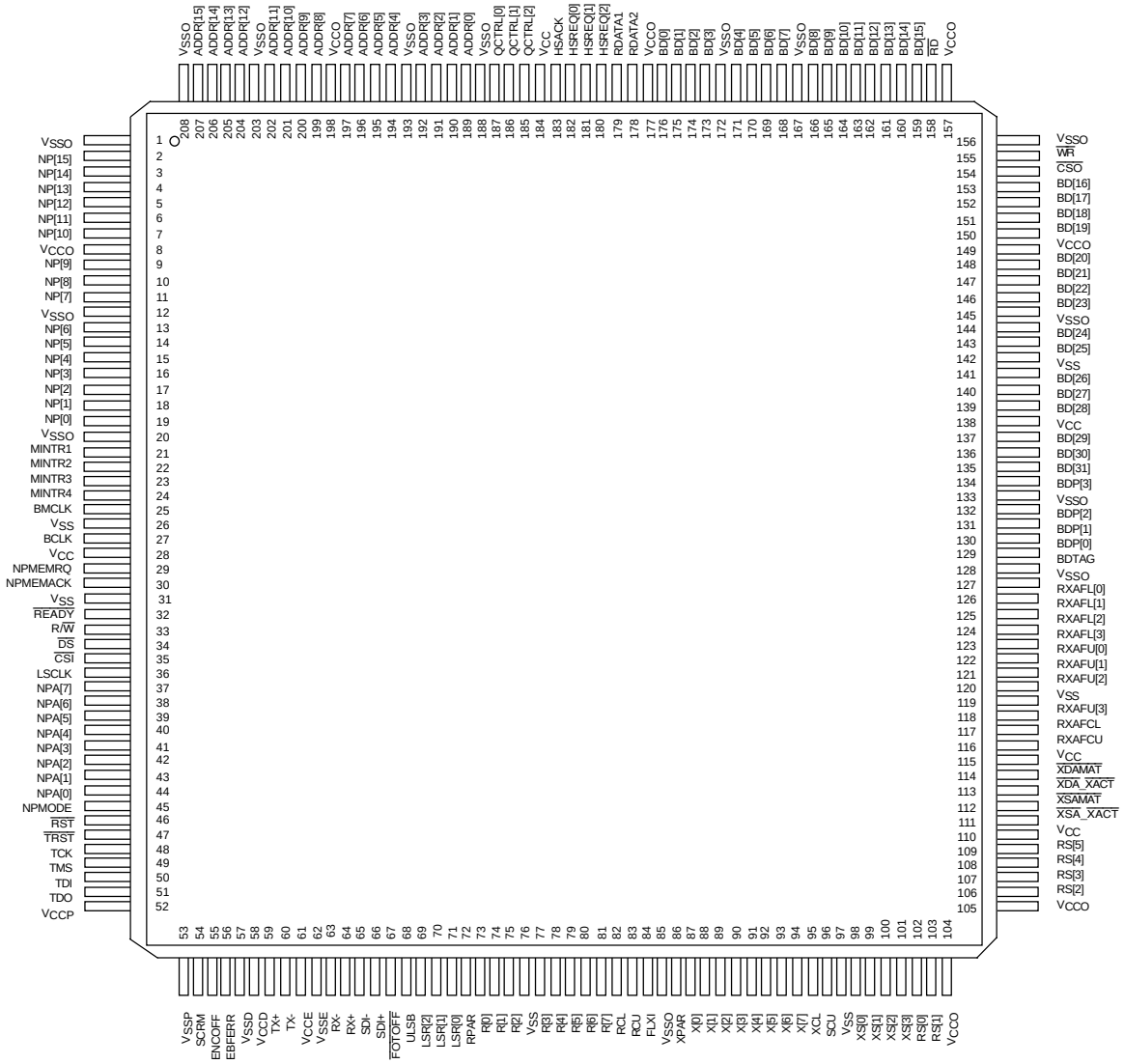
CONNECTION DIAGRAM

208-Pin PQR (Top View)



19574A-1

PQFP PIN DESIGNATIONS
Listed by Pin Number

Pin #	Description	Pin #	Description	Pin #	Description	Pin #	Description
1	VSSO	**35**	$\overline{CSI}$	**69**	LSR[2]	**103**	RS[1]
2	NP[15]	**36**	LSCLK	**70**	LSR[1]	**104**	VCCO
3	NP[14]	**37**	NPA[7]	**71**	LSR[0]	**105**	VCCO
4	NP[13]	**38**	NPA[6]	**72**	RPAR	**106**	RS[2]
5	NP[12]	**39**	NPA[5]	**73**	R[0]	**107**	RS[3]
6	NP[11]	**40**	NPA[4]	**74**	R[1]	**108**	RS[4]
7	NP[10]	**41**	NPA[3]	**75**	R[2]	**109**	RS[5]
8	VCCO	**42**	NPA[2]	**76**	VSS	**110**	VCC
9	NP[9]	**43**	NPA[1]	**77**	R[3]	**111**	$\overline{XSA}\_\overline{XACT}$
10	NP[8]	**44**	NPA[0]	**78**	R[4]	**112**	$\overline{XSAMAT}$
11	NP[7]	**45**	NPMODE	**79**	R[5]	**113**	$\overline{XDA}\_\overline{XACT}$
12	VSSO	**46**	$\overline{RST}$	**80**	R[6]	**114**	$\overline{XDAMAT}$
13	NP[6]	**47**	$\overline{TRST}$	**81**	R[7]	**115**	VCC
14	NP[5]	**48**	TCK	**82**	RCL	**116**	RXAFCU
15	NP[4]	**49**	TMS	**83**	RCU	**117**	RXAFCL
16	NP[3]	**50**	TDI	**84**	FLXI	**118**	RXAFU[3]
17	NP[2]	**51**	TDO	**85**	VSSO	**119**	VSS
18	NP[1]	**52**	VCCP	**86**	XPAR	**120**	RXAFU[2]
19	NP[0]	**53**	VSSP	**87**	X[0]	**121**	RXAFU[1]
20	VSSO	**54**	SCRM	**88**	X[1]	**122**	RXAFU[0]
21	MINTR1	**55**	ENCOFF	**89**	X[2]	**123**	RXAFL[3]
22	MINTR2	**56**	EBFERR	**90**	X[3]	**124**	RXAFL[2]
23	MINTR3	**57**	VSSD	**91**	X[4]	**125**	RXAFL[1]
24	MINTR4	**58**	VCCD	**92**	X[5]	**126**	RXAFL[0]
25	BMCLK	**59**	TX+	**93**	X[6]	**127**	VSSO
26	VSS	**60**	TX–	**94**	X[7]	**128**	BDTAG
27	BCLK	**61**	VCCE	**95**	XCL	**129**	BDP[0]
28	VCC	**62**	VSSE	**96**	XCU	**130**	BDP[1]
29	NPMEMRQ	**63**	RX–	**97**	VSS	**131**	BDP[2]
30	NPMEMACK	**64**	RX+	**98**	XS[0]	**132**	VSSO
31	VSS	**65**	SDI–	**99**	XS[1]	**133**	BDP[3]
32	$\overline{READY}$	**66**	SDI+	**100**	XS[2]	**134**	BD[31]
33	R/$\overline{W}$	**67**	$\overline{FOTOFF}$	**101**	XS[3]	**135**	BD[30]
34	$\overline{DS}$	**68**	ULSB	**102**	RS[0]	**136**	BD[29]

PQFP PIN DESIGNATIONS

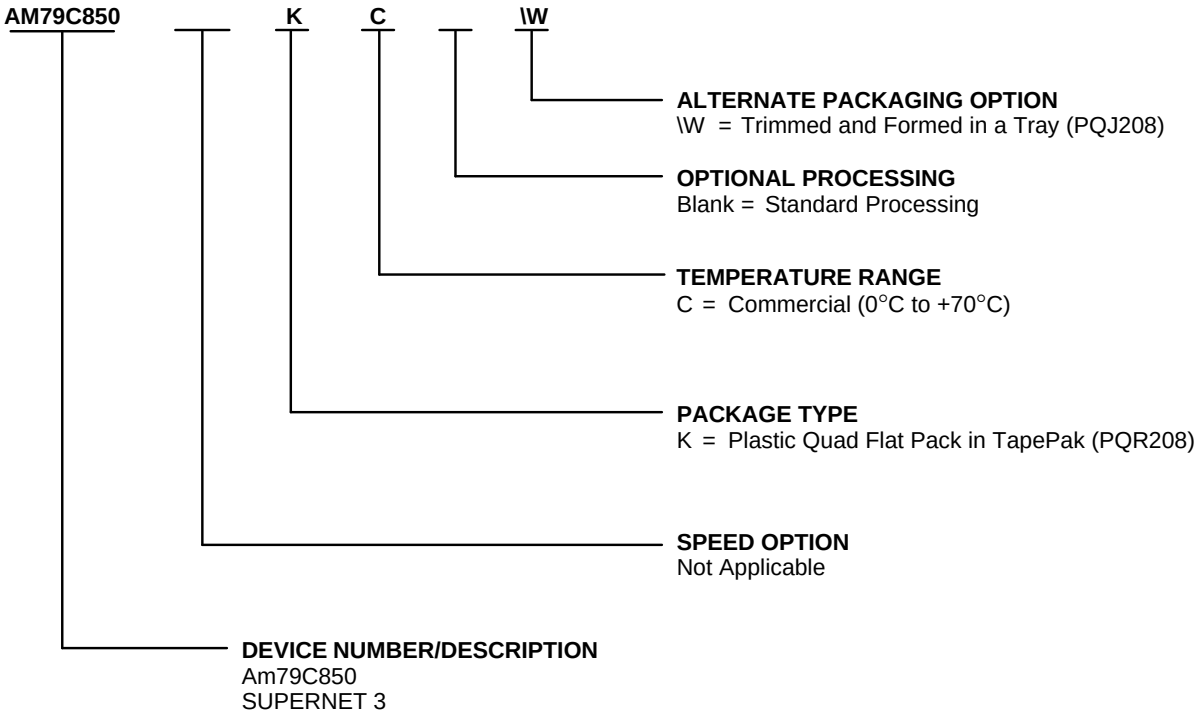
Listed by Pin Number

Pin #	Description	Pin #	Description	Pin #	Description	Pin #	Description
137	VCC	**155**	$\overline{WR}$	**173**	BD[3]	**191**	ADDR[2]
138	BD[28]	**156**	VSSO	**174**	BD[2]	**192**	ADDR[3]
139	BD[27]	**157**	VCCO	**175**	BD[1]	**193**	VSSO
140	BD[26]	**158**	$\overline{RD}$	**176**	BD[0]	**194**	ADDR[4]
141	VSS	**159**	BD[15]	**177**	VCCO	**195**	ADDR[5]
142	BD[25]	**160**	BD[14]	**178**	RDATA2	**196**	ADDR[6]
143	BD[24]	**161**	BD[13]	**179**	RDATA1	**197**	ADDR[7]
144	VSSO	**162**	BD[12]	**180**	HSREQ[2]	**198**	VCCO
145	BD[23]	**163**	BD[11]	**181**	HSREQ[1]	**199**	ADDR[8]
146	BD[22]	**164**	BD[10]	**182**	HSREQ[0]	**200**	ADDR[9]
147	BD[21]	**165**	BD[9]	**183**	HSACK	**201**	ADDR[10]
148	BD[20]	**166**	BD[8]	**184**	VCC	**202**	ADDR[11]
149	VCCO	**167**	VSSO	**185**	QCTRL[2]	**203**	VSSO
150	BD[19]	**168**	BD[7]	**186**	QCTRL[1]	**204**	ADDR[12]
151	BD[18]	**169**	BD[6]	**187**	QCTRL[0]	**205**	ADDR[13]
152	BD[17]	**170**	BD[5]	**188**	VSSO	**206**	ADDR[14]
153	BD[16]	**171**	BD[4]	**189**	ADDR[0]	**207**	ADDR[15]
154	$\overline{CSO}$	**172**	VSSO	**190**	ADDR[1]	**208**	VSSO

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM79C850	KC, KC\W

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PIN DESCRIPTION

I/O pins can only be high impedance in Test Access Port (TAP) operation. Refer to TAP Testability section.

PHY/PMD Interface (46 Pins)

RX+, RX-

Receive Data (PECL Input)

These pins receive differential NRZI data.

TX+, TX-

Transmit Data (PECL Output)

These transmit outputs carry differential NRZI data. They can be forced to logical 0 (TX+ LOW, TX- HIGH) by asserting the $\overline{\text{FOTOFF}}$ input.

RCU

Receive Control Upper (TTL input)

RCU is asserted high to indicate that the upper nibble of the R bus (R7–4) is a network control character. When RCU is low, this nibble contains data. RCU is synchronous to BCLK. This pin has internal pull-up.

RCL

Receive Control Lower (TTL input)

RCL is asserted high to indicate that the lower nibble of the R bus (R3–0) is a network control character. When RCL is low, this nibble contains data. RCL is synchronous to BCLK. This pin has internal pull-up.

R7–0

Receive Bus (TTL input)

The R bus is used to receive information from the external physical layer (PHY) device. Bytes clocked from the physical layer (PHY) into the SUPERNET 3 R-bus input are synchronous to the BCLK. These pins have internal pull-up.

RPAR

Receive parity (TTL input)

RPAR is an input signal used to enhance error detection on the external PHY interface R7:0 bus. RPAR is an input signal used to implement even parity checking on R bus. If there is an odd number of 1's on {R7:0, RCU, RCL}, then RPAR should be 1 and if there is an even number of 1's on {R7:0, RCU, RCL} then RPAR should be 0. This pin has internal pull-up.

RXAFU3–0

Receive Bus Tap for External AF (TTL output, high impedance)

The internal MAC Receive bus lines upper nibble are tapped and brought out as the RXAFU 3–0 pins. These pins are used by an external AF to do external SA and/or DA match.

RXAFL3–0

Receive Bus Tap for External AF (TTL output, TTL input, high impedance)

The internal MAC Receive bus lines lower nibble are tapped and brought out as the RXAFL 3–0 pins. These pins are used by an external AF to do external SA and/or DA match.

Note: *The RXAFL[3:0] input pins are for diagnostic purposes only.*

RXAFCU

Control Upper for AF Receive Bus (TTL output, high impedance)

The RXAFCU output signal is used to flag control symbols being presented on the nibble (3:0) of the RXAFU bus. This signal is synchronous to BCLK. If RXAFCU is asserted high, the nibble on the RXAFU bus is interpreted as a network control character. Otherwise, it is interpreted as a data nibble.

RXAFCL

Control Lower for AF Receive Bus (TTL output, TTL input, high impedance)

The RXAFCL output signal is used to flag control symbols being presented on the nibble (3:0) of the RXAFL bus. This signal is synchronous to BCLK. If RXAFCL is asserted high, the nibble on the RXAFL bus is interpreted as a network control character. Otherwise, it is interpreted as a data nibble.

Note: *The RXAFCL input is for diagnostic purposes only.*

X7–0

Transmit Bus (TTL output, high impedance)

This eight-bit output bus is used to send control and data information to the external physical layer (PHY) device to be transmitted over the medium. Information on the X-bus output is synchronous to the BCLK.

XPAR

Transmit parity (TTL output, high impedance)

XPAR is an output signal used to enhance error detection on the MAC—external PHY interface X7:0 bus. If there is an odd number of 1's on {X7:0, XCU, XCL}, then XPAR should be 1 and if there is an even number of 1's on {X7:0, XCU, XCL} then XPAR should be 0.

XCU

Transmit Control Upper (TTL output, high impedance)

The XCU output signal is used to flag control symbols being presented on the upper nibble of the transmit bus. This signal is synchronous to BCLK. If XCU is asserted

high, the upper nibble of the X-bus is interpreted as a network control character. Otherwise, it is interpreted as a data nibble.

XCL
Transmit Control Lower (TTL output, high impedance)

The XCL output signal is used to flag control symbols being presented on the lower nibble of the transmit bus. This signal is synchronous to BCLK. If XCL is asserted high, the lower nibble of the X-bus is interpreted as a network control character. Otherwise, it is interpreted as a data nibble.

$\overline{\text{FOTOFF}}$
Fiber Optic Transmitter Off (TTL Output, Active Low, high impedance)

The $\overline{\text{FOTOFF}}$ signal, when asserted, causes the optical transmitter to turn off.

SDI+, SDI-
Signal Detect (PECL Differential Line Receiver Inputs)

The SDI input signal pair is from the optical or copper transceivers to indicate whether the received optical or electrical signal is above its threshold. The inverted value of this signal is held in the PHY_STATUS_A register, and the LSDO interrupt bit in the PHY is set whenever SDI becomes asserted.

SCRM
Scrambler/Descrambler enable (DC Input, Active High)

When this pin is strapped high, the SUPERNET 3 is set to operate with a copper PMD and the scrambler/descrambler is enabled. When the pin is strapped to ground, then the scrambler/descrambler function is disabled in the SUPERNET 3, and the SUPERNET 3 is set to operate with a fiber PMD. This pin is ORed with the bit 0 (CIPHER_ENABLE) in the PLC_CNTRL_C register and the result is indicated in the same bit (bit 0). The PMD selection and scrambler/descrambler (S/D) enabling is as follows:

SCRM pin	CIPHER_ ENABLE bit	Result
Low	Reset	Fiber PMD. S/D disabled.
Low	Set	Copper PMD. S/D enabled.
High	Reset	Copper PMD. S/D enabled.
High	Set	Copper PMD. S/D enabled.

LSR 2–0
Line State Register (TTL Output, high impedance)

The LSR2–0 signals directly output the LINE_ST field of the PLC_STATUS_A register to ring test and monitor equipment.

EBFERR
Elasticity Buffer Error (TTL Output, Active High, high impedance)

EBFERR indicates when an overflow or underflow condition occurs in the Elasticity Buffer.

ENCOFF
Encoder Off (TTL Input, Active High)

ENCOFF signal turns off the 4B/5B encoding and decoding function of the PLC core.

ULSB
Unknown Line State (TTL Output, high impedance)

The ULSB signal directly outputs the UNKN_LINE_ST bit of the PLC_STATUS_A register to ring test and monitor equipment.

Clock Pins (3 Pins)

LSCLK
Local Symbol Clock pin (TTL input)

The LSCLK is a 25 MHz clock. It is used by the PLC core.

BCLK
Byte Clock pin (TTL input)

The BCLK is a 12.5 MHz clock. It is used by the PLC and the MAC cores.

BMCLK
Buffer Memory Clock pin (TTL input)

The BMCLK is the clock signal that the MAC core uses for generating the signals to the buffer memory. BMCLK is driven with either a 12.5 or 25 MHz clock signal. If 12.5 MHz operation is desired, then this pin can be tied to BCLK pin. If 25 MHz operation is desired, then this pin can be tied to LSCLK pin.

Node Processor (NP) Interface (35 Pins)

The following paragraphs describe the pins used to interface the SUPERNET 3 with the node processor (NP) or other control devices. The NP interface is used for initializing the SUPERNET 3 as well as for reporting status.

$\overline{\text{CSI}}$
Chip Select Input (TTL input, active low)

– Asynchronous when NPMODE = 0

– Synchronous when NPMODE = 1

The Chip Select Input (active low) enables Read and Write operations to the SUPERNET 3. In the asynchronous mode, the data output is enabled while $\overline{\text{CSI}}$ and $\overline{\text{DS}}$ are both low and R/$\overline{\text{W}}$ is high. In the synchronous mode, the data output is enabled while $\overline{\text{CSI}}$ is low and R/$\overline{\text{W}}$ is high.

$\overline{DS}$

Data Strobe/ (TTL input, active low)

– Asynchronous when NPMODE = 0
– Synchronous when NPMODE = 1

The $\overline{DS}$ input (active low) is used in the handshake between the NP and SUPERNET 3 when the SUPERNET 3 acts as bus slave during register accesses. In the asynchronous mode, this input signal is set by the node processor to transfer data between the NP and the SUPERNET 3. The direction of the data transfer is dictated by the logic level of the R/$\overline{W}$ line. The NP sets $\overline{DS}$ low to initiate a data transfer. $\overline{DS}$ is not used in the synchronous mode. The chip-select input ($\overline{CSI}$) must be low while $\overline{DS}$ is low in order to start an NP bus transaction.

NPADDR7–0

NP Address Bus (TTL input)

The NPADDR7–0 input lines allow direct access to SUPERNET 3 internal registers. In addition, these lines are used to place SUPERNET 3 into different operating states.

The NPADDR bus of the SUPERNET 3 performs two control functions. First, the input on NPADDR7–0 acts as an address, selecting the proper internal register for a read or write operation that is controlled by the R/$\overline{W}$ pin. The data is either read onto or loaded from the 16-bit NP bus. For a discussion of the results of read and load instructions, see the section under Programming the FORMAC Plus in the SUPERNET 2 data book. Second, instructions or commands can be issued to SUPERNET 3 by using the NPADDR bus.

NPDATA15–0

NP Data Bus (TTL input, TTL output, high impedance)

The NP data bus is a 16-bit wide bidirectional data bus used to interface the SUPERNET 3 to the node processor. Data transfer on the NP data bus can be synchronous or asynchronous depending upon the setting of the NPMODE pin. For asynchronous operation, a two-wire handshake is provided through the $\overline{READY}$ and data-strobe ($\overline{DS}$) lines.

NPMODE

NP Bus Mode (TTL input)

The level on the NPMODE pin defines the type of NP-bus interface with the SUPERNET 3. When NPMODE is strapped high, the NP interface operates synchronously with BCLK. When NPMODE is strapped low, asynchronous interface operation is selected.

$\overline{READY}$

Ready (TTL output, open drain, active low, high impedance)

In asynchronous mode, the $\overline{READY}$ output (active low) is used in the handshake between the NP and SUPERNET 3. The SUPERNET 3 $\overline{READY}$ output provides an asynchronous acknowledgment to the NP that data transfer is complete. The SUPERNET 3 asserts $\overline{READY}$ when it has put the data onto the NP bus during a read cycle, or when it has taken the data from the NP bus during a write cycle. $\overline{READY}$ is a response to the $\overline{CSI}$ and $\overline{DS}$ inputs, and returns high after the $\overline{CSI}$ or $\overline{DS}$ signals go high.

In the synchronous mode, the $\overline{READY}$ line goes active on the BCLK edge when $\overline{CSI}$ and $\overline{DS}$ are active. $\overline{READY}$ goes inactive on the following BCLK edge. In the case of loading/reading of the MDR (memory data register), $\overline{READY}$ goes active on the BCLK edge after the completion of any pending data transfer from/to buffer memory.

R/$\overline{W}$

Read/Write Select (TTL input)

The R/$\overline{W}$ line is used to select the type of access (i.e., read or write) between the SUPERNET 3 and the NP. If R/$\overline{W}$ is high, data is read from the SUPERNET 3 to the NP. If R/$\overline{W}$ is low, the data flow is from the NP to the SUPERNET 3.

$\overline{MINTR1}$

Maskable Interrupt 1 (TTL output, open drain, high impedance)

The $\overline{MINTR1}$ output (active low) is an attention line to the NP. $\overline{MINTR1}$, when active, indicates an interrupt due to one or more unmasked flags in status register 1. In general, the active state of $\overline{MINTR1}$ indicates that an unmasked interrupt condition or a transmit condition has occurred. $\overline{MINTR1}$ is deactivated once either the lower or upper 16 bits of status register 1 (ST1L or ST1U) are read. Once $\overline{MINTR1}$ is asserted, all 32 bits of status register 1 must be read to enable any future interrupt on this pin.

$\overline{MINTR2}$

Maskable Interrupt 2 (TTL output, open drain, high impedance)

The $\overline{MINTR2}$ output (active low) is an attention line to the NP. $\overline{MINTR2}$, when active, indicates an interrupt due to one or more unmasked flags in status register 2. In general, the active state of $\overline{MINTR2}$ indicates that an unmasked interrupt condition, a receive condition, or a

change in ring status has occurred. $\overline{\text{MINTR2}}$ is deactivated once either the lower or upper 16 bits of status register 2 (ST2L or ST2U) are read. Once $\overline{\text{MINTR2}}$ is asserted, all 32 bits of status register 2 must be read in order to enable any future interrupt on this pin.

$\overline{\text{MINTR3}}$

Maskable Interrupt 3 (TTL output, open drain, high impedance)

The $\overline{\text{MINTR3}}$ output (active low) is an attention line to the NP. $\overline{\text{MINTR3}}$, when active, indicates an interrupt due to one or more unmasked flags in status register 3. In general, the active state of $\overline{\text{MINTR3}}$ indicates that an unmasked interrupt condition, a receive condition in the second receive queue has occurred. $\overline{\text{MINTR3}}$ is deactivated once either the lower or upper 16 bits of status register 3 (ST3L or ST3U) are read. Once $\overline{\text{MINTR3}}$ is asserted, all 32 bits of status register 3 must be read in order to enable any future interrupt on this pin.

$\overline{\text{MINTR4}}$

Maskable Interrupt 4 (TTL output, open drain, high impedance)

The $\overline{\text{MINTR4}}$ output (active low) is an attention line to the NP. $\overline{\text{MINTR4}}$, when active, indicates an interrupt due to one or more unmasked flags in the PHY interrupt event (INTR_EVENT) register. In general, the active state of $\overline{\text{MINTR4}}$ indicates that a change in PCM state machine or timer expiration or counter overflow has occurred. $\overline{\text{MINTR4}}$ remains active until cleared by reading the INTR_EVENT register.

When the MENSNGLINT (MDREG 3, bit 10) is set, the SUPERNET 3 generates only one interrupt ($\overline{\text{MINTR4}}$) and the other interrupt lines ($\overline{\text{MINTR1}}$, $\overline{\text{MINTR2}}$, and $\overline{\text{MINTR3}}$) are not toggled. The SUPERNET 3 operates in a vectored interrupt mode, i.e., a vector register is read to determine which status register is the source of the interrupt.

NPMEMRQ

Node Processor Memory Request (TTL input)

The input signal NPMEMRQ is a request by the node processor to obtain control of buffer memory.

NPMEMACK

Node Processor Memory Access Acknowledge (TTL output, high impedance)

This signal indicates that an NPMEMRQ has been granted and that the NP now has control of buffer memory (ADDR-bus, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{CSO}}$, BDP, BD, and BDTAG). If NPMEMACK is forced low while NPMEMRQ is active (due to a higher priority request), the NP must release control of the bus within two BMCLK periods after the NPMEMACK line goes inactive.

SUPERNET 3/Buffer Memory Interface (56 Pins)

ADDR15–0

Buffer Memory Address (TTL output, high impedance)

The 16-bit ADDR-bus provides the addresses that access the buffer memory. The address selection depends on the result of bus arbitration in the SUPERNET 3. Each memory access lasts for two BMCLK clock cycles and the address is valid for both of these cycles. When buffer memory control has been released to the NP, the ADDR bus is in the high-impedance state.

Note: As long as the use of the buffer memory has not been granted to the node processor or host (HSACK and NPMEMACK not active), the SUPERNET 3 may drive the address lines even though no control signals are active.

BD31–0

Buffer Memory Data Bus (TTL input, output, high impedance)

The 32-bit BD bus interfaces the SUPERNET 3 to the buffer memory or any external logic using this bus. These lines transfer data to and from the buffer memory for the SUPERNET 3. These signals are synchronous to BMCLK.

BDP3–0

Buffer Data Parity Bus (TTL input, output, high impedance)

The BDP3–0 bus contains the four byte-parity lines for the BD bus as shown in the following table:

BD-Bus Lines	Corresponding Parity Lines
BD7–0 and tag bit	BDP0
BD15–8	BDP1
BD23–16	BDP2
BD31–24	BDP3

Note: *BD bus parity can be either even or odd, based on the state of the parity bit (bit 12) in mode register 2 (MDREG2).*

BDTAG

Buffer Data Tag Indication (TTL input, output, high impedance)

In receive mode, this bit defines whether the information on the BD bus is data (BDTAG = 0) or frame status (BDTAG = 1). In transmit mode, when BDTAG = 1, it indicates that the end of a frame has been reached, as indicated by the presence of a tag bit in both the last long

word and the descriptor word at the end of the frame. In transmit mode, when BDTAG = 0, it indicates that the information on the BD bus is data, i.e., end-of-frame not yet reached.

$\overline{\text{CSO}}$

Chip-Select Output (TTL output, high impedance, active low)

The chip-select output (active low) is a select signal for buffer memory read and write operations. This line is in the high-impedance state when buffer memory control is released to the NP.

$\overline{\text{RD}}$

Buffer Memory Read (TTL output, high impedance, active low)

This output signal (active low) controls the buffer memory during a buffer-memory read accesses. This line is in the high-impedance state when buffer memory control is released to the NP.

$\overline{\text{WR}}$

Buffer Memory Write (TTL output, high impedance, active low)

This (active low) output signal, in its active-low state, allows write accesses to buffer memory. This line is in the high-impedance state when buffer memory control is released to the NP.

Host/Buffer Memory Interface (10 Pins)

All these signals are synchronous to BMCLK.

HSACK

Host Acknowledge (TTL output, high impedance)

This signal indicates that the current host read/write request is being granted by SUPERNET 3 and allows read/write accesses of buffer memory by the host.

HSREQ2–0

Host Request Bus (TTL input)

The host request bus specifies to SUPERNET 3 the type of buffer memory access the host requires, as described in the following table.

Special-frame write requests are used to set up claim, beacon, and auto-void frames in the buffer memory (see the discussion under Buffer Memory Operation in SUPERNET 2 data book). These requests make use of the WPXSF register to set up special frames in the special-frame area.

Read request is used to retrieve received frames from buffer memory and store them in the system memory. Write requests are used to set up frames in buffer memory for transmission.

HSREQ2	HSREQ1	HSREQ0	Type of Request
0	0	0	None.
0	0	1	Read Request: Second Receive Queue*
0	1	0	Special Frame Write Request.
0	1	1	Read Request: Receive Queue.
1	0	0	Write Request: Synchronous Queue.
1	0	1	Write Request: Asynchronous Queue 0.
1	1	0	Write Request: Asynchronous Queue 1.
1	1	1	Write Request Asynchronous Queue 1.

Note: ** Only if two receive queue operation is selected through MDREG3.*

QCTRL2–0

Buffer Queue Control (TTL output, high impedance)

The QCTRL2–0 status output lines are encoded as described in the following table.

QCTRL2	QCTRL1	QCTRL0	Indicated Status
0	0	0	(1) Quiescent. (2) Space remains for more data while loading a transmit queue
0	0	1	Unloading transmit frame from Synchronous Queue
0	1	0	Unloading transmit frame from Asynchronous Queue 0
0	1	1	Unloading transmit frame from Asynchronous Queue 1
1	0	0	Reserved
1	0	1	Current transmit frame Underrun
1	1	0	Current transmit queue full.
1	1	1	Current transmit queue almost full

These signals communicate to the host the current condition of the transmit queues. This provides useful information for doing the host interface. The meaning of these states are as follows:

A. QCTRL[2:0] = 000

The quiescent state exists when SUPERNET 3 is neither transmitting nor receiving. This state is also true while loading a transmit queue (making a write request to a queue) and not yet unloading it, and when there is space in the queue for more data.

B. QCTRL[2:0] = 001, 010 or 011

These states indicate unloading frame from the Synchronous Queue, Asynchronous Queue 0 or Asynchronous Queue 1, respectively. They are valid as long as the corresponding queue is not yet in the almost full or full state and, at the same time, the SUPERNET 3 is reading out of the queue. The host can transfer more data into the corresponding queue when any of these states is present. These three combinations may appear one BMCLK period later than the time indicated in the timing diagram.

C. QCTRL[2:0] = 101

This state is present when all of the following three conditions are satisfied:

1. The host has issued a write request for this queue
2. Transmit FIFO underrun occurs
3. Transmit buffer-memory underrun occurs for this queue

D. QCTRL[2:0] = 110

When the transmit queue being requested is full, this state is presented at the queue control signals. Note that this state does not exist in SUPERNET 2, it is added in SUPERNET 3.

E. QCTRL[2:0] = 111

This state means the number of free long words remaining in the transmit queue which the current write request is for has decreased to the almost-full value (AFULL3-0) programmed in mode register 2. This signal condition is asserted for one BMCLK cycle only as in the FORMAC PLUS if the MENAFULL bit in the mode register 3 is not set. If this bit is set, this state will remain for every cycle as long as the queue is in almost full condition and it is not yet full.

Note: *If AFULL3-0 is set to 000, this state is not presented, even when the transmit FIFO in buffer memory is full.*

RDATA1

Receive Data for Receive Queue #1
(TTL output, high impedance)

This signal indicates that received data is present in the buffer memory and is ready to be transferred by the host to system memory. Read requests are not acknowledged when RDATA1 is inactive.

RDATA2

Receive Data for Receive Queue #2
(TTL output, high impedance)

This signal indicates that received data is present in the buffer memory and is ready to be transferred by the host to system memory. Read requests are not acknowledged when RDATA2 is inactive.

Special Functions and Control Pins (16 Pins)

FLXI

Flush/Inhibit (TTL input)

The SUPERNET 3 FLXI pin can be programmed to perform either of two functions: it can provide a flush received frame function for the chip or it can provide an unconditional transmit-inhibit function.

If the FLUSH function is selected and the pin is asserted by external logic, then the incoming frame is flushed. The buffer memory pointers are not advanced from where they were before the frame was received. This prevents unwanted frames and fragments from occupying receive buffer space and taking up the buffer memory bus bandwidth.

If the TRANSMIT INHIBIT function is selected and the pin is asserted by external logic, then the SUPERNET 3 completes transmitting the current frame (if transmitting) releases the token and no further transmissions can occur until the pin is deasserted. During the time that the TRANSMIT INHIBIT function is enabled, the network timers and state machines operate normally.

RS5–0

Receive Status (TTL output, high impedance)

The receive-status (RS4–0) pins indicate the type of frame received, and the condition of the receive state machine. The RS4–0 status output pins are encoded as illustrated in Table 3 in the SUPERNET 2 data book and the enhancements RS5–0 are described here.

RS5	RS4	RS3	RS2	RS1	RS0	Indicated Status
0	X	X	X	X	X	As in SUPERNET 2 FORMAC Plus
1	0	0	0	0	0	Reserved
1	0	X	0	0	1	Starting Delimiter and non-data symbol received
1	0	0	0	1	0	OSM mode: Stripping frame
1	0	0	0	1	1	Reserved
1	0	0	1	0	0	Reserved
1	0	0	1	0	1	Frame Abort
1	0	0	1	1	0	Frame Flush
1	0	0	1	1	1	Reserved
			through			
1	1	1	1	1	1	Reserved

XS3–0

Transmit Status (TTL output, high impedance)

The transmit-status (XS3–0) pins indicate the transmit status conditions of the MAC and are valid for one clock cycle. These status signals are not present for repeated or stripped frames. These status output pins are encoded as illustrated in Table 4 (SUPERNET 2 data book) and the enhancements are described here.

XS3	XS2	XS1	XS0	Indicated Status
0	0	0	0	Quiescent.
0	0	0	1	Transmit Aborted.
0	0	1	0	Token Issued
0	0	1	1	Reserved.
0	1	0	0	Transmitting Synchronous Queue.
0	1	0	1	Transmitting Asynchronous Queue 0.
0	1	1	0	Transmitting Asynchronous Queue 1.
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Initiated Claim.
1	0	1	0	Initiated Beacon.
1	0	1	1	Initiated Void
1	1	0	0	MAC Frame Aborted
1	1	0	1	Void Frame Aborted

$\overline{\text{XDAMAT}}$

External Destination Address Match (TTL input, active low)

This input provides a means for additional destination-address detection external to the SUPERNET 3. This pin should be tied high when external destination-address detection is not used. This input should remain asserted for at least one BCLK cycle, and must be deasserted for at least one BCLK cycle before a subsequent external destination address match is recognized.

The $\overline{\text{XDAMAT}}$ pin which is generated by the external AF is logically ORed with the “af_da” output signal generated by the internal AF logic. This pin should be tied high when external address detection (such as an external AF) is not used.

$\overline{\text{XDA\_XACT}}$

External Destination Address Exact Match (TTL input, active low)

This input indicates whether the external address match was exact (low) or inexact (high). This input should remain asserted for at least one BCLK cycle, and must be deasserted for at least one BCLK cycle before a subsequent external source address match is recognized. It must be asserted and deasserted in an identical

fashion to the $\overline{\text{XDAMAT}}$ pin. This input is used in conjunction with the $\overline{\text{XDAMAT}}$ pin as follows:

Match	Action
$\overline{\text{XDA\_XACT}}$ and $\overline{\text{XDAMAT}}$	A, C indicators set and frame copied*.
$\overline{\text{XDA\_XACT}}$ and XDAMAT	Invalid combination. Ignored by MAC.
XDA_XACT and $\overline{\text{XDAMAT}}$	A, C indicators not set and frame copied.
XDA_XACT and XDAMAT	No action.

** Frame is copied if valid frame or if in promiscuous or limited promiscuous mode. In OSM, the A, C indicators are set according to the OSM rules if bits 4, 5 (MEIND0,1) are set.*

The $\overline{\text{XDA\_XACT}}$ pin which is generated by the external AF is logically ORed with the "af_dax" output signal generated by the internal AF logic. This pin is enabled only if the MENXACT bit in the mode register 3 is set. This pin should be tied high when external address detection (such as an external AF) is not used.

$\overline{\text{XSAMAT}}$

External Source Address Match (TTL input, active low)

This input provides a means for additional source-address detection external to the SUPERNET 3. This pin should be tied high when external source-address detection is not used. This input should remain asserted for at least one BCLK cycle, and must be deasserted for at least one BCLK cycle before a subsequent external destination address match is recognized.

The $\overline{\text{XSAMAT}}$ pin which is generated by the external AF is logically ORed with the "af_sa" output signal generated by the internal AF logic. This pin should be tied high when external address detection (such as an external AF) is not used.

$\overline{\text{XSA\_XACT}}$

External Source Address Exact Match (TTL input, active low)

This input indicates whether the external source address match was exact (low) or inexact (high). This input should remain asserted for at least one BCLK cycle, and must be deasserted for at least one BCLK cycle before a subsequent external source address match is recognized. It must be asserted and deasserted in an identical fashion to the $\overline{\text{XSAMAT}}$ pin. This input is used in conjunction with the $\overline{\text{XSAMAT}}$ pin as follows:

Match	Action
$\overline{\text{XSA\_XACT}}$ and $\overline{\text{XSAMAT}}$	Frame stripped.
$\overline{\text{XSA\_XACT}}$ and XSAMAT	Invalid combination. Ignored by MAC.
XSA_XACT and $\overline{\text{XSAMAT}}$	Frame not stripped.
XSA_XACT and XSAMAT	No action.

The $\overline{\text{XSA\_XACT}}$ pin which is generated by the external AF is logically ORed with the "af_sax" output signal generated by the internal AF logic. This pin is enabled only if the MENXACT bit in the mode register 3 is set. This pin should be tied high when external address detection (such as an external AF) is not used.

$\overline{\text{RST}}$

Reset (TTL input)

The $\overline{\text{RST}}$ signal (active low) is an asynchronous input that initializes the internal SUPERNET 3 state machines and registers. Once $\overline{\text{RST}}$ is asserted low, it must remain asserted for at least twenty BCLK cycles. When it is deasserted the SUPERNET 3 is ready to begin normal operation only after 750 LSCLK cycles. The 750 LSCLK cycles are needed for calibration of the PDX core. Assertion and deassertion are asynchronous. A warm reset (assertion of $\overline{\text{RST}}$ after the device is in operation) will cause device outputs to be unpredictable until the device is initialized.

Testability Interface (5 Pins)

TCK

Test Clock In (TTL input)

TCK provides the clock for the test logic. Any stored-state devices contained in the test logic must retain their state indefinitely if the signal applied to TCK is held high or low.

TMS

Test Mode Select In (TTL input, Synchronous to TCK)

The test mode select input directs the operation of the generation of the TAP controller. The state of the TMS signal is sampled on the rising edge of TCK. If for some reason TMS is not driven externally, the TAP controller should behave as if this signal were driven with a logic 1 (internal pull-up).

TDI

Test Data In (TTL input, Synchronous to TCK)

This pin provides for the application of serial instructions and data. The state of this signal is sampled on the rising edge of TCK. If for some reason TDI is not driven externally, the test logic should behave as if a logic 1 were applied to this signal (internal pull-up).

TDO

Test Data Output (TTL Output, 3-state, Synchronous to TCK)

This pin provides the serial output for instructions and data from the test logic. No inversion of data is allowed between TDI and TDO during shift operations. The state of TDO changes on the falling edge of TCK. TDO is in the high impedance state except during shifting operations.

$\overline{\text{TRST}}$

Test Reset (asynchronous TTL input, active low)

This input is provided for asynchronous initialization of the TAP controller. When a logic 0 is applied, the TAP controller must go to the Test-Logic-Reset state. If for some reason $\overline{\text{TRST}}$ is not driven externally, the test logic should behave as if a logic 1 were applied (internal pull-up). This pin can not be used to initialize any system logic.

Power and Ground (37 Pins)

GND

Ground (input)

There are 23 ground (GND) pins on the SUPERNET 3 chip. They must all be connected to a common external ground reference.

V_{CC}

+5 V Power (input)

There are 15 pins carrying +5-V power (VCC) on the SUPERNET 3 chip. They must all be connected to a 5 V ±5% source.

SUPERNET 2 Features not Supported

The following features are not supported in SUPERNET 3 in any mode.

- SUPERNET 3 supports the Tag Mode of operation for the system-to-buffer-memory and network (MAC)-to-buffer-memory interfaces. Non-Tag mode of operation is no longer supported.
- SUPERNET 3 supports three transmit queues: Synchronous, Async0 and Async1. Async2 is no longer supported.
- The 'Disable Carry' (DISCRY) function is no longer supported. Setting of the DISCRY bit in the mode register 1 (MDREG1: bit 6) allowed segmenting of the TRT, THT, TVX, and TMSYNC registers into 4 and 5 bits each for diagnostic purposes. This is no longer necessary due to the testability enhancements.
- Single-Frame Receive mode is no longer supported.
- Symbol Control is no longer supported in the MAC. This function was used for diagnostics purposes to transmit user-controlled data, control and violation symbols to the PHY.
- The HOLD function and associated logic is eliminated and it is no longer supported.

Miscellaneous Changes from SUPERNET 2

- The 'Current Queue Almost Full' (AFULL) encoding of the QCTRL signals is modified to be asserted for every clock after the AFULL boundary is crossed until the queue is full while a Host write request is asserted. Currently, the signal is asserted for one clock only.
- '$\overline{\text{XDA}}\_\overline{\text{XACT}}$' and '$\overline{\text{XSA}}\_\overline{\text{XACT}}$' input signals are provided for the external CAM (if implemented).
- For increased robustness, all internal tri-state busses will have a driven default state and will not be allowed to float.
- The Node Processor access interface has been streamlined to two modes:
  1) The FORMAC Plus asynchronous access mechanism for accessing all blocks.
  2) The PLC two-cycle synchronous access mechanism for accessing all blocks.
- There are four interrupt pins: two generated by the two MAC status registers, one generated by the AF and one generated by the PHY status register.

EXPLANATION OF ENHANCEMENTS

Status Pins

XS 3:0

Transmit Status pins (outputs)

An additional transmit status pin has been added to provide more transmit information. The encoding of the status pins is fully backward compatible with the SUPERNET 2 chipset. The enhanced encoding is enabled by setting the MENXS bit in the mode register 3 (MDREG3). The encoding of the XS pins is as follows:

XS3	XS2	XS1	XS0	Indicated Status
0	0	0	0	Quiescent
0	0	0	1	Transmit Aborted
0	0	1	0	Token Issued
0	0	1	1	Reserved
0	1	0	0	Transmitting Synchronous Queue
0	1	0	1	Transmitting Asynchronous Queue 0
0	1	1	0	Transmitting Asynchronous Queue 1
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Initiated Claim
1	0	1	0	Initiated Beacon
1	0	1	1	Initiated Void
1	1	0	0	MAC Frame Aborted
1	1	0	1	Void Frame Aborted
1	1	1	0	Reserved
1	1	1	1	Reserved

RS 5:0

Receive Status pins (outputs)

An additional receive status pin has been added to provide more receive information. The encoding of the status pins is fully backward compatible with the SUPERNET 2 chipset. The enhanced encoding is enabled by setting the MENRS bit in the mode register 3 (MDREG3). The encoding of the RS pins is shown on the following table.

RS5	RS4	RS3	RS2	RS1	RS0	Indicated Status
0	X	X	X	X	X	As in SUPERNET 2 FORMAC Plus
1	0	0	0	0	0	Reserved
1	0	X	0	0	1	Starting Delimiter and non-data symbol received
1	0	0	0	1	0	OSM mode: Stripping frame
1	0	0	0	1	1	Reserved
1	0	0	1	0	0	Reserved
1	0	0	1	0	1	Frame Abort
1	0	0	1	1	0	Frame Flush
1	0	0	1	1	1	Reserved
			through			
1	1	1	1	1	1	Reserved

QCTRL 2:0

Queue Control pins (outputs)

The encoding of the QCTRL pins is as follows:

QCTRL2	QCTRL1	QCTRL0	Indicated Status
0	0	0	(1) Quiescent. (2) Space remains for more data while loading a transmit queue
0	0	1	Unloading transmit frame from Synchronous Queue
0	1	0	Unloading transmit frame from Asynchronous Queue 0
0	1	1	Unloading transmit frame from Asynchronous Queue 1
1	0	0	Reserved
1	0	1	Current transmit frame Underrun
1	1	0	Current transmit queue full
1	1	1	Current transmit queue almost full

Slower Buffer Memory Interface

The buffer memory interface has been modified enabling slower SRAMs (35 ns) to be used as buffer memory. This reduces the system cost. The interface is fully backward compatible with the SUPERNET 2 buffer memory interface.

Clocking

LSCLK

Local Symbol Clock pin (input)

The LSCLK is a 25 MHz clock. It is used by the PLC-S and PDX cores.

BCLK

Byte Clock pin (input)

The BCLK is a 12.5 MHz clock. It is used by the PLC-S and the MAC cores.

BMCLK

Buffer Memory Clock pin (input)

The BMCLK is the clock signal that the MAC core uses for generating the signals to the buffer memory. BMCLK is driven with either a 12.5 or 25 MHz clock signal. If 12.5 MHz operation is desired, then this pin must be tied to BCLK pin. If 25 MHz operation is desired, then this pin must be tied to LSCLK pin.

A, C Indicators

The setting of the A, C indicators has been modified to allow the indicator setting to be selectable in any of the modes: online, online special mode, or external loopback. The A, C indicators can be set as normal, MSC method, or not modified at all. The modified setting of the A, C indicators can be selected by setting the

MEIND0 and MEIND1 bits in the mode register 3 (MDREG3).

MEIND1	MEIND0	Description
0	0	Default SUPERNET 2 behavior
0	1	Set A, C as in ONLINE mode. This overrides OSM status indicator setting (i.e., if MDREG1 bits MMODE2=0, MMODE1=1, MMODE0=0).
1	0	Set A, C as in OSM mode. This overrides the MMODE2–0 bits in the MDREG2 for the status indicator setting.
1	1	Do not set the A, C indicators in any mode.

MEIND[1:0]	OSM	EN_XACT	XDA_XACT	XDA	DA_INT	A_FLAG	C_FLAG	A_BIT	C_BIT
00	0	x	x	0	0	0	0	NM	NM
00	0	x	x	x	1	1	1	1	1
00	0	x	x	1	0	1	1	1	1
00	1	x	x	0	0	0	0	NM	NM
00	1	x	x	x	1	1	1	1	1
00	1	x	x	1	0	0	1	NM	1
01	x	0	x	0	0	0	0	NM	NM
01	x	0	x	x	1	1	1	1	1
01	x	0	x	1	0	1	1	1	1
01	x	1	x	0	0	0	0	NM	NM
01	x	1	x	x	1	1	1	1	1
01	x	1	0	1	0	0	1	NM	1
01	x	1	1	1	0	1	1	1	1
10	x	0	x	0	0	0	0	NM	NM
10	x	0	x	x	1	1	1	1	1
10	x	0	x	1	0	0	1	NM	1
10	x	1	x	0	0	0	0	NM	NM
10	x	1	x	x	1	1	1	1	1
10	x	1	0	1	0	0	1	NM	1
10	x	1	1	1	0	1	1	1	1
11	x	x	x	x	x	0	0	NM	NM

where,

MEIND[1:0] Bit 4 and 5 of MDREG3

OSM - Bit 14-12 of MDREG1

EN_XACT - Bit 2 of MDREG3

XDA_XACT - Pin 113, is an active low signal. “1” indicates signal is active and “0” indicates signal is inactive

XDA - Pin 114, is an active low signal. “1” indicates signal is active and “0” indicates signal is inactive.

DA_INT - Internal DA match signal

A_FLAG - DA Match Flag

C_FLAG - Frame Copied Flag

A_BIT - A bit in the End Delimiter

C_BIT - C bit in the End Delimiter

x - Don’t care condition.

NM - Not modified by the MAC

Transmit Queues

ASYNC2 Transmit Queue Not Supported

The SUPERNET 3 supports SYNCHRONOUS, and two ASYNCHRONOUS priorities. The ASYNC2 queue is no longer supported. This causes the following changes:

1. TPRI2 (16-bit priority register for asynchronous queue 2) is no longer implemented.
2. EAA2, WPXA2, SWPXA2, RPXA2 registers are no longer implemented.
3. The 'Clear Asynchronous Queue 2 Lock' and 'Transmit Asynchronous Queue 2' commands are no longer available in the command registers 1 and 2, respectively. The value 0x18 in command register 1 and 0x08 in command register 2 shall not be decoded to any other instruction. These values are reserved.
4. The STEFRMA2, STECFRMA2 and STXABRA2 bits in the upper 16 bits of the status register 1 (ST1U) are reserved and set to zero. Similarly SQLCK2, STXINFLA2, SPCEPDA2, and STBURA2 are reserved and set to zero.
5. The QCTRL[2:0] = 100 encoding is now invalid. This encoding indicated 'Request transfer into Asynchronous Queue 2' which is no longer available. The encoding is reserved and shall not be used to indicate any other QCTRL condition. (See NOTE)
6. The HSREQ[2:0] = 111 is now decoded as "Write Request: Asynchronous Queue 1". In FORMAC+ this request indicated a write request to asynchronous queue 2 which is no longer available.

Note: *If the encoding HSREQ[2:0] = 111 is used, the SUPERNET 3 would not use the QCTRL[2:0] = 100 encoding to indicate status of Asynchronous Queue, but instead the QCTRL[2:0] = 011 ("Request transfer into Asynchronous Queue 1") encoding would be indicated by SUPERNET 3 and external logic could be added to invert this encoding to be compatible with FORMAC+.*

AFULL Encoding of QCTRL Signals Modified

The QCTRL2–0 pins provide the encoded status of the buffer memory transmit queues. The value QCTRL[2:0] = 111, 'Current queue almost full', was asserted for one host write cycle in SUPERNET 2. This signal shall now be generated for every host write cycle until the queue becomes full or the almost full threshold is no longer exceeded.

This new signal assertion is implemented only if the bit MENAFULL is set in mode register 3 (MDREG3)

Transmit Frame Format

In SUPERNET 2 transmit frames must consist of aligned data, i.e. all words in the buffer memory must contain four valid bytes, except that the last data word may consist of less than four bytes. This required that the Frame Control (FC) of the frame be written as the most significant byte of the frame data long word. SUPERNET 3 would support an enhanced feature, where in the Frame Control (FC) could be any byte of the frame data long word. The Destination Address (DA) would follow the FC as the next byte in any mode of operation. This feature is enabled only when the bits MENFCLOC (bit 12 & 13) is set in mode register 3 (MDREG3). Upon reset these bits would be both zero and the Frame Control (FC) has to be written as the most significant byte of the frame data long word. The following table describes the decoding of the MENFCLOC bits in the mode register 3 (MDREG 3):

	If MENFCLOC 13-12 =	00	01	10	11
Case 1: LSB = 0 (MDREG 2 bit 11)	Then FC starts at:	Byte 1 (MSBYTE)	Byte 2	Byte 3	Byte 4 (LSBYTE)
Case 1: LSB = 1 (MDREG 2 bit 11)	Then FC starts at:	Byte 4 (MSBYTE)	Byte 3	Byte 2	Byte 1 (LSBYTE)

Non-Tag Mode of Operation No Longer Supported

The SUPERNET 3 only supports the tag mode of operation for transmit and receive. The non-tag mode of operation is no longer supported. All functionality related to the non-tag mode of operation is removed. This causes the following changes:

1. Bits [7:4] in status register 1 upper (ST1U), indicating 'Transmit End of Chain of Frames' (STECFRM-S, A0, A1, A2) are now reserved. They shall be read as zero.
2. Bits [7:4] in status register 1 lower (ST1L), indicating 'Transmit Instruction Full' (STXINFL-S, A0, A1, A2) are now reserved. They shall be read as zero.
3. In Command register 2, the commands 'Transmit Synchronous Queue' [0x01], 'Transmit Asynchronous Queue 0' [0x02], and 'Transmit Asynchronous Queue 2' [0x08] are now reserved. These values shall not be decoded to any other instruction.
4. Bit 15 in mode register 2 (MDREG2) indicating Buffer Memory Mode is now decoded differently. This bit shall be read as one upon reset, indicating TAG mode of operation. If programmed to zero, the modified TAG mode of operation will be enabled. This bit selection applies to both receive queues if MENDRCV bit is set in mode register 3 (MDREG 3).

Modified TAG Mode Operation

The SUPERNET 3 will have two modes of host interface to buffer memory. The two modes are distinct and independent ways of accessing the buffer memory depending upon the selection of the TAG mode or modified TAG mode. In TAG mode the SUPERNET 3 provides the local buffer management, i.e the queue pointers are maintained by SUPERNET 3. Modified TAG mode is used when the NON-TAG mode users of FORMAC+ are redesigning for SUPERNET 3. Loading of transmit frames in modified TAG is identical to TAG mode. The unloading of received frames is different in Modified TAG mode of operation. The format of a receive frame is as shown Figure 1. The first long word in each frame consists of a 16-bit status word and a 16-bit word that gives the length of the frame in bytes. The status/length word is followed by the data words. The location of the first byte in the first long word of data is defined by the byte boundary bits RXFBB1–0 of mode register (MDREG 2). At the end of the frames that make up a receive queue, SUPERNET 3 writes a long word with all bits as a logic 0, which indicates that there is no more data in this queue. The only function of this word is to act as an end delimiter. Note that the MSVALID bit in bit 31 of the status word at the start of the frame is always in the logic 1 state. Also, when another frame follows this queue, it overwrites the end delimiter word with the receive status word of the new frame. After each frame has been written into buffer memory, SUPERNET 3 write the status and frame length at the start of each frame, and places an end-indicator word of all 0's at the end of the queue. Once a frame is completely received, the status bit SRCOMP in status register 2 (ST2U) is set. If the received frame is aborted, the SUPERNET 3 will write the status word indicating the aborted status (bit 30) and the length field bits will be all zero. If the receive queue has an overflow condition during frame reception, the status register bit indicating SRCVOVR in status register 2 (ST2U bit 11), is set high and the frame is aborted. An overflow also sets the MSRABT bit (bit 30) in the receive frame status word of the incomplete frame. The received frames are unloaded by the host from the buffer memory by using the host request pins (HSREQ). The RDATA signal is always in the 0 state and receive frame threshold (RTHR) is not applicable in modified TAG mode for asserting the RDATA pin. If dual receive queue operation is selected (MENDRCV, bit 11 in MDREG 3) then the receive status information would be indicated in the corresponding status register (ST2U for RECV1 and ST3U for RECV2).

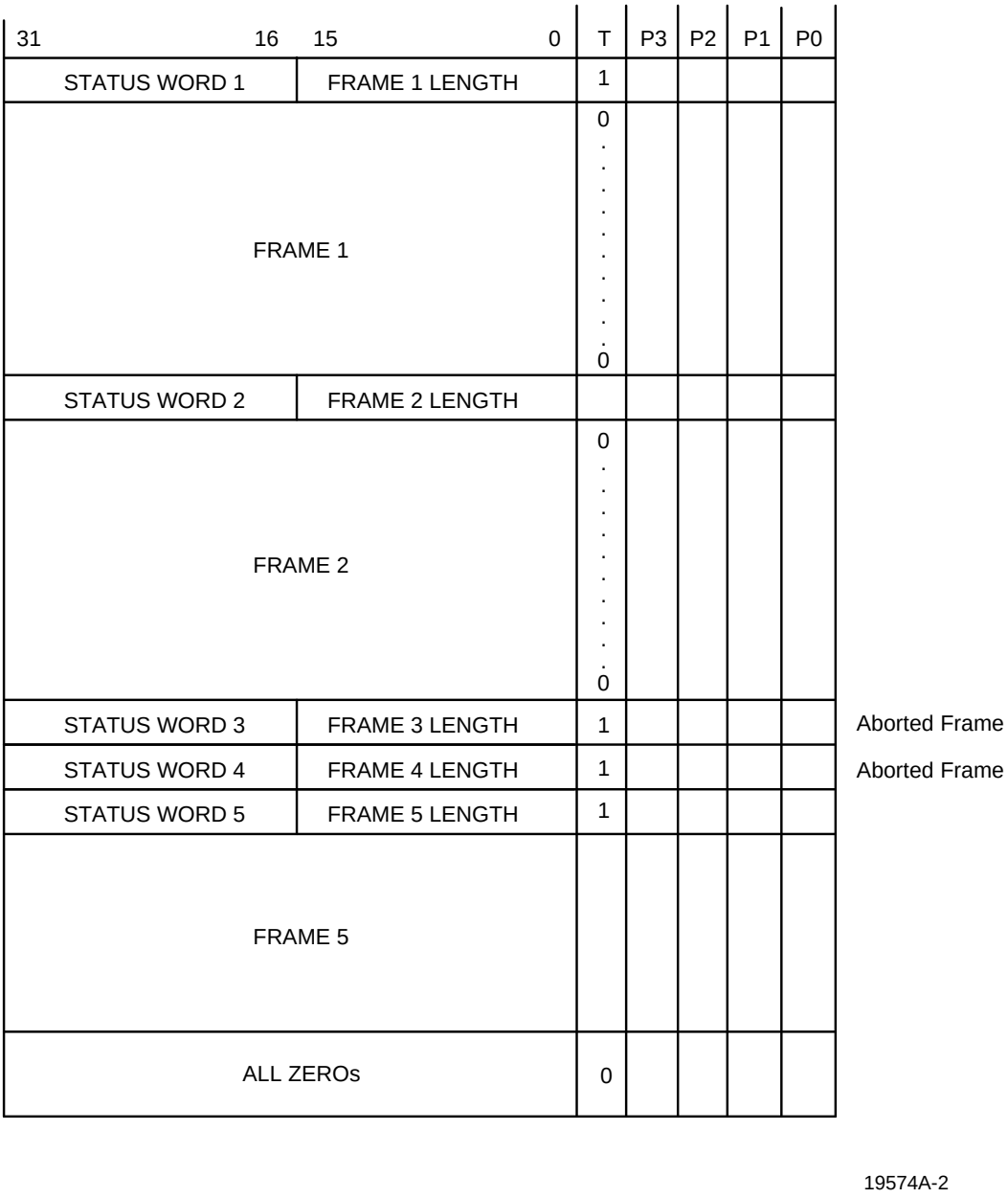


Figure 1. Memory Receive Queue (Modified TAG Mode)

Transmit Command

The SUPERNET 3 provides a feature to control transmission of frames from ASYNC1 queue in both TAG and Modified TAG modes. This feature can be enabled by programming the MENTRCMD (bit 14) in mode register 3 (MDREG3). This feature, when enabled, would wait for the "Transmit Asynchronous Queue1" command. This feature would be applicable only to ASYNC1 queue. The SUPERNET 3 has to be in initialize mode to enable the transmit command feature. Once this is enabled the SUPERNET 3 will not transmit from ASYNC1 queue unless a command in given by the Node Processor. To disable this feature, the SUPERNET 3 has to be in initialize or memory active mode. The read pointer (RPXA1), write pointer (WPXA1) and shadow write pointer (SWPXA1) are under the control of the user. The frames to be transmitted could be loaded by the host into the buffer memory either by using the host request pins, or by using NPDMA pins or by using the MARW and MDR registers.

When using the host request pins, the SUPERNET 3 responds to the host request as in any mode, except that the transmit threshold register value would be ignored. IFPC would not monitor the frames being loaded into buffer memory for memory full condition, buffer empty condition etc. After the last data word and descriptor are written to complete the frame, transmit command can be issued to start transmission.

When NPMEMRQ pin is used by the NP the address bus and memory control signal lines are placed in the high-impedance state by the SUPERNET 3. This gives the NP free access to load the buffer memory, however, the frames must conform to the format defined. The NP is also responsible in keeping track of Async 1 pointers (WPXA1, RPXA1, LTDPA1) prior to issuing the transmit command.

When the NP uses the MARW and MDR to load the buffer memory, it first loads the MARW with the starting address of the frame. Then the MDRU is loaded from the NP, followed by the MDRL. As soon as the second 16-bit data word is loaded, SUPERNET 3 sets an internal request to move the contents of the MDR to the buffer memory. The MARW is incremented after the write operation is completed. The NP could use the set tag command in CMDREG2 to set the tag bit for the MDR write cycle, however, the tag bit command is valid for one NP write operation only.

After the complete frame(s) have been loaded for transmission, the NP has to program the last transmit descriptor pointer (LTDPA1) to be equal to the address of the last descriptor written. Also, the ASYNC1 queue (WPXA1) write pointer needs to be programmed to LTDPA1 + 1. The SUPERNET 3 would assume that the read pointer is at the correct address. The NP should then give an instruction to SUPERNET 3 to transmit the ASYNC1 queue. The SUPERNET 3 would transmit till the read pointer (RPXA1) equals the last transmit descriptor pointer (LTDPA1). The user could load multiple frames before issuing the command. The NP cannot issue more than one transmit command until the SUPERNET 3 indicates the "End of transmit command" status (STECMDA1) in status register 1 - upper (ST1U).

TDAT Loopback

The SUPERNET 3 provides a feature to control the loopback of transmit datapath after the PLC (TDAT) back to the receive data path of the PLC (RDAT). This loopback path is enabled when MDREG3, bit 15 (MENTDLPBK) bit is set to logic "1".

Mode Register 3 (MDREG3)

An additional 16-bit mode register 3 is provided. The new features and modifications are enabled by the setting of the bits in the MDREG3. By default, the register bits are reset to zero. This register can only be written when the SUPERNET 3 is in Initialize or Memory Active modes.

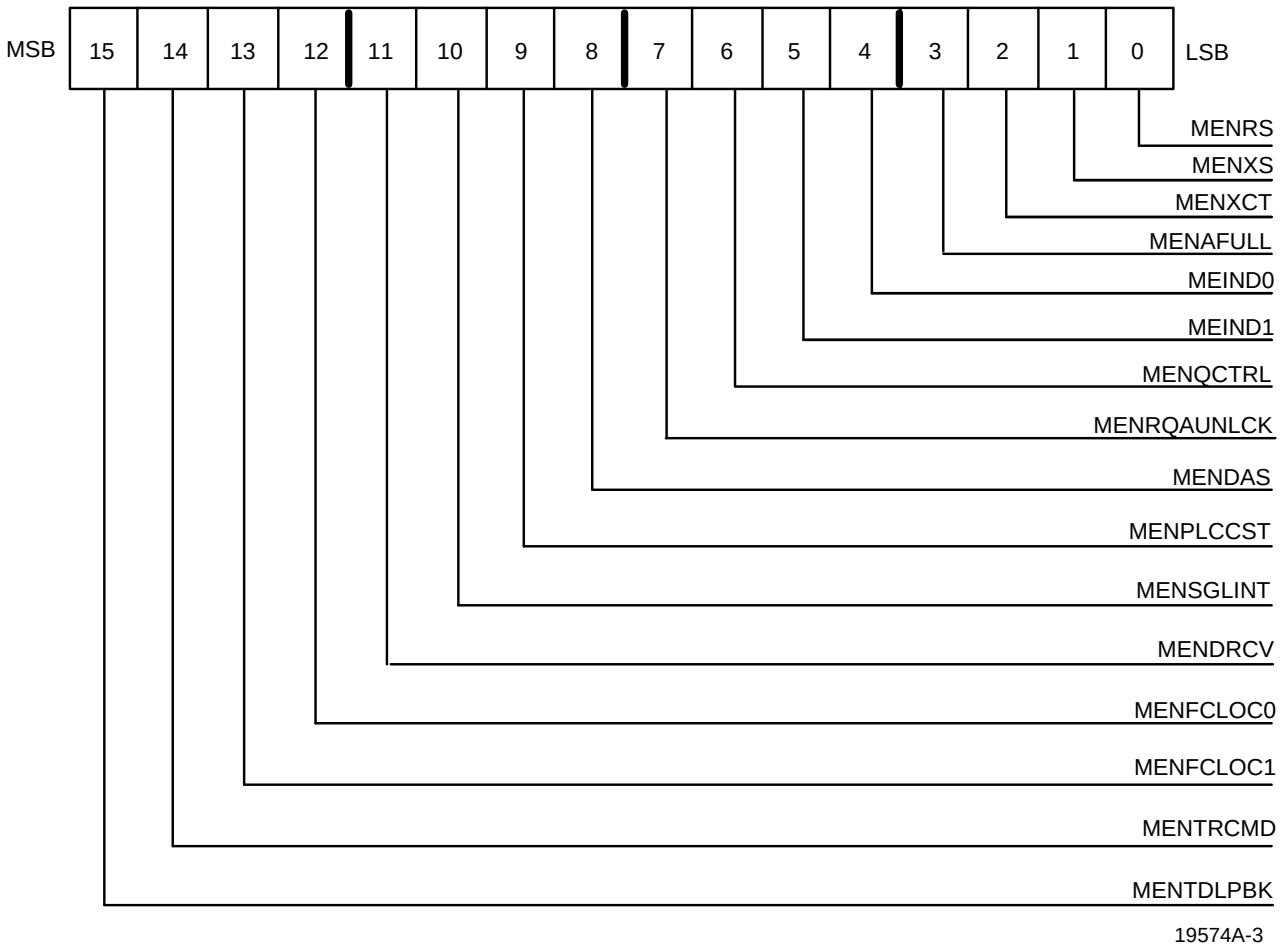


Figure 2. Register 3 (MDREG3) (NPADDR = 60h)

Bit	Description
MENRS (bit 0)	Enable enhanced Receive status encoding.
MENXS (bit 1)	Enable enhanced Transmit status encoding.
MENXCT (bit 2)	Enable EXACT/INEXACT matching.
MENAFULL (bit 3)	Enable enhanced QCTRL encoding for AFULL.
MEIND0, MEIND1 (bits 4, 5)	Enables enhanced A, C indicator setting.
MENQCTRL (bit 6)	Enables enhanced QCTRL encoding.
MENRQAUNLCK (bit 7)	Enable Receive Queue Auto Unlock.
MENDAS (bit 8)*	Enables DAS connections by controlling the MUX.
MENPLCCST (bit 9)	Enables Counter Segmentation Test in PLC block
MENSGLINT (bit 10)	Enables Vectored Interrupt reading. The MINTR4 is used as the Vectored Interrupt.
MENDRCV (bit 11)	Enables dual receive queue operation.
MENFCLOC (bit12,13)	Enables the FC location within the frame data long word.
MENTRCMD (bit 14)	Enables the ASYNC1 queue to transmit only after the command is issued.
MENTDLPBK (bit 15)	Enable TDAT to RDAT loopback

** This bit should only be set if the external PHY is available for a DAS configuration.*

Address Space

The FORMAC Plus uses seven pins (0–6) and the PLC uses five pins (0–4). The new address space uses eight pins (0–7) with the following decoding:

Address 7:0	Comment
00–7F	MAC addresses. Up to 128 addresses can be accessed. Currently 127 addresses are used. Full backward compatibility
80–AF	PHY addresses. Currently the PLC has 28 registers defined. This would allow up to 48 addresses to be accessed
B0–CF	Address Filter (AF) addresses. Note that the AF currently has ten addresses all of which are read /written by the user
D0–DF	PDX address space. There are 16 possible addresses.
E0–FF	Reserved for future use

Interrupts

There are four interrupts: two for the MAC, one for the MAC/BIST, and one for the PHY. The two interrupts for the MAC ensure that the interrupt service routine (ISR) does not have to perform two reads to determine which of the status registers generated the interrupt. The third interrupt is generated when the BIST operations are complete or when the second receive queue has changes in its status. The fourth interrupt indicates the status of the PHY.

Interrupt Mechanisms

SCALAR: There are four interrupts, two from MAC, one from MAC and BIST, and one from PHY. These interrupts can be tied together externally or serviced separately. This method is the default and is backwards compatible with the SUPERNET 2 interrupt generation and servicing mechanisms.

VECTORED: Only one interrupt is monitored (MINTR4), and upon an interrupt being generated, a 16-bit maskable Interrupt Vector Register (IVR) is read. Each bit in the vector register indicates the source of the interrupt. The vector register bits are:

Bits	Interrupt Source
bit 0	MAC Status register 1 Upper (ST1U)
bit 1	MAC Status register 1 Lower (ST1L)
bit 2	MAC Status register 2 Upper (ST2U)
bit 3	MAC Status register 2 Lower (ST2L)
bit 4	MAC Status register 3 Upper (ST3U)
bit 5	MAC Status register 3 Lower (ST3L)
bit 6	PHY Interrupt Event register (INTR_EVENT)
bit 7–15	Reserved. Shall be read as zero.

This method of interrupt generation and processing can be enabled by setting the MENSGLINT (bit 10) in the mode register 3 (MDREG3). If enabled, this mechanism requires the user to read the Interrupt Vector Register (IVR), locate the bit which is set, and read the corresponding interrupt event or status register. Each bit in the IVR is maskable. The interrupts can be unmasked by setting the corresponding bit in the Interrupt Mask Register (IMR). By default, all bits in the IMR are reset (to zero) and all interrupts are masked. The mask register bits are:

Bits	Interrupt Source
bit 0	Mask MAC Status register 1 Upper (ST1U) interrupt.
bit 1	Mask MAC Status register 1 Lower (ST1L) interrupt.
bit 2	Mask MAC Status register 2 Upper (ST2U) interrupt.
bit 3	Mask MAC Status register 2 Lower (ST2L) interrupt.
bit 4	Mask MAC Status register 3 Upper (ST3U) interrupt
bit 5	Mask MAC Status register 3 Lower (ST3L) interrupt.
bit 6	PHY Interrupt Event register (INTR_EVENT) interrupt.
bit 7–15	Reserved. Shall be read as zero.

Once MINTR4 is activated, the corresponding status or event register must be read to enable any further interrupt on MINTR4.

Receive Flush/Transmit Inhibit pin FLXI (input)

The HOFLXI pin is now the FLXI pin and the HOLD function is no longer supported. The functional timing for this pin is as specified in the SUPERNET 2 data book.

If the FLUSH function is selected and the pin is asserted by external logic, then the incoming frame is flushed. The buffer memory pointers are not advanced from where they were before the frame was received (i.e. WPR = SWPR). The receive flush pin is asserted by the host to flush the current frame being received based on an external criterion regardless of the address match. This prevents unwanted frames and fragments from occupying receive buffer space and taking up the buffer memory bus bandwidth. If receive threshold is non-zero, then the frame will be flushed only if the pin is asserted before the threshold is crossed. Refer to timing diagram for details.

If the TRANSMIT INHIBIT function is selected and the pin is asserted by external logic, then the SUPERNET 3 completes transmitting the current frame

(if transmitting), releases the token, and no further transmissions can occur until the pin is deasserted. During the time that the TRANSMIT INHIBIT function is enabled the network timers and state machines operate normally.

As a result of the change to the FLXI pin, which of the two functions is selected depends upon the state of FLXI bits, as follows:

FLXI Pin	FLXI1	FLXI0	Function Implemented
0	0	0	Normal Operation
1	0	0	Normal Operation
0	0	1	Normal Operation
1	0	1	FLUSH received frame
0	1	0	Normal Operation
1	1	0	INHIBIT transmission
0	1	1	Reserved
1	1	1	Reserved

Upon reset, the FLXI1:0 bits would read all zeros.

Single Frame Receive Mode

The Single Frame Receive Mode function has been removed from the SUPERNET 3. All associated status, modes and commands are deleted and replaced with reserved. This causes the following changes:

1. Status Register 2 Upper:
   The 'Receive Frame' (SRCVFRM) bit 10 and 'Receive Frame Counter Overflow' (SRFRCTOV) bit 9 are now reserved and return a value of zero when read.
2. Command Register 2:
   The 'Enable Receive Single Frame' command (0x40) is no longer a valid command. This is now reserved.
3. Mode Register 1:
   The 'Single-Frame Receive Mode' bit [15] is no longer valid. It is now a reserved bit and shall return a value of zero when read.

Receive Queue Operation

SUPERNET 3 provides a new feature where the user can configure the buffer memory for incoming valid frame into two separate receive queues. The type of frames that each queue would receive is selected in a separate register, the Frame Selection Register (FRSELREG). To enable two receive queues operation, MENDRCV bit in Mode Register 3 (MDREG3) needs to be set. If this bit is cleared, which is the case at the time of reset, then SUPERNET 3 behaves like F+ (i.e only one receive queue is supported, and SUPERNET 3 defaults to Receive Queue 1). If MDREG3 bit 11, MENDRCV and both RECVX3:0 in Frame Selection Register (FRSELREG) is programmed to be "0000" then the SUPERNET 3 would behave like FORMAC+ and the second queue is ignored. However, if one of the RECVX3:0 bits in FRSELREG are programmed to be "0000" then the corresponding queue would receive all frames except the frame type selected for the other queue. Only the second receive queue (i.e. RECV2) can be programmed to be "0000". Programming the RECV1 bits in the Frame Selection Register (FRSELREG) with "0000" and RECV2 bits with a non-zero selection, will result in no data being written in the RECV1 queue. Only the frame type selected by RECV2 bits will be received in the second queue.

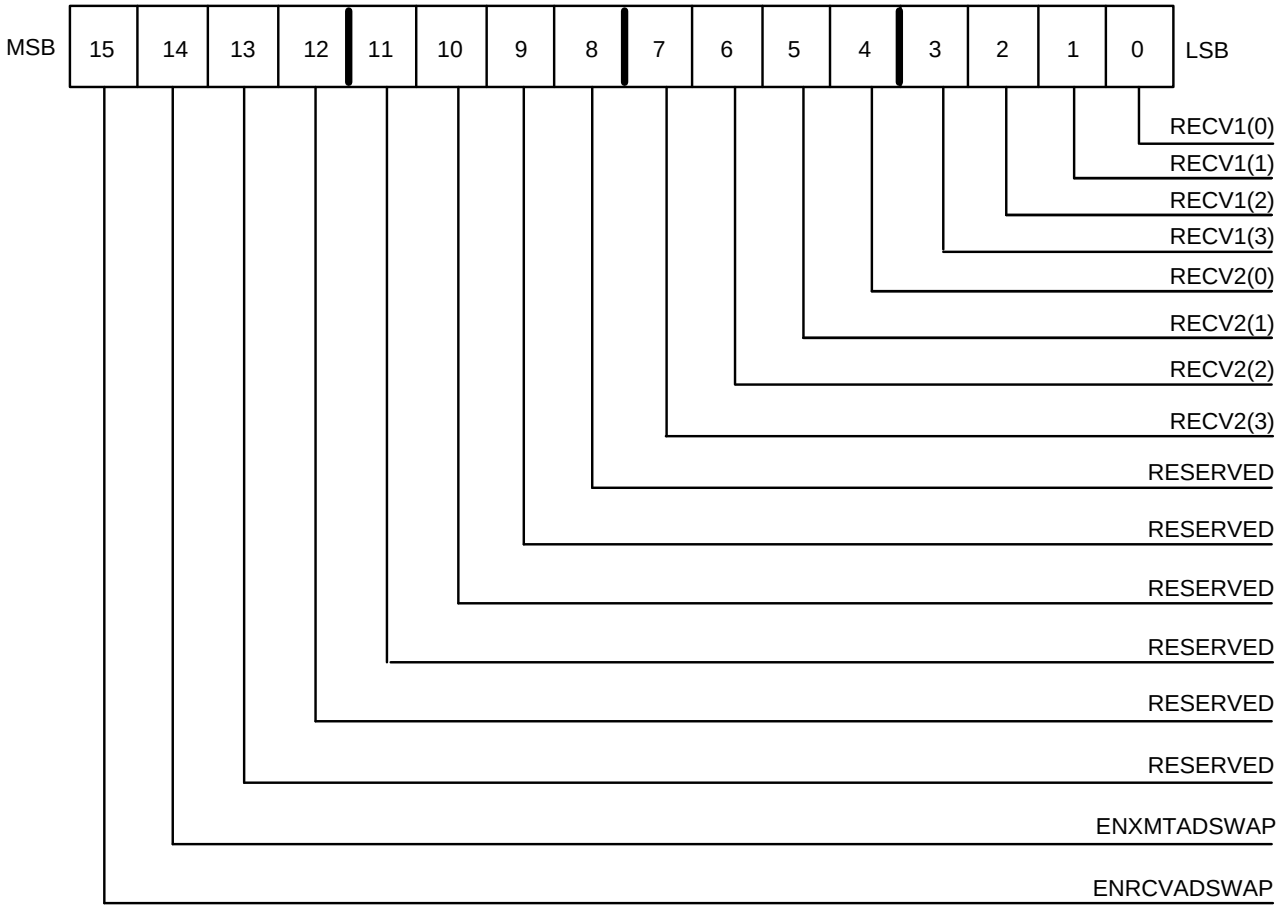


Figure 3. Frame Selection Register (FRSELREG) 19574A-4

Options for selecting frame types under two receive queues operation is as follows:

RECVX3:0	Frame Type
0000	Receive all frames except the frame type selected for other queue. RECV1[3:0] bits cannot be programmed as “0000” when RECV2[3:0] bits are non-zero.
0001	LLC (includes both Sync. & Async. LLC frames)
0010	SMT
0011	Non-SMT (includes all non-SMT frames except MAC & Void, MAC & Void frames are received if Promiscuous mode is selected in MDREG1)
0100	Implementor
0101	MAC
0110	Sync. LLC
0111	Async. LLC
1000	Void
1001	Async. LLC & SMT
1010–1111	Reserved

The above selection of frames for each queue is made by programming appropriate bits in the Frame Selection register (FRSELREG) and is applicable to only those frames that meet the criteria for copying as defined by ADDET2–0 bits of Mode Register 1 (MDREG1) of SUPERNET 3. The following restrictions apply to frame selection:

1. The same selection is not allowed for both queues. Programming the Frame Selection register with the same selection in both the RECVx3:0 bits would result in SUPERNET 3 operating as a single receive queue mode, and would default to Receive Queue 1. This overrides the MENDRCV bit in the Mode Register 3 (MDREG3).
2. If high level selection option is used for a given frame type, then sub-level selection for the same frame type is not allowed [i.e. If LLC (0001) option is selected for one queue, then Sync. LLC (0110) or Async. LLC (0111) or Async. LLC & SMT options are not allowed for the second queue]. If a selection is made where one frame type is a sub-set of the other frame type, the selection made for RECV1 queue supersedes the selection for RECV2 queue.

The two receive queues will have independent receive FIFO's. There will be two instructions to clear locks on the two receive queues.

"Clear Receive Queue Lock" (instruction code 20h) will be for RECV1 and the new instruction" Clear Receive2 Queue Lock "(instruction code 21h) will be for RECV2 queue.

"Clear All Queue Locks" command would clear locks on all queues. Clearing the queues would enable further transfer of data received from the corresponding receive FIFO. The received data present in the buffer memory for each queue is indicated by the corresponding RDATA pin. RECV1 data is indicated by RDATA1 and RECV2 data is indicated by RDATA2. If the two receive queue feature is not selected, RDATA1 would indicate received data present in buffer memory. Read requests will not be acknowledged when RDATA pins are inactive. The status bits SRCOMP, SRBMT, SRABT, SRBFL, SRCVOVR of status register 2 upper ST2U (bit 15–11) would be for RECV1 queue. The status bits SRCOMP2, SRBMT2, SRABT2, SRBFL2, SRCVOVR2 of status register 3 upper ST3U (bit 15–11) would be for RECV2 queue. The host interface to read the data received in the second receive queue would use HSREQ2–0 lines and the encoding would be HSREQ[2:0] =001.

Address Bit Swapping

The SUPERNET 3 provides the necessary logic for swapping the address fields within each frame between FDDI and IEEE Canonical bit order. This involves a bit reversal within each byte of the address field. This feature is user selectable for transmit, receive or both, however, once selected the bit swapping applies to all queues. This is an useful feature for bridging Ethernet to FDDI or for other higher level protocols. Bit 15 of the FRSELREG, ENRCVADSWAP, enables the bit swap on the receive queues. The FC field of the received frame would decide whether the frame has long address or short address. Bit 14 of FRSELREG, ENXMTADSWAP, enables the bit swap of the transmit queues. The FC field of the frame to be transmitted will decide whether the frame to be transmitted has long address or short address. The CRC written into the buffer memory will be the same as received. This logic will not re-generate CRC after bit swapping on the receive queues. The user can set MDREG2 bit 14, STRPFCS, to strip receive FCS and prevent FCS being copied into the buffer memory. On the transmit side, the address bits are swapped before the CRC generator, and therefore, the transmitted CRC will be correct for the bit swapped address.

Auto-Unlocking of Receive Queues

The buffer memory receive queue is locked out for any further input when the receive buffer is full (RPRx = WPRx after an increment of WPRx). The lock can be cleared using the node processor commands "clear receive queue lock (20h)" or "clear all queue locks (3Fh)". Once the lock has been cleared, the receive buffer is available for further input. However, the node processor has to clear the lock by using the CMDREG1 to enable reception of frames in the receive buffer. The SUPERNET 3 provides an enhancement feature to allow automatic unlocking of the receive queue based on user-programmable host read count threshold. To enable this feature, MENRQAUNLCK bit in Mode Register 3 (MDREG3) needs to be set. If this bit is cleared, which is the case at the time of reset, the SUPERNET 3 behaves like FORMAC+ (i.e Upon buffer full condition the receive queue is locked for further input and needs a node processor command to clear the lock).

If MENRQAUNLCK is enabled, the UNLCKDLY register needs to be programmed with a 8 bit threshold value for each receive queue. Upon receive buffer full condition, the UNLCKDLY value times 4 will be loaded into a counter. The counter will count down for every corresponding host read receive acknowledge. After the number of host read receive acknowledges exceeds the user programmable count (UNLCKDLY) times 4, the SUPERNET 3 would start receiving frames into the corresponding receive buffer queue The SRBFLx bit in ST2U and ST3U would indicate the status of the corresponding receive buffer queue. If this bit is set it indicates that the corresponding receive buffer queue is locked. If the MENRQAUNLCK bit is set in MDREG3 this bit will be auto-cleared after the user programmed delay or on receive buffer empty, otherwise, the node processor has to clear the lock by issuing a command. The auto-unlock will not work if host interface is not used to read the receive queue and the lock can be cleared only by the node processor. This feature can be enabled/disabled in memory active or initialization mode only. Once enabled/disabled the feature applies to both the receive queues (if selected using MENDRCV in MDREG3).

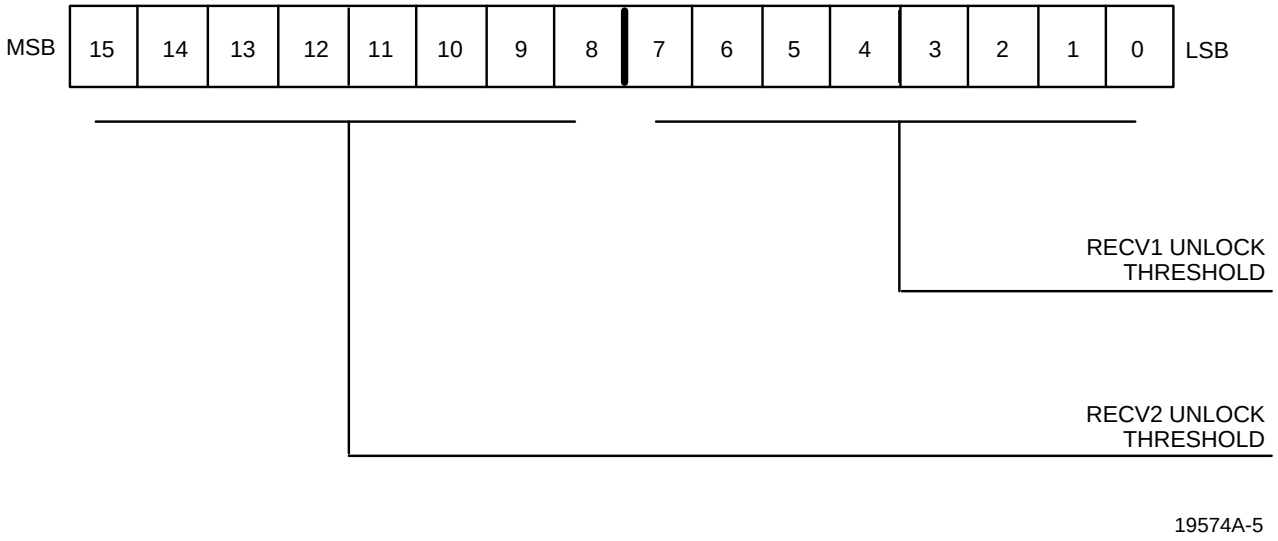


Figure 4. Delay Register (UNLCKDLY)

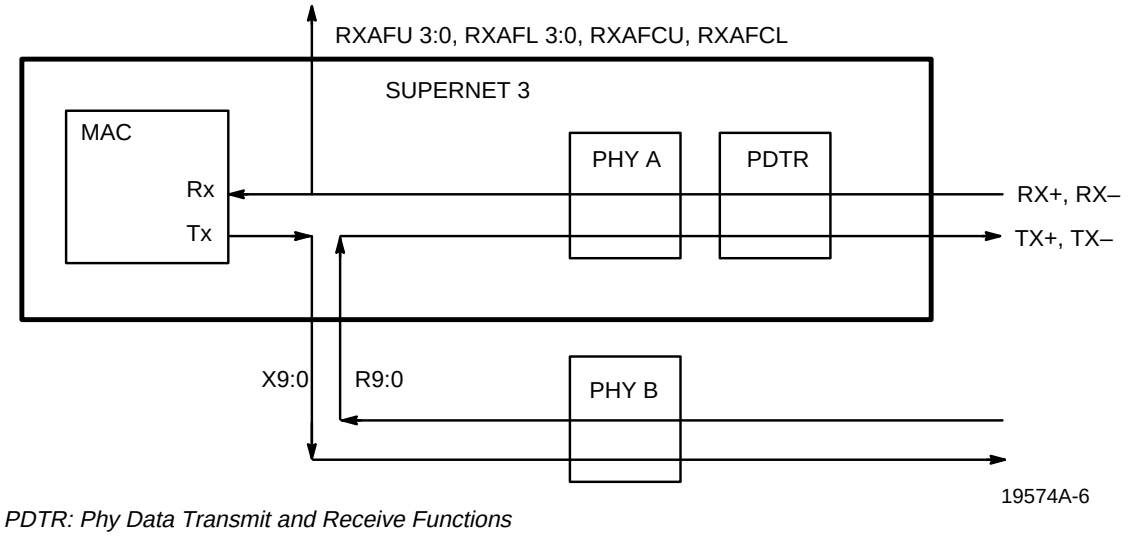
Symbol Control

The SUPERNET 3 no longer supports the ability to transmit raw symbols from the Buffer Memory to the PHY. This feature has been removed and the mode bit SYMCTL (bit 5, MDREG2) is now reserved and read as zero.

Dual Attachment Station (DAS) support

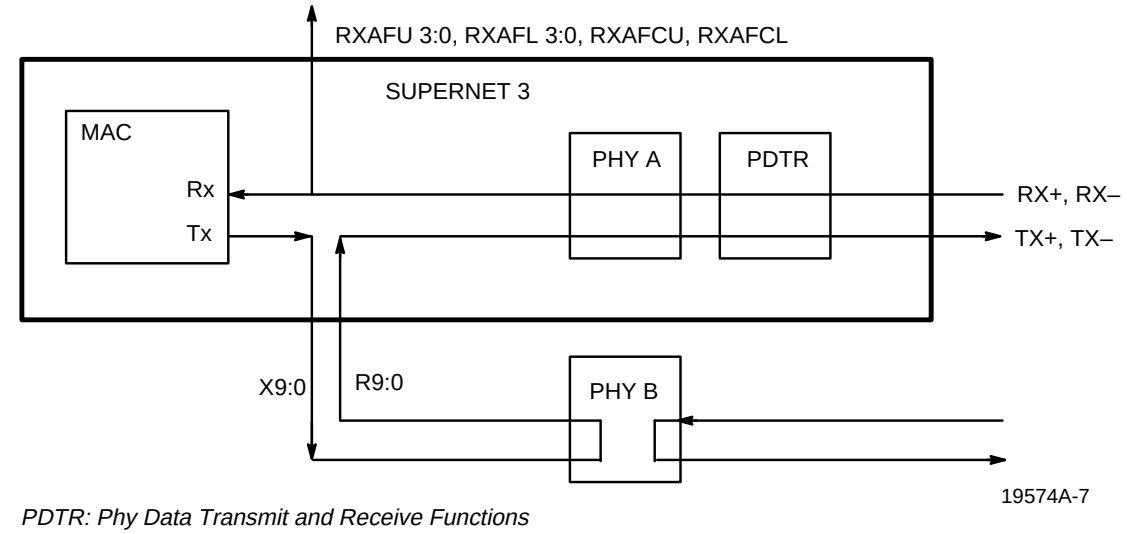
The SUPERNET 3 is a SAS only device which is extensible to a DAS configuration. For a DAS implementation, the MENDAS bit of the MDREG3 must be set and the external PHY must be present. In a SAS configuration, the R9:0 lines are tied to ground and X9:0 lines are driven at all times. The following configurations are supported:

CFM State	Figure	Description
Thru_A	Figure 5	The internal PHY is the A-port and the external PHY is the B-port. The MAC is placed as shown in the figure. The MENDAS bit in the MDREG3 must be set.
Wrap_A	Figure 6	The internal PHY is the A-port and the external PHY is the B-port which must be in BYPASS (if PLC). The MAC is placed as shown in the figure. The MENDAS bit in the MDREG3 must be set.
Wrap_B	Figure 7	The internal PHY is the A-port which must be in BYPASS and the external PHY is the B-port. The MAC is placed as shown in the figure. The MENDAS bit in the MDREG3 must be set.
Wrap_S	Figure 8	This is the default configuration of the SUPERNET 3. No external PHY is required. The MENDAS bit in the MDREG3 must be reset (by default). This decouples the busses from the external PHY as shown in the figure.
Isolated		The internal PHY (A-port) and the external PHY (B-port) are isolated. This is the default reset state.
Thru_B		This configuration is not supported.



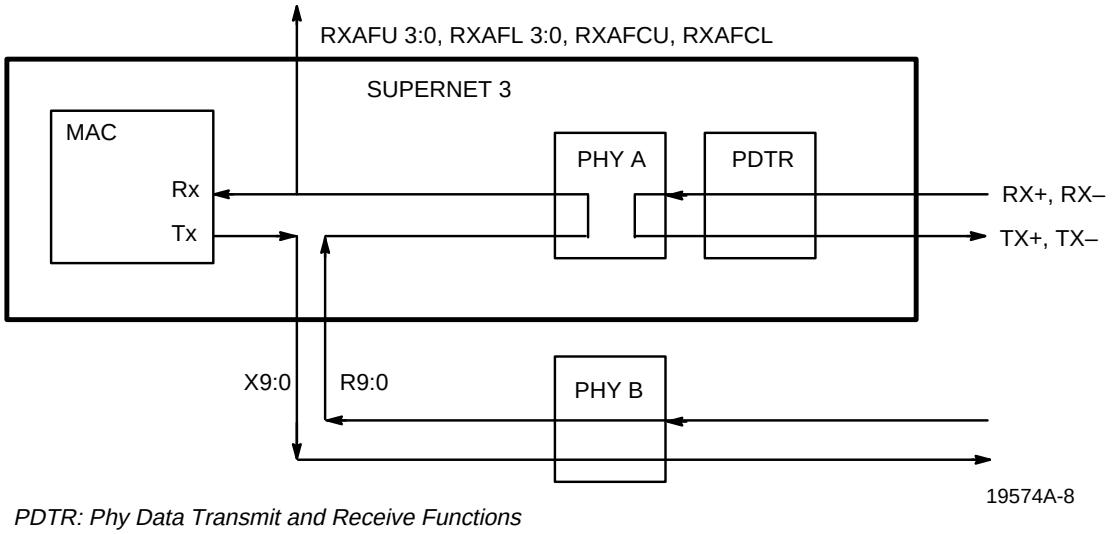
PDTR: Phy Data Transmit and Receive Functions

Figure 5. THRU_A Configuration



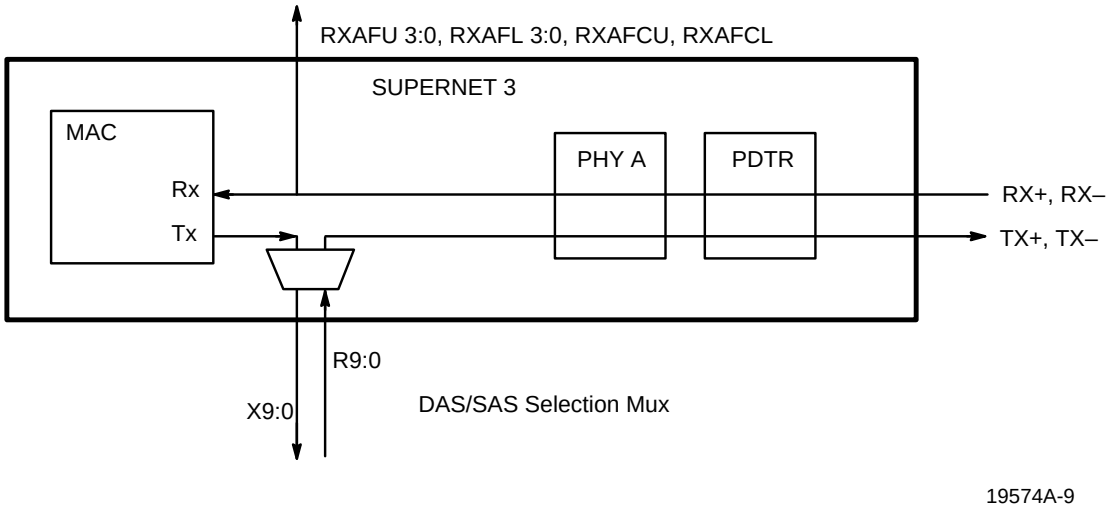
PDTR: Phy Data Transmit and Receive Functions

Figure 6. WRAP_A Configuration



PDTR: Phy Data Transmit and Receive Functions

Figure 7. WRAP_B Configuration



PDTR: Phy Data Transmit and Receive Functions

Figure 8. WRAP_S or SAS Configuration

Changes and Enhancements to PHY

Changes from SUPERNET 2 PLC

Addition of Scrambler/Descrambler

Scrambler/descrambler is implemented. Scrambling/descrambling can be disabled either through a pin or through bit 0 in the PLC_CNTRL_C register.

ENCOFF pin function changed

The function of this pin has changed slightly. In addition to turning off the Encoder (as in SUPERNET 2 PLC), this pin, when asserted, now also turns off the Decoder.

BIST enhanced

The Built-In Self Test (BIST) test now covers part of the Elasticity Buffer and Framer logic.

Revision Identification

In SUPERNET 3 PHY, bits 15:11 of the PLC_STATUS_A register will indicate 01111 on a read operation. The Revision ID for SUPERNET 2 PLC-S is 11111.

Addition of Scrambler/Descrambler Function to Support Copper PMD

This is a description of the Stream-Cipher Scrambler and Descrambler as implemented in the physical layer controller block.

The Stream-Cipher Scrambler adds the output of a random generator to the data stream. The purpose is to spread the spectrum and reduce frequency peaks. As a result, higher signal amplitudes can be transmitted over copper that meet the requirements of the FCC and other regulatory agencies.

The random generator is the polynomial $2^{11} + 2^9$. The SUPERNET 3 implementation uses a 5-bit parallel technique. The 5-bit output of the random generator is exclusive-ORed with the input to produce scrambled data for transmission.

The descrambler has a random generator which is identical to the random generator in the scrambler. The output of this generator is used to decipher the received scrambled data using the same exclusive-OR function. Since both random generators are identical, the output of the receiver random generator is the original data (data XOR Random → XOR Random = data).

This process is open loop in nature, i.e., the data has no effect on the states of the random generators. Therefore, the descrambler must incorporate synchronization circuitry to preset its state to the same state as the scrambler. Once both random generators start from the same state, they will remain in synchronization.

The synchronization circuitry, CREG and HREG registers, are designed to take advantage of the scrambled FDDI line states. During the line states (HLS, QLS, MLS and ILS), CREG and HREG generate known patterns. When the synchronization circuitry detects these patterns, it generates a capture signal and the corresponding output data pattern.

CAPTURE controls the random generator. When it is false, the random generator operates open loop. When it is true, the random generator is preset to the deduced output data exclusive-ORed with the input scrambled data. This is equal to the state of the scrambler's random generator.

FDDI Line States & Detected Signals

Line State	Data Bits	Detected Bits
HLS	00010000100	00111001110
QLS	00000000000	00000000000
MLS	00000000100	00000001110
ILS	11111111111	11111111111

CAPTURE is enabled by SAMPLE, which is enabled by SCRM_RESYNC. SCRM_RESYNC is active when PHY line state is not Active Line State, or Unknown Line State. A false SCRM_RESYNC indicates that the decoded data is correct. Therefore the random generator is synchronized and SAMPLE is set false. SAMPLE is set true when SCRM_RESYNC is true except during the following condition:

If two consecutive IDLE bytes and then non-idle bytes are detected when SCRM_RESYNC is true, SAMPLE goes false and stays false for 32 RSCLK cycles. After that the state of SAMPLE depends on SCRM_RESYNC.

Testability

The Test Access Port (TAP)

An IEEE 1149.1 boundary-scan architecture is provided for board level testing and diagnostics. All pins are part of the boundary-scan ring except Digital Transmitter/Receiver pseudo-analog (PECL) pins. The TAP consists of five pins, TCK, TMS, TDI, TDO and $\overline{\text{TRST}}$. These pins are dedicated connections and may not be used for any other purpose. The boundary-scan architecture includes a TAP controller, an instruction register and instruction decode logic, and a test data register array.

The functional description of the TAP that follows is not a complete description of the IEEE boundary-scan architecture. Additional information and a more detailed functional description can be found in the standard document (IEEE Std 1149.1–1990). The description provided here covers the specifics of this particular implementation.

TAP Controller

The TAP controller is a synchronous 16-state finite state machine which is driven by the TCK and TMS pins. All state transitions of the TAP controller occur at the rising edge of TCK. The transitions are based on the value of TMS at the rising edge of TCK. In the Test-Logic-Reset state the instruction register is initialized with the IDCODE instruction. The TAP controller is forced to the Test-Logic-Reset state whenever a logic 0 is placed on the $\overline{\text{TRST}}$ pin. A system reset has no effect on the TAP controller.

Instructions Supported

This section describes the public and private instructions that are supported in this implementation. The instruction register is a 4-bit register. The least significant bit of the instruction register is the bit nearest the TDO output. The encoding of the instructions is as follows:

Instruction	Description	Reg. Selected	INST[3:0]
EXTEST	External test	B.S.R.	0000
IDCODE	Device identification	IDREG	0001
SAMPLE	Sample/preload B.S.R.	B.S.R.	0010
TRI_ST	Force outputs to Hi-Z	Bypass	0011
RUNBIST	Self-test	BIST Execution	0101
SCANBIST	Manufacturing Testing	Scan Results	0110
BYPASS	Bypass register scan	Bypass	1111

EXTEST Instruction

The EXTEST instruction is used to test board level interconnect and for testing of circuitry external to SUPERNET 3. This instruction selects the Boundary Scan register (BSR) for scanning between TDI and TDO when in the Shift-DR controller state. During execution:

1. SUPERNET 3 outputs are driven from the Parallel Data register (PDR).
2. SUPERNET 3 internal outputs are sampled into the BSR.
3. SUPERNET 3 inputs are sampled into the BSR.
4. SUPERNET 3 internal inputs are driven from the Parallel Data register (PDR).

IDCODE Instruction

The IDCODE instruction is provided for access to the manufacturer's identity, the part number, and the version of the SUPERNET 3. This instruction selects the 32-bit identification register for scanning between TDI and TDO in the Shift-DR controller state. The IDCODE instruction is forced into the instruction registers parallel output latches during the Test-Logic-Reset controller state. The 32 bits of the identification register are broken down as follows:

Bits	Description
IDREG[31:28]	Version number (initially 0001)
IDREG[27:12]	Part number - 2870 (Hex)
IDREG[11:1]	Manufacturer's ID. The 11-bit manufacturer's ID. for AMD is 00000000001 according to JEDEC publication 106-A.
IDREG[0]	Always set to logic 1.
IDREG[31:0]	Value = 1287 0003 (Hex)

SAMPLE Instruction

The SAMPLE/PRELOAD instruction is used to observe the normal operation of the SUPERNET 3 without affecting system operation. It is also used to load values into the PDR prior to the selection of another instruction. This instruction selects the BSR for scanning between TDI and TDO during the Shift-DR controller state. During execution:

1. SUPERNET 3 outputs are driven by the SUPERNET 3.
2. SUPERNET 3 internal outputs are sampled into the BSR.
3. SUPERNET 3 inputs are sampled into the BSR.
4. SUPERNET 3 internal inputs are driven from the SUPERNET 3 inputs.

TRI_ST Instruction

The TRI_ST instruction is provided for easy tri-state of all SUPERNET 3 outputs. This instruction selects the bypass register for scanning between TDI and TDO during the Shift-DR controller state.

RUNBIST Instruction

The RUNBIST instruction is provided for self-test of the SUPERNET 3. This instruction must not be selected during the normal operation of the part.

Once the RUNBIST instruction is selected, the BIST operation is enabled by applying a minimum of 65000 TCK clock cycles while in the RUN-TEST/IDLE TAP controller state. Once the minimum number of clock cycles have elapsed, proceed to load the SCANBIST instruction.

SCANBIST Instruction

The SCANBIST instruction selects the BIST result register for scanning between TDI and TDO during the Shift-DR controller state. The BIST results can be

shifted out in the SHIFT_DR TAP controller state. The BIST result register is 33 bits in length.

BYPASS Instruction

The BYPASS instruction is used to bypass the SUPERNET 3 BSR and shorten access times to other devices on a board. This instruction selects the bypass register for scanning between TDI and TDO during the Shift-DR controller state. The SUPERNET 3 is not otherwise affected by this instruction.

Boundary Scan Cells

In boundary scan most of the chip input and output latches are linked together to form a scan chain. The main purpose of this is for board level testing. The boundary scan ring order is listed in the following table.

BSR Cell No.	Pin No.	Pin Type	Description
1	54	input	scrm
2	55	input	encoff
3	56	output	ebferr
4	67	output	$\overline{\text{fotoff}}$
5	68	output	ulsb
6	69	output	lsr[2]
7	70	output	lsr[1]
8	71	output	lsr[0]
9	72	input	rpar
10	73	input	r[0]
11	74	input	r[1]
12	75	input	r[2]
13	77	input	r[3]
14	78	input	r[4]
15	79	input	r[5]
16	80	input	r[6]
17	81	input	r[7]
18	82	input	rcl
19	83	input	rcu
20	84	input	flxi
21	N/A	–	oe control (1 to enable)
22	86	output	xpar
23	87	output	x[0]
24	88	output	x[1]
25	89	output	x[2]
26	90	output	x[3]
27	91	output	x[4]
28	92	output	x[5]
29	93	output	x[6]

BSR Cell No.	Pin No.	Pin Type	Description
30	94	output	x[7]
31	95	output	xcl
32	96	output	xcu
33	98	output	xs[0]
34	99	output	xs[1]
35	100	output	xs[2]
36	101	output	xs[3]
37	102	output	rs[0]
38	103	output	rs[1]
39	106	output	rs[2]
40	107	output	rs[3]
41	108	output	rs[4]
42	109	output	rs[5]
43	111	input	$\overline{\text{xsa\_xact}}$
44	112	input	$\overline{\text{xsamat}}$
45	113	input	$\overline{\text{xda\_xact}}$
46	114	input	$\overline{\text{xdamat}}$
47	116	output	rxafcu
48	N/A	–	oe control (1 to enable)
49, 50	117	inout	rxafl
51	118	output	rxafu[3]
52	120	output	rxafu[2]
53	121	output	rxafu[1]
54	122	output	rxafu[0]
55, 56	123	inout	rxafl[3]
57, 58	124	inout	rxafl[2]
59, 60	125	inout	rxafl[1]
61, 62	126	inout	rxafl[0]
63, 64	128	inout	bdtag
65, 66	129	inout	bdp[0]
67, 68	130	inout	bdp[1]
69, 70	131	inout	bdp[2]
71, 72	133	inout	bdp[3]
73, 74	134	inout	bd[31]
75, 76	135	inout	bd[30]
77, 78	136	inout	bd[29]
79, 80	138	inout	bd[28]
81, 82	139	inout	bd[27]
83, 84	140	inout	bd[26]

BSR Cell No.	Pin No.	Pin Type	Description
85, 86	142	inout	bd[25]
87, 88	143	inout	bd[24]
89, 90	145	inout	bd[23]
91, 92	146	inout	bd[22]
94	147	inout	bd[21]
95, 96	148	inout	bd[20]
97, 98	150	inout	bd[19]
99, 100	151	inout	bd[18]
101, 102	152	inout	bd[17]
103, 104	153	inout	bd[16]
105	154	output	$\overline{\text{cso}}$
106	155	output	$\overline{\text{wr}}$
107	N/A	–	oe control (1 to enable)
108	158	output	$\overline{\text{rd}}$
109, 110	159	inout	bd[15]
111, 112	160	inout	bd[14]
113, 114	161	inout	bd[13]
115, 116	162	inout	bd[12]
117, 118	163	inout	bd[11]
119, 120	164	inout	bd[10]
121, 122	165	inout	bd[9]
123, 124	166	inout	bd[8]
125, 126	168	inout	bd[7]
127, 128	169	inout	bd[6]
129, 130	170	inout	bd[5]
131, 132	171	inout	bd[4]
133, 134	173	inout	bd[3]
135, 136	174	inout	bd[2]
137, 138	175	inout	bd[1]
139, 140	176	inout	bd[0]
141	178	output	rdata2
142	179	output	rdata1
143	180	input	hsreq[2]
144	181	input	hsreq[1]
145	182	input	hsreq[0]
146	183	output	hsack
147	185	output	qctrl[2]
148	186	output	qctrl[1]
149	187	output	qctrl[0]
150	N/A	–	oe control (1 enable)

BSR Cell No.	Pin No.	Pin Type	Description
151	189	output	addr[0]
152	190	output	addr[1]
153	191	output	addr[2]
154	192	output	addr[3]
155	194	output	addr[4]
156	195	output	addr[5]
157	196	output	addr[6]
158	197	output	addr[7]
159	199	output	addr[8]
160	200	output	addr[9]
161	201	output	addr[10]
162	202	output	addr[11]
163	204	output	addr[12]
164	205	output	addr[13]
165	206	output	addr[14]
166	207	output	addr[15]
167, 168	2	inout	np[15]
169, 170	3	inout	np[14]
171, 172	4	inout	np[13]
173, 174	5	inout	np[12]
175, 176	6	inout	np[11]
177, 178	7	inout	np[10]
179, 180	9	inout	np[9]
181, 182	10	inout	np[8]
183, 184	11	inout	np[7]
185, 186	13	inout	np[6]
187, 188	14	inout	np[5]
189, 190	15	inout	np[4]
191, 192	16	inout	np[3]
193, 194	17	inout	np[2]
195, 196	18	inout	np[1]
197, 198	19	inout	np[0]
199	N/A	–	oe control (1 to enable)
200	21	output	mintr1 (oecell -1 to force 0, 0 to disable)
201	22	output	mintr2 (oecell -1 to force 0, 0 to disable)
202	23	output	mintr3 (oecell -1 to force 0, 0 to disable)
203	24	output	mintr4 (oecell -1 to force 0, 0 to disable)
204	25	input	bmclk
205	27	input	bclk
206	29	input	npmemrq

BSR Cell No.	Pin No.	Pin Type	Description
207	30	output	npmemack
208	32	output	$\overline{\text{ready}}$ (oecell –1 to force 0, 0 to disable)
209	33	input	r/$\overline{\text{w}}$
210	34	input	$\overline{\text{ds}}$
211	35	input	$\overline{\text{csi}}$
212	36	input	lsclk
213	37	input	npa[7]
214	38	input	npa[6]
215	39	input	npa[5]
216	40	input	npa[4]
217	41	input	npa[3]
218	42	input	npa[2]
219	43	input	npa[1]
220	44	input	npa[0]
221	45	input	npmode
222	46	input	$\overline{\text{rst}}$

Built-In Self Test (BIST)

The BIST feature of the SUPERNET 3 is provided to ease board and system level testing, as well as our own manufacturing testing. This feature can be accessed through the TAP as well as the system interface. It is expected that board level testing will use the TAP interface, while system level testing will not have access to the TAP interface and will need to run BIST through the system interface.

There are two functional units in the SUPERNET 3 that are tested with BIST. These are the AF CAM core and the enhanced PHY. The BIST testing of the two functional units is available through the node processor interface. See the AF specification for a description of how to run the BIST for the AF. The enhanced PHY BIST is run using the PHY BIST access as described in the SUPERNET 2 PLC data sheet.

Function	BIST Signature (hex)
Internal PLC BIST	5B6B
Address Filter BIST	0553
SCANBIST	1 5B6B 0553

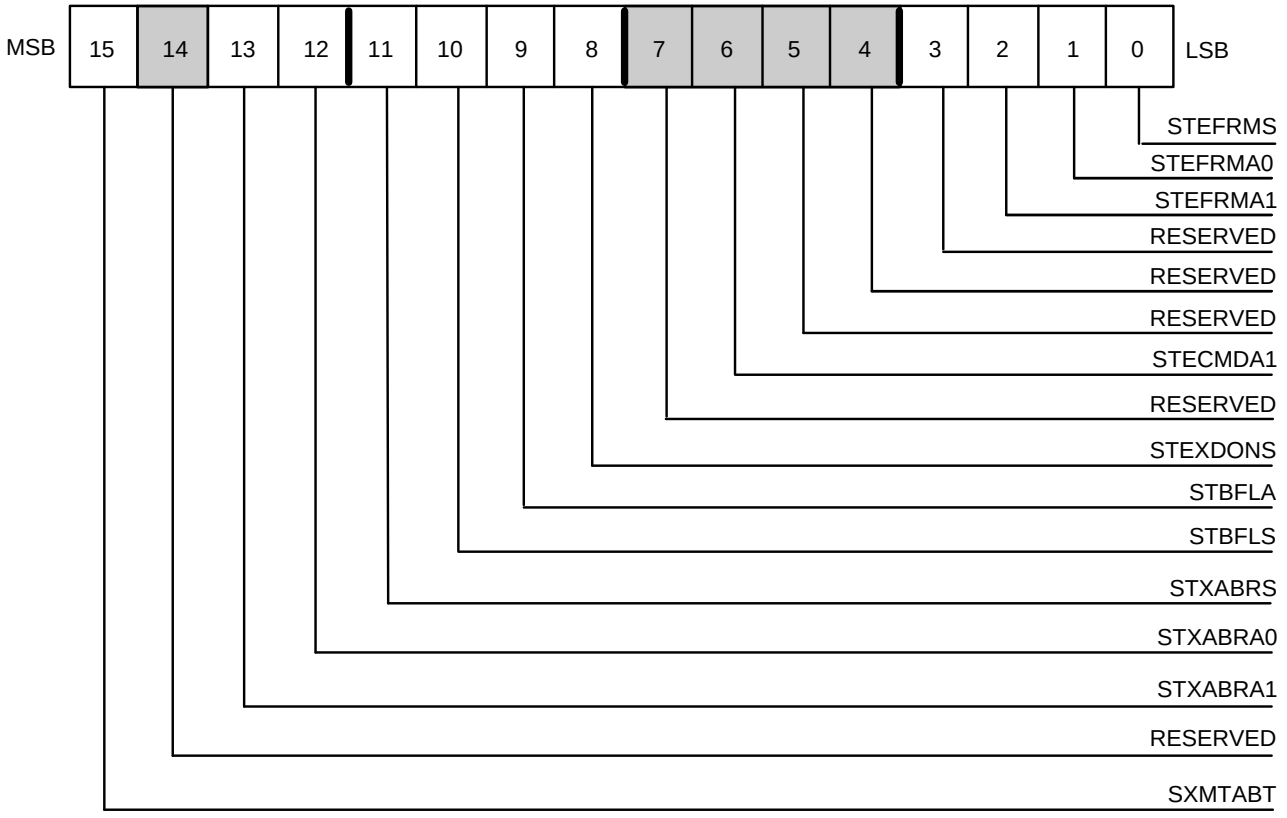
DISCRY function no longer supported

Setting the DISCRY bit in mode register 1 (MDREG1, bit 6) permitted testing the operation of certain internal timers such as TRT, THT, TVX, and TMSYNC by breaking them into smaller segments.

With the enhanced testability features of SUPERNET 3, the DISCRY function is no longer provided. The bit 6 of mode register 1 (MDREG1) is reserved and shall return a value of zero when read.

Summary of Changes to Status and Mode Registers

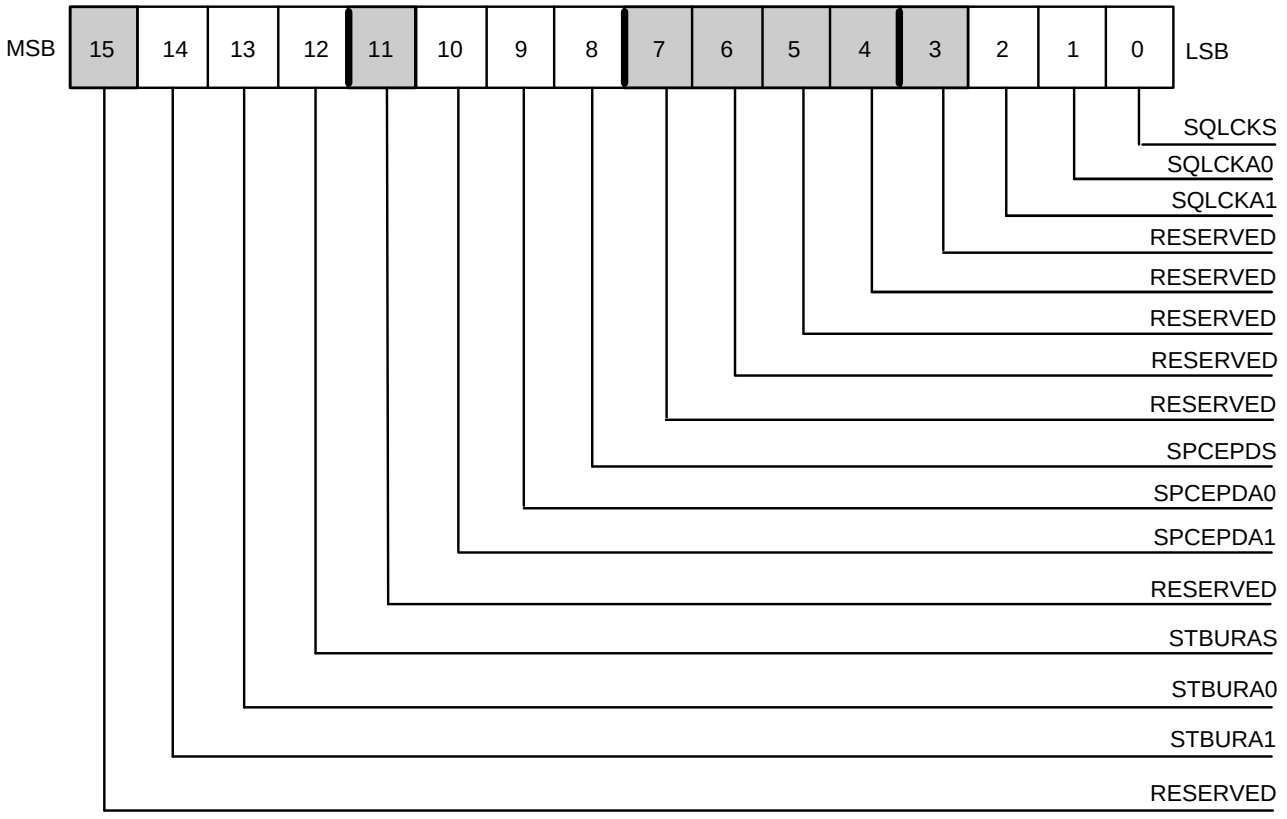
The following is the summary of changes. The bits in the register which are shaded indicate change from SUPERNET 2. All reserved bits shall be read as zero except where noted.



Reserved Bits are Read as Zero Unless Otherwise Stated.

19574A-10

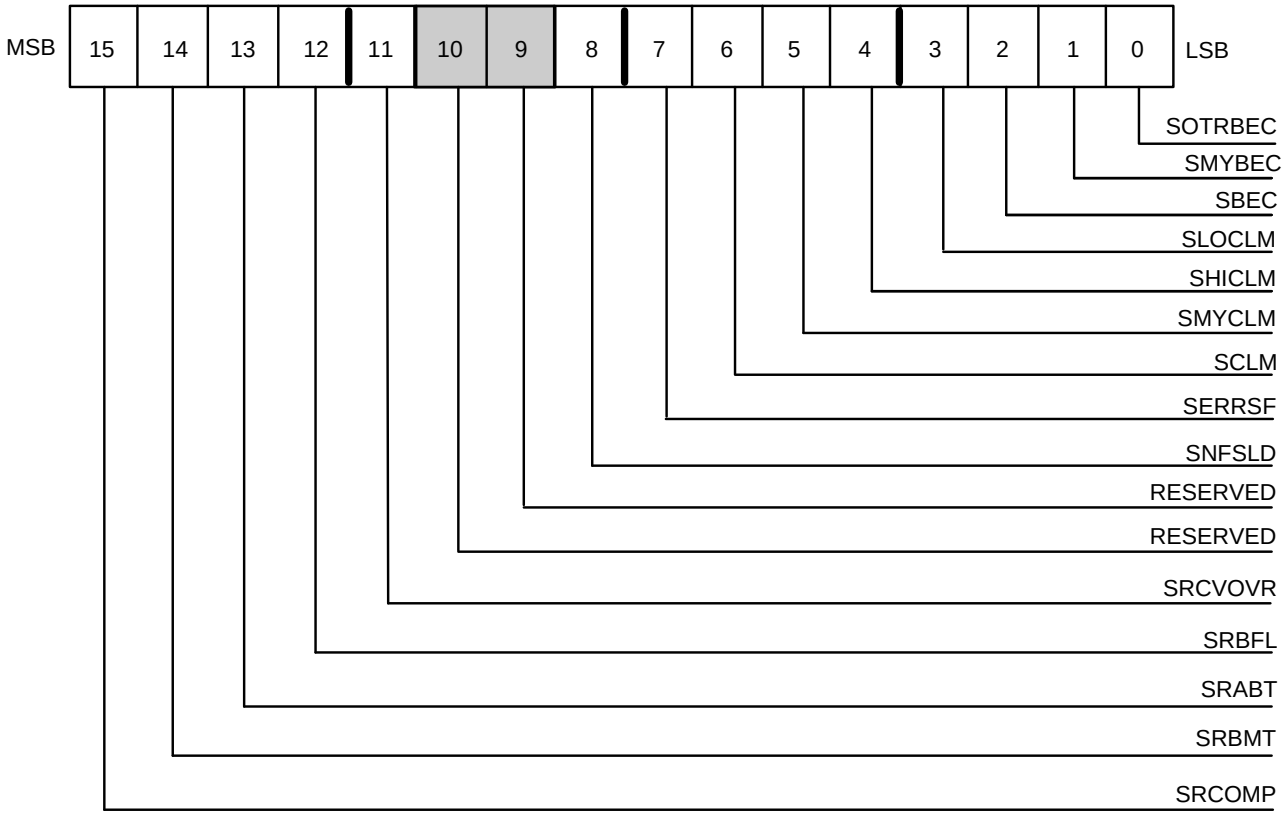
Figure 9. Status Register 1 – Upper 16 Bits (ST1U) (NPADDR = 00h)



Reserved Bits are Read as Zero Unless Otherwise Stated.

19574A-11

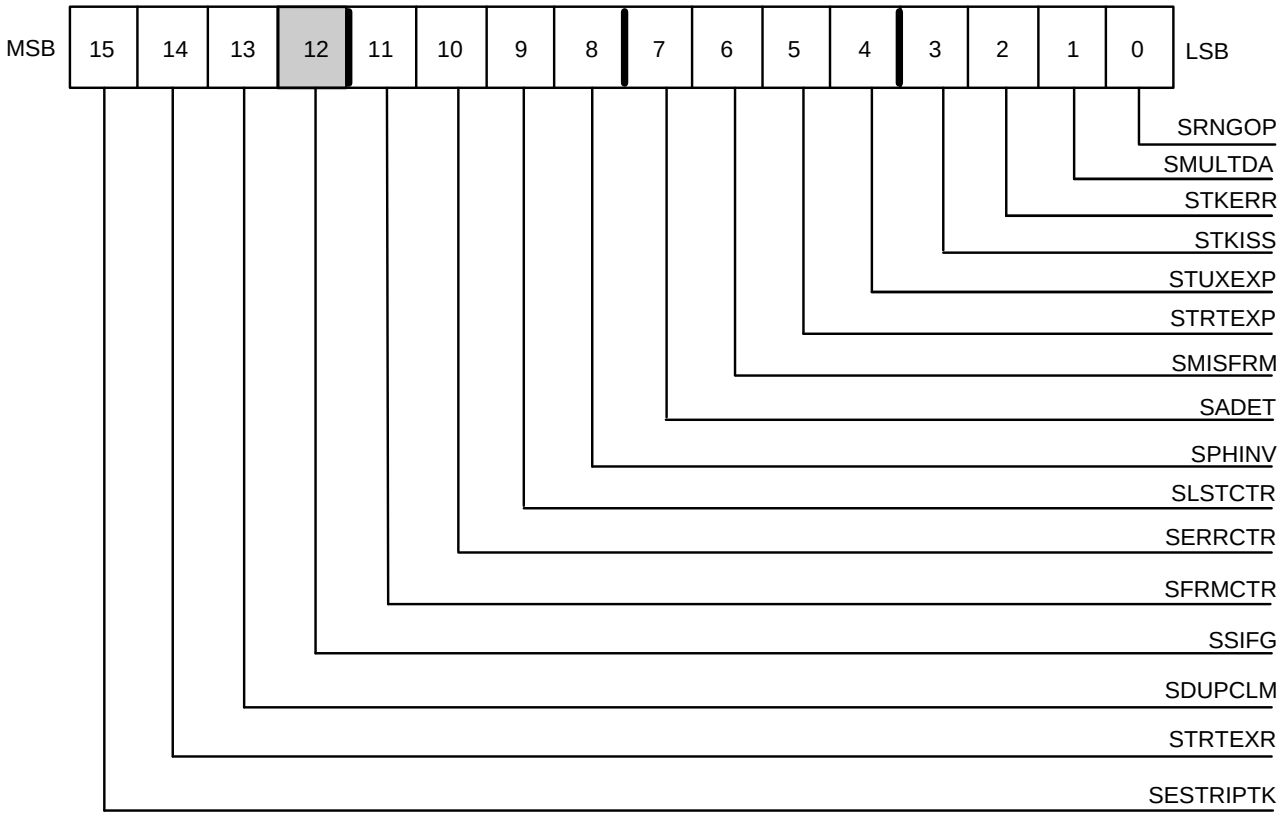
Figure 10. Status Register 1 – Lower 16 Bits (ST1L) (NPADDR = 01h)



Reserved Bits are Read as Zero Unless Otherwise Stated.

19574A-12

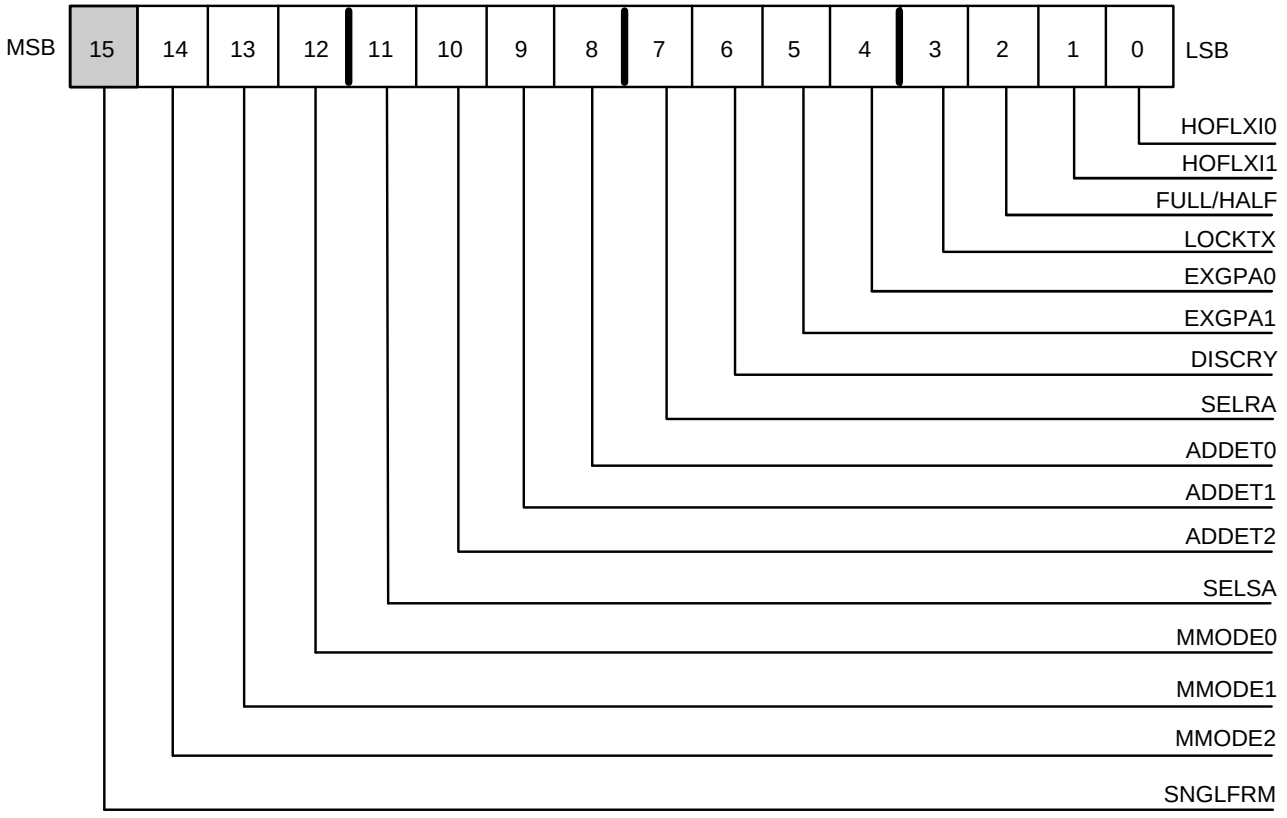
Figure 11. Status Register 2 – Upper 16 Bits (ST2U) (NPADDR = 02h)



Reserved Bits are Read as Zero Unless Otherwise Stated.

19574A-13

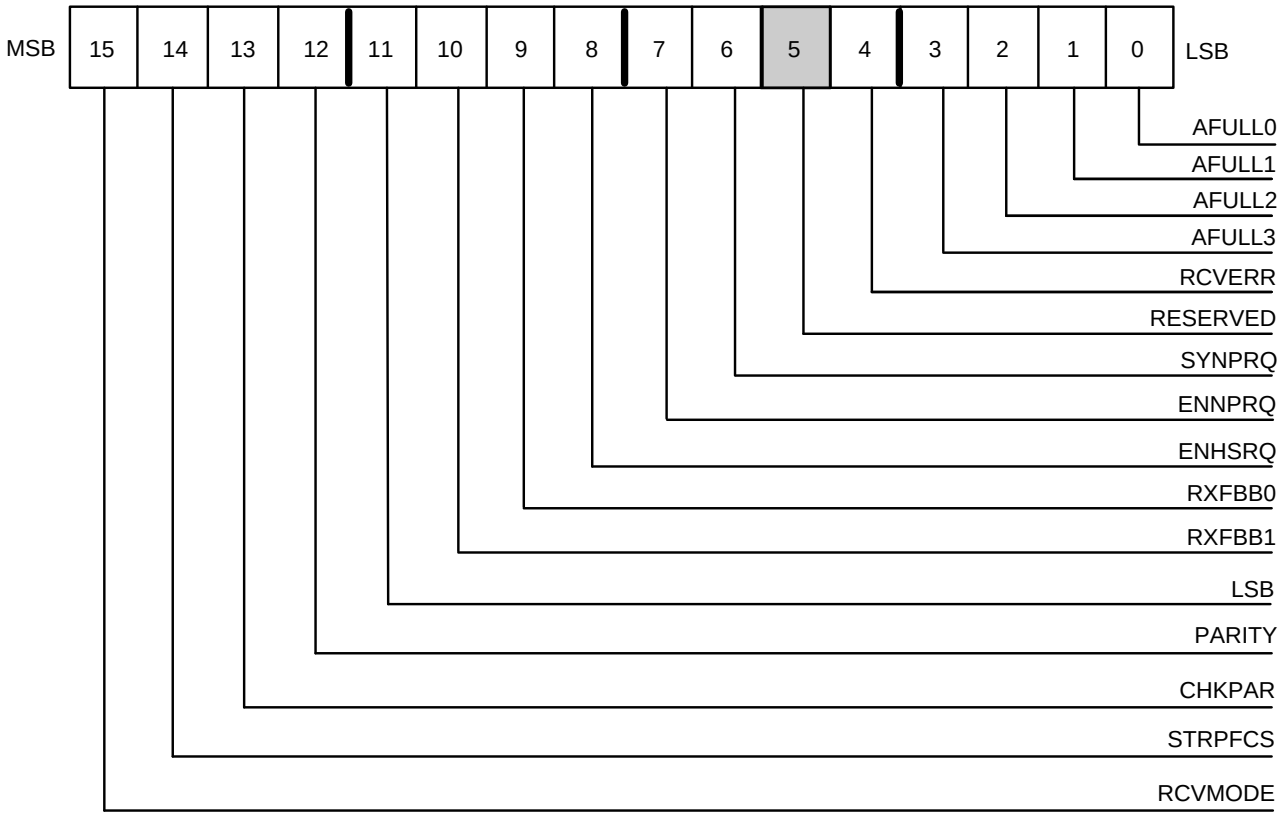
Figure 12. Status Register 2 – Lower 16 Bits (ST2L) (NPADDR = 03h)



Reserved Bits are Read as Zero Unless Otherwise Stated.

19574A-14

Figure 13. Mode Register 1 (MDREG1) (NPADDR = 10h)



Reserved Bits are Read as Zero Unless Otherwise Stated.

19574A-15

Figure 14. Mode Register 2 (MDREG2) (NPADDR = 20h)

Status Register 3 (ST3U & ST3L)

A 32-bit read only register, designated ST3, and a 32 bit read/write register, designated IMSK3, has been added in SUPERNET 3. This register is dedicated to status handling and interrupt reporting. Any of the bits in this status register can be used generate an interrupt. The bits in ST3 may be masked by the interrupt mask registers (IMSK3) for complete control of the interrupt conditions. ST3 has status bits associated with receive operation for RECV2 queue, status of internal CAM match operation, and BIST operation for the various sub-blocks of the SUPERNET 3. All status bits except SRBMT2 and SRBFL2 are auto-cleared on reading the register. The remaining bits are set/reset depending upon the state of the monitored conditions. Refer to Interrupt Mechanisms for more detailed information regarding interrupt handling.

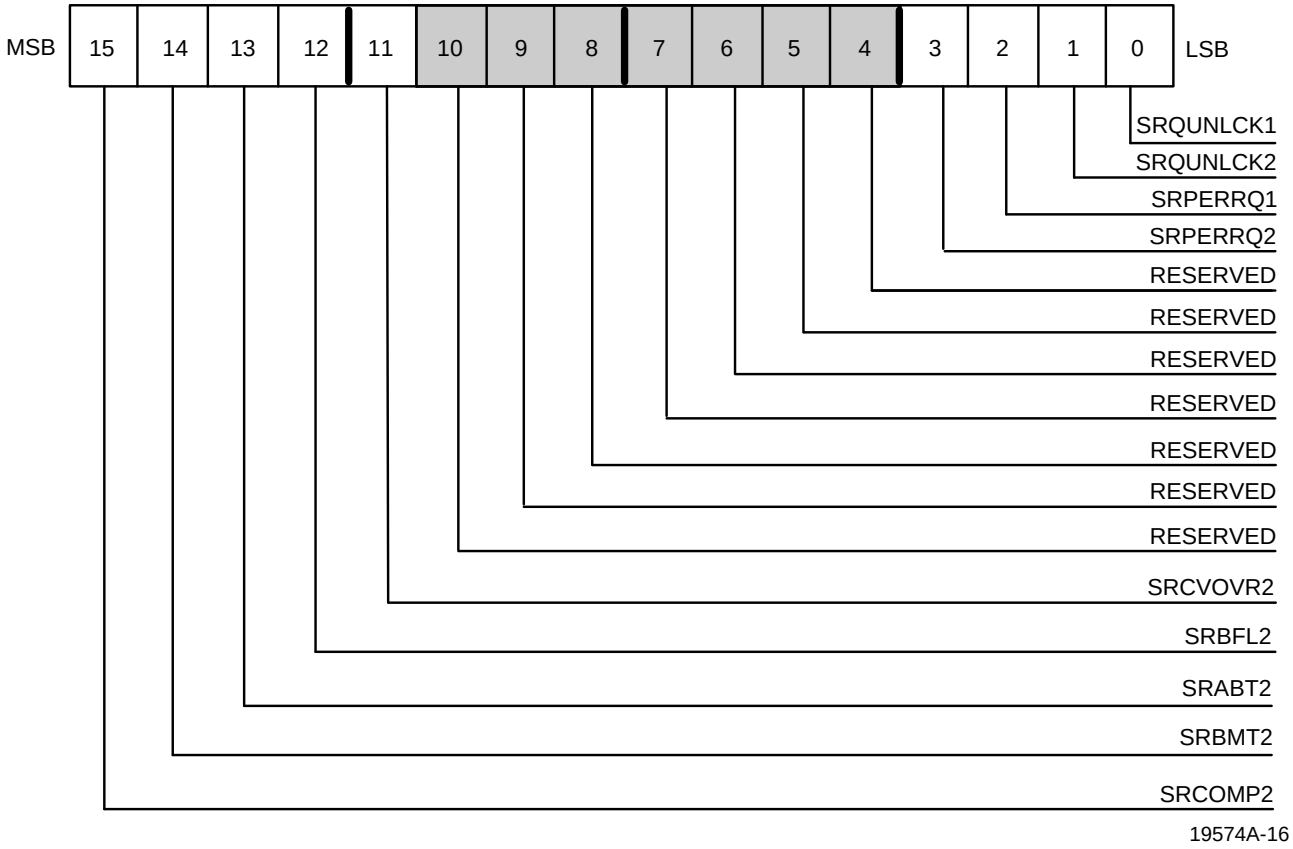


Figure 15. Status Register 3 – Upper 16 Bits (ST3U) (NPADDR = 61h)

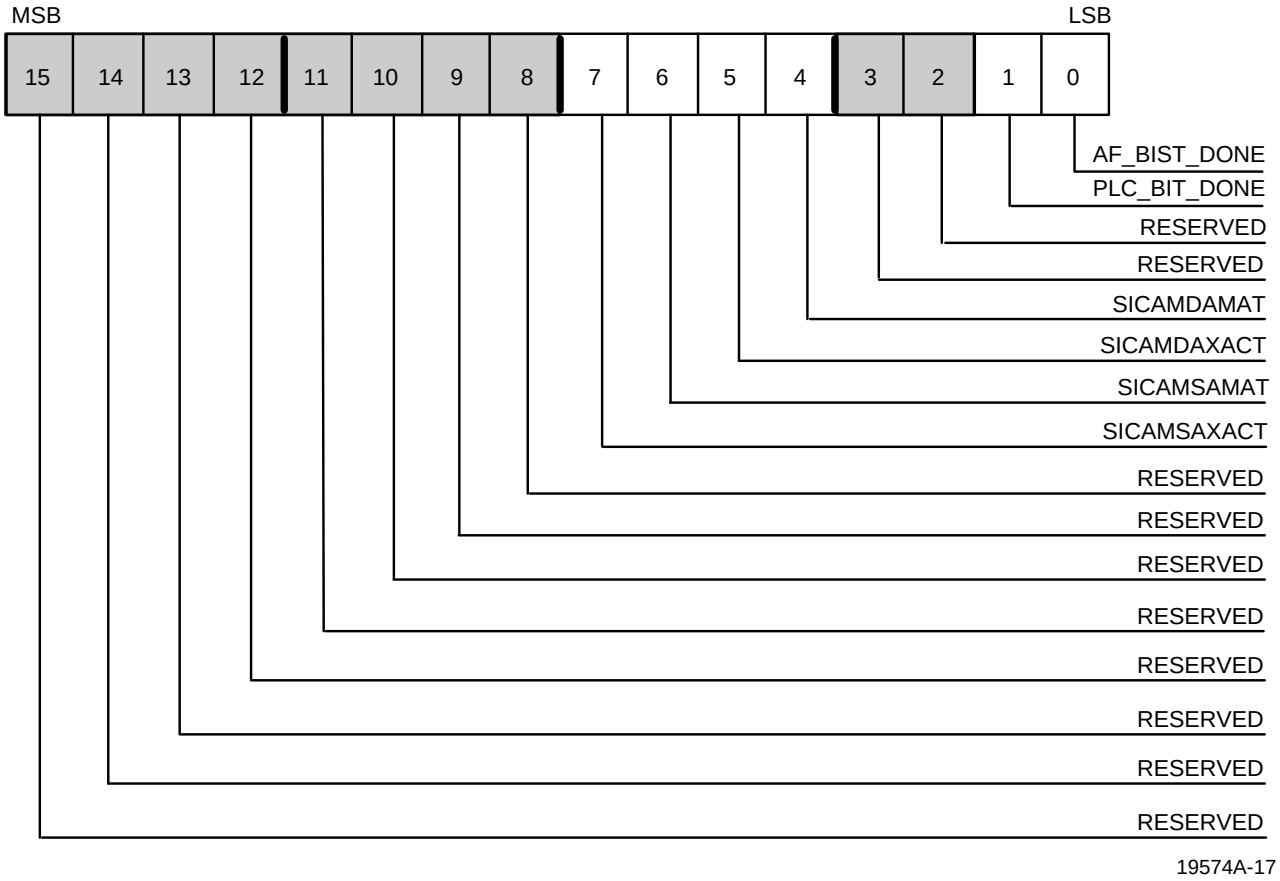


Figure 16. Status Register 3 – Lower 16 Bits (ST3L) (NPADDR = 62h)

The following bits are in ST3U (the upper half of ST3).

Status Receive Complete (Receive Queue 2) SRCOMP2 (bit 15)

This bit is set at the completion of a frame reception following the writing of the frame status and length. Receive frames that are aborted set this bit, but flushed frames do not. This is valid in tag and modified tag mode.

Status Receive Buffer Empty (Receive Queue 2) SRBMT2 (bit 14)

This bit is set when the receive buffer is empty (i.e. RPR2 = WPR2 after an increment of RPR), and is reset when frames are in the receive buffer. This bit is not auto-cleared when read. An interrupt is generated due to setting of this bit when read from the receive queue is attempted while the receive buffer is empty.

Status Receive Abort (Receive Queue 2) SRABT2 (bit 13)

The SRABT2 bit is set when the frame being received is aborted. Frames that normally would be flushed but are aborted due to threshold criterion in tag mode would set this bit.

Status Receive Buffer Full (Receive Queue 2) SRBFL2 (bit 12)

This bit is set when the receive buffer is full (RPR2 = WPR2 after an increment of WPR2). The buffer-memory receive queue is then locked for further input. SRBFL2 can be cleared using the clear receive queue lock (20h) or clear all queue locks (3fh) commands, or by using the auto-unlock feature.

Status Receive FIFO Overflow (Receive Queue 2) SRCVOVR2 (bit 11)

This bit when set, indicates that the SUPERNET 3 receive 2 FIFO has overflowed and receive data has been lost. This condition may occur during the receive buffer full state. SUPERNET 3 will not set the frame-status C indicator (frame copied) on repeated frames when this bit is set.

Reserved (bit 10–bit 4)

These bits are reserved for future use. Some of these reserved bits may read zero or one and the user should ignore these bits. The corresponding mask register bits should be programmed to mask out the interrupts from these bits.

Status Receive Parity Error Queue 2
SRPERRQ2 (bit 3)

This bit is set when there is parity error in the data received in queue 2.

Status Receive Parity Error Queue 1
SRPERRQ2 (bit 2)

This bit is set when there is parity error in the data received in queue 1.

Status Receive Queue 2 Unlocked
SRQUNLCK2 (bit 1)

This bit is set when the auto-unlock feature unlocks the Receive Queue 2 lock due to buffer full condition. Once the unlock threshold is crossed due the host read operation, the SUPERNET 3 will clear the lock on the receive queue 2 and enable the queue for further input.

Status Receive Queue 1 Unlocked
SRQUNLCK2 (bit 0)

This bit is set when the auto-unlock feature unlocks the Receive Queue 1 lock due to buffer full condition. Once the unlock threshold is crossed due the host read operation, the SUPERNET 3 will clear the lock on the receive queue 1 and enable the queue for further input.

The following bits are in ST3L (the lower half of ST3).

Reserved (bit 15–bit 8)

These bits are reserved for future use. Some of these reserved bits may read zero or one and the user should ignore these bits. The corresponding mask register bits should be programmed to mask out the interrupts from these bits.

Status Internal CAM Source Address Exact Match.
SICAMSAXACT (bit 7)

This bit when set indicates that the source address of the incoming frame exactly matches an entry in the internal CAM. This bit is useful for monitoring frame reception and internal CAM operation.

Status Internal CAM Source Address Match
SICAMSAMAT (bit 6)

This bit when set indicates that the source address of the incoming frame matches an entry in the internal CAM based on the internal CAM match logic. This bit is useful for monitoring frame reception and internal CAM operation.

Status Internal CAM Destination Address Exact Match
SICAMDAXACT (bit 5)

This bit when set indicates that the received frame DA exactly matches an entry in the internal CAM. This bit is useful for monitoring frame reception and internal CAM operation.

Status Internal CAM Destination Address Match
SICAMDAMAT (bit 4)

This bit when set indicates that the received frame DA matches an entry in the internal CAM based in the internal CAM match logic. This bit is useful for monitoring frame reception and internal CAM operation.

Reserved (bit 3)

This bit is reserved for future use. The bit may read zero or one and the user should ignore this bit. The corresponding mask register bit should be programmed to mask out the interrupts from this bit.

Reserved (bit 2)

This bit is reserved for future use. The bit may read zero or one and the user should ignore this bit. The corresponding mask register bit should be programmed to mask out the interrupts from this bit.

Status Physical Layer Controller BIST Done
PLC_BIST_DONE (bit 1)

This bit when set indicates that the PLC BIST is complete.

Status Address Filter BIST Done
AF_BIST_DONE (bit 0)

This bit when set indicates that Address Filter (Internal CAM) BIST is complete.

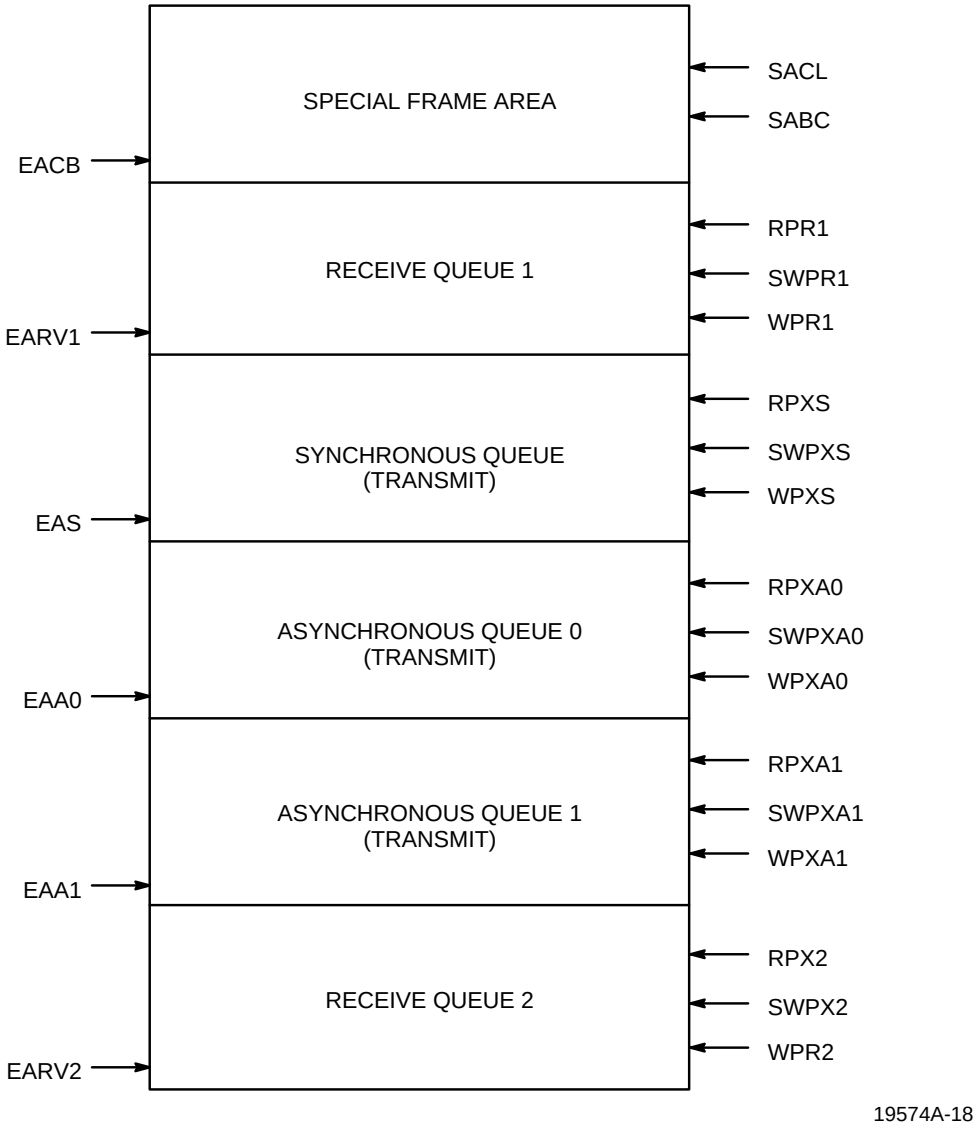


Figure 17. Buffer Memory Queue Organization

Parity Generation and Checking

The SUPERNET 3 will have the following sequence of parity generation and checking:

Transmit Path:

The parity, (even or odd) will be checked at the buffer memory interface (BDP pins). Even parity will be regenerated at the MAC—external PHY interface.

Receive Path:

Parity (even or odd) will be generated at the buffer memory interface. Even parity will be checked at the external PHY (R Bus) interface, if ENA_PAR_CHK (bit 10) in PLC_CNTRL_A register is set.

Node Processor Synchronous Mode Operation

The NPMODE pin (external pin) must be strapped high to select SUPERNET 3 synchronous operation and strapped low to select SUPERNET 3 asynchronous operation.

There are two possible methods of synchronous operation of the SUPERNET 3:

1. BMCLK frequency equals BCLK frequency. (i.e. 12.5 MHz), and both clocks must be in phase.
2. BMCLK operates at twice BCLK (i.e. BMCLK = 25 MHz), and both clocks must be in phase.

In either method, the $\overline{DS}$ is ignored and should be inactive (HIGH) during all synchronous accesses. The read cycle is initiated by asserting the $\overline{CSI}$, NPADDR, NPRW signal which is sampled by the rising edge of the clock. The NPRW signal should be high for read and low for write. At least one clock cycle after the sampling edge, the SUPERNET 3 will begin to drive the NP bus, and this allow the chip driving the NP bus in the previous read or write cycle time to tristate the NP bus. After the next rising edge of clock (the second rising edge after the assertion of $\overline{CSI}$) the data on the NP bus will be valid and the $\overline{READY}$ signal will be asserted. The data will remain valid until the second rising edge of clock after the de-assertion of $\overline{CSI}$. The SUPERNET 3 will tristate the NP bus within 1/2 clock cycle after this clock edge. Regardless of how many clock cycles are needed for executing any SUPERNET 3 instruction, $\overline{READY}$ stays active only for one clock cycle.

A write cycle is very similar to the read cycle. The principal difference are as follows:

1. The NPRW signal must be low while $\overline{CSI}$ is asserted.
2. The data written must be valid on the second rising edge of clock after $\overline{CSI}$ is asserted and remain valid until the next rising edge of the clock and $\overline{READY}$ signal goes active (i.e. LOW). Regardless of how many clock cycles are needed for executing any SUPERNET 3 instruction, $\overline{READY}$ stays active only for one clock cycle.

The Node Processor must tristate the NP bus within one half clock period after the second rising edge after the assertion of $\overline{CSI}$. The Node Processor can extend the write cycle and the time it has to tristate the NP bus by delaying the de-assertion of $\overline{CSI}$ signal.

All register access is complete in two cycles and $\overline{READY}$ is asserted at the positive edge of the second clock cycle. An exception is for MDR accesses that may take more than two clock cycles, at which point the assertion of $\overline{READY}$ is deferred until the last clock period of the execution cycle. Regardless of how many clock cycles are needed for executing any SUPERNET 3 instruction, $\overline{READY}$ stays active only for one clock cycle. Refer to timing diagrams in specifications for details. The assertion of $\overline{READY}$ signal could be delayed during MDR accesses by “n” multiples of clock period.

Address Filter (AF) Support

$\overline{XDA\_XACT}$ and $\overline{XSA\_XACT}$ input signals are provided for the external CAM.

$\overline{XDA\_XACT}$

External Destination Address Exact Match (input, active low)

This input indicates whether the external address match was exact (low) or inexact (high). This input should remain asserted for at least one BCLK cycle, and must be deasserted for at least one BCLK cycle before a subsequent external source address match is recognized. It must be asserted and deasserted in an identical fashion to the $\overline{XDAMAT}$ pin. This input is used in conjunction with the $\overline{XDAMAT}$ pin as follows:

Match	Action
$\overline{XDA\_XACT}$ and $\overline{XDAMAT}$	A, C indicators set and frame copied*.
$\overline{XDA\_XACT}$ and XDAMAT	Invalid combination. Ignored by MAC.
XDA_XACT and $\overline{XDAMAT}$	A, C indicators not set and frame copied.
XDA_XACT and XDAMAT	No action.

**Frame is copied if valid frame or if in promiscuous or limited promiscuous mode. In OSM, the A, C indicators are set according to the OSM rules if both bit 4 and bit 5 (MEIND0,1) of MDREG3 are not set.*

The $\overline{XDA\_XACT}$ pin, which is generated by the external AF, is logically ORed with the “af_dax” output signal generated by the internal AF logic. This pin is enabled only if the MENXACT bit in the mode register 3 (MDREG3) is set. This pin should be tied high (V_{CC}) when external address detection (an external AF) is not used.

$\overline{XSA\_XACT}$

External Source Address Exact Match (input, active low)

This input indicates whether the external source address match was exact (low) or inexact (high). This input should remain asserted for at least one BCLK cycle, and must be deasserted for at least one BCLK cycle before a subsequent external source address match is recognized. It must be asserted and deasserted in an identical fashion to the $\overline{XSAMAT}$ pin. This input is used in conjunction with the $\overline{XSAMAT}$ pin as follows:

Match	Action
$\overline{XSA\_XACT}$ and $\overline{XSAMAT}$	Frame stripped.
$\overline{XSA\_XACT}$ and XSAMAT	Invalid combination. Ignored by MAC.
XSA_XACT and $\overline{XSAMAT}$	Frame not stripped.
XSA_XACT and XSAMAT	No action.

The $\overline{XSA\_XACT}$ pin which is generated by the external AF is logically ORed with the “af_sax” output signal generated by the internal AF logic. This pin is enabled only if the MENXACT bit in the mode register 3 (MDREG3) is set. This pin should be tied high (V_{CC}) when external address detection (an external AF) is not used.

Introduction

The Address Filter (AF) is a functional block that extends the group and/or individual MAC address recognition capabilities of the core FDDI MAC. The AF

recognizes both source and destination addresses, extending the strip and copy functions of the core FDDI MAC.

The AF is a content addressable memory (CAM) that contains 32 entries. Each entry consists of a 48-bit comparand, a 48-bit mask and a 6-bit "personality." The comparand holds the MAC addresses (individual and/or group addresses) for which to look in frames received by the MAC. The mask identifies those bits that are to participate in the address comparison. The personality holds information pertaining to the comparand such as its validity, whether it is a source or destination address, and whether a match by this comparand is to be considered exact.

The AF provides quasi-parallel operation, allowing simultaneous manipulation of the CAM from the node processor interface and address matching from the FDDI MAC receive bus interface. The AF receives a byte-wide data stream from the FDDI MAC receive bus as well as the necessary control information to identify the location of the source and destination addresses in the byte stream. It provides an indication of source and destination match and exact match to the FDDI MAC. The AF also has a 16-bit wide interface to the node processor bus. This interface allows the node processor access to the AF data registers and the command and status registers.

Function of the Address Filter

The AF performs the function of matching source and destination addresses presented on the receive data bus and indicating such matches to the MAC. The MAC uses this information in such decisions as stripping frames, copying frames and setting frame status indicators. The AF also matches addresses presented through the node processor interface and indicates these matches in the status register. This allows the node processor to efficiently manage the contents of the AF.

To perform the function of matching addresses from the receive data bus, the AF loads bytes from the receive data bus into a comparand register. The MAC indicates the bytes to be loaded. Once the AF receives this indication from the MAC, the AF loads six consecutive bytes into the comparand register. Upon loading the comparand register, the AF performs a parallel comparison of all the valid CAM entries in the AF with the comparand register. The AF then indicates the result of this comparison to the MAC. During AF address comparision operation from the received data bus, the node processor interface operations are ignored, and the ERROR bit, along with the DONE bit, is set in the status register.

To perform the function of matching addresses from the node processor interface, the node processor loads six bytes of information, two bytes at a time, into the node processor comparand registers. The node processor then issues a command to the AF to perform the comparison operation. The AF ensures that the node processor commanded comparison does not interfere with a comparison from the MAC receive data bus. The AF indicates the result of the comparison to the node processor in the status register.

To perform any comparison operations, comparands must be written into the CAM of the AF. The node processor performs this operation. Writing a comparand to the CAM in the AF is done by loading the new comparand into the node processor comparand registers. The node processor then loads a 48-bit mask associated with this comparand by loading the mask into the node processor mask registers. Finally, the node processor loads the personality associated with this comparand by loading the node processor personality register. The node processor now completes the operation by issuing a command to write into the CAM through the command register. The status register reflects the current state of the operation, indicating when the AF is busy or full. Once completed, the comparand is available for comparison operations through both the node processor and MAC receive bus interfaces. Additional comparands may be loaded by repeating this operation until no empty locations remain in the CAM.

The AF also provides a mechanism to remove entries from the CAM. This process is called invalidation. To invalidate an entry in the AF, the node processor will load the contents of the CAM that are to be invalidated into the node processor comparand registers. The node processor then issues an instruction to find the entry in the CAM through the command register. When it is determined that the entry that has been found is the one to be deleted, the node processor issues a command to invalidate the entry. Since it is possible that more than one entry in the AF may match the comparand, the AF indicates when a multiple match occurs. When this occurs, the node processor may temporarily prevent an entry in the AF from participating in find commands issued by the node processor until the correct entry is found. The status register indicates when the AF is not busy, i.e., when operations are complete.

There is one more function of the AF that allows the entire CAM to be invalidated in a single operation. The node processor may issue an instruction to invalidate the entire CAM through the command register.

Node Processor Registers

There are ten registers in the node processor interface of the AF. They are the command register, the status register, the built-in self test signature register, the personality register, three comparand registers and three mask registers.

Command Register (AFCMD)

The command register is a 16-bit register that may be read and written through the node processor interface. Writing to this register causes the AF to perform the commanded operation. All data necessary for an operation must be set up in the appropriate registers before the command being issued for an operation. This register will be cleared (filled with zeroes) on a reset and will retain its data after each time it is written until the next reset.

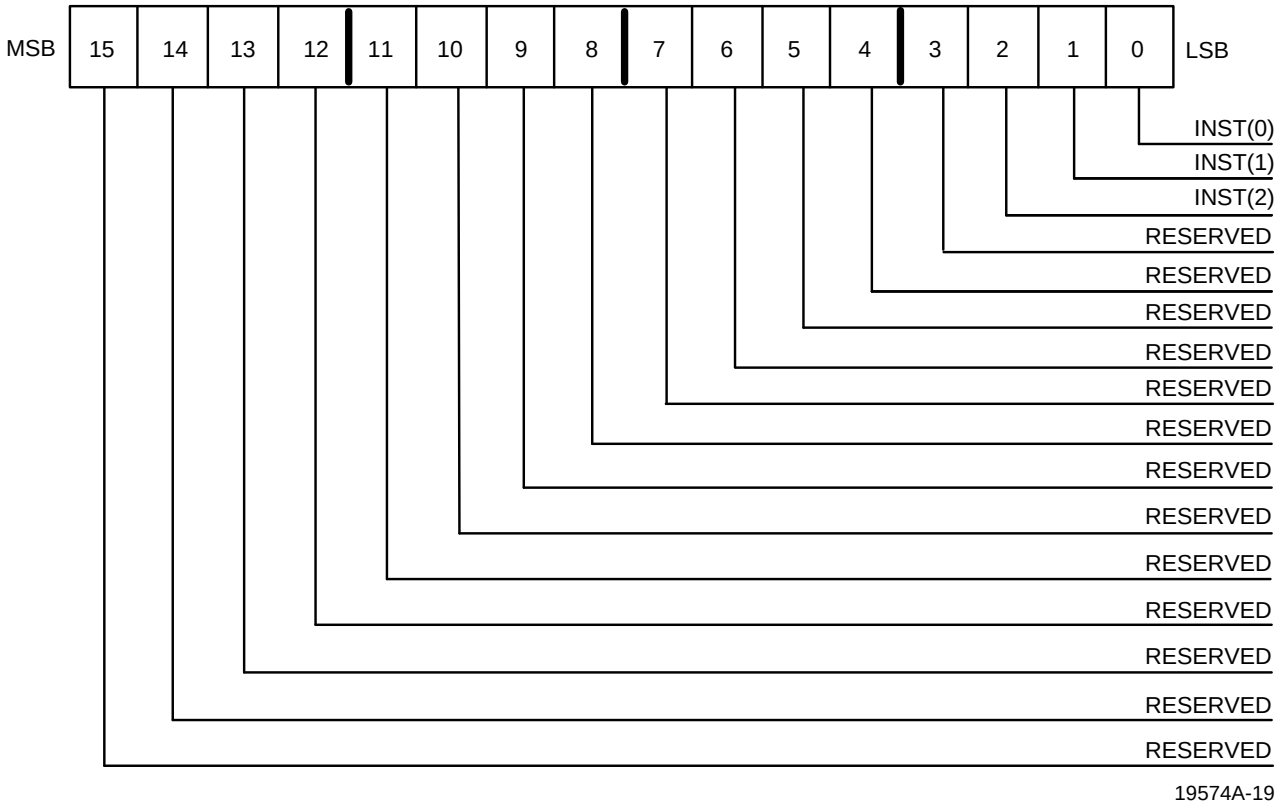


Figure 18. Command Register

Reserved (bits 15:3)
Reserved

These bits are reserved for future use. These bits will always read back as zeroes.

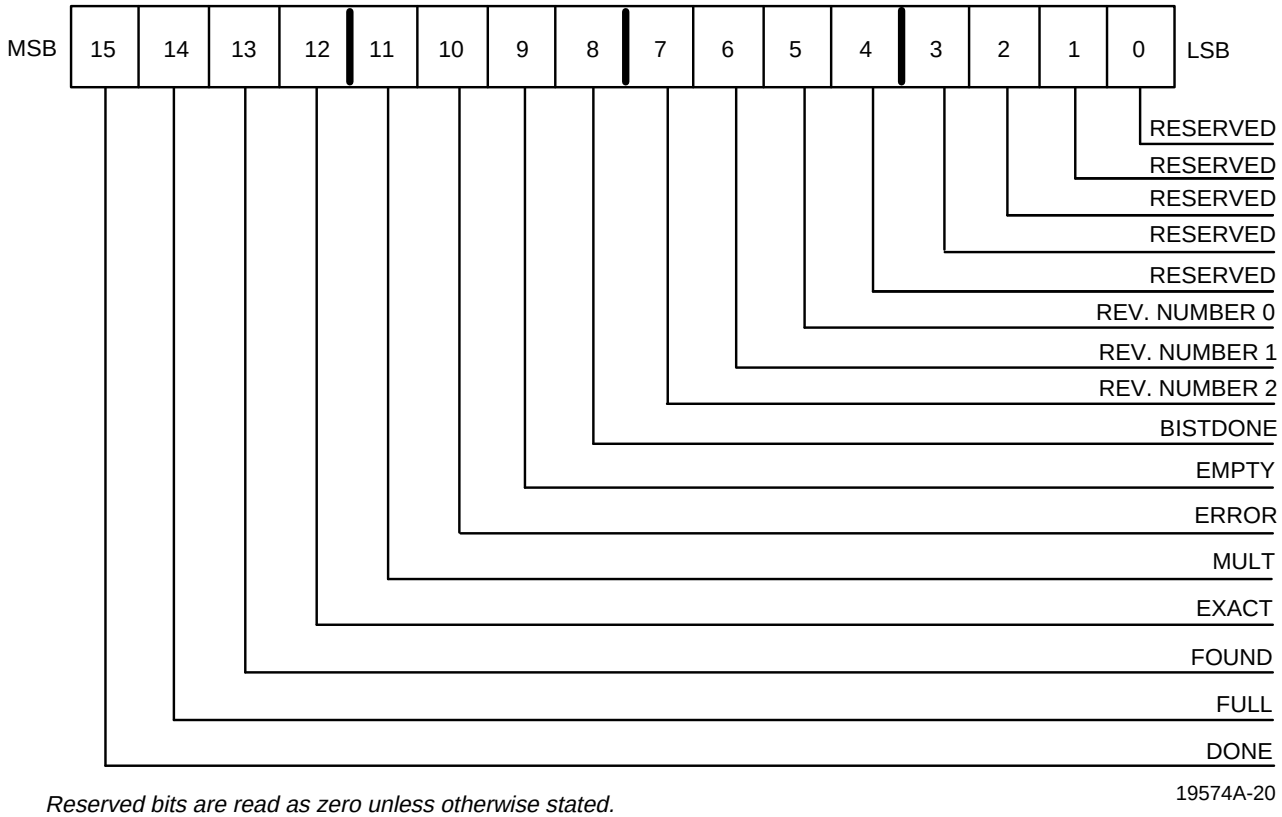
INST (bits 2:0)
Instruction

These bits are the encoded instructions to the AF. When these bits are written, the AF is commanded to perform the associated function. The encoding of the instructions is presented in the table below. These bits will read back the last data that was written to this register.

INST 2:0	Function
000	**Invalidate CAM:** This function invalidates all entries in the CAM. The DONE, FULL, FOUND, MULT, ERROR, BISTDONE and EXACT bits in the status register will be cleared when this command is issued. The DONE and EMPTY bits in the status register will be set upon completion of this operation.
001	**Write CAM:** This function writes the contents of the comparand, mask and personality registers into an empty location in the CAM. The DONE, FULL, FOUND, MULT, BISTDONE and EXACT bits in the status register will be cleared when this command is issued. The DONE bit in the status register will be set upon completion of this operation. The FULL bit in the status register will be set if the CAM is full when this operation is completed. If the FULL bit is set when this command is issued, the write operation will not be performed and the ERROR bit in the status register will be set. Otherwise, the ERROR bit will be cleared.
010	**Read CAM:** This function causes the contents of the CAM entry matching the comparand (indicated by the FOUND bit in the status register after a FIND command) to be written to the comparand, mask and personality registers in the node processor interface. If more than one entry matches the comparand (indicated by the MULT bit in the status register), one of the entries will be chosen arbitrarily. The DONE, FOUND, MULT, ERROR, BISTDONE and EXACT bits in the status register will be cleared when this command is issued. Upon completion of this operation, the DONE bit in the status register will be set. The ERROR bit will be set if this operation is attempted while the CAM is empty or if the FOUND bit is not set.
011	**Run BIST:** This function causes the AF to initiate its built-in self test. The contents of the CAM, including all of its registers, may be modified by the operation of this self test. The DONE, FOUND, MULT, ERROR, BISTDONE and EXACT bits in the status register will be cleared when this command is issued. Upon completion of this operation, the DONE and BISTDONE bits in the status register will be set. Other status bits may be in arbitrary states. The AF must be reset after BIST is completed to return it to a known state before performing any other operations on the AF.
100	**Find:** This function causes the AF to perform a parallel comparison of the comparand registers with the contents of the CAM. CAM entries that have the SKIP bit set will not match the comparand. The node processor mask registers do not participate in this operation. The DONE, FOUND, MULT, ERROR, BISTDONE and EXACT bits in the status register will be cleared when this command is issued. Upon completion of this operation, the DONE bit in the status register will be set and the FOUND, MULT and EXACT bits will be updated with the appropriate status of the operation.
101	**Invalidate:** This function operates on the result of the last “Find” instruction, above, and sets the INVALID bit in the personality of the first matching entry in the CAM. The DONE, FOUND, MULT, ERROR, BISTDONE and EXACT bits in the status register will be cleared when this command is issued. Upon completion of this operation, the DONE bit in the status register will be set. The EMPTY bit will be updated with the appropriate status after the operation. The ERROR bit will be set if this operation is attempted while the FOUND bit is not set. Otherwise, the ERROR bit will remain cleared.
110	**Skip:** This function operates on the result of the latest “Find” operation and causes the AF to set the SKIP bit in the personality of the first matching CAM entry. The SKIP bit will be set in the same entry that will be read by issuing a “Read CAM” instruction. The DONE, FOUND, MULT, ERROR, BISTDONE and EXACT bits in the status register will be cleared when this command is issued. Upon completion of this operation, the DONE bit in the status register will be set. The ERROR bit will be set if this operation is attempted while the FOUND bit is not set. Otherwise, the ERROR bit will remain cleared.
111	**Clear all SKIP bits:** This function causes the CAM to clear all SKIP bits. The DONE, FOUND, MULT, ERROR, BISTDONE and EXACT bits in the status register will be cleared when this command is issued. Upon completion of this operation, the DONE bit in the status register will be set.

Status Register (AFSTAT)

The status register is a 16-bit register that may be read and written through the node processor interface. This register contains the status of the AF. All bits of the status register are static; they are not cleared after a read operation.



Reserved bits are read as zero unless otherwise stated.

Figure 19. Status Register

DONE (bit 15)
Done Indicator

The DONE bit indicates to the node processor that the AF is finished performing a previously commanded operation. The node processor must not issue any command to the AF when this bit is not set. This bit may be used to generate an interrupt to the node processor indicating the completion of an operation.

FULL (bit 14)
CAM Full

This bit indicates the state of the CAM array. When this bit is set, there are no invalid CAM entries, i.e., all CAM entries have their VALID bit set. When this is reset, there is at least one invalid entry in the CAM. If this bit is set, the AF should not be commanded to "Write CAM." If that instruction is issued when this bit is set, the operation will not be performed.

Note: *The ERROR bit in the status register will not be set if a "Write CAM" instruction is issued when this bit is set. The user has to read this bit status before attempting to write an entry into the CAM.*

FOUND (bit 13)
Comparand Found in CAM

This bit indicates the result of a "Find" operation. When set, this bit indicates that the data in the comparand register matches at least one entry in the CAM (as masked by the mask entries). If this bit is reset, this bit indicates that no entry in the CAM matches the data in the comparand register. This bit is cleared as a result of a "Skip" or "Invalidate" operation.

EXACT (bit 12)
Exact Match

This bit reflects the result of a "Find" operation. When set, this bit indicates that at least one matching CAM entry (as masked by its mask entry) has the DAX bit set in its personality byte. If this bit is reset, no matching CAM entries have the DAX bit set in the corresponding personality bytes. This bit is cleared as a result of a "Skip" or "Invalidate" operation.

MULT (bit 11)
Multiple Match

This bit reflects the result of a “Find” operation. This bit has meaning only if the FOUND bit is set. If this bit is set, it indicates that more than one entry in the CAM matches the value in the node processor comparand register. This bit is cleared as a result of a “Skip” or “Invalidate” operation.

ERROR (bit 10)
Error

This bit indicates that an improper operation was attempted. This bit will be set for the following condtions:

If an attempt is made to issue the “Read CAM” instruction while the EMPTY bit is set.

If the “Invalidate” or “Skip” instructions are issued and the FOUND bit is not set.

If the Node Processor command operation is ignored due to Receive Bus address match operation.

EMPTY (bit 9)
CAM EMPTY

This bit reflects the state of the CAM array. This bit will be set if all entries in the CAM have their VALID bits reset. EMPTY bit will be reset after write CAM command.

BISTDONE (bit 8)
BIST Complete

This bit reflects the state of the built-in self test (BIST). This bit will be cleared after reset, while BIST is running and after an instruction is issued to the command register. It will be set once BIST is complete.

Revision Number

Bits 7, 6 and 5 provide a three-bit binary value that indicates the revision number of the Address Filter.

Reserved (bits 4:0)
Reserved

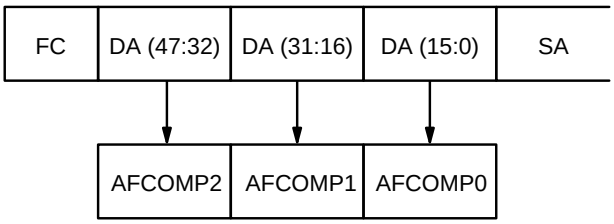
These bits are reserved for future use. These bits should always be written with zeroes to ensure compatibility with future revisions of the AF. These bits will always read back as zeroes.

BIST Signature Register (AFBIST)

This is a 16-bit register that may be read and written by the node processor. After the initiation of BIST, this register will hold the signature resulting from the execution of built-in self test when the BISTDONE bit is set in the status register.

Comparand Registers (AFCOMP2:0)

The comparand registers are 16-bit registers that may be read and written by the node processor. AFCOMP0 corresponds to bits 15:0 of the CAM entry. AFCOMP1 corresponds to bits 31:16 of the CAM entry. AFCOMP2 corresponds to bits 47:32 of the CAM entry. This register will be cleared (filled with zeroes) on a reset and will retain its data after each time it is written until the next reset. This register will be updated with the contents of the first matching entry in the CAM if a “Read CAM” instruction is issued to the command register while the FOUND bit is set.



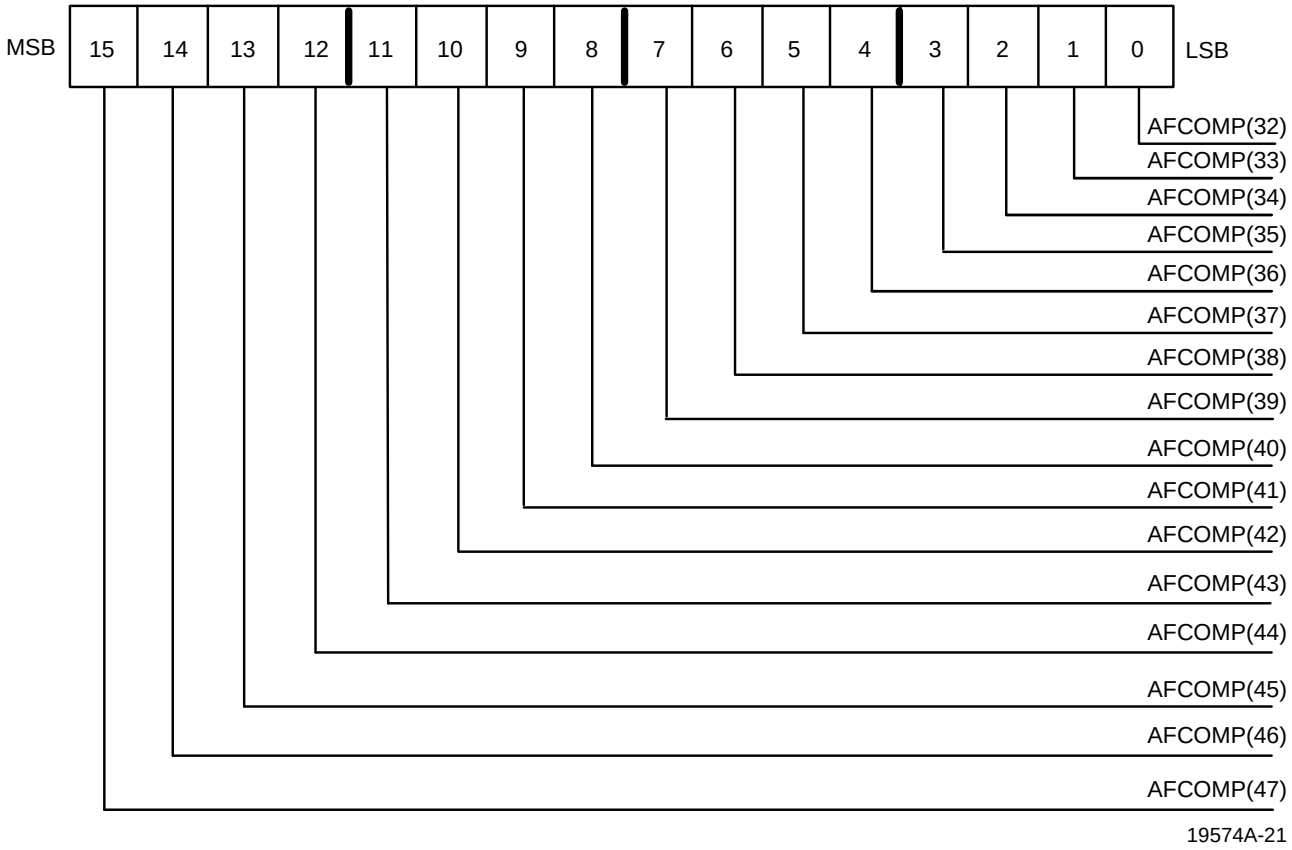


Figure 20. Node Processor Comparand Register (AFCOMP2)

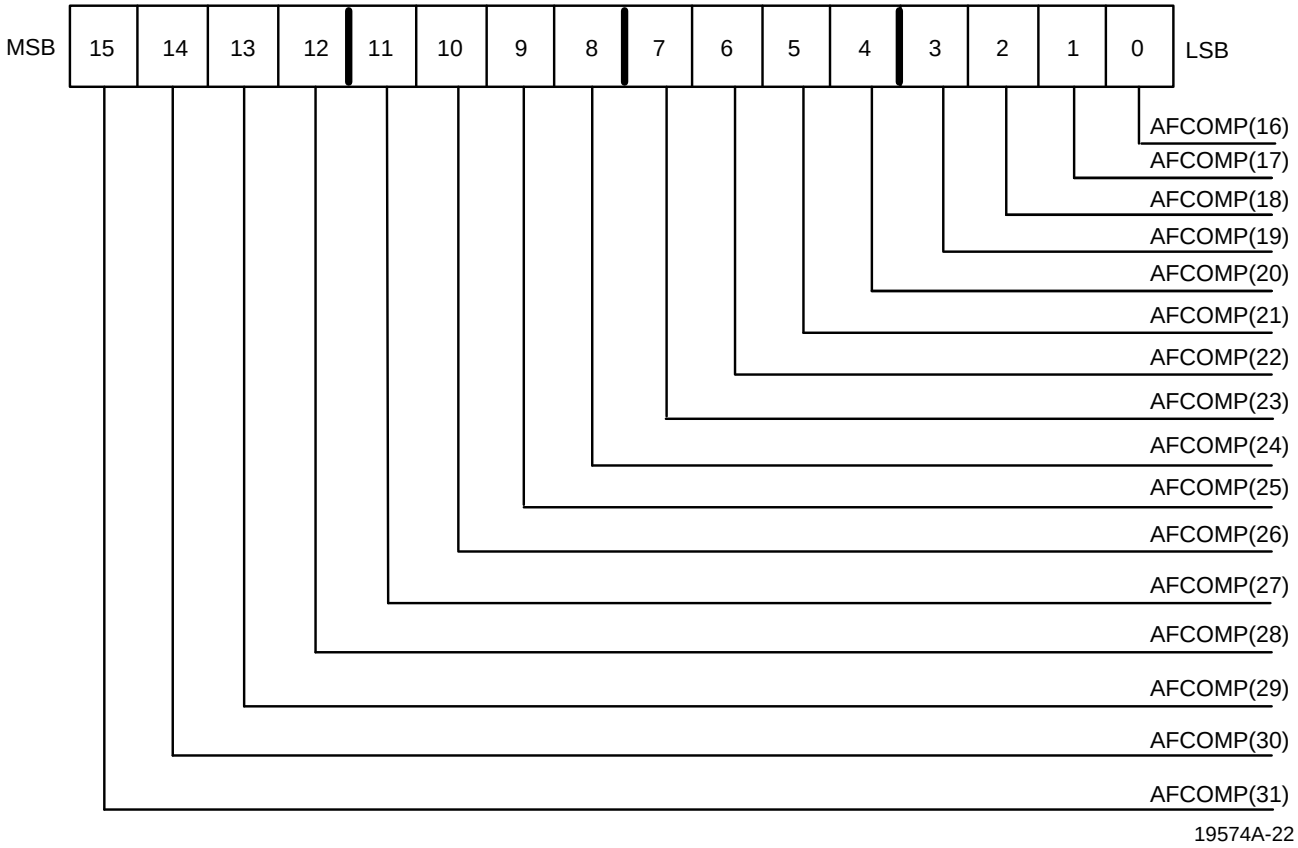


Figure 21. Node Processor Comparand Register (AFCOMP1)

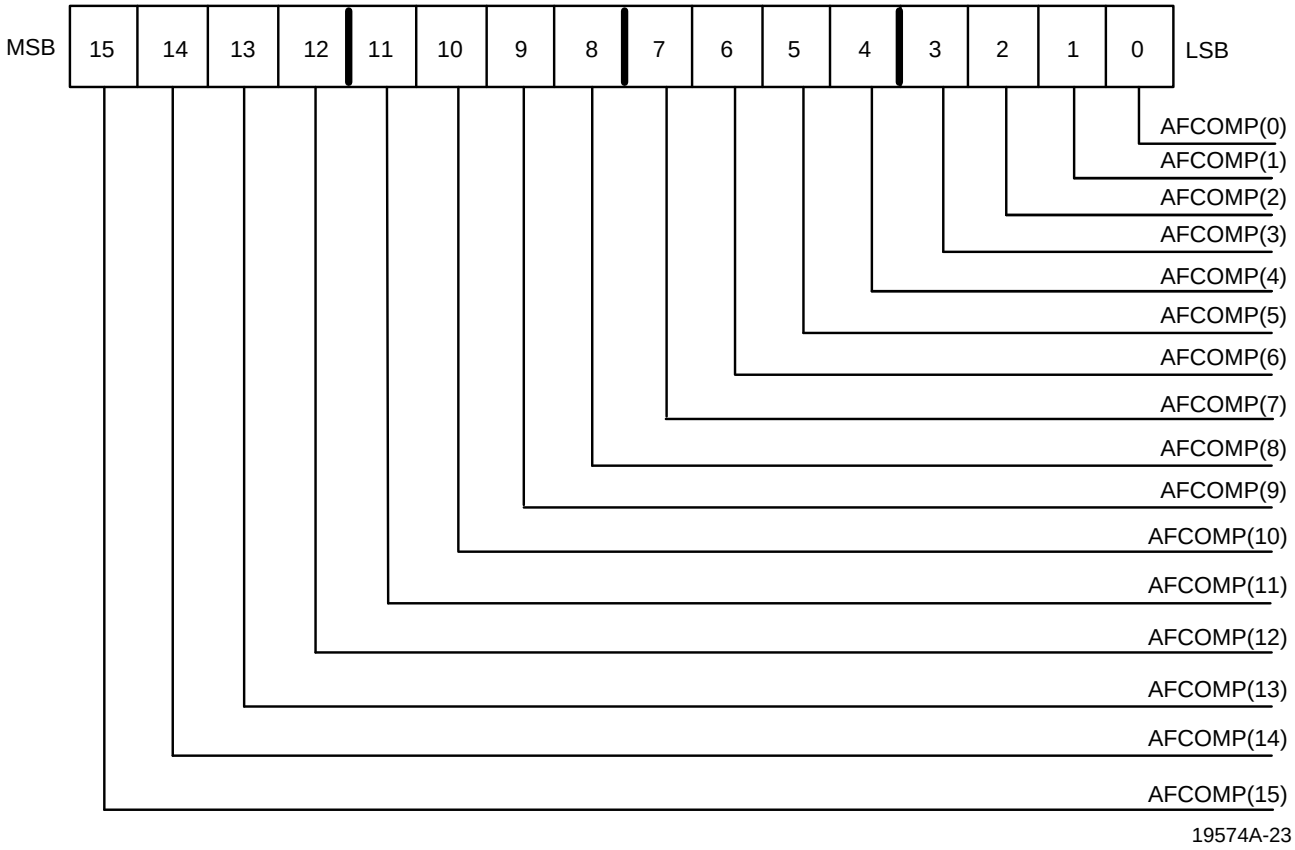


Figure 22. Node Processor Comparand Register (AFCOMP0)

Mask Registers (AFMASK2:0)

The mask registers are 16-bit registers that may be read and written by the node processor. AFMASK0 corresponds to bits 15:0 of the CAM mask entry. AFMASK1 corresponds to bits 31:16 of the CAM mask entry. AFMASK2 corresponds to bits 47:32 of the CAM mask entry. A “1” written to a bit position in the mask register will enable the corresponding bit in the comparand to participate in the comparison operation. A “0” written to a bit in the mask register will disable, or mask, the corresponding bit in the comparand. A bit that is masked will always match the corresponding bit in a comparison operation. This register will be cleared (filled with zeroes) on a reset and will retain its data after each time it is written until the next reset. This register will be updated with the contents of the first matching entry in the CAM if a “Read CAM” instruction is issued to the command register while the FOUND bit is set.

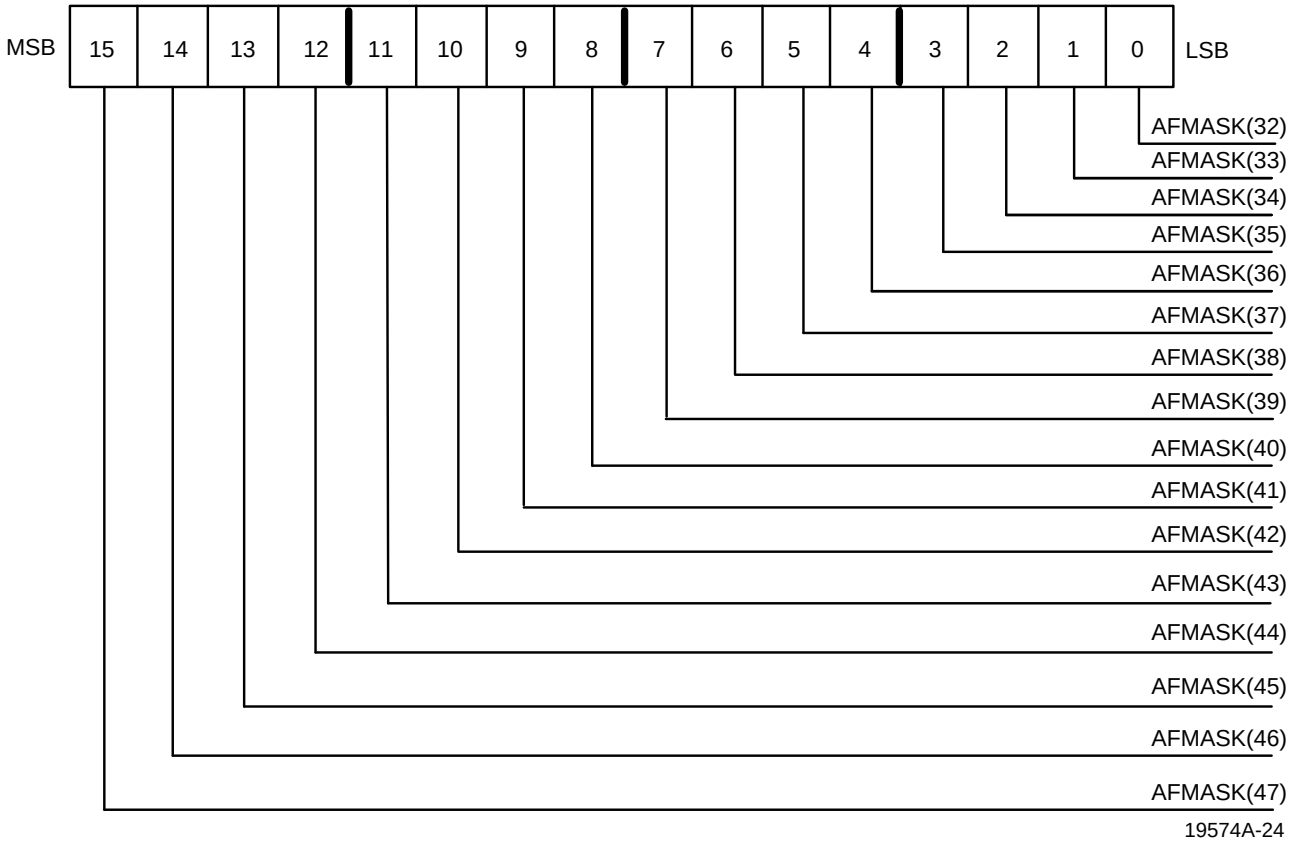


Figure 23. Mask Register (AFMASK2)

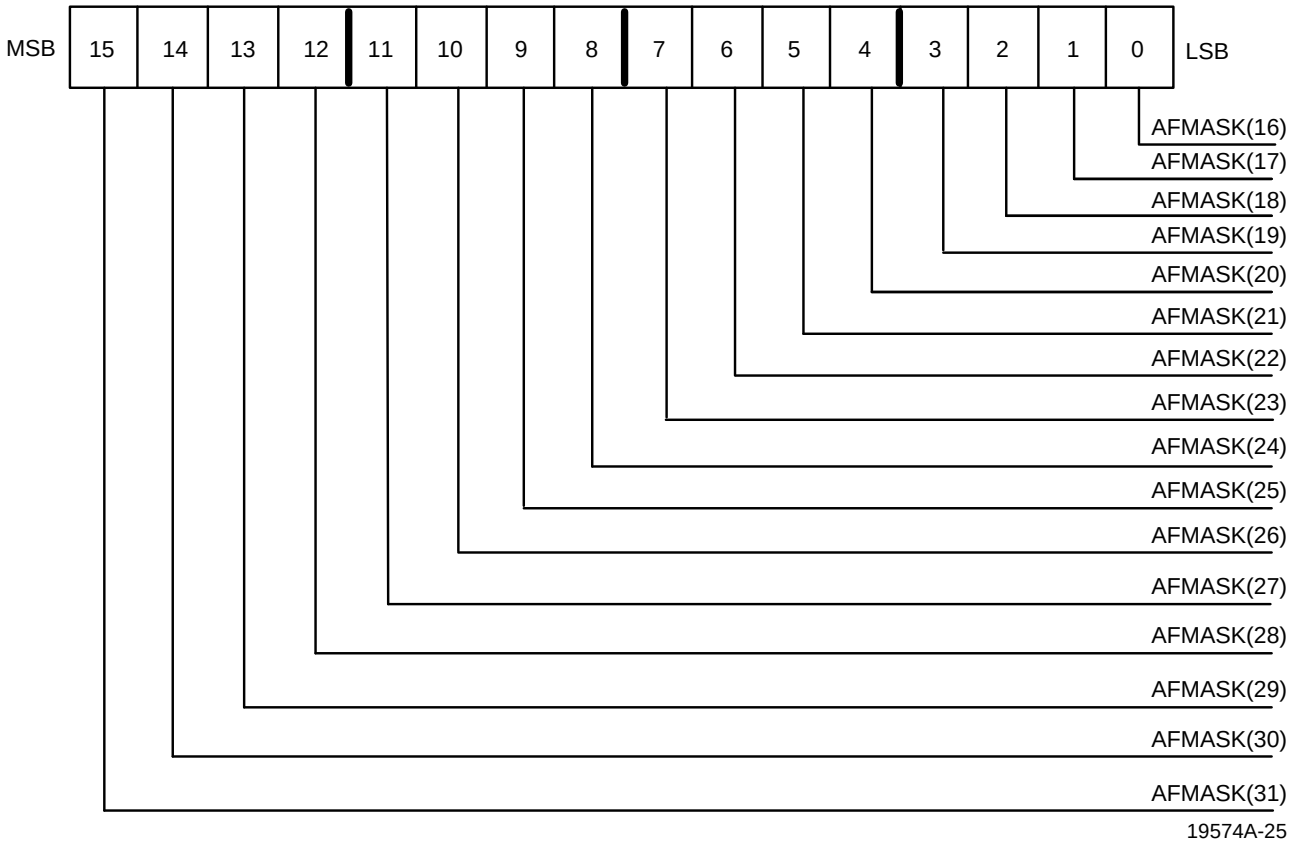


Figure 24. Mask Register (AFMASK1)

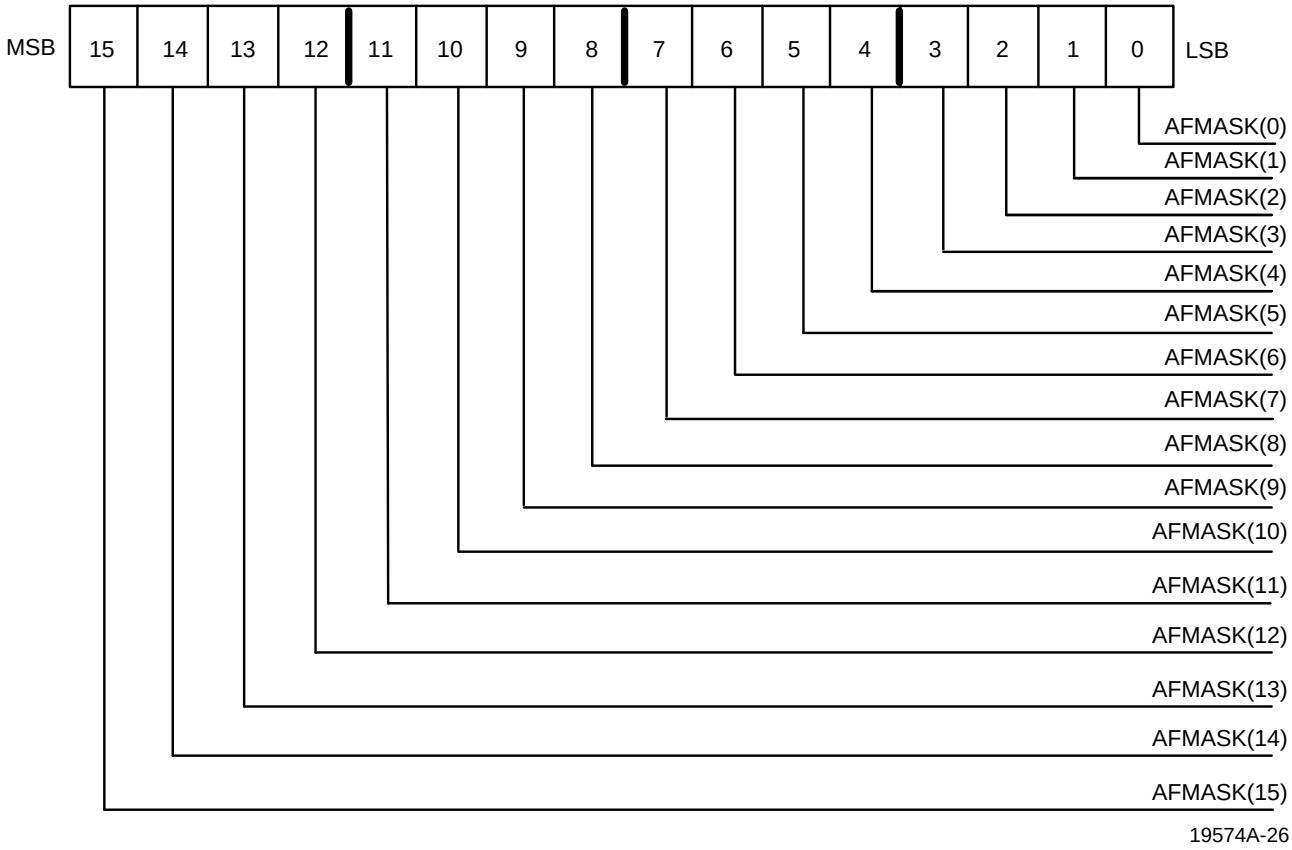


Figure 25. Mask Register (AFMASK0)

Personality Register (AFPERS)

The personality register is a 16-bit register that may be read and written by the node processor. This register will be cleared (filled with zeroes) on a reset and will retain its data after each time it is written until the next reset.

This register will be updated with the contents of the first matching entry in the CAM if a "Read CAM" instruction is issued to the command register while the FOUND bit is set.

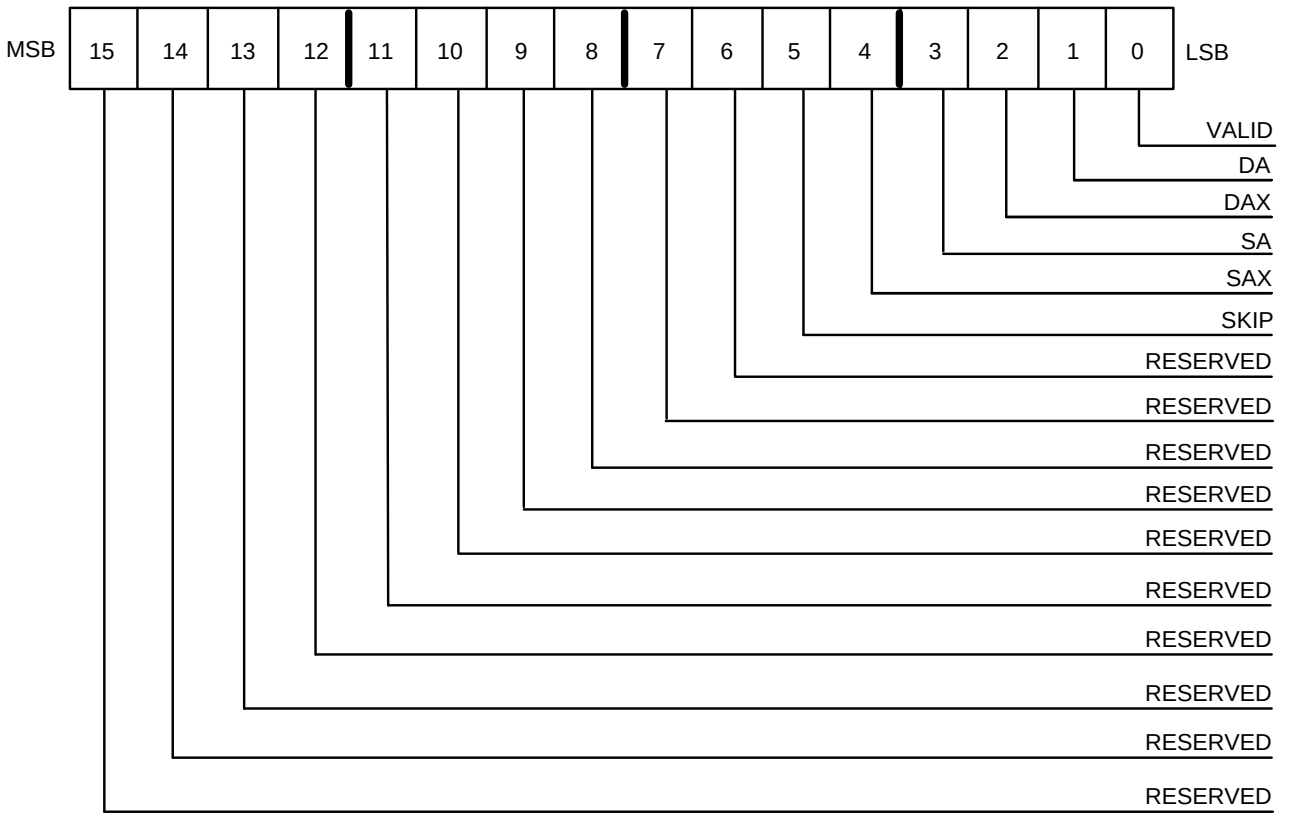


Figure 26. Personality Register

Reserved (bits 15:6)
Reserved

These bits are reserved for future use. These bits should always be written with zeroes to ensure compatibility with future revisions of the AF. These bits will always read back as zeroes.

SKIP (bit 5)
Skip This Entry

This bit prevents the associated entry from indicating a match during a "Find" operation begun through the command register. This bit has no effect on comparisons with comparands received from the MAC interface.

SAX (bit 4)
Source Address Exact

This bit causes the AF to indicate that any comparison matching this CAM entry to a source address will be indicated as being an exact match. An exact match may contain masking done while comparing the entry. Invalid if SA is zero.

SA (bit 3)
Source Address

This bit enables the CAM entry for comparison with source addresses.

DAX (bit 2)
Destination Address Exact

This bit causes the AF to indicate that any comparison matching this CAM entry to a destination address will be indicated as being an exact match. An exact match may contain masking done while comparing the entry. Invalid if DA is zero.

DA (bit 1)
Destination Address

This bit enables the CAM entry for comparison with destination addresses.

Valid (bit 0)
CAM Entry Valid

This bit indicates that the CAM entry is valid and is enabled for comparisons with addresses indicated by the SA and DA bits.

Node Processor Register Address Map

The registers accessible through the node processor interface are addressed as shown in the table below.

Register Mnemonic	Address	Register Name
AFCMD	"b0"	Address Filter Command Register
AFSTAT	"b2"	Address Filter Status Register
AFBIST	"b4"	Address Filter BIST Signature
AFCOMP2	"b6"	Address Filter Comparand 2 Register
AFCOMP1	"b8"	Address Filter Comparand 1 Register
AFCOMP0	"ba"	Address Filter Comparand 0 Register
AFMASK2	"bc"	Address Filter Mask 2 Register
AFMASK1	"be"	Address Filter Mask 1 Register
AFMASK0	"c0"	Address Filter Mask 0 Register
AFPERS	"c2"	Address Filter Personality Register

MAC Interface

The AF interfaces to the FDDI MAC through the receive data bus, MAC status and control signals, and the AF match output signals. As described above, the AF loads addresses to be compared as they are received from the network. The MAC signals the AF at the beginning of the source and/or destination address through the MAC address state machine's state variable. The AF uses this state variable to load six consecutive bytes into the MAC comparand register and perform the comparison of the address against the contents of the CAM when the complete address is in the register. The AF signals the MAC with the result of the comparison and if the comparison is exact (as determined by the appropriate bit in the personality byte). The AF will decode the Frame Control (FC) field of the received frame and will not participate in the address match if bit 6 of the FC is zero (indicating a short address frame).

MAC Comparand Register

This is a 48-bit register that is loaded from the MAC receive data bus. The data arrives one byte at a time and is loaded byte serially into the register. An internal multiplexer is driven by the state variable of the MAC address state machine. Once started, the state machine causes the register to load six consecutive bytes from the receive data bus into the comparand register. Upon completion of the loading of the register, the contents will be transferred to the MAC comparand shadow register for comparison with the contents of the CAM.

MAC Comparand Shadow Register

The MAC comparand shadow register receives the contents of the MAC comparand register once that register has been loaded with six bytes of address information from the MAC receive data bus. This allows the MAC comparand register to immediately begin loading a subsequent address from the receive data bus without interfering with the comparison function of the AF. Once data has been transferred into the MAC comparand shadow register, the contents of the shadow register are compared with the contents of the CAM.

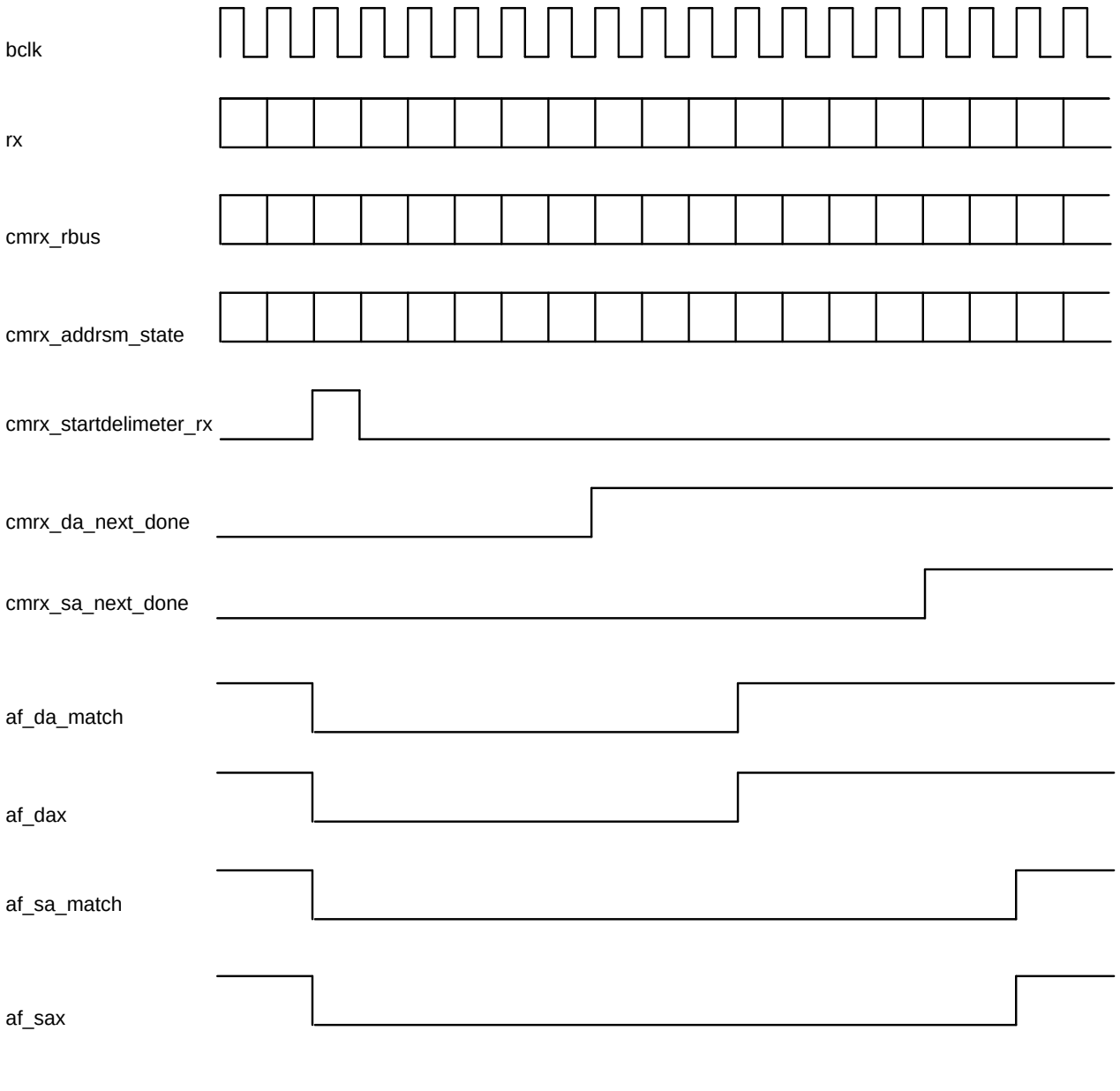


Figure 27. AF–MAC Interface Handshake (Internal Signals)

ADDRESS FILTER TEST SPECIFICATION

Introduction

The Address Filter (AF) core requires a special set of test patterns to provide adequate fault coverage. The mask and data bits of the AF are similar to an SRAM cell and must be tested with the types of test patterns that are used to test SRAM's. The main fault models that are applied in SRAM testing are the stuck-at fault model, the transition fault model, and the coupling fault model. The stuck-at fault model describes the condition where a cell or line is always 0 or 1 and can't be changed to the opposite state. The transition fault model describes the condition where a cell or line fails to undergo a transition from 0_1 or from 1_0 when it is written. The coupling fault model describes the condition where a write to a cell that causes a transition in that cell, also causes a transition in another cell. In addition to the test necessary for the above fault models, the CAM contains additional personality bits, match logic and a priority encoder that must also be tested.

The AF core will be tested through the use of built-in self test (BIST). The patterns that need to be applied to the SRAM portion of the CAM are algorithmic in nature and can be easily implemented with BIST. The components of the AF BIST logic will include a state machine, a data generator, a signature register, and an address generator.

Test Logic Description

This section provides a description of the AF test logic.

BIST Operation

The BIST feature can be accessed by one of two methods. The first means of access is a serial mode of access meant to be used with an IEEE 1149.1 Test Access Port (TAP) controller. The second means of access is a parallel mode of access using the node processor interface. Each means of access is described further below.

TAP Interface

Access to BIST through the TAP interface is provided so that the core can be tested in a product that supports the RUNBIST instruction of the IEEE 1149.1 standard. As such, the implementation of the BIST should conform to all the rules described for the RUNBIST instruction in the standard. Some of these rules apply only to the design of the TAP controller itself, while others affect the implementation of the AF BIST logic. The rules that affect the implementation of the AF BIST logic are summarized below.

The AF will have a serial input and serial output through which the results of the BIST can be shifted. These resuls shall be shifted in response to the appropriate TAP interface signals.

The AF BIST execution will depend on signals provided by the TAP controller and will run at a rate determined by the TAP test clock. The clocking of the BIST will be taken care of external to the AF. This can be done by multiplexing the normal AF clock with the test clock during the RUNBIST instruction.

The AF BIST implementation shall not require a seed value to be serially shifted in.

The minimum number of test clock cycles necessary for the completion of BIST needs to be provided. After the minimum number of clock cycles the AF must hold the results of the BIST constant until requested to shift them out by the TAP controller.

Each execution of BIST shall provide the same result and shall not depend on the state of signals received at non-TAP interface signal.

The serial BIST operation is begun when the tl_bistena signal from the TAP controller is asserted. This signal must remain asserted for the minimum duration specified to guarantee a valid signature. When the minimum number of clock cycles has passed the tl_bistena signal will be de-asserted and a short time later the tl_bistse signal will be asserted to shift out the contents of the signature register through the af_tdo output. When the tl_bistena signal becomes de-asserted, the signature register should hold its content until the tl_bistena signal is asserted again, or the AF is reset. If the minimum number of clock cycles for the completion of BIST is not met, an intermediate signature will be obtained. This can be used to aid in fault isolation for internal manufacturing testing.

Node Processor Interface

Access to BIST through the node processor interface is provided for board and system level testing. BIST is initiated through this interface by writing the Run BIST instruction to the AFCMD register. The BISTDONE and DONE bits in the AFSTAT register are cleared upon issuing this instruction and the BIST state machine moves from the idle to the operational state. At the completion of self test, the BISTDONE and DONE bits will be set in the AFSTAT register. The DONE bit can be used to generate an interrupt to the node processor indicating the completion of the self test. The result of the self test can be obtained by reading the AFBIST register and comparing it to the known good signature.

BIST Pattern Requirements

This section presents the pattern requirements that the BIST implementation should try to meet. The implementation should try to meet as many of the requirements as possible, however, overhead considerations may make this goal unattainable. In the case that the requirements are not met, a means of applying these patterns functionally must be found. The functional application of patterns may dictate additional testability requirements in the AF. The pattern requirements are divided into two sections, the first deals with the testing of the portion of the AF that is SRAM-like, the second deals with the testing of the remaining AF logic such as the match logic, priority encoder, exact logic, etc.

Pattern requirements for the SRAM-like portion of the AF

The following pattern requirements are taken from a paper by Jain and Stroud. Some of the requirements may be architecture specific and may not be necessary. Additional requirements may be necessary depending on the architecture of the AF. This paper describes two algorithms that may be used in the implementation of the BIST test.

1. Each cell must undergo a 0_1 transition and then a 1_0 transition or vice versa. Each cell must be read after each transition.
2. For every pair of physically adjacent cell i and j the test writes cell i with and 1 and cell j with a 0 and then cell i with a 0 and cell j with a 1. It then reads after each write. To consider coupling faults between master/slave bits, cells i and j are written with the same data.
3. Each cell must be read twice after writing a 1 and a 0.
4. Decoder faults should be detected by writing unique data in every memory word and then reading the AF.
5. A special sequence of data patterns should be written and read to detect stuck-at faults in the read column decoder logic.
6. Some memory words should be written and read with data having different logic values on every pair of adjacent input data lines.

Pattern requirements for the non-SRAM portion of the AF

The following pattern requirements may be difficult to implement in silicon and may have to be applied functionally. Some of the patterns described in this section can be applied at the same time as the SRAM tests are being applied. The non-SRAM portion of the AF consists of the comparator, the source address exact/inexact match logic, the destination exact/inexact match logic, and the multiple match logic (which includes the priority encoder logic). The stuck-at fault model is the only fault model used in developing the pattern requirements for this portion of the AF. The other fault models discussed earlier were developed for memory arrays and it would not make sense to try to apply them to this section of the AF.

Comparator

The output of the comparator logic is the 32 match lines for each AF entry. The output of the comparator is further modified by the state of the personality bits. The comparator can be viewed as 32 48-bit wide comparators with one half of the inputs to each comparator supplied by the corresponding mask and data bits for each comparator, and the other half of the inputs to each comparator supplied by the comparand register. For the purpose of describing the data patterns necessary to test each comparator it will be assumed that all valid bits are set, all skip bits are reset and that either the SA or DA bits are set to allow a match operation to be visible outside the AF. The following table summarizes the truth table for a single bit of the comparator:

Table 1. Truth Table for the Comparator

MASK	DATA	COMP	MATCH
0	X	X	YES
1	0	0	YES
1	0	1	NO
1	1	0	NO
1	1	1	YES

1. The stuck-at 1 (s@1) condition in the mask bits for a comparator can be checked by first writing all mask bits to 0's, all data bits to 0's and the comparand register to all 1's. If any single mask bit is s@1, no match will occur otherwise a match will result as can be seen from the first line of table 1. To speed the testing for this condition, all entries can be tested in parallel if an all match indication is provided. All mask and data bits are written with 0's and compared simultaneously with the comparand. Each entry should match resulting in the all match condition. If any mask bit is s@1, the all match condition will not occur and the fault can be detected.
2. The stuck-at 0 (s@0) condition in the mask bits for a comparator are tested by the data patterns shown in the third and fourth lines of table 1. These lines are a subset of the patterns needed to test the XNOR faults that are represented by lines 2 through 5 of table 1. The outputs of the XNOR gates for each bit are all AND'ed together to form the match output of the comparator. The following test description will cover all stuck-at faults for the remainder of the comparator logic. These tests assume that all mask bits are written with 1's and assume the existence of an all match indication. The test is described in two parts:

Part #1

a) Write each data entry with all 0's.

b) Write the comparand register with all 0's.

c) Perform a match operation—should get an all match indication.

d) Repeat steps a through c but this time use all 1's. At this point half of the XNOR tests (lines 2 and 5 in table 1) have been completed and the AND circuitry has been tested for s@0 faults.

Part #2

a) Write each data entry with all 0's.

b) Do 48 matches while walking a 1 through a field of 0's in the comparand register. Since a single bit is in error for each match, a match condition should never occur.

c) Repeat steps a and b with each data entry being all 1's and walking a 0 through a field of 1's in the comparand. At this point, all the XNOR tests are completed. This also checks for s@1 faults in the AND circuitry since all but a single bit match. This test also tests for the mask bit s@0.

Source address exact/inexact logic:

The SRAM portion of this logic, namely the storage for the SA and SAX personality bits will be tested by the SRAM tests presented earlier. What remains to be tested is the logic that generates the source address match and the source address match exact logic. The test pattern description that follows does not yet take into account the impact of the SKIP bit since its use hasn't been completely determined as yet. The patterns also assume the existence of an all match indication as described earlier. The following table summarizes the patterns that need to be applied to check each entry match and exact indicators:

Table 2. Patterns necessary for match and exact indicators

SAX	VALID	SA	MATCH[i]	EXACT[i]	ALL MATCH?
1	1	1	1	1	YES
0	1	1	1	0	YES
1	0	1	0	0	NO
1	1	0	0	0	NO

The individual match lines for each entry must be OR'd together to determine if a match has occurred. The individual exact match lines must also be OR'd together to determine if an exact match has occurred. The pattern shown in the first line of the table will detect all s@0 faults on the logic that generates each match and exact line for an entry. It will also check for a s@0 fault on the final match and exact outputs. The pattern shown in the second line of the table will check for all s@1 faults arising from the SAX personality bits and will also detect a s@1 fault on the final exact output. The pattern shown in the third line of the table will check for s@1 faults on the VALID personality bits as well as on the final match and exact outputs. The final pattern shown in the fourth line of the table will check for s@1 faults on the SA personality bits as well as on the final match and exact outputs.

One could argue that the first pattern is not sufficient to cover all possible s@0 faults in the final OR'ing of the individual match and exact lines since these faults are detected on the assumption of the existence of an all match indication (an all exact indication is also necessary). The all match indicator is used to speed the testing of the AF since all entries can be written with the same values. If someone is uncomfortable with this potential loss in coverage, then an additional 32 patterns are needed that only apply the first pattern of the table to each entry by itself so that only one entry

causes the match and exact lines to be asserted. This pattern will take much longer to apply than the minimal set presented in table 2.

Destination address exact/inexact logic:

Since the destination address matching logic is identical to the source address matching logic, the same test can be applied as described in the previous section of this document. These tests can be applied simultaneously with the source address patterns.

PROGRAMMING METHODS

This section provides details of how the AF is intended to be used. This section provides a description of the methods to write entries into the AF, to find entries in the AF and to invalidate entries in the AF.

Writing Entries into the AF

In order for the AF to perform the function of matching addresses in network frames, the desired addresses must be loaded into the CAM portion of the AF. The following procedure should be followed to accomplish this operation.

1. Write the comparand value into the NP comparand registers. Note that the comparand register will retain any previous value if it is not overwritten.
2. Write the NP mask register if it is desired to mask any portion of the comparand. Note that the mask register will retain any previous value if it is not overwritten.
3. Write the NP personality register with the desired configuration of the SA, SAX, DA and DAX bits. The VALID bit must be set if this entry is to participate in any comparisons (either NP or network). If the VALID bit is not set, this entry may be overwritten when another entry is written to the CAM. The SKIP bit should be cleared if this it will be necessary to find this entry through the NP interface at a later time. Note that the personality register will retain any previous value if it is not overwritten.
4. Write the “Write CAM” instruction into the NP command register.
5. The status register should be read once the DONE bit is set to ensure that the ERROR bit was not set.

Note: *The ERROR bit in the status register will not be set if a “Write CAM” instruction is used when this bit is set. The user has to read this bit status before attempting to write an entry into the CAM.*

Finding Entries in the AF

Once a number of entries are resident in the AF, it may be necessary to find one or more of them. The process below should be used to perform this operation.

1. Load the value of the comparand that it is desired to find into the NP comparand register.
2. Write the “Find” instruction into the NP command register. Note: the comparand is not modified by the NP mask registers.
3. Read the NP status register when the DONE bit is set. If the FOUND bit is set, there is at least one matching entry in the AF that does not have its SKIP bit set. If the MULT bit is also set, there is more than one entry that matches the comparand that does not have the SKIP bit set.

Invalidating Entries in the AF

In conjunction with managing the contents of the AF, it may be required to remove entries. This process is called “invalidation.” To invalidate an entry in the AF, the following steps should be followed.

1. Load the NP comparand register with the value of the AF entry that is to be removed.
2. Write the “Find” instruction into the NP command register.
3. When the DONE bit is set, read the NP status register. Do one of the following:

3a. If the FOUND bit is not set, there is no entry in the AF that matches the comparand that does not have its SKIP bit set.

3b. If the FOUND bit is set and the MULT bit is not set, there is only one entry in the AF that matches the comparand that does not have its SKIP bit set. Write the “Invalidate” instruction into the NP command register.

3c. If the FOUND and MULT bits are set, there is more than one entry in the AF that matches the comparand that does not have its SKIP bit set. If all of these entries should be invalidated, write the “Invalidate” instruction followed by the “Find” instruction into the NP command register repeatedly until the FOUND bit is not set in the NP status register. If only one of the multiple matching entries should be invalidated, write the “Read CAM” instruction to the NP command register, compare the contents read back from the CAM to the desired comparand, mask and personality. If the currently matching AF entry is the one that should be invalidated, write the “Invalidate” instruction to the NP command register. If the currently matching AF entry should not be invalidated, write the “Skip” instruction to the NP command register and repeat the invalidate process from the beginning.

4. Write the “Clear all SKIP” instruction to the NP command register.

PDX FUNCTIONAL DISCRIPTION

Introduction

The PDX is a digital CMOS core that is used in SUPERNET 3. It employs new circuit techniques to achieve clock and data recovery.

Traditionally, Phase-Locked-Loops (PLL) are used for the purpose of clock recovery in data communication areas. There are both analog and digital versions of the PLL components such as phase detector, filter, charge pump. A traditional PLL always contains a voltage-controlled oscillator (VCO) to regenerate a clock which is frequency synchronized to and phase aligned with the received data.

The PDX employs techniques that are significantly different from the traditional PLL. Not only are the control functions completely digital, the VCO function is also replaced by a proprietary delay-line technique. The result is a highly integratable core which can be manufactured in a standard digital CMOS process.

The PDX transmitter serializes encoded NRZ symbols. The clock multiplier circuit generates a bit rate (125 MHz) clock from the LSCLK reference. The serial data stream is converted into NRZI for output to the PMD transceiver.

The PDX receiver uses the clock recovery circuit to extract clock information from the received data. The recovered clock is used to operate the serial-to-parallel conversion logic.

PDX FUNCTIONAL DESCRIPTION

The PDX accepts 4B5B encoded data symbols scramble or non-scrambled from the PLC-S core at TDAT 4–0 inputs. The 5-bit symbol is clocked into the PDX by the rising edge of LSCLK, serialized, converted to NRZI format and shifted to the outputs. The TX+/TX– pair carries PECL-compatible differential NRZI data to the fiber optic transmitter or to the twisted-pair transceiver interface.

The PDX uses LSCLK as the frequency reference to generate the serial link data rate. The external clock source must be crystal controlled and continuous. All of the internal logic of PDX runs on internal clocks that are derived from the external reference source or extracted from the received data. The PDX's clock multiplier is referenced to the rising edges of LSCLK only.

In order to generate the serial output waveforms conforming to the FDDI specifications, the external reference clock must meet FDDI frequency and stability requirements. Under normal conditions, the frequency of LSCLK must be within the FDDI specified ±50 ppm of the received data for the PDX to operate optimally. (***Note:*** *The 50 ppm is the tolerance of the crystal-controlled source.*)

The TX+/TX– serial outputs comply to the FDDI SMF-PMD jitter allocation and typically contains less than 0.4 ns peak-to-peak jitter at 125 MBaud.

The PDX accepts encoded PECL NRZI signal levels at the RX+/RX– inputs and converts them to NRZ format. The receiver circuit recovers data from the input stream by regenerating clocking information embedded in the serial stream. The PDX then clocks the unframed symbol (5 bits) to the RDAT 4–0 interface on the falling edge of RSCLK to the PLC-S core.

The PDX receiver uses advanced circuit techniques to extract embedded clock information from the serial input stream and recovers the data. Its operating frequency is established by the reference at LSCLK. The PDX is capable of tracking data correctly within 1000 ppm of LSCLK (exceeds the frequency range defined by the FDDI specification). FDDI 4B5B encoding scheme ensures run-length limitation and adequate transition density of the encoded data stream, while TP-PMD achieves this on a statistical basis through data scrambling. The PDX clock recovery circuit is designed to meet and exceed a worst-case run-length tolerance of 60-bits in order to function correctly with both fiber-optic and twisted-pair PMDs. The actual run-length tolerance is more than 1000 bits due to the unique data recovery technique.

The PDX receiver has input jitter tolerance characteristics that meet or exceed the recommendations of Physical Layer Medium Dependent (PMD) FDDI document. Typically, at 125 MBaud (8 ns/bit), the peak-to-peak Duty-Cycle Distortion (DCD) tolerance is 1.4 ns, the peak-to-peak Data Dependent Jitter (DDJ) tolerance is 2.2 ns, and the peak-to-peak Random Jitter (RJ) tolerance is 2.27 ns. The total combined peak-to-peak jitter tolerance is typically 5 ns with bit error rate (BER) better than 2.5×10^{-10}.

Default Timer and Register Values

The following are the default timer/register values on power-up reset.

Timer/Register	NPADDR	Default Value	Actual Time Value
MIR (1–0) register	12h & 13h	00 00 00 00h	-NA-
TMAX register	14h	03C7h	165.29664 ms
TVX register and timer	15h	85h	3.4068 ms
TRT timer (bit 20–5)	16h	03C7h[*1]	165.29664 ms
THT timer	17h	FFFFh[*2]	-NA-
TNEG register (bit 20–5)	18h	03C7h	165.29664 ms
TMRS register	19h	801Fh	-NA-
TREQ0 register	1ah	78E0h	165.29664 ms
TREQ1 register	1bh	0000h[*3]	
TPRI(1–0) register	1c & 1d	FFFFh	-NA-
TSYNC register	1fh	0000h	-NA-
TMSYNC timer	40h	FA97h[*1]	3.5456 ms (2xDMAX when ring not operational)
CMDREG1	00h	0000h	-NA-
CMDREG2	01h	0000h	-NA-
ST1U	00h	0000h	-NA-
ST1L	01h	0007h	-NA-
ST2U	02h	4000h	-NA-
ST2L	03h	0000h	-NA-
ST3U	61h	4000h	-NA-
ST3L	62h	0000h	-NA-
IMSK1U	04h	FFFFh	-NA-
IMSK1L	05h	FFFFh	-NA-
IMSK2U	06h	FFFFh	-NA-
IMSK2L	07h	FFFFh	-NA-
IMSK3U	63h	FFFFh	-NA-
IMSK3L	64h	FFFFh	-NA-
IVR	65h	0000h	-NA-
IMR	66h	0000h	-NA-
SAID	08h	0000h	-NA-
LAIM	09h	0000h	-NA-
LAIC	0ah	0000h	-NA-
LAIL	0bh	0000h	-NA-
SAGP	0ch	0000h	-NA-
LAGM	0dh	0000h	-NA-
LAGC	0eh	0000h	-NA-
LAGL	0fh	0000h	-NA-

Timer/Register	NPADDR	Default Value	Actual Time Value
MDREG1	10h	0080h	-NA-
MDREG2	20h	8000h	-NA-
MDREG3	60h	0000h	-NA-
STMCHN	11h	xxx0 0000 0000 0000b	Bits 15, 14, 13 are for the revision number.
FCNTR	41h	0000h	-NA-
LCNTR	42h	0000h	-NA-
ECNTR	43h	0000h	-NA-
FSCNTR	44h	0000h	-NA-
EACB, EARV1, EAS, EAA0, EAA1, EARV2	22h, 23h, 24h, 25h, 26h, 6bh	unknown	-NA-
SACL, SABC	28h & 29h	unknown	-NA-
RPR1, WPR1, SWPR1	2dh, 2eh, 2fh	unknown	-NA-
RPR2, WPR2, SWPR2	68h, 69h, 6ah	unknown	-NA-
WPXS, WPXA0, WPXA1	30h, 31h, 32h	unknown	-NA-
SWPXS, SWPXA0, SWPXA1	34h, 35h, 36h	unknown	-NA-
RPXS, RPXA0, RPXA1	38h, 39h, 3ah	unknown	-NA-
MARR, MARW	3ch, 3dh	unknown	-NA-
WPXSF, RPXSF	2ah, 2bh	unknown	-NA-
FRMTHR	21h	0000h	-NA-

Notes:

**1 Lower 5 bits are all zero.*

**2 Lower 5 bits are all one.*

**3 Only lower 5 bits are valid.*

SUPERNET 3 REGISTERS

SUPERNET 3 Programmable Registers

Register Mnemonic	NPADDR7–0	Description
“cmdreg1”	“00”	Load the Command register 1 instruction
“cmdreg2”	“01”	Load the Command register 2 instruction
“st1u”	“00”	Upper 16 bits of status register 1 (Read Only)
“st1l”	“01”	Lower 16 bits of status register 1 (Read Only)
“st2u”	“02”	Upper 16 bits of status register 2 (Read Only)
“st2l”	“03”	Lower 16 bits of status register 2 (Read Only)
“imsk1u”	“04”	Upper 16 bits of IMSK register 1
“imsk1l”	“05”	Lower 16 bits of IMSK register 1
“imsk2u”	“06”	Upper 16 bits of IMSK register 2
“imsk2l”	“07”	Lower 16 bits of IMSK register 2
“said”	“08”	Short Address—individual
“laim”	“09”	Long Address, individual (MSW of LAID)
“laic”	“0a”	Long Address, individual (middle of LAID)
“lail”	“0b”	Long Address, individual (LSW of LAID)
“sagp”	“0c”	Short Address—group
“lagm”	“0d”	Long Address, group (MSW of LAGP)
“lagc”	“0e”	Long Address, group (middle of LAGP)
“lagl”	“0f”	Long Address, group (LSW of LAGP)
“mod1”	“10”	Mode Register 1
“stmchn”	“11”	State Machine register
“mir1”	“12”	Upper 16 bits—MAC information register (Read Only)
“mir0”	“13”	Lower 16 bits—MAC information register (Read Only)
“tmax”	“14”	TMAX register
“tvx”	“15”	TVX register
“trt”	“16”	Upper 16 bits of TRT timer
“tht”	“17”	Upper 16 bits of THT timer
“tneg”	“18”	Upper 16 bits of TNEG register
“tmrs”	“19”	Lower 5 bits of TNEG, TRT, THT timers Bit 14–10—Lower 5 bits of TNEG Bit 9–5—Lower 5 bits of TRT Bit 4–0—Lower THT timer Bit 15 is the Late Count
“treq0”	“1a”	Station’s LSW of requested TRT
“treq1”	“1b”	Station’s MSW of requested TRT
“pri0”	“1c”	Priority register for ASYNC0

SUPERNET 3 Programmable Registers (continued)

Register Mnemonic	NPADDR7–0	Description
“pri1”	“1d”	Priority register for ASYNC1
“pri2”	“1e”	Reserved
“tsync”	“1f”	TSYNC register
“mod2”	“20”	Mode register 2
“frmthr”	“21”	Frame threshold register
“eacb”	“22”	End Address of Claim/Beacon area
“earv1”	“23”	End Address of receive queue
“eas”	“24”	End Address of synchronous queue
“eaa0”	“25”	End Address of asynchronous queue 0
“eaa1”	“26”	End Address of asynchronous queue 1
“eaa2”	“27”	Reserved
“sacl”	“28”	Start Address of Claim frame
“sabc”	“29”	Start Address of Beacon frame
“wpxsf”	“2a”	Write pointer for special frames
“rpxsf”	“2b”	Read pointer for special frames
“rpr1”	“2d”	Read Pointer for receive queue
“wpr1”	“2e”	Write pointer for receive queue
“swpr1”	“2f”	Shadow write pointer for receive queue
“wpxs”	“30”	Write pointer for synchronous queue
“wpxa0”	“31”	Write pointer for asynchronous queue 0
“wpxa1”	“32”	Write pointer for synchronous queue 1
“wpxa2”	“33”	Reserved
“swpxs”	“34”	Shadow write pointer for synchronous queue
“swpxa0”	“35”	Shadow write pointer for asynchronous queue 0
“swpxa1”	“36”	Shadow write pointer for asynchronous queue 1
“swpxa2”	“37”	Reserved
“rpxs”	“38”	Read pointer for synchronous queue
“rpxa0”	“39”	Read pointer for asynchronous queue 0
“rpxa1”	“3a”	Read pointer for asynchronous queue 1
“rpxa2”	“3b”	Reserved
“marr”	“3c”	Memory read address register
“marw”	“3d”	Memory write address register
“mdru”	“3e”	Upper 16 bits of memory data register
“mdrl”	“3f”	Lower 16 bits of memory data register
“tmsync”	“40”	TMSYNC register

SUPERNET 3 Programmable Registers (continued)

Register Mnemonic	NPADDR7–0	Description
“fcntr”	“41”	Frame Counter
“lcntr”	“42”	Lost Counter
“ecntr”	“43”	Error Counter
“fscntr”	“44”	Frame Strip Counter
“frselreg”	“45”	Frame Selection Register
“46”	“46”	
“47”	“47”	
“48”	“48”	
“49”	“49”	
“4a”	“4a”	
“4b”	“4b”	
“4c”	“4c”	
“4d”	“4d”	
“4e”	“4e”	
“4f”	“4f”	
“50l”	“50”	
“51”	“51”	
“52”	“52”	
“53”	“53”	
“54”	“54”	
“55”	“55”	
“56”	“56”	
“57”	“57”	
“58”	“58”	
“59”	“59”	
“5a”	“5a”	
“5b”	“5b”	
“5c”	“5c”	
“5d”	“5d”	
“5e”	“5e”	
“5f”	“5f”	
“mdreg3”	“60”	Mode register 3
“st3u”	“61”	Upper 16 bits of status register 3 (Read Only)
“st3l”	“62”	Lower 16 bits of status register 3 (Read Only)
“imsk3u”	“63”	Upper 16 bits of IMSK register 3

SUPERNET 3 Programmable Registers (continued)

Register Mnemonic	NPADDR7–0	Description
“imsk3l”	“64”	Lower 16 bits of IMSK register 3
“ivr”	“65”	Interrupt Vector register (Read Only)
“imr”	“66”	Interrupt mask register
“ilr”	“67”	(Hidden)
“rpr2”	“68”	Read pointer for second receive queue
“wpr2”	“69”	Write pointer for second receive queue
“swpr2”	“6a”	Shadow write pointer for second receive queue
“earv2”	“6b”	End Address of Receive 2 Queue
“unlckdly”	“6c”	Auto Unlock Delay Register
“6d”	“6d”	
“6e”	“6e”	
“lwpr1”	“6f”	(Hidden)
“lrwd1”	“70”	(Hidden)
“lwpr2”	“71”	(Hidden)
“lrwd2”	“72”	(Hidden)
“fifoflag”	“73”	(Hidden)
“74”	“74”	
“75”	“75”	
“76”	“76”	
“77”	“77”	
“78”	“78”	
“ltdpa1”	“79”	Last Transmit Descriptor Pointer for Async 1 queue
“lsa0”	“7a”	(Hidden)
“lss”	“7b”	(Hidden)
“7c”	“7c”	
“7d”	“7d”	
“7e”	“7e”	
“7f”	“7f”	
“plc_cntrl_a”	“80”	PLC–S control register A
“plc_cntrl_b”	“81”	PLC–S control register B
“intr_mask”	“82”	PLC–S interrupt mask register
“xmit_vector”	“83”	PLC–S transmit vector register
“vector_length”	“84”	PLC–S vector length register
“le_threshold”	“85”	PLC–S link error threshold register

SUPERNET 3 Programmable Registers (continued)

Register Mnemonic	NPADDR7–0	Description
“c_min”	“86”	PLC–S Connect state timer register
“tl_min”	“87”	PLC–S line state transmit timer register
“tb_min”	“88”	PLC–S break state timer register
“t_out”	“89”	PLC–S signalling timeout register
“plc_cntrl_c”	“8a”	PLC_S control register C
“lc_length”	“8b”	PLC–S link confidence test timer register
“t_scrub”	“8c”	PLC–S scrub timer register
“ns_max”	“8d”	PLC–S noise timer register
“tpc_load_value”	“8e”	PLC–S TPC timer load register (Write Only)
“tne_load_value”	“8f”	PLC–S TNE timer load register (Write Only)
“plc_status_a”	“90”	PLC–S status register A (Read Only)
“plc_status_b”	“91”	PLC–S status register B
“tpc”	“92”	PLC–S TPC (Read Only)
“tne”	“93”	PLC–S TNE (Read Only)
“clk_div”	“94”	PLC–S clk_div register (Read Only)
“bist_signature”	“95”	PLC–S BIST signature (Read Only)
“rcv_vector”	“96”	PLC–S PCM receive vector register (Read Only)
“intr_event”	“97”	PLC–S interrupt event register (Read Only)
“viol_sym_ctr”	“98”	PLC–S violation symbol counter (Read Only)
“min_idle_ctr”	“99”	PLC–S minimum idle counter (Read Only)
“link_err_ctr”	“9a”	PLC–S link error counter (Read Only)
	“9b – af”	Reserved for future use
“afcmd”	“b0”	Address Filter Command Register
“afstat”	“b2”	Address Filter Status Register
“afbist”	“b4”	Address Filter BIST Signature
“afcomp2”	“b6”	Address Filter Comparand 2 Register
“afcomp1”	“b8”	Address Filter Comparand 1 Register
“afcomp0”	“ba”	Address Filter Comparand 0 Register
“afmask2”	“bc”	Address Filter Mask 2 Register
“afmask1”	“be”	Address Filter Mask 1 Register
“afmask0”	“c0”	Address Filter Mask 0 Register
“afpers”	“c2”	Address Filter Personality Register
	“c3 – cf”	Reserved for future use

SUPERNET 3 Programmable Registers (continued)

Register Mnemonic	NPADDR7–0	Description
“orstat”	“d2”	PDX Status Register
	“d3–df”	Reserved for future use

SUPERNET 3 COMMAND REGISTERS

SUPERNET 3 Command Registers 1

Instruction Name	Code	Mnemonic
Software Reset	01h	
Load MDR from buffer memory with MARR increment	02h	IRMEMWI
Load MDR from buffer memory without MARR increment	03h	IRMEMWO
Idle/Listen	04h	
Claim/Listen	05h	
Beacon/Listen	06h	
Load TVX timer from TVX register	07h	
Nonrestricted Token Mode	08h	
Enter Nonrestricted Token Mode	09h	
Enter Restricted Token Mode	0Ah	
Restricted Token Mode	0Bh	
Send Unrestricted Token	0Ch	
Send Restricted Token	0Dh	
Enter Send-Immediate Mode	0Eh	
Exit Send- Immediate Mode	0Fh	
Clear Synchronous Queue Lock	11h	
Clear Asynchronous Queue 0 Lock	12h	
Clear Asynchronous Queue 1 Lock	14h	
Reserved	18h	
Clear Receive Queue 1 Lock	20h	
Clear Receive Queue 2 Lock	21h	
Tristate X Bus (in SAS only)	22h	
Drive X Bus	23h	
Clear All Queue Locks	3Fh	

SUPERNET 3 Command Registers 2

Instruction Name	Code	Mnemonic
Reserved	01h	
Reserved	02h	
Reserved	04h	
Reserved	08h	
Abort Current Transmit Activity	10h	
Reset Transmit Queues	20h	
Set Tag Bit	30h	
Reserved	40h	
Transmit Command	50h	

Revision I.D.

The bits 13, 14, 15 of the State Machine Register provides a three-bit binary value that indicates the revision number of the SUPERNET 3. The revision I.D. shall be '111' for the first revision.

The PLC_STATUS_A register, bit 15–11, provides a five-bit binary value that indicates the revision number of the PLC-S block within the SUPERNET 3. The revision I.D. shall be '01111'.

The AFSTAT register, bit 7–5, provides a three-bit binary value that indicates the revision number of the Address Filter block. The revision I.D. shall be '111'.

The ORSTAT register, bit 2–0, provides a three-bit binary value that indicates the revision number of the PDX block. The revision I.D. shall be '111'. All other bits of ORSTAT register are reserved.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature . . . . . 0°C to +70°C

Supply Voltage
Referenced to V_{SS} . . . . . –0.3 V to +6.0 V

DC Voltage applied to any
Pin Referenced to V_{SS} . . . . . –0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Temperature, T_A . . . . . 0°C to +70°C

Supply Voltages, V_{CC} . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

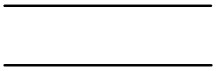
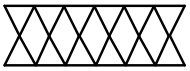
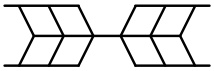
DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{IL}	Input Low Voltage (Note1)		V_{CC}–1.81	V_{CC}–1.475	V
V_{IH}	Input High Voltage (Note 1)		V_{CC}–1.165	V_{CC}–0.88	V
I_{IL}	Input Low Current (Note 9)	V_{CC} = Maximum, V_{IN} = 0.5 V		–200	µA
I_{IH}	Input High Current (Note 9)	V_{CC} = Maximum, V_{IN} = 2.7 V		–100	µA
I_{OZ}	Output Leakage Current (Note 10)	0.4 V < V_{OUT} < V_{CC}	–10	10	µA
V_{OH}	Output High Voltage (Note 2)	PECL Load (Note 3)	V_{CC}–1.025	V_{CC}–0.6	V
V_{OL}	Output Low Voltage (Note 2)	PECL Load (Note 3)	V_{CC}–1.81	V_{CC}–1.62	V
V_{OL}	Output Low Voltage	I_{OL} = Maximum		0.4	V
V_{OH}	Output High Voltage (Note 4)	I_{OH} = –I_{OL}/2	2.4		V
I_{OL}	Output Low Current (Note 5)			8.0	mA
I_{OL}	Output Low Current (Note 6)			4.0	mA
I_{OH}	Output High Current			–I_{OL}/2	mA
I_{OZ}	Output Leakage Current (Note 7)	0.4 V < V_{OUT} < V_{CC}	–10	10	µA
I_{IX}	Input Leakage Current (Note 8)	0 V < V_{IN} < V_{CC}	–10	10	µA
I_{CC}	Power Supply Current	V_{CC} = Maximum		400	mA

Notes:

1. *Applies to PECL inputs only RX+ ,RX–, SDI+,SDI–.*
2. *Applies to PECL outputs only TX+,TX–.*
3. *Tested for V_{CC} = Minimum, shown limits are specified over entire V_{CC} operating range.*
4. *V_{OH} does not apply to open-drain pins* $\overline{\text{READY}}$, $\overline{\text{MINTR}}$*[4:1].*
5. *An I_{OL} value of 8.0 mA applies to the following signals:*
   ADDR[15:0], $\overline{\text{WR}}$, $\overline{\text{RD}}$, *BD[31:0], BDP[3:0], BDTAG,* $\overline{\text{CSO}}$, $\overline{\text{MINTR}}$*[4:1], and* $\overline{\text{READY}}$.
6. *An I_{OL} value of 4.0 mA applies to all signals except those listed in Note 5.*
7. *I_{OZ} applies to all three-state output pins and bidirectional pins.*
8. *I_{IX} applies to all non-PECL input-only pins.*
9. *I_{IL}, I_{IH} applies to all TTL pins.*
10. *I_{OZ} applies to TDO.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don’t Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance “Off” State

KS000010

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

Clocks

No.	Parameter Symbol	Parameter Description	Min	Max	Unit
1	t_{PER}	LSCLK Period	40	40	ns
2	t_{PWH}	LSCLK High Pulse Width	18	22	ns
3	t_{PWL}	LSCLK Low Pulse Width	18	22	ns
4	t_{PER}	BCLK Period	80	80	ns
5	t_{PWH}	BCLK High Pulse Width	35	45	ns
6	t_{PWL}	BCLK Low Pulse Width	35	45	ns
7	t_{PER}	BMCLK Period (BMCLK tied to BCLK)	80	80	ns
8	t_{PWH}	BMCLK High Pulse Width (BMCLK tied to BCLK)	35	45	ns
9	t_{PWL}	BMCLK Low Pulse Width (BMCLK tied to BCLK)	35	45	ns
10	t_{PER}	BMCLK Period (BMCLK tied to LSCLK)	40	40	ns
11	t_{PWH}	BMCLK High Pulse Width (BMCLK tied to LSCLK)	18	22	ns
12	t_{PWL}	BMCLK Low Pulse Width (BMCLK tied to LSCLK)	18	22	ns
13	t_{SK}	BMCLK to BCLK Skew (BMCLK tied to BCLK)	0	0	ns
14	t_{SK}	BMCLK to LSCLK Skew (BMCLK tied to LSCLK)	0	0	ns
15	t_{SK}	LSCLK to BCLK Skew	0	10	ns

SWITCHING WAVEFORMS

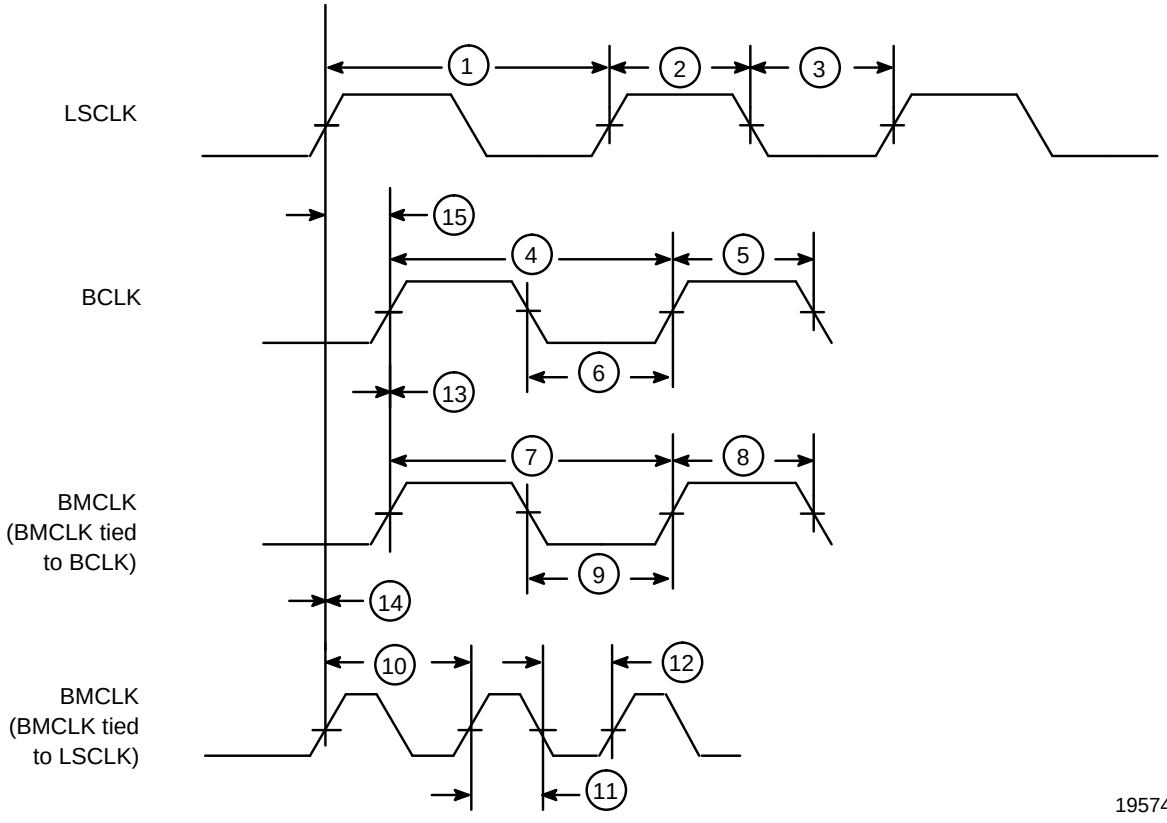


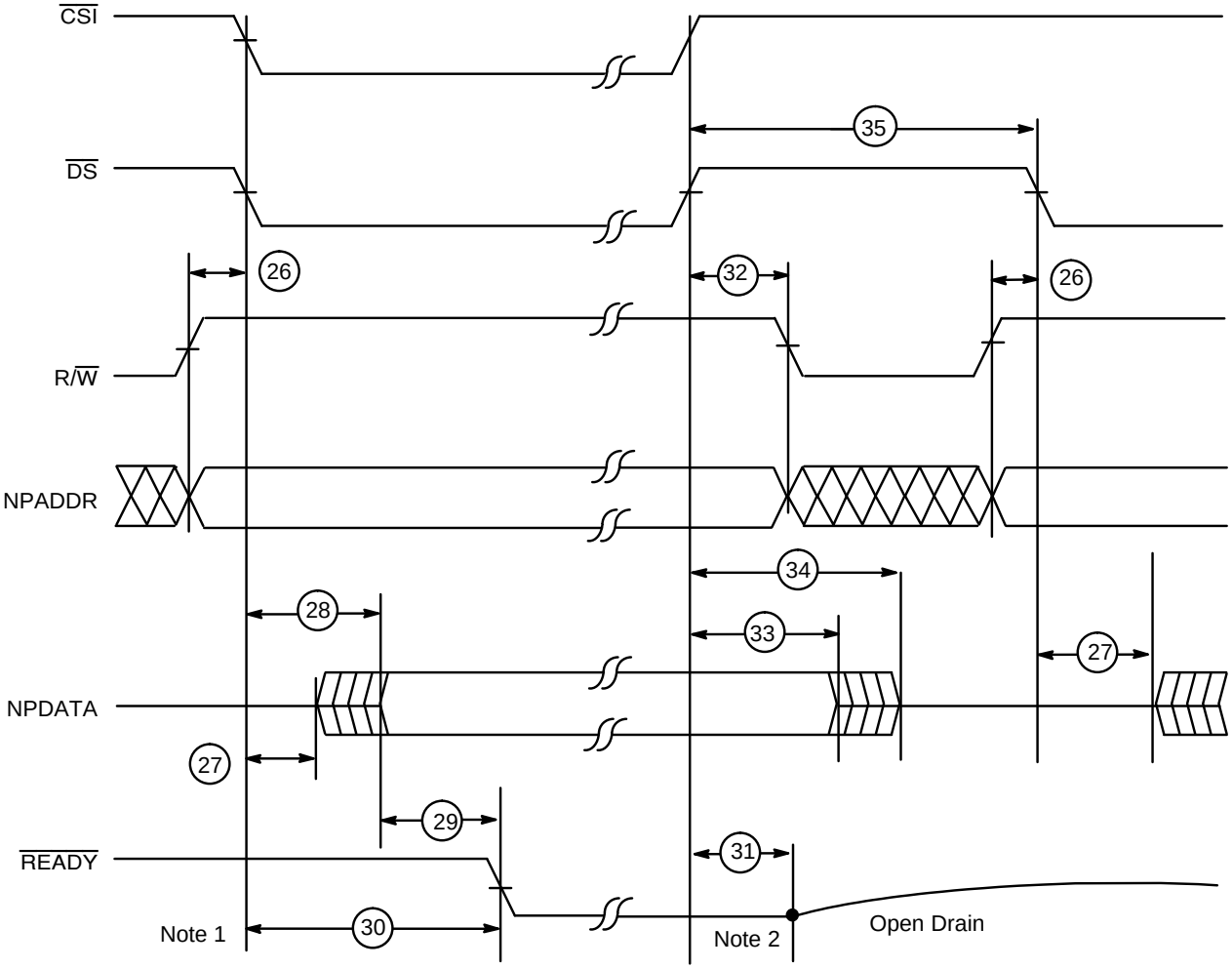
Figure 28. Clock Timings

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

NP

No.	Parameter Symbol	Parameter Description	Min	Max	Unit
26	t_S	R/$\overline{W}$ and NPADDR[7:0] Setup Time to $\overline{DS}$ ($\overline{CSI}$) Low	0		ns
27	t_{EN}	$\overline{DS}$($\overline{CSI}$) Low to NPDATA[15:0] Enabled (Asynchronous Read)	0		
28	t_{PD}	$\overline{DS}$($\overline{CSI}$) Low to NPDATA[15:0] Valid (Asynchronous Read)		275	ns
29	t_S	NPDATA[15:0] Setup Time before $\overline{READY}$ Low (Asynchronous Read)	15		ns
30	t_{PD}	$\overline{DS}$ ($\overline{CSI}$) Low to $\overline{READY}$ Low		310	ns
31	t_Z	$\overline{DS}$ ($\overline{CSI}$) High to $\overline{READY}$ Deasserted		35	ns
32	t_H	R/$\overline{W}$ and NPADDR[7:0] Hold Time from $\overline{DS}$ ($\overline{CSI}$) High	0		ns
33	t_{INV}	NPDATA[15:0] Invalid from $\overline{DS}$ ($\overline{CSI}$) High (Asynchronous Read)	5		
34	t_Z	$\overline{DS}$($\overline{CSI}$) High to NPDATA[15:0] Deasserted		35	ns
35	t_{PWH}	$\overline{DS}$ High to $\overline{DS}$ Low (Asynchronous Read/Write Recovery Time)	100		ns
36	t_S	NPDATA[15:0] Setup Time to $\overline{DS}$ ($\overline{CSI}$) Low (Asynchronous Write)	–60		ns
37	t_H	NPDATA[15:0] Hold Time from $\overline{DS}$ ($\overline{CSI}$) High (Asynchronous Write)	0		ns
38	t_S	$\overline{CSI}$ Setup Time to BCLK	10		ns
39	t_H	$\overline{CSI}$ Hold Time to BCLK	10		ns
40	t_S	R/$\overline{W}$ and NPADDR[7:0] Setup Time to BCLK	10		ns
41	t_H	R/$\overline{W}$ and NPADDR[7:0] Hold Time to BCLK	10		ns
42	t_Z	BCLK to NPDATA[15:0] Deasserted		30	ns
43	t_{EN}	BCLK to NPDATA[15:0] Enabled	2		ns
44	t_{PD}	BCLK to NPDATA[15:0] Valid		30	ns
45	t_{INV}	BCLK to NPDATA[15:0] Invalid	2		ns
46	t_S	NPDATA[15:0] Setup Time to BCLK	30		ns
47	t_H	NPDATA[15:0] Hold Time to BCLK	20		ns
48	t_{PD}	BCLK LOW to $\overline{READY}$ LOW		25	ns
49	t_Z	BCLK HIGH to $\overline{READY}$ Deasserted		35	ns
50	t_{PD}	BCLK to $\overline{MINTR}$[4:1] Valid		25	ns
51	t_Z	BCLK to $\overline{MINTR}$[4:1] Deasserted		25	ns
52	t_{PWL}	$\overline{RST}$ Pulse Width Low	(20*t_{PER}4)		ns
53	t_S	NPMEMREQ Setup Time to BMCLK	15		ns
54	t_H	NPMEMREQ Hold Time to BMCLK	10		ns
55	t_{PD}	BMCLK to NPMEMACK High		20	ns
56	t_{PD}	BMCLK to NPMEMACK Low		20	ns
57	t_{PD}	BMCLK High to $\overline{CSO}$, $\overline{RD}$, $\overline{WR}$, ADDR15–0 Disabled		30	ns

SWITCHING WAVEFORMS



Notes:

1. *26, 27, 28, and 30 are measured from* $\overline{\text{CSI}}$ *or* $\overline{\text{DS}}$ *whichever goes LOW last.*
2. *31, 33, 34, and 32 are measured from* $\overline{\text{CSI}}$ *or* $\overline{\text{DS}}$ *whichever goes HIGH first.*

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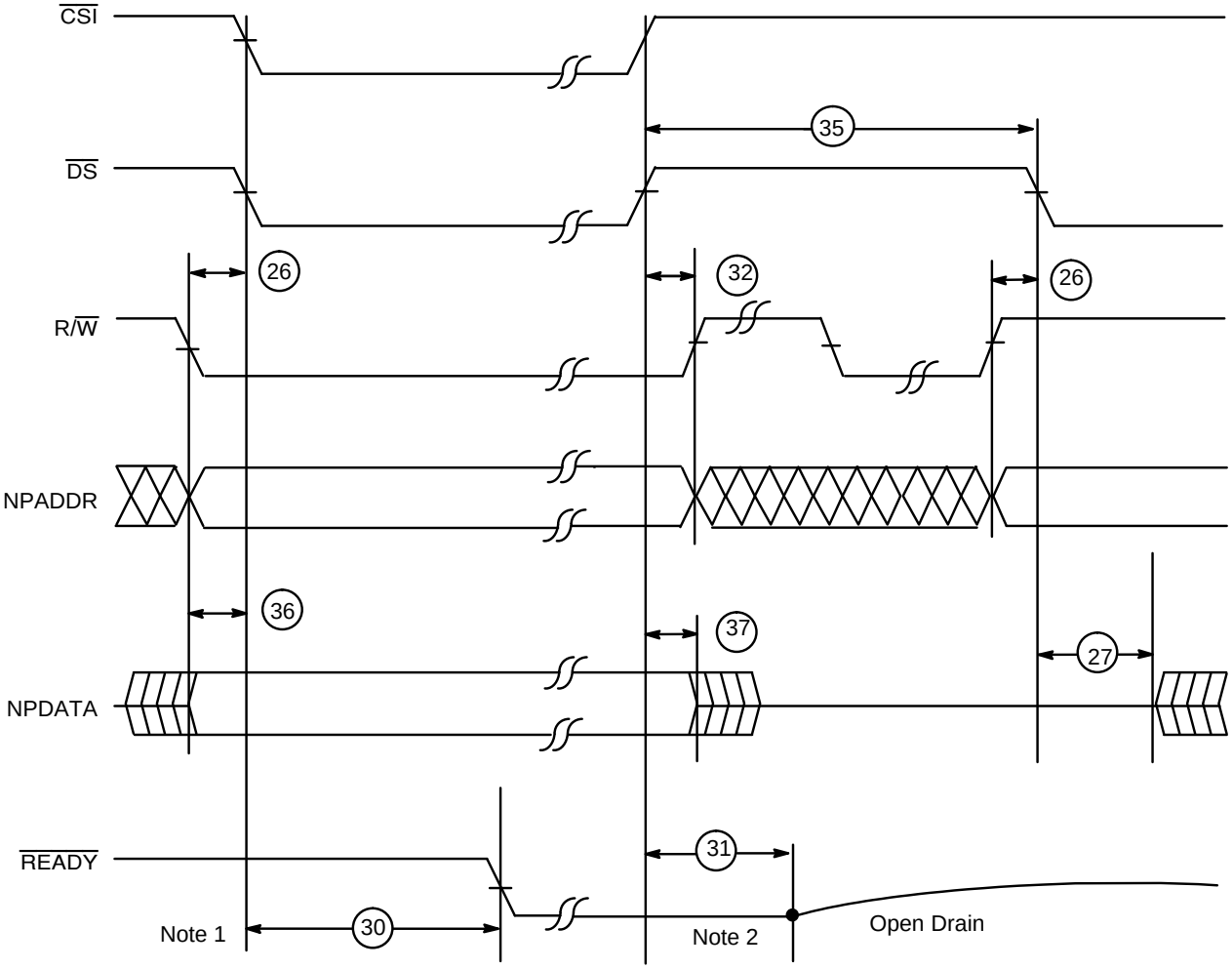
Figure 29. NP Asynchronous Read

SWITCHING WAVEFORMS



Notes:

1. *26, 36, and 30 are measured from* $\overline{\text{CSI}}$ *or* $\overline{\text{DS}}$ *whichever goes LOW last.*
2. *31, 32, and 37 are measured from* $\overline{\text{CSI}}$ *or* $\overline{\text{DS}}$ *whichever goes HIGH first.*

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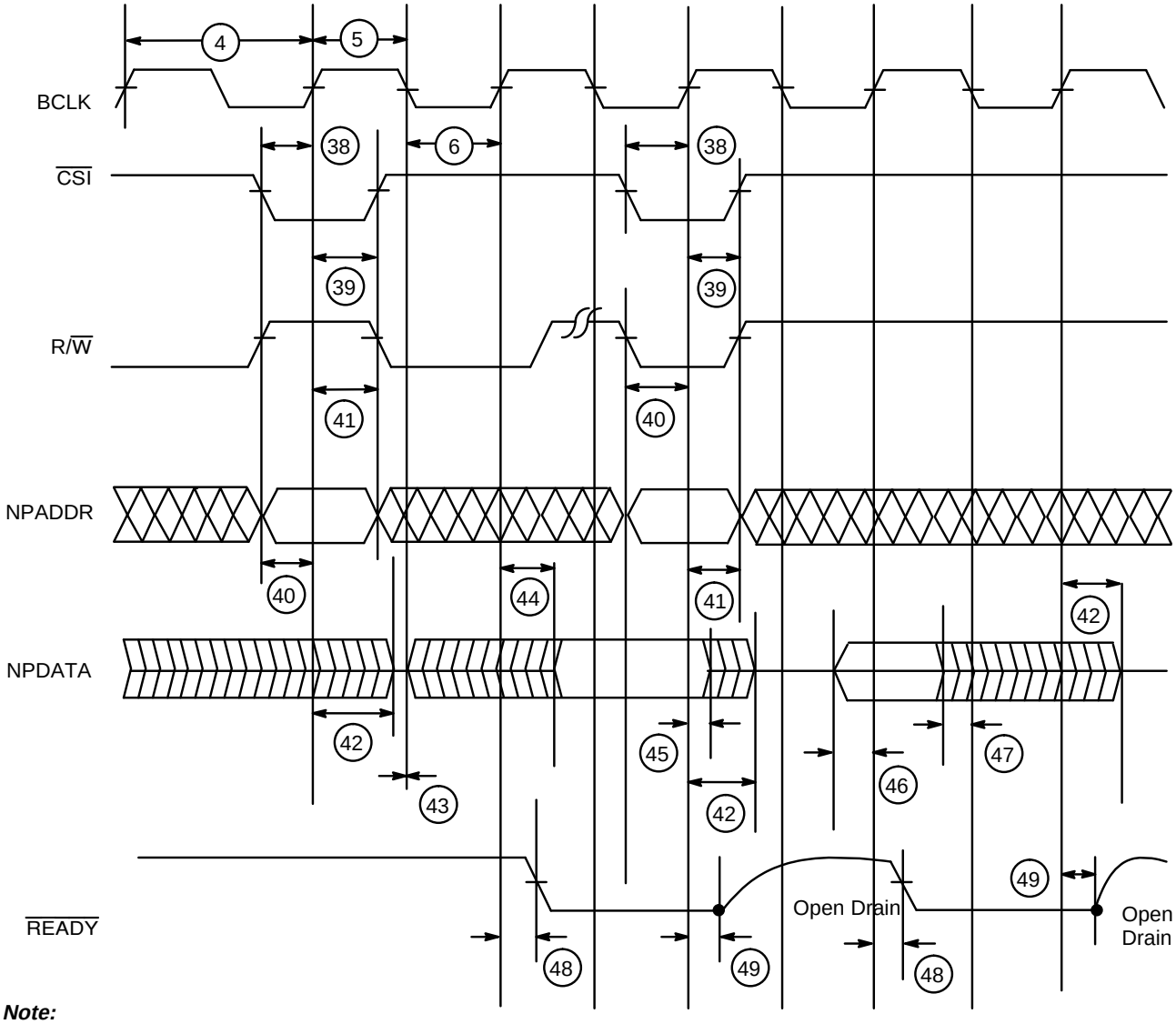
Figure 30. NP Asynchronous Write

SWITCHING WAVEFORMS



Note:

1. DS is ignored in Synchronous mode and should be inactive (High) during all Synchronous accesses.

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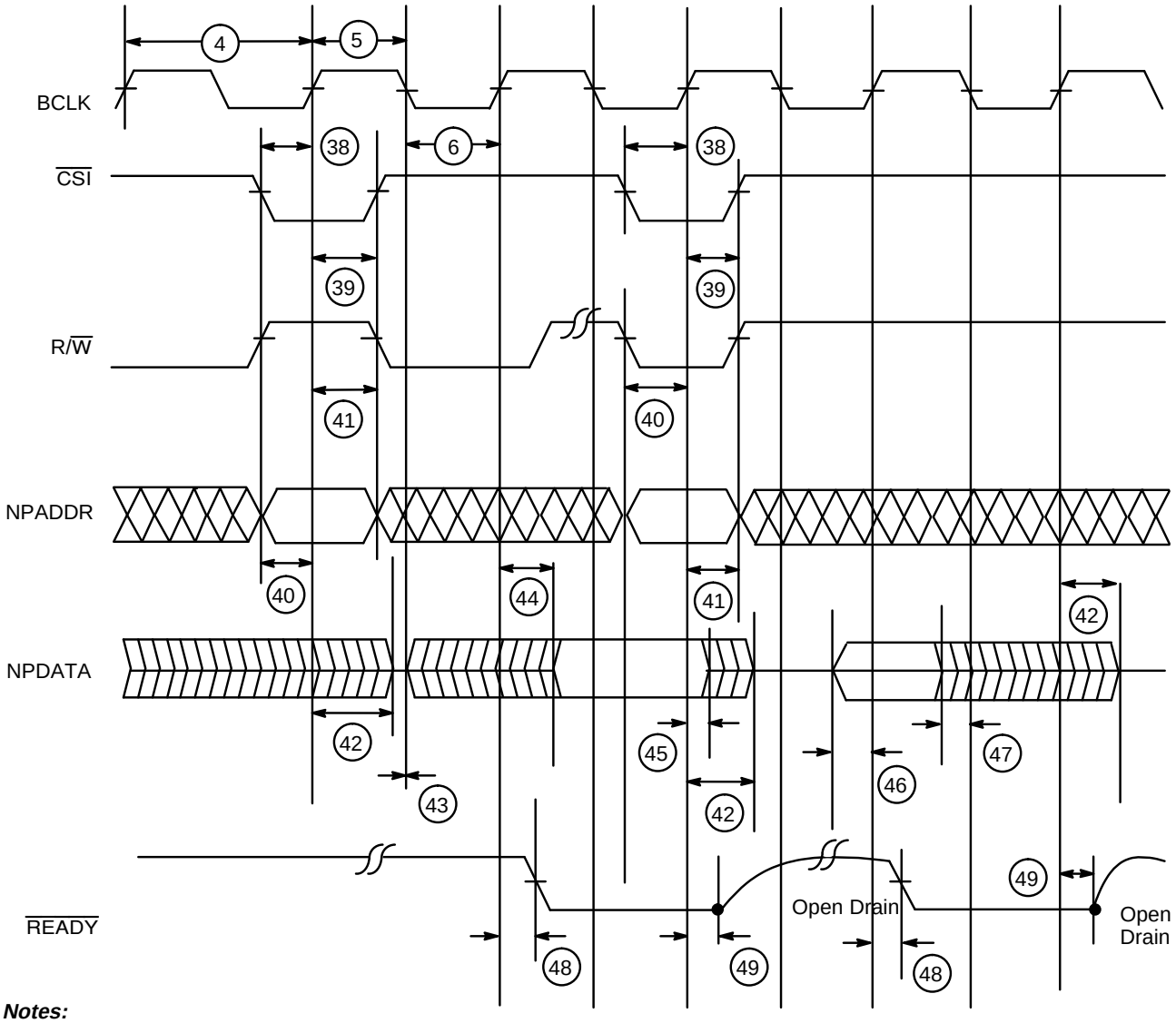
Figure 31. NP Synchronous Read and Write Except MDR Accesses



Notes:

1. $\overline{DS}$ *is ignored in Synchronous mode and should be inactive (High) during all Synchronous accesses.*

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2. *Read and Write Cycles could extend beyond two clock cycles.*

Figure 32. NP Synchronous Read and Write MDR Accesses

SWITCHING WAVEFORMS

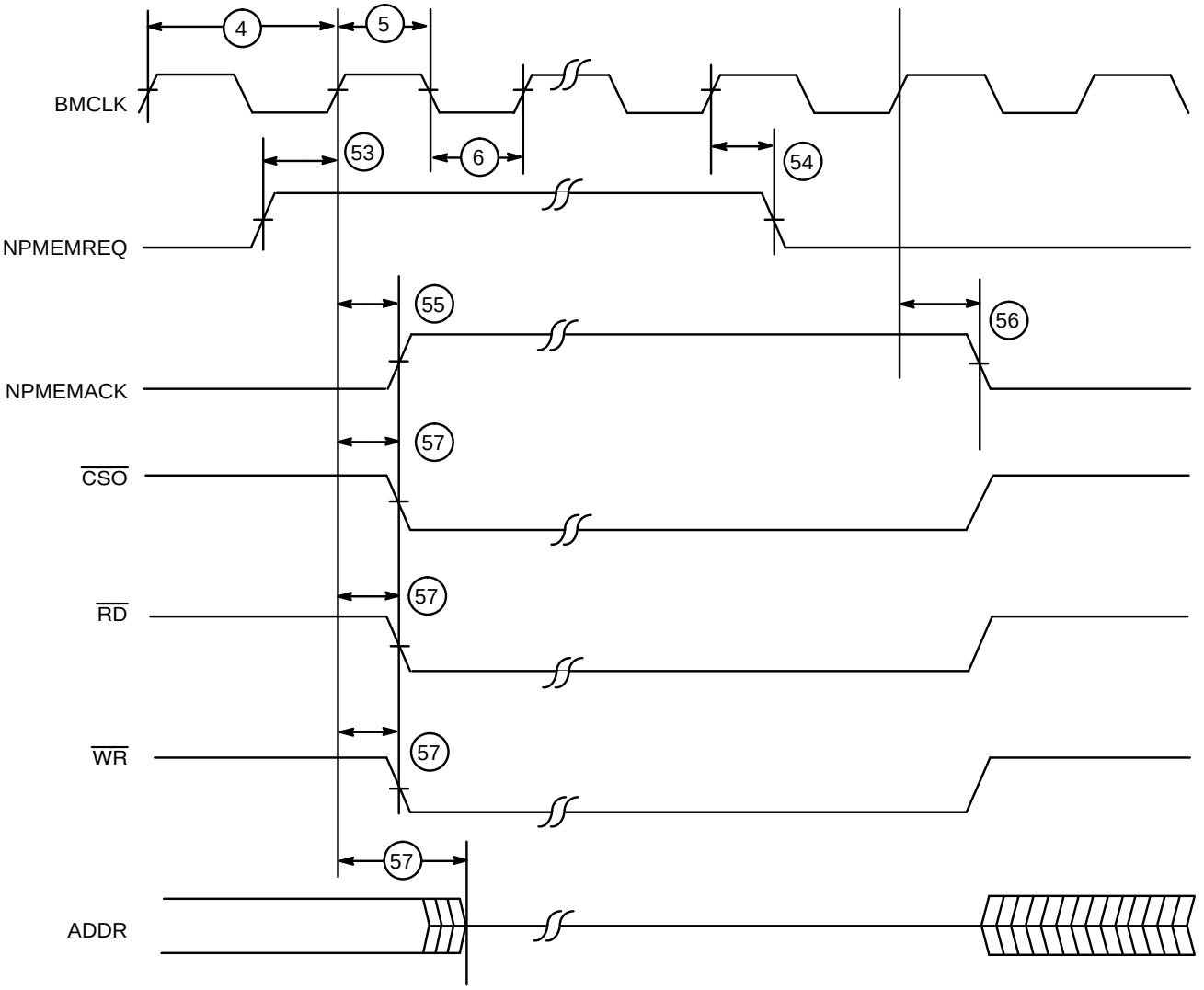

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Figure 33. NP DMA Signals

SWITCHING WAVEFORMS

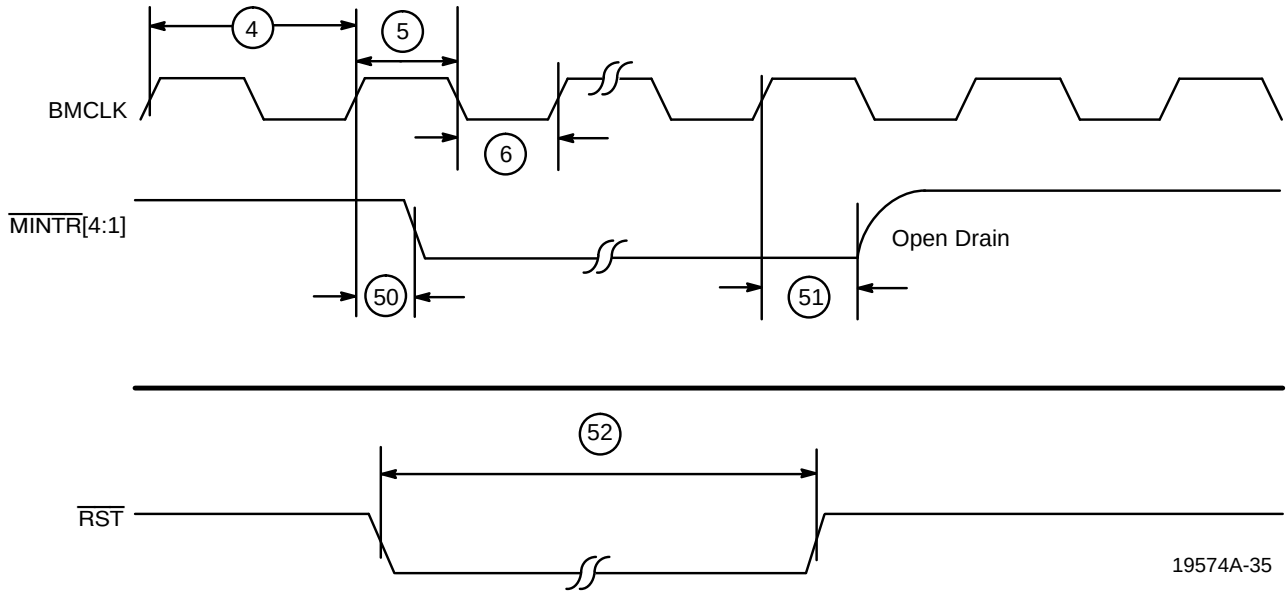

Figure 34. NP Miscellaneous Signals

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

Host Interface & Buffer Memory

No.	Parameter Symbol	Parameter Description	Min	Max	Unit
76	t_S	HSREQ2–0 Setup Time to BMCLK High	15		ns
77	t_H	HSREQ2–0 Hold Time to BMCLK High	5		ns
78	t_{PD}	BMCLK High to HSACK High		25	ns
79	t_{PD}	BMCLK High to HSACK Low		25	ns
80	t_{PD}	BMCLK High to RDATA High		25	ns
81	t_{PD}	BMCLK High to RDATA Low		25	ns
82	t_{PD}	BMCLK High to QCNTRL2–0 Valid		25	ns
83	t_{PD}	QCNTRL2–0 Invalid from BMCLK High	5		ns
84	t_{PD}	BMCLK High to ADDR 15–0 Enabled	0		ns
85	t_{PD}	BMCLK High to ADDR 15–0 Valid		27	ns
86	t_{PD}	BMCLK High to $\overline{CSO}$ Low		26	ns
87	t_{PD}	BMCLK Low to $\overline{RD}$ Low		22	ns
88	t_S	BD 31:0, BDP 3:0, BDTAG Setup Time to $\overline{RD}$ High	10		ns
89	t_H	BD 31:0, BDP 3:0, BDTAG Hold Time from $\overline{RD}$ High	0		ns
90		Reserved			ns
91	t_{PD}	$\overline{CSO}$ Invalid from $\overline{RD}$ or $\overline{WR}$ High	0		ns
92	t_{PD}	ADDR 15:0 Invalid from $\overline{RD}$ or $\overline{WR}$ High	4		ns
93	t_{PD}	BMCLK Low to $\overline{WR}$ Low		18	ns
94	t_S	ADDR 15:0 Valid to $\overline{WR}$ Low Setup Time	0		ns
95	t_{PD}	BMCLK Low to BD 31:0, BDP 3:0, BDTAG Enabled	0		ns
96	t_{PD}	BMCLK Low to BD 31:0, BDP 3:0, BDTAG Valid		26	ns
97	t_{PD}	BD 31:0, BDP 3:0, BDTAG Valid before $\overline{WR}$ High	15		ns
98		Reserved			ns
99	t_{PD}	BD 31:0, BDP 3:0, BDTAG Invalid from $\overline{WR}$ High	0		ns
100	t_{PD}	BMCLK High to BD 31:0, BDP 3:0, BDTAG Disabled		30	ns
121	t_{PD}	Read Pulse Width	38	43	ns
122	t_{PD}	Write Pulse Width	37		ns
123	t_S	ADDR 15:0 Valid to $\overline{RD}$ Low Setup Time	7	14	ns

SWITCHING WAVEFORMS

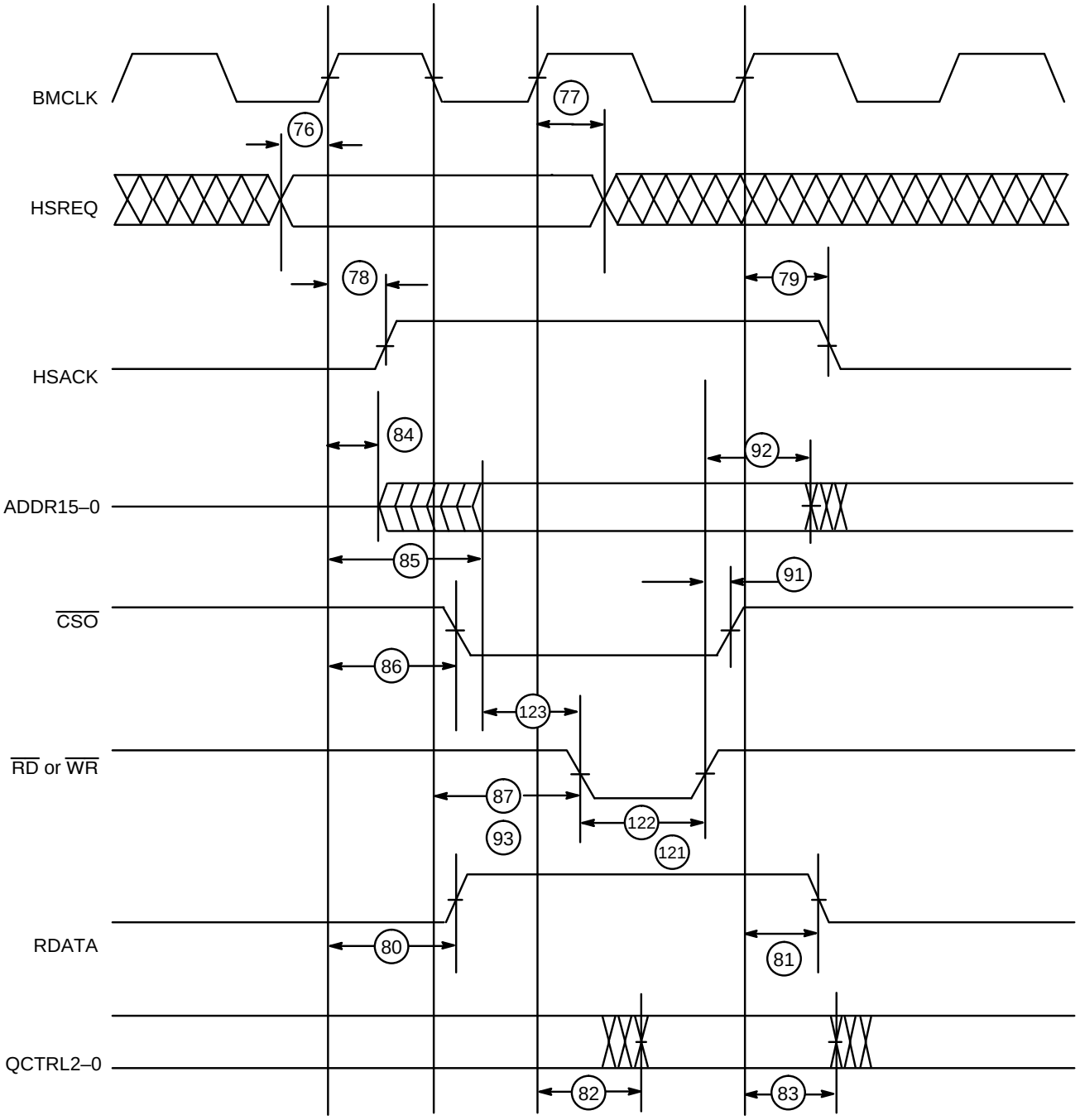

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Figure 35. Host Interface Signal Timings

SWITCHING WAVEFORMS

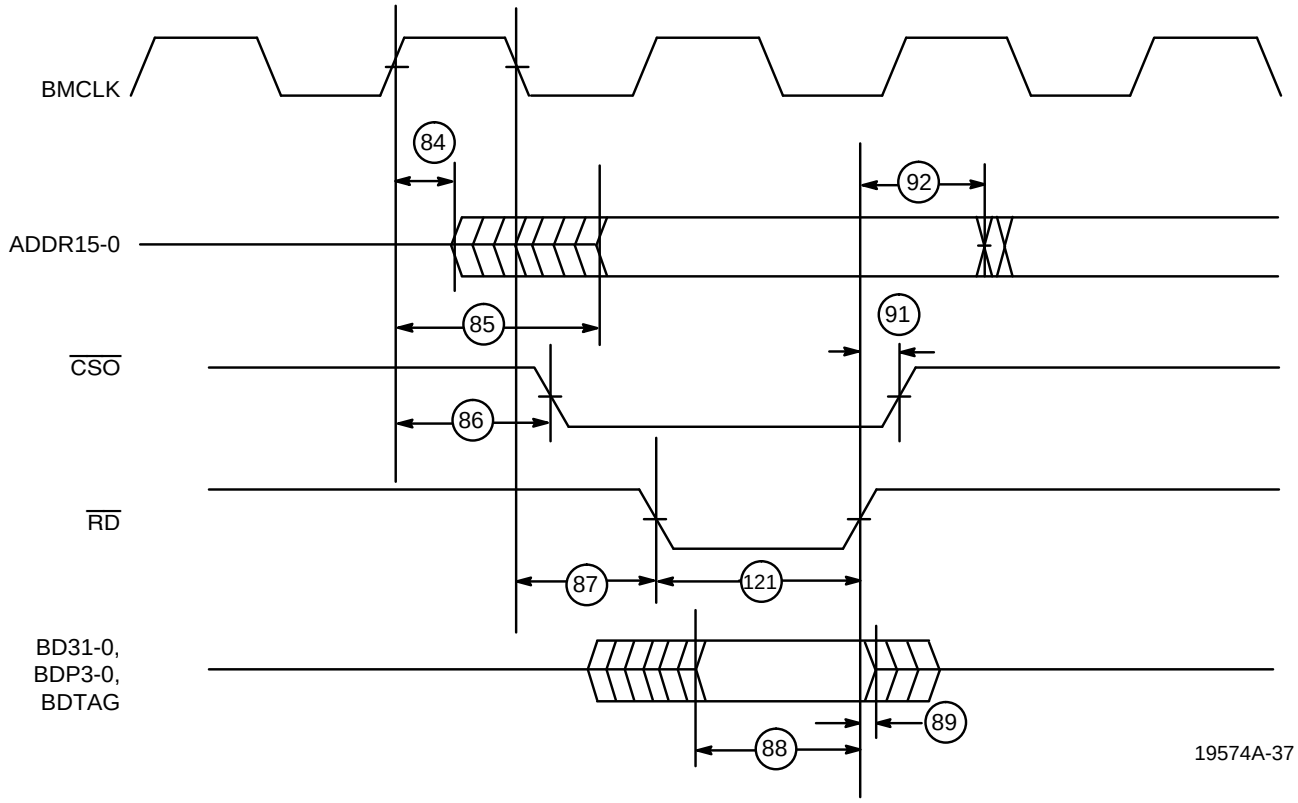

Figure 36. Buffer Memory Read Cycle Timings

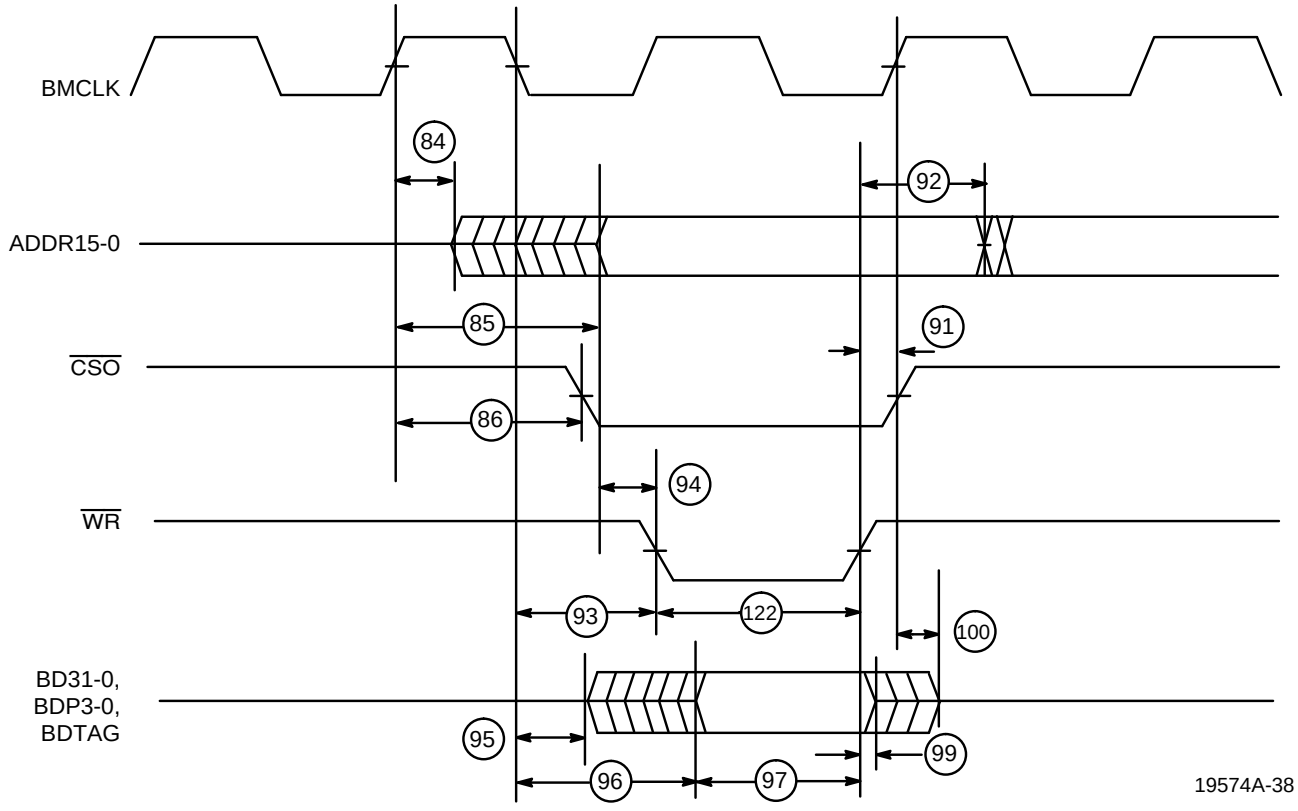

Figure 37. Buffer Memory Write Cycle Timings

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

External PHY Interface Timing

No.	Parameter Symbol	Parameter Description	Min	Max	Unit
126	t_{PD}	BCLK High to X–Bus (X0–7, XCU, XCL) Valid		35	ns
127	t_{PD}	X–Bus (X0–7, XCU, XCL) Invalid from BCLK High	6		ns
130	t_S	R0–7, RCU, RCL Setup Time to LSCLK Low	10		ns
131	t_H	R0–7, RCU, RCL Hold Time to LSCLK Low	5		ns

SWITCHING WAVEFORMS

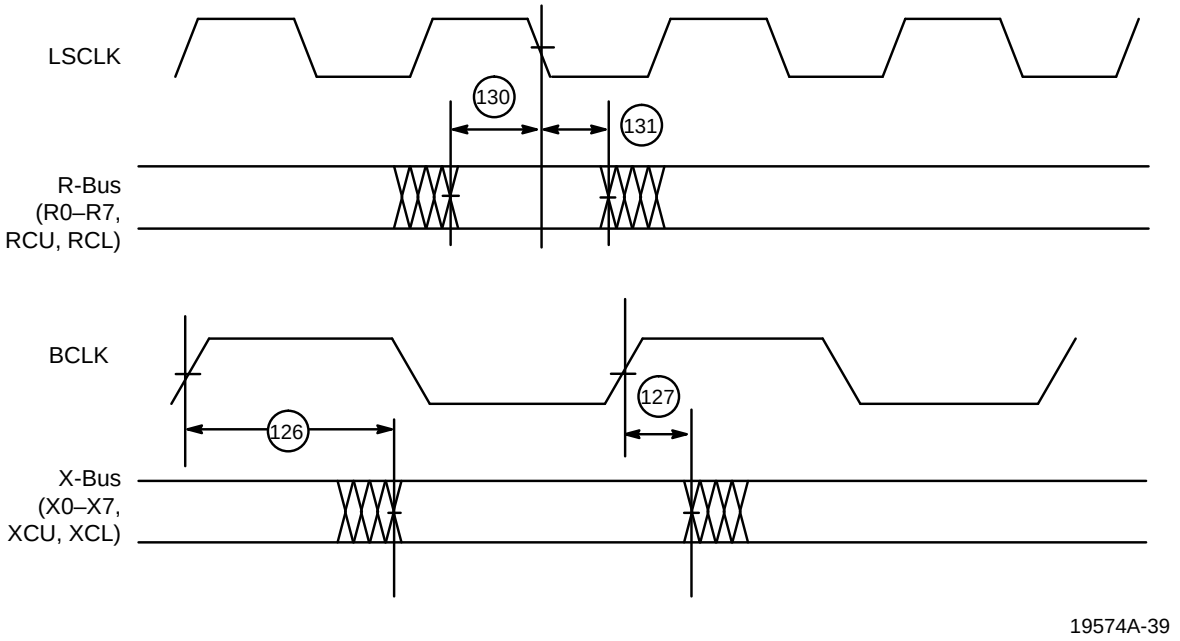

Figure 38. PHY Interface Timings

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

MAC Miscellaneous Signal Timing

No.	Parameter Symbol	Parameter Description	Min	Max	Unit
140	t_S	FLXI/XMTINH Setup Time to BCLK High	30		ns
141	t_H	FLXI/XMTINH Hold Time from BCLK High	5		ns
142	t_{PD}	BCLK High to RS5–0, XS3–0 Valid		35	ns
143	t_{PD}	RS5–0, XS3–0 Invalid from BCLK High	5		ns
144	t_S	$\overline{XSAMAT}$, $\overline{XDAMAT}$, $\overline{XSA\_XACT}$, $\overline{XDA\_XACT}$ Setup Time to BCLK High	20		ns
145	t_H	$\overline{XSAMAT}$, $\overline{XDAMAT}$, $\overline{XSA\_XACT}$, $\overline{XDA\_XACT}$ Hold Time from BCLK High	5		ns

SWITCHING WAVEFORMS

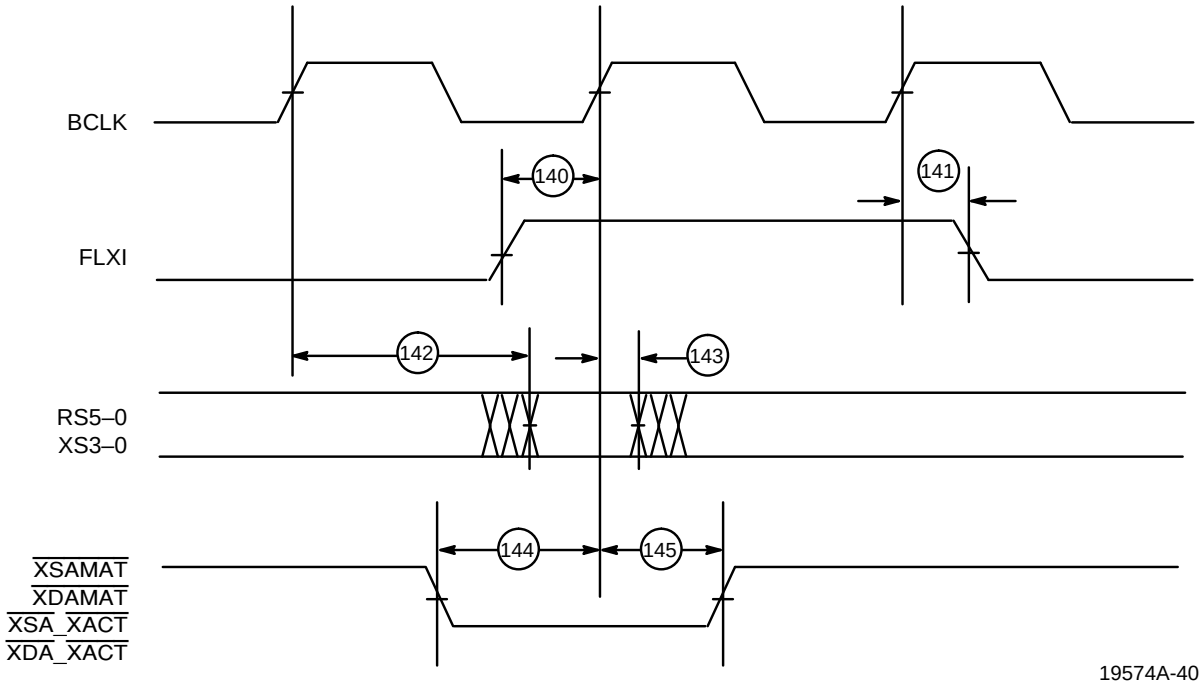

Figure 39. MAC Miscellaneous Signal Timings

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

External CAM Interface Timing

No.	Parameter Symbol	Parameter Description	Min	Max	Unit
156	t_{PD}	BCLK High to RXAFU3–0, RXAFL3–0, RXAFCU, RXAFCL Valid		25	ns
157	t_{PD}	RXAFU3–0, RXAFL3–0, RXAFCU, RXAFCL Invalid from BCLK High	0		ns

SWITCHING WAVEFORMS

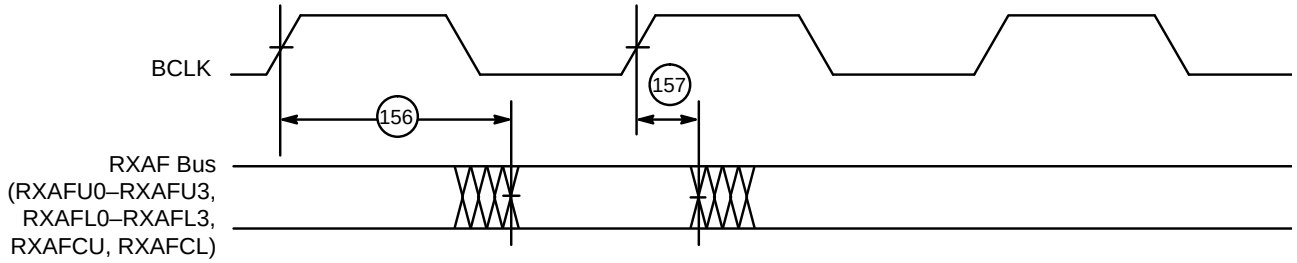

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Figure 40. External CAM Interface Timings

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

PHY Miscellaneous Signal Timing

No.	Parameter Symbol	Parameter Description	Min	Max	Unit
200	t_{PD}	$\overline{\text{FOTOFF}}$, LSR 2–0, ULSB, EBFERR Valid from BCLK High		25	ns
201	t_{PD}	$\overline{\text{FOTOFF}}$, LSR 2–0, ULSB, EBFERR Invalid from BCLK High	0		ns
210	t_S	ENCOFF Setup Time to BCLK High	15		ns
211	t_H	ENCOFF Hold Time from BCLK High	10		ns

SWITCHING WAVEFORMS

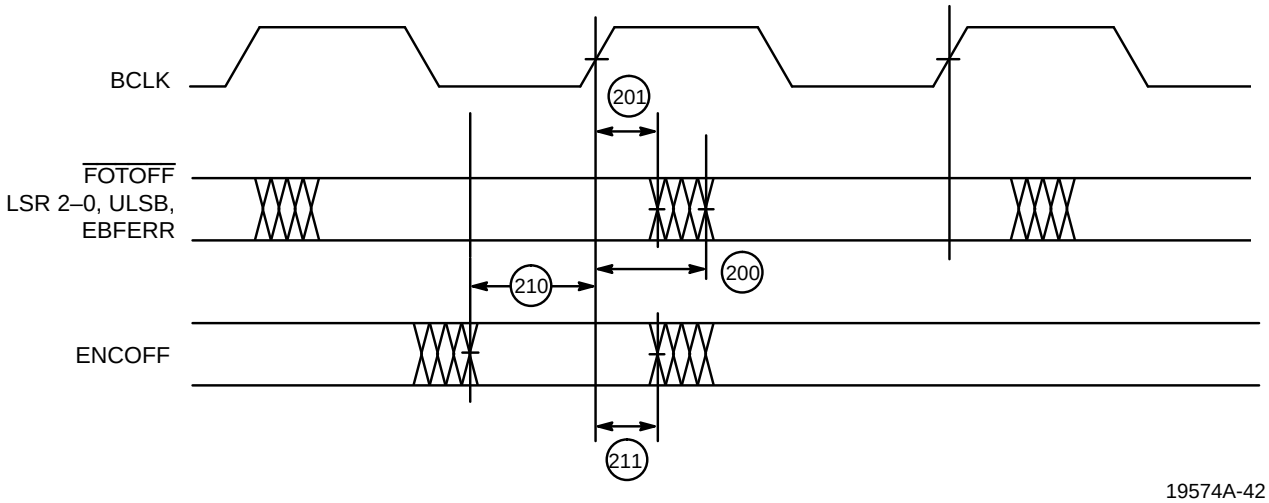


Figure 41. PHY Miscellaneous Signal Timings

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

Test Interface Signal Timing

No.	Parameter Symbol	Parameter Description	Min	Max	Unit
226	t_{PER}	TCLK Period	80	1000	ns
227	t_{PWH}	TCLK Pulse Width High	45%	55%	
228	t_{PWL}	TCLK Pulse Width Low	45%	55%	
229	t_S	TDI, TMS, $\overline{TRST}$ Setup Time to TCLK High	25		ns
230	t_H	TDI, TMS, $\overline{TRST}$ Hold Time from TCLK High	6		ns
231	t_{INV}	TDO Invalid from TCLK Low	0		ns
232	t_{PD}	TDO Valid from TCLK Low		30	ns

SWITCHING WAVEFORMS

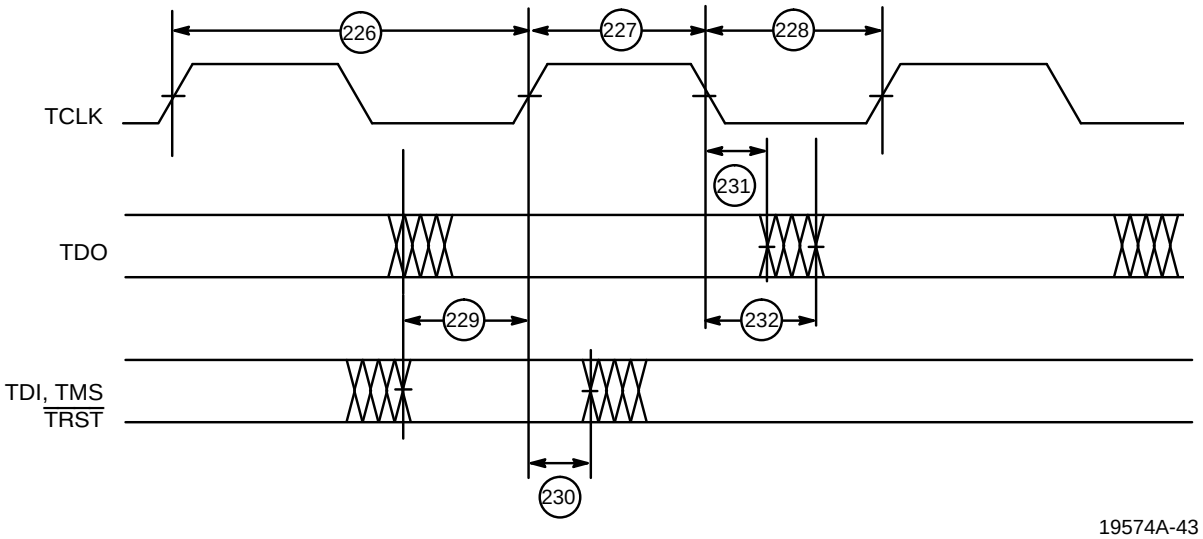


Figure 42. TEST Interface Signal Timings

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

PMD Interface Signal Timing

No.	Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
250	t_R†	TX+, TX– Rise Time	PECL Load	0.3	3	ns
251	t_F†	TX+, TX– Fall Time	PECL Load	0.3	3	ns
252	t_{SK}†	TX+ to TX– Skew	PECL Load		±200	ps
253	t_S	SDI Setup Time to LSCLK High		7		ns
254	t_H	SDI Hold Time from LSCLK High		5		ns

Note: *†: Not included in the production test.*

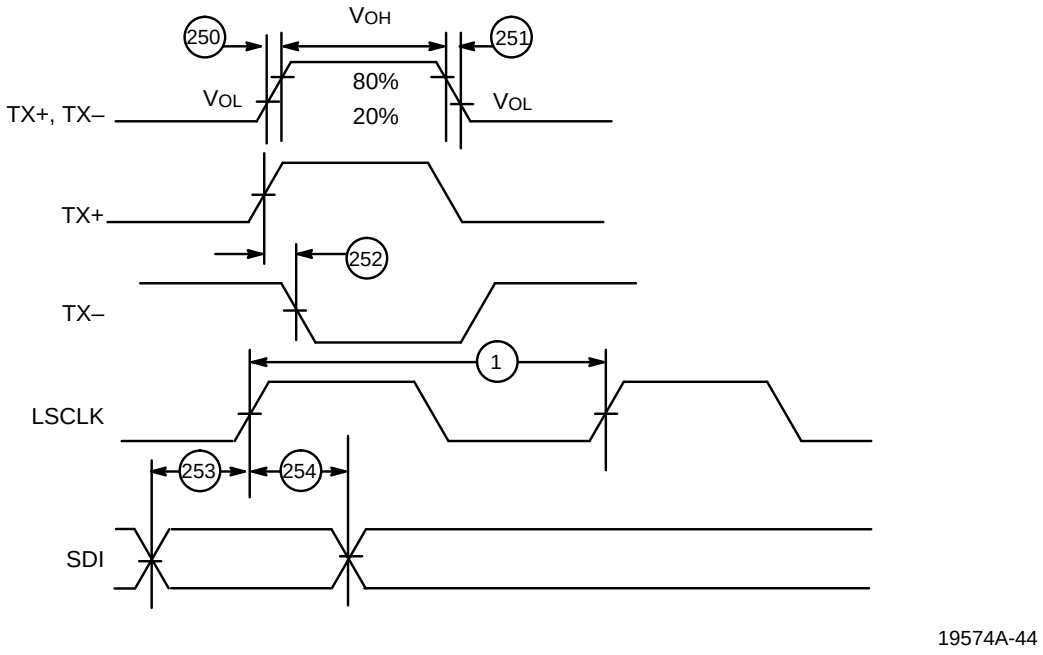


Figure 43. PMD Interface Signal Timings

REFERENCES

PHY Device

1] AMD *Am79C864A* in *The SUPERNET 2 Family for FDDI*, Publication no. 15502, Rev. C, *Physical Layer Controller with Scrambler/ Descrambler* (PLC-S).

2] *ANSI X3.148-1988, FDDI Physical Layer Specification.*

3] *ANSI X3T9 SMT Ver. 7.2, Station Management Specification.*

MAC Device

1] AMD *Am79C830A Formac Plus* datasheet in *The SUPERNET 2 Family for FDDI*, Publication no. 15502, Rev. C.

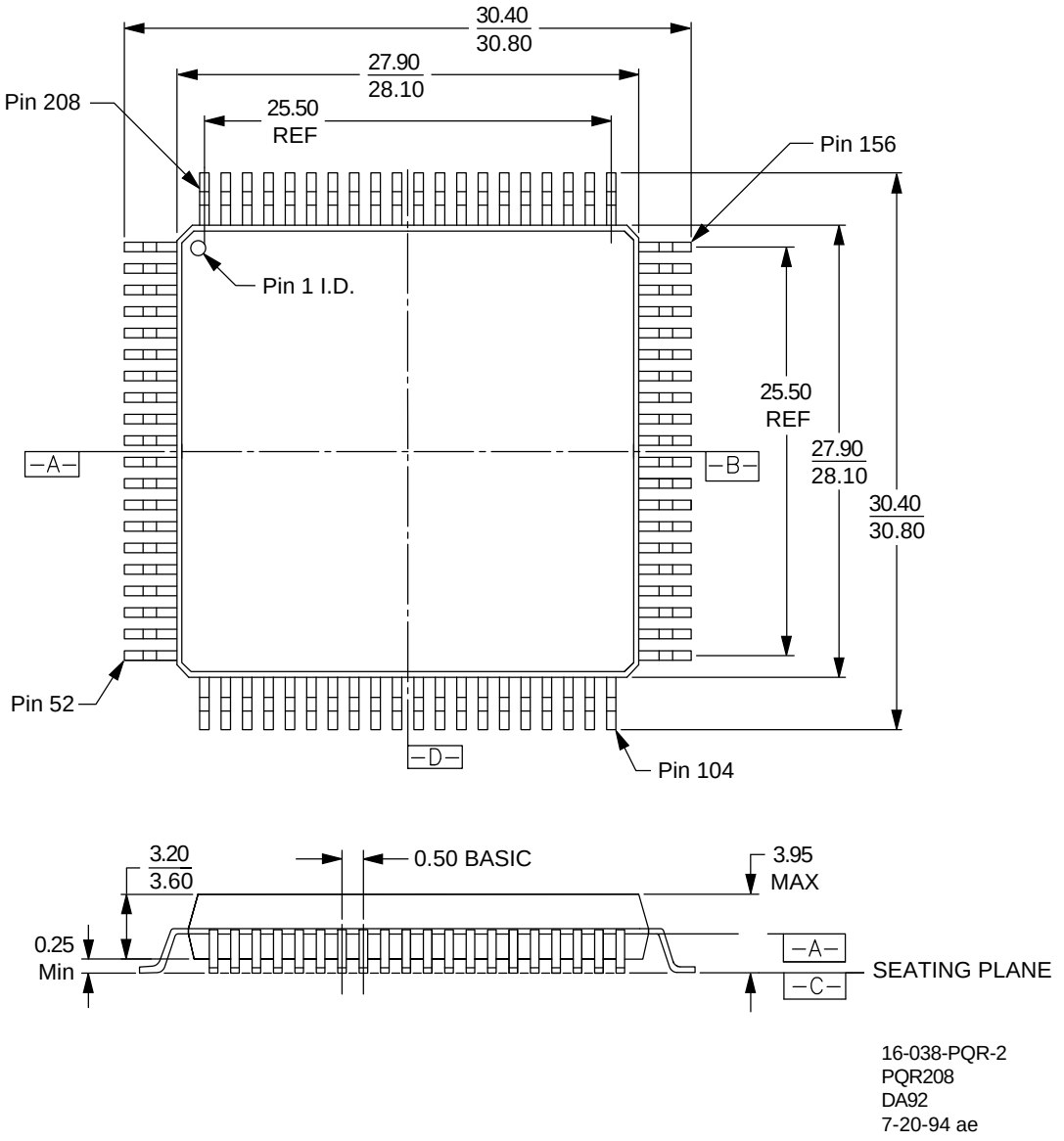
2] *ANSI X3.139-1987, FDDI Media Access Control Specification.*

Testability

IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Standard 1149.1-1990 (Approved Feb. 15, 1990)

PHYSICAL DIMENSIONS*

PQR208, Trimmed and Formed
208-Pin Plastic Quad Flat Pack (measured in millimeters)



16-038-PQR-2
PQR208
DA92
7-20-94 ae

**For reference only. BSC is an ANSI standard for Basic Space Centering.*