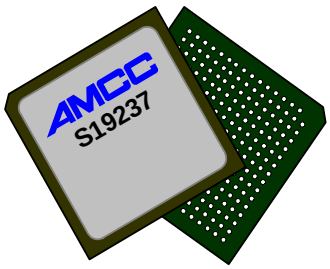


## Description

The S19237 SONET/SDH/FEC and 10 Gigabit Ethernet (GbE) transceiver is one of the latest additions to AMCC's SuperPHY™ product family. The S19237 device provides fully integrated serialization/de-serialization capabilities for low power intermediate and long reach OC-192 applications. The device performs all necessary parallel-to-serial and serial-to-parallel functions in conformance with SONET/SDH and 10 GbE transmission standards. The standard operating range is from 9.953 Gbps to 10.709 Gbps. Figure 1 shows a typical network application. Other application block diagrams are shown in Figure 2, Figure 3 and Figure 4.

## Overview

The S19237 can be used to implement the front end of SONET/SDH/FEC/10GbE equipment which consists primarily of the serial transmit interface and the serial receive interface. The system timing circuitry consists of a high-speed phase detector, clock dividers, and clock distribution. The device utilizes on-chip clock synthesis PLL components that allow the use of a slower external clock reference, 155.52 MHz or 622.08 MHz (or equivalent FEC/10GbE rate), in support of existing system clocking schemes. The low-jitter, 16-bit, Low Voltage Differential Signaling (LVDS) interfaces guarantee compliance with the bit-error rate requirements of the Telecordia and ITU-T (GR-253 ILR) standards. The device is also compliant to 300 Pin MSA standard for 10G Transponders, the OIF SFI4 Phase 1 Parallel Electrical Interface standard, IEEE Draft P802.3ae, and XFP MSA standard.

***AMCC Suggested Interface Devices***

| | |
|---|---|
| VERRAZANO (S2509) | Quad STS-48 SONET/SDH/ Digital Wrapper Backplane SERDES |
| GANGES (S19202) | STS-192 POS/ATM SONET/ SDH Mapper |
| GANGES II (S19202) | STS-192 POS/ATM SONET/ SDH Mapper |
| HUDSON (S19203) | Variable Rate Digital Wrapper Framer/Deframer, Performance Monitor, and FEC Device |
| MEKONG (S19204) | STS-192 Pointer Processor |
| KHATANGA (S19205) | STS-192c SONET/SDH Framer/Mapper with Integrated MAC |
| S3390 | 10 Gbps TIA |

## – At a Glance –

### Features

- Operational from 9.953 Gbps to 10.709 Gbps
- Low Power (1.0 W Typical)
- CMOS 0.13 Micron Technology
- 1.2 V and 1.8/2.5/3.3 V Power Supply
- Built-In Self Test (BIST) feature with Error Counter
- On-chip High-Frequency PLLs for Clock Recovery and Clock Generation
- 16-bit LVDS Parallel Data Path
- TX and RX Lock Detect Indicators
- Serial and Reference Loop Timing Modes
- Line and Diagnostic Loopback Mode for Faulty Mode Identification
- SONET Jitter Transfer Compliance with External XVCO
- -40°C to 85°C Industrial Temperature Range
- Supports High Speed Management Data Bus for I/O Control (MDIO)
- Complies with OIF SFI-4 Phase 1, Telecordia/ITU-T GR-253-ILR, 300-pin MSA, IEEE Draft P802.3ae and XFP MSA Standards
- 500 V ESD Rating on All Pins
- No heatsink or airflow required
- No power sequencing required
- 255 PBGA Package, two options 14 x 14 mm, 0.8 mm pitch or 17 x 17 mm, 1.0 mm pitch

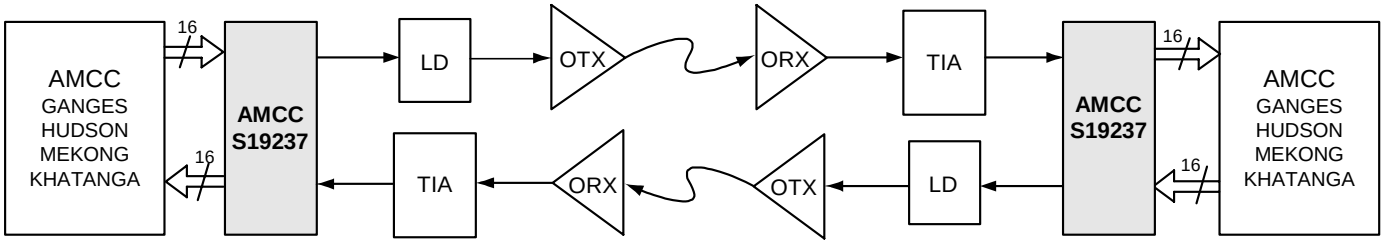


**Figure 1. System Block Diagram**

The sequence of operations is as follows:

### Transmitter Operations

1. 16-bit parallel input
2. Parallel-to-serial conversion
3. Serial data output

### Receiver Operations

1. Serial input to limiting post-amp
2. ISI compensation
3. Variable gain limiting amplifier
4. Threshold and phase adjustment for improved BER
5. Clock and data recovery
6. Serial-to-parallel conversion
7. 16-bit parallel data and clock output

Internal clocking and control functions are transparent to the user.

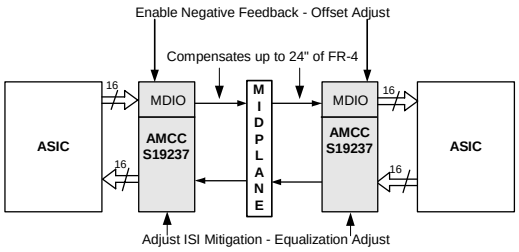


**Figure 2. Mid-Plane Application Block Diagram**

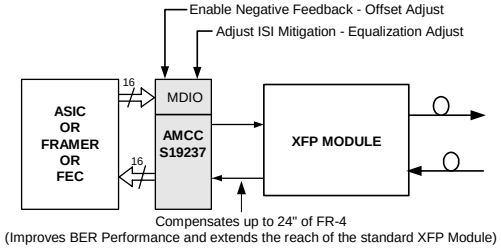


**Figure 3. XFP Application Block Diagram**

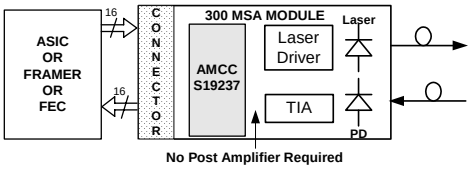


**Figure 4. 300 MSA Application Block Diagram**

| Prefix | Device | Package |
|---|---|---|
| S – Integrated Circuit | 19237 | PB12 – (255 PBGA, 17 x 17 mm, 1.0 mm pitch)<br>FP – (255 PBGA, 14 x 14 mm, 0.8 mm pitch) |

X Prefix
XXXXX Device
XX Package

**Figure 5. S19237 Ordering Information**

### Transmitter Features

- Reference Frequency of 155.52 or 622.08 MHz (or equivalent FEC/ 10GbE rate)
- 155.52 MHz and 622.08 MHz (or equivalent FEC/10GbE rate) Clock Outputs
- Internal, Self-Initializing FIFO to Decouple Transmit Clocks
- Programmable TSD Output Differential Swing

### Receiver Features

- Clock Recovery from 9.953 to 10.709 Gbps
- ISI compensation. Tolerates additional 255 ps/nm of CD with an OSNR penalty of 1.0 dB.
- Tolerates up to 24” of Standard FR-4 Material
- 10GbE Jitter Tolerance Compliance
- Adaptive Post-Amplifier Offset Adjust to minimize offset for high OSNR conditions
- Phase Adjust of -0.11 to +0.085 UI
- Reference Frequency of 155.52 MHz (or equivalent FEC/ 10GbE rate)
- Capability to Interface with Single-Ended or Differential TIAs (Center Tap Option)
- Input Sensitivity of 10 mV p-p (single-ended measurement) at $10^{-12}$ BER

### Applications

- SONET/SDH and 10GbE-Based Transmission Systems
- SONET/SDH Modules
- Section Repeaters
- Add Drop Multiplexers (ADM)
- Broad-Band Cross-Connects
- Fiber Optic Terminators and Test Equipment



6290 Sequence Drive • San Diego, CA 92121 • Tel: 858 450-9333 • Fax: 858 450-9885 • http://www.amcc.com