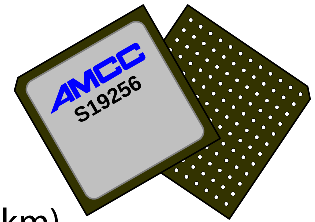
PRODUCT BRIEF

AMCC

S19256

10 G Ethernet / Fibre Channel / SONET / SDH Dual CDR (2km - 30km)



Features

- Complies with XFP MSA Specifications
- 25 mUI_{pp} Jitter Generation
- TX Equalizer to Mitigate Data Dependent Jitter
- Low Power 540 mW
- Dual CDR - 9.95 to 11.32 Gbps operation
- Footprint compatible to the EDC based 10G Dual CDR S19233
- CDR Power Down Option Ideal - 300 mW (with TX EQ and RX EQ)
- LOS Function - Compliant to GR-253
- RSSI Function (8 mV to 800 mV)
- Squelch Control (LOS or LOL conditions)
- Squelch Output Polarity Control
- Polarity Invert Control on Output Buffers
- Lock detect indication
- Automatic Threshold Adjust (Maximizes Sensitivity)
- External threshold & Phase Adjust Through I2C Bus®
- Superior Crosstalk Isolation
- Loopback (Optical and Electrical interface)
- AGC embedded equalizer TX and RX
- Integrated equalizer that support over 24" FR-4 on Transmitter Electrical Side
- TX Output Buffer Slew Rate Control
- Lock detect indication
- -40 to 85°C operation
- CMOS 0.13 Micron Technology
- 1.8 and 3.3 Volt Power Supply
- 6x6 mm^2 PBGA package with 0.8 mm pitch
- ESD - 1500 V, 500 V High Speed Inputs

Applications

- 10G Fibre Channel and Ethernet Designs
- 10GbE with FEC
- 10G SONET/SDH/FEC Designs
- SONET/SDH Test Equipment
- SONET/SDH/FEC DWDM Equipment
- XFP MSA Modules (2 km, 10 km, and 40 km)

Description

The S19256 is a fully integrated low power dual CDR device suitable for short reach module applications. It is used in 10GbE / 10GFC / OC-192 SONET/SDH PMD modules, such as the XFP MSA modules. Integrated in this device on the receive optical side, an AGC amplifier with offset cancellation circuitry, and CDR. On the transmit electrical side the S19256 also has an equalization circuit, and CDR that reshapes the data after up to 24" of transmission over copper on FR-4 PWB material, with low jitter generation of 25 mUI. For SFP+ applications, this device allows both CDR's to be powered-down and bypassed while using only the equalization circuitry needed to mitigate Data Dependent Jitter caused by the interconnect. The low-jitter CML interface guarantees compliance with the bit error rate requirements of the Telcordia and ITU-T standards. The S19256 is packaged in a 6x6 mm^2 PBGA, offering designers a small package outline.

Value Proposition - Design multiple XFP modules ranging from 2 km to 120 km link with one footprint. The S19256 (no EDC) is pin compatible to the EDC based 10G Dual CDR S19233.

S19256: 2 km-30 km;

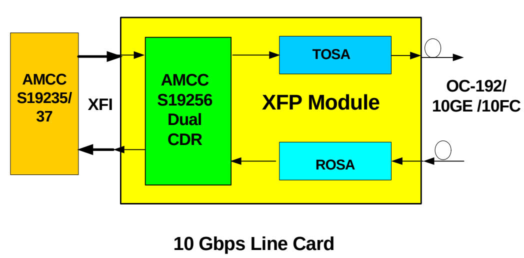
S19233: 2 km-120 km

Overview

The S19256 can be used to implement the front end of SONET/SDH/FEC/10GbE/FC/G.709 equipment which consists primarily of the serial transmit interface and the serial receive interface. The system timing circuitry consists of a high-speed phase detector, clock and data recovery unit and equalization circuitry. The device utilizes on-chip clock recovery PLL components that allow the use of a slower external clock reference, 155.52 MHz (or equivalent FEC/10GbE/10 Gbps FC rate), in support of existing system clocking schemes.

On the transmitter side, an equalizer is integrated in the receive front end to reshape the data after transmission over FR-4. This enables low bit error rate and transmission over longer trace length.

The low-jitter, 1-bit, CML interfaces guarantee compliance with the bit-error rate requirements of the Telcordia and ITU-T standards. The 10 Gbps serial electrical interface specifications are compliant with the XFI as specified in the XFP MSA module specification. The high speed serial input and output can be connected to the AMCC SerDes (S19235 or S19237) across 60 cm (24") of improved FR-4 material or across 40 cm of standard FR-4 with one connector.



System Block Diagram with the S19256

S19256

AMCC Suggested Interface Devices

S19235	SFI-4 Phase 1 SONET/SDH STS-192/10 Gig Ethernet CMOS Transceiver with ISI Compensation
S19237	SFI-4 Phase 1 SONET/SDH STS-192/10 Gig Ethernet CMOS Transceiver with ISI Compensation

Transmitter Side Operations

- 1-bit serial data input
- Equalization to compensate for FR-4
- Threshold and Offset cancellation adjust
- Clock and Data recovery
- Data retime
- Serial data output

Receiver Side Operations

- Serial input with AGC (Equalization)
- 30 mVpp Differential Sensitivity with threshold adjust
- Loss of signal detection
- Clock and Data recovery
- Serial data output

Common Operations

- Optical and Electrical Loopbacks
- Power Down CDR
- Squelch
- Polarity Invert

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