

S19260

STS-192 SONET/SDH/FEC/GbE/FC 16-bit Mux with 10G Clock

Features

- Operational from 9.9 Gbps to 11.32 Gbps
- On-chip High-Frequency PLLs for Clock Recovery and Clock Gen.
- 16-bit LVDS Parallel Data Path
- TX Lock Detect Indicator
- Reference Clock input with Divide by 16, 64, or 66 of the Incoming Serial Data Rate
- Internal, Self-Initializing FIFO to Decouple Transmit Clocks
- Programmable TSD Output Differential Swing
- 10 G Transmitter Serial Clock Output
- Duo Binary Encoding
- 40°C to 85°C Industrial Temperature Range
- Supports MDIO, I2C and SPI serial interface
- Complies with applicable OIF SFI-4 Phase 1, Telcordia/ITU-T, 300-pin MSA, IEEE 802.3ae and XFP MSA Standards
- 2000 V ESD rating on low speed pins, 1000 V on high speed I/Os
- 15 mm x 15 mm², 0.8 mm pitch package
- 560 mW typical
- JTAG support

Applications

- SONET/SDH and 10GbE-Based Transmission Systems
- Broad-Band Cross-Connects
- Fiber Optic Test Equipment
- 300 pin MSA Modules

Description

The S19260 Mux chip is a fully integrated serialization SONET STS-192/10 Gigabit Ethernet/Fiber Channel device with 10G clock output. This device can be used to compensate channel impairments caused by Single Mode Fiber (SMF) and copper medium. The chip performs all necessary parallel-to-serial functions in conformance with SONET/SDH, 10 Gigabit Ethernet (10GbE) and 10 Gigabit Fibre Channel (10GFC) transmission standards. The figure below shows a typical network application. The other application block diagrams are shown on page 2.

On-chip clock synthesis PLL components are contained in the S19260 chip, allowing the use of a slower external transmit clock reference. The chip can be used with 155.52 MHz or 622.08 MHz (or equivalent FEC/10GbE/10GFC rates) reference clocks, in support of existing system clocking schemes. The low-jitter LVDS interface guarantees compliance with the bit-error rate requirements of the Telcordia and ITU-T standards.

Overview

The S19260 transceiver incorporates SONET/SDH/10 GbE/10GFC serialization functions. This chip can be used to implement SONET/10 GbE/10GFC equipment, which consists primarily of the serial transmit interface. The chip includes parallel-to-serial conversion and system timing.

AMCC Suggested Interface Devices

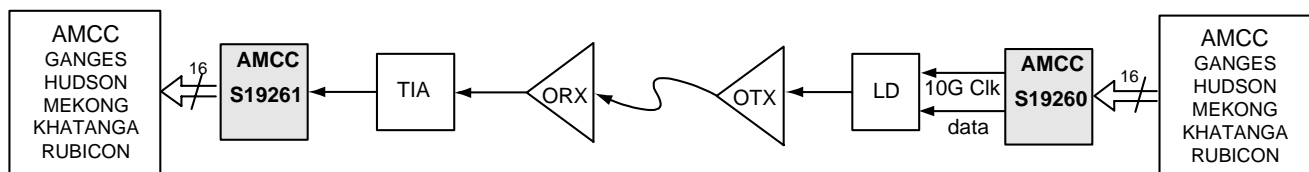
RUBICON (S19227)	OC-192/48/12/3 DW/FEC/PM and ASYNC Mapper Device with Strong FEC
GANGES III (S19202CBI20)	STS-192 POS/ATM SONET/SDH Mapper
HUDSON 2.0 (S19203)	Variable Rate Digital Wrapper Framer/Deframer, Performance Monitor, and FEC Device
KHATANGA (S19205)	STS-192c SONET/SDH Framer/Mapper with Integrated MAC
MEKONG (S19204)	STS-192 Pointer Processor
S19233	Dual CDR imbedded in XFP module

The sequence of operations is as follows:

Transmitter Operations

- 16-bit parallel input
- Parallel-to-serial conversion
- Serial data output
- Serial clock output

Internal clocking and control functions are transparent to the user.



System Block Diagram with the S19260

S19260

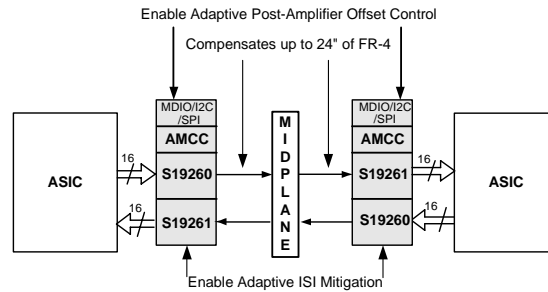


Figure 1. Mid-Plane Application Block Diagram

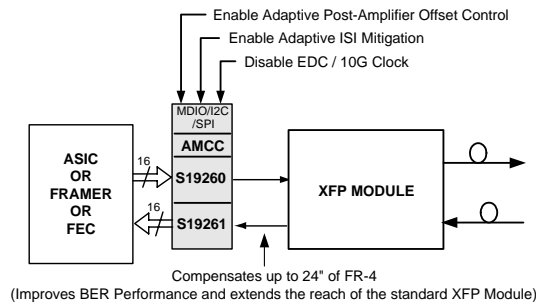


Figure 2. XFP Application Block Diagram

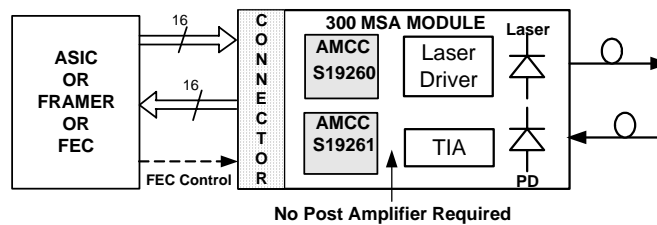


Figure 3. 300 MSA Application Block Diagram

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