AMCC

S19261
STS-192 SONET/SDH/FEC/GbE/FC 16-bit DeMux with EDC

Features

- Operational from 9.9 Gbps to 11.32 Gbps
- On-chip High-Frequency PLLs for Clock Recovery and Clock Gen.
- 16-bit LVDS Parallel Data Path
- RX Lock Detect Indicator
- LOS/RSSI
- ISI compensation. Tolerates additional 350 ps/nm of chromatic dispersion with an OSNR penalty of 1.0dB over a traditional demux
- Tolerates up to 34" of Standard FR-4 Material
- Adaptive Post-Amplifier Offset Adjust
- Phase Adjust of -0.11 to +0.085 UI
- Reference Clock input with Divide by 16, 64 or 66 of the Incoming Serial Data Rate
- Capability to Interface with Single-Ended or Differential TIAs (Center Tap Option)
- Input Sensitivity of 10 mV p-p (one wire or two wire) at 10^{-12} BER
- -40°C to 85°C Industrial Temperature Range
- Supports MDIO, I2C and SPI serial interface
- Complies with applicable OIF SFI-4 Phase 1, Telcordia/ITU-T, 300-pin MSA, IEEE 802.3ae and XFP MSA Standards
- 2000 V ESD rating on low speed pins, 1000 V on high speed I/Os
- 15 mm x 15 mm^2, 0.8 mm pitch package
- 830 mW typical
- JTAG support

Applications

- SONET/SDH and 10GbE-Based Transmission Systems
- Broad-Band Cross-Connects
- Fiber Optic Test Equipment
- 300 pin MSA Modules

Description

The S19261 DeMux chip is a fully integrated de-serialization SONET STS-192/10 Gigabit Ethernet/Fiber Channel DeMux with Electronic Dispersion Compensation (EDC). This device can be used to compensate channel impairments caused by Single Mode Fiber (SMF) and copper medium. The chip performs all necessary serial-to-parallel functions in conformance with SONET/SDH, 10 Gigabit Ethernet (10GbE) and 10 Gigabit Fibre Channel (10GFC) transmission standards. The figure below shows a typical network application. The other application block diagrams are shown on page 2.

The chip can be used with 155.52 MHz or 622.08 MHz (or equivalent FEC/10GbE/10GFC rates) reference clock in support of existing system clocking schemes. The low-jitter LVDS parallel interface guarantees compliance with the bit-error rate requirements of the Telcordia and ITU-T standards.

Overview

The S19261 De-Mux incorporates SONET/SDH/10GbE/10GFC deserialization functions. This chip can be used to implement the front end of SONET/10GbE/10GFC equipment, which consists primarily of the serial receive interface. The chip includes serial-to-parallel conversion and system timing.

AMCC Suggested Interface Devices

RUBICON (S19227)	OC-192/48/12/3 DW/FEC/PM and ASYNC Mapper Device with Strong FEC
GANGES III (S19202)	STS-192 POS/ATM SONET/SDH Mapper
Hudson 2.0 (S19203)	Variable Rate DW/FEC/PM
KHATANGA (S19205)	STS-192c SONET/SDH Framer/Mapper w/Integrated MAC
MEKONG (S19204)	STS-192 Pointer Processor
S19233	Dual CDR imbedded in XFP module

The sequence of operations is as follows:

Receiver Operations

- Serial input to post-Amplifier
- ISI compensation
- LOS and RSSI
- Threshold and phase adjustment for improved BER
- Clock and data recovery
- Serial-to-parallel conversion
- 16-bit parallel data and clock output

Internal clocking and control functions are transparent to the user.
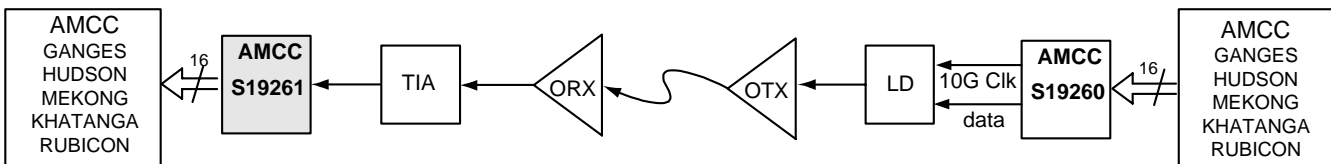
System Block Diagram with the S19261

S19261
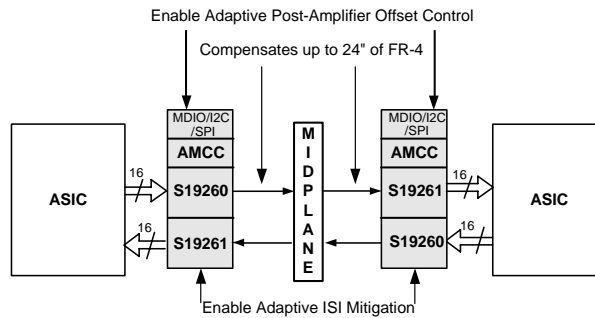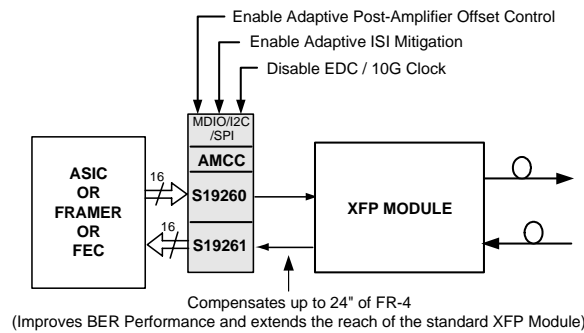

Figure 1. Mid-Plane Application Block Diagram
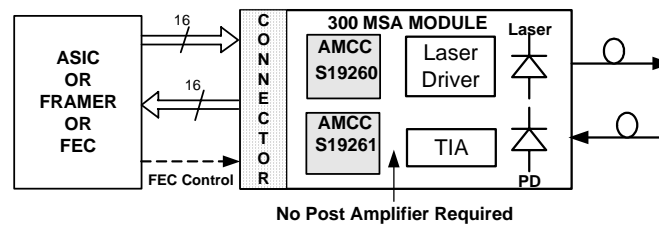

Figure 2. XFP Application Block Diagram

Figure 3. 300 MSA Application Block Diagram

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