Features

- Configurable for parallel-to-serial or serial-to-parallel conversion of 1024 channels
- Supports serial data rates of 2.048 Mbit/s or 4.096 Mbit/s
- Interfaces to Zarlink's MT9080 Switch Matrix Module (SMX)
- Generates all framing signals required in 1 K or 2 K switching applications
- Expandable to 2048ch. systems
- Compatible to ST-BUS

Applications

- Custom designed small and medium digital switch matrices using Zarlink MT9080B
- Rate conversion applications
- Interfacing a parallel system bus to devices utilizing serial I/O
- Telephony:PBX, CO, digital cross connects, digital local loop
- Datacom: Integrated Access Concentrators, WAN/LAN gateways

September 2005

Ordering Information

MT9085BP	68 Pin PLCC	Tubes
MT9085BPR	68 Pin PLCC	Tape & Reel
MT9085BP1	68 Pin PLCC*	Tubes
MT9085BPR1	68 Pin PLCC*	Tape & Reel

*Pb Free Matte Tin

-40°C to +70°C

Description

The MT9085 Parallel Access Circuit (PAC) provides an interface between an 8 bit, parallel time division multiplexed bus and a serial time division multiplexed bus. A single PAC device will accept data clocked out on the parallel bus of the Zarlink MT9080 (SMX) and output it on 32/16 time division multiplexed serial bus streams. A second device can be configured to perform the conversion from the serial format into an SMX compatible parallel format. The time division, serial multiplexed streams may operate at 2.048 Mbit/s or at 4.096 Mbit/s. The PAC generates all framing signals required by the SMX for 1024 and 2048 channel configurations.

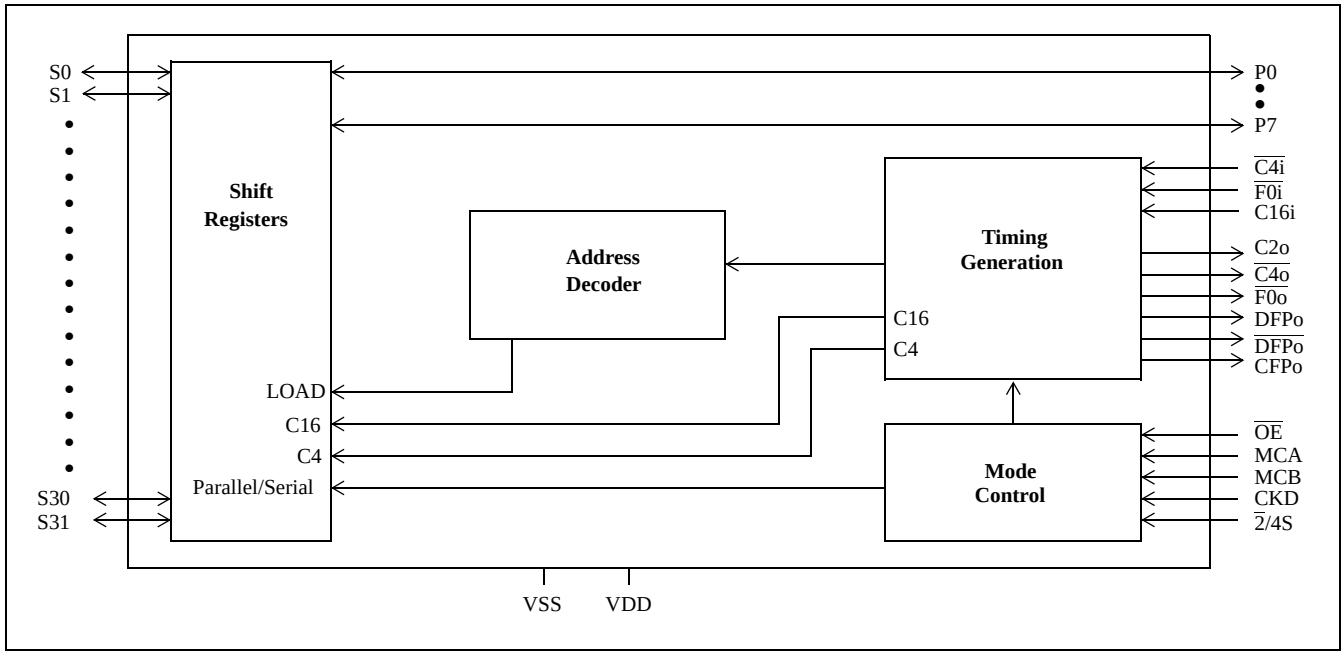


Figure 1 - Functional Block Diagram

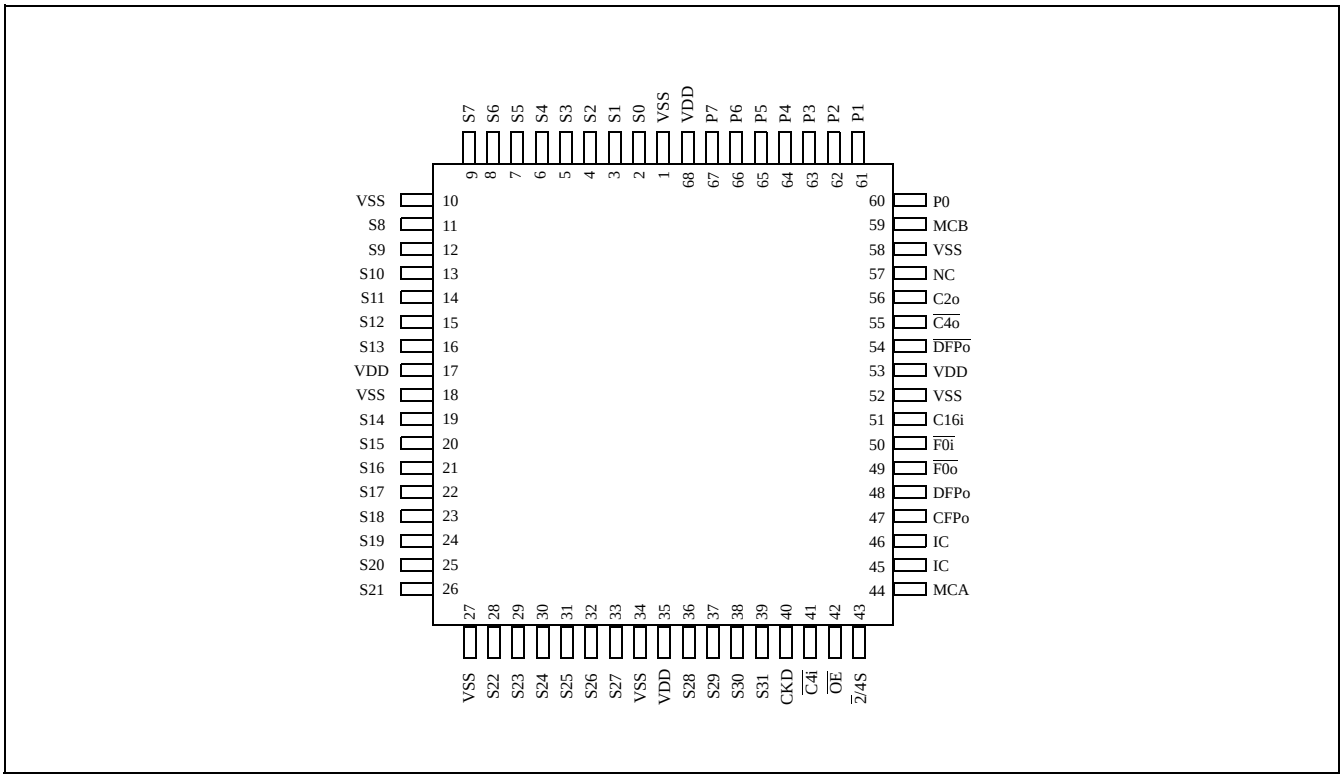


Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	V_{SS}	Ground.
2-9	S0-S7	**Serial Input/Outputs** (TTL compatible with internal pullups). Time division, multiplexed serial bus streams; inputs in serial to parallel mode (MCA=0), and outputs in parallel to serial mode (MCA=1). Data rate on the serial streams can be selected to be 2.048 Mbit/s (2/4S=0) or 4.096 Mbit/s (2/4S=1). Refer to Figures 3, 4 and 5 for functional timing information.
10	V_{SS}	Ground.
11-16	S8-S13	**Serial Input/Outputs.** See description for pins 2 - 9 above.
17	V_{DD}	**Supply Input.** +5V .
18	V_{SS}	Ground.
19-20	S14-S15	**Serial Input/Outputs.** See description for pins 2 - 9 above.
21-26	S16-S21	**Serial Input/Outputs** (TTL compatible with internal pullups). Time division, multiplexed serial bus streams which are configured as inputs in serial to parallel mode (MCA =0), and outputs in parallel to serial mode (MCA=1). Data is clocked at 2.048 Mbit/s ($\overline{2}$/4S = 0). These input/outputs are inactive when the device is configured for 4.096 Mbit/s operation ($\overline{2}$/4S=1).
27	V_{SS}	Ground.
28-33	S22-S27	**Serial Input/Outputs.** See description for pins 21-26 above.
34	V_{SS}	Ground.
35	V_{DD}	**Supply Input +5 V**
36-39	S28-S31	**Serial Input/Outputs.** See description for pins 21-26 above.
40	CKD	**Clock Delay (Input).** Control input which configures internal device timing. CKD=0 Internal master counter is reset at the system frame boundary established by the frame pulse ($\overline{F0i}$). CKD=1 Internal master counter is reset one C16 clock period after system frame boundary. All data input/output will be delayed by one C16 clock period. Timing for data input/output and for $\overline{OE}$ is affected by the level asserted on CKD. The relative phase between the frame boundary established by $\overline{F0i}$ and output signals $\overline{F0o}$, C2o, $\overline{C4o}$, DFPo, $\overline{DFPo}$ and CFPo is also affected by the state of the CKD input. See descriptions pertaining to each specific pin for more information.
41	$\overline{C4i}$	**4.096 MHz Clock Input.** The 4.096 MHz clock signal must be phase locked to the 16.384 MHz. clock. The falling edge of C4i is used to clock in the frame pulse ($\overline{F0i}$).
42	$\overline{OE}$	**Output Enable (Input).** When low, output data bus (serial or parallel) is actively driven. When set high, the output bus drivers are disabled. In serial to parallel mode, the outputs are disabled immediately after $\overline{OE}$ is taken High. See Figures 6 and 21 for timing information pertaining to parallel to serial mode.
43	$\overline{2}$/4S	**2.048/4.096 Mbit/s Select (Input).** Selects the data rate for the time division, multiplexed serial streams. When tied low, the data rate is 2.048 Mbit/s. When tied high, the data rate is 4.096 Mbit/s.
44	MCA	**Mode Control-A (Input).** The device will perform a serial to parallel conversion when this input is tied low. When the input is tied high, the device operates in the parallel to serial mode.
45	IC	**Internal Connection.** Must be tied to V_{SS} for normal device operation.
46	IC	**Internal Connection.** Should be left unconnected.

Pin Description (continued)

Pin #	Name	Description
47	CFPo	**Connect Memory Frame Pulse (Output).** Framing signal with a nominal 8 kHz frequency; goes low 71 (CKD=0) or 68 (CKD=1) C16 clock cycles before the frame boundary established by $\overline{F0i}$. The signal is used by the connection memory in a typical 1 k or 2 k switch configuration. See Figure 15 for timing information.
48	DFPo	**Data Memory Frame Pulse (Output).** Framing signal with nominal 4 kHz frequency; changes state 64 (CKD=0) or 65 (CKD=1) C16 clock cycles after the frame boundary established by $\overline{F0i}$. This signal is a complement of $\overline{DFPo}$. See Figure 15 for timing information. The signal is used by SMXs (MT9080s) making up the Data Memory in a typical 1 k or 2 k switch configuration.
49	$\overline{F0o}$	**Framing Type 0 Signal (Output).** 8 kHz framing signal output by the PAC to indicate the frame boundary synchronized to C16. This framing signal is aligned with $\overline{C4o}$ and is output by the PAC for use by other devices in a typical switch configuration. Refer to Figures 4 and 5 for functional timing information.
50	$\overline{F0i}$	**Framing Type 0 Signal (TTL compatible input).** This input signal establishes the frame boundary for the serial input/output streams. The first falling edge of $\overline{C4i}$ following the falling edge of $\overline{F0i}$ establishes the frame boundaries. Refer to Figure 13 for timing information.
51	C16i	**16 MHz Clock Input.** The 16.384 MHz clock signal input at this pin must be phase-locked to the 4.096 MHz clock input at $\overline{C4i}$. See Figure 13 for timing information.
52	V_{SS}	Ground.
53	V_{DD}	**Supply Input. +5 V**
54	$\overline{DFPo}$	**Data Memory Frame Pulse (Output).** 4 kHz framing signal; changes state 64 (CKD=0) or 65 (CKD=1) C16 clock cycles after the frame boundary established by $\overline{F0i}$. This signal is a complement of DFPo. See Figure 15. The signal is used by SMXs (MT9080s) making up the Data Memory in a typical 2 k switch configuration.
55	$\overline{C4o}$	**4.096 MHz Clock Output.** This is a 4.096 MHz clock signal derived from the 16 MHz master clock input at C16. The falling edge of $\overline{C4o}$ occurs in the middle of the regenerated frame pulse output at $\overline{F0o}$. Refer to Figures 4 and 5 for functional timing information.
56	C2o	**2.048 MHz Clock Output.** This is a 2.048 MHz clock signal derived from the 16 MHz master clock input. The rising edge of this clock signal occurs in the middle of the regenerated frame pulse output at $\overline{F0o}$. Refer to Figures 4 and 5 for functional timing information.
57	NC	**No Connection.**
58	V_{SS}	Ground.
59	MCB	**Mode Control-B (Input).** This control input performs two different functions, depending on the state of MCA pin. In parallel to serial mode (MCA=1), MCB defines which clock edge latches in the data. MCB=0 Data on the parallel bus is latched into the device with the every second falling edge of C16. See Figure 6. MCB=1 Data on the parallel bus is latched into the device with every alternate positive clock edge. In serial to parallel mode (MCA=0), the MCB pin controls the state of the parallel bus driver as follows: MCB=0 The output drivers are enabled for only half the timeslot. The data is clocked out on the first falling edge within the timeslot and disabled on the next falling edge. See Figure 7. MCB=1 The parallel data bus output drivers are enabled for the duration of the channel timeslot (two C16 Clock Periods). The data is clocked out on the first positive edge within a timeslot and disabled on the last edge.

Pin Description (continued)

Pin #	Name	Description
60-67	P0-P7	**Parallel Input/Output Data Bus.** This 8 bit data bus is an output in serial to parallel mode (MCA=0), and an input in parallel to serial mode (MCA=1). Data is clocked in and out of the port by the C16 clock. The state of the CKD pin determines the relative phase of the critical clock edges with respect to the frame pulse. All inputs/outputs have internal pullups. Refer to Figures 6 and 7 for functional timing information.
68	V_{DD}	**Supply.** +5 V

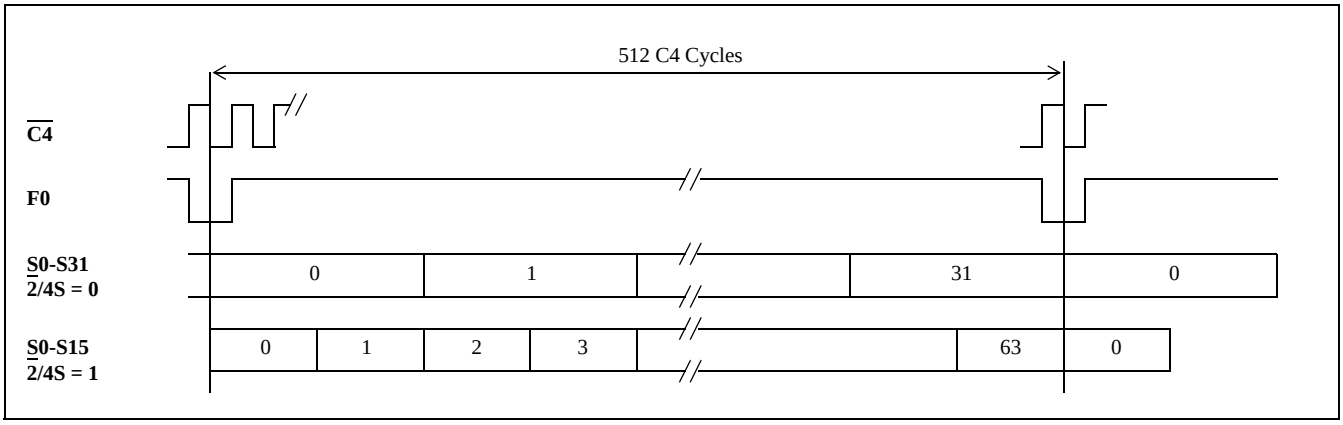


Figure 3 - Serial Input/Output Functional Timing

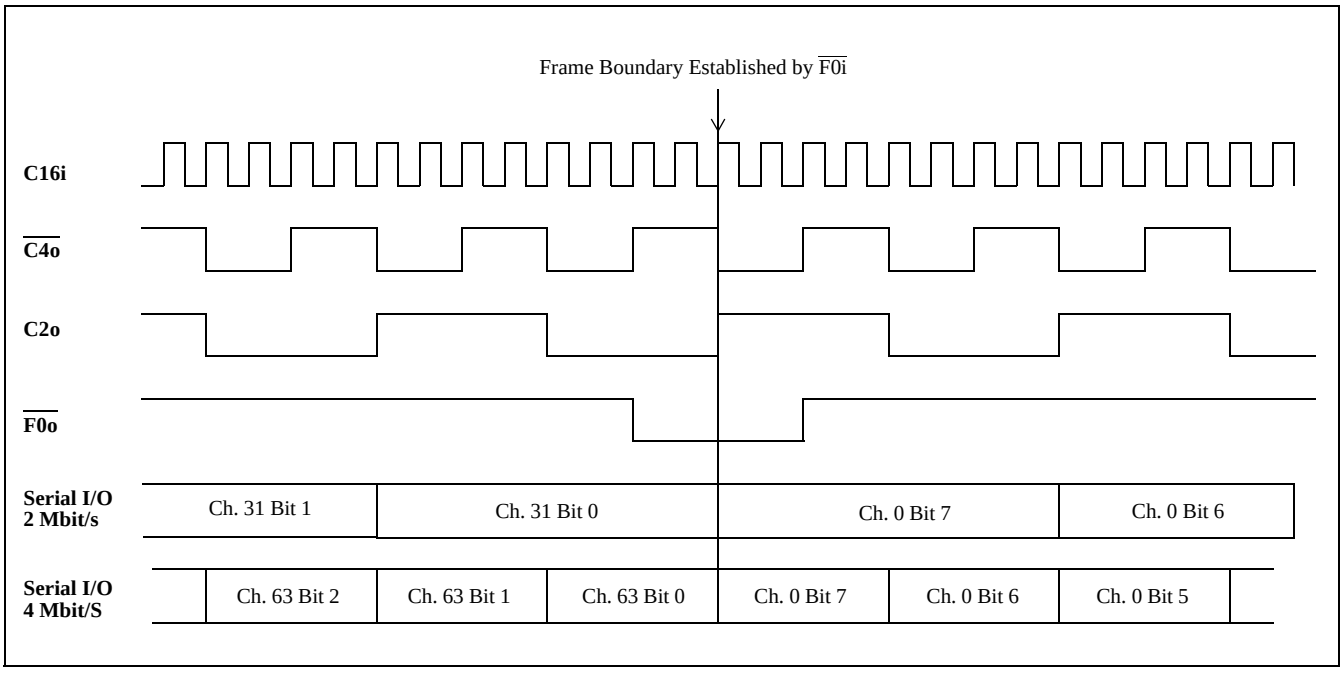


Figure 4 - Channel and Frame Alignment (CKD = 0)

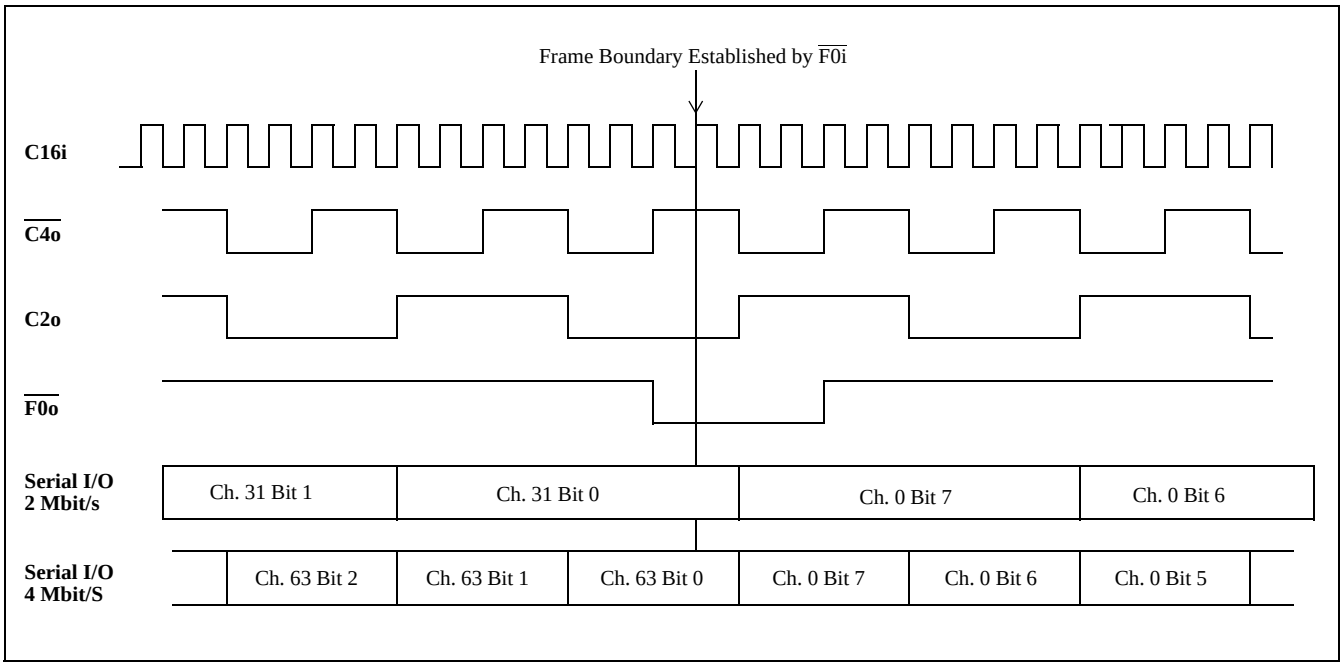
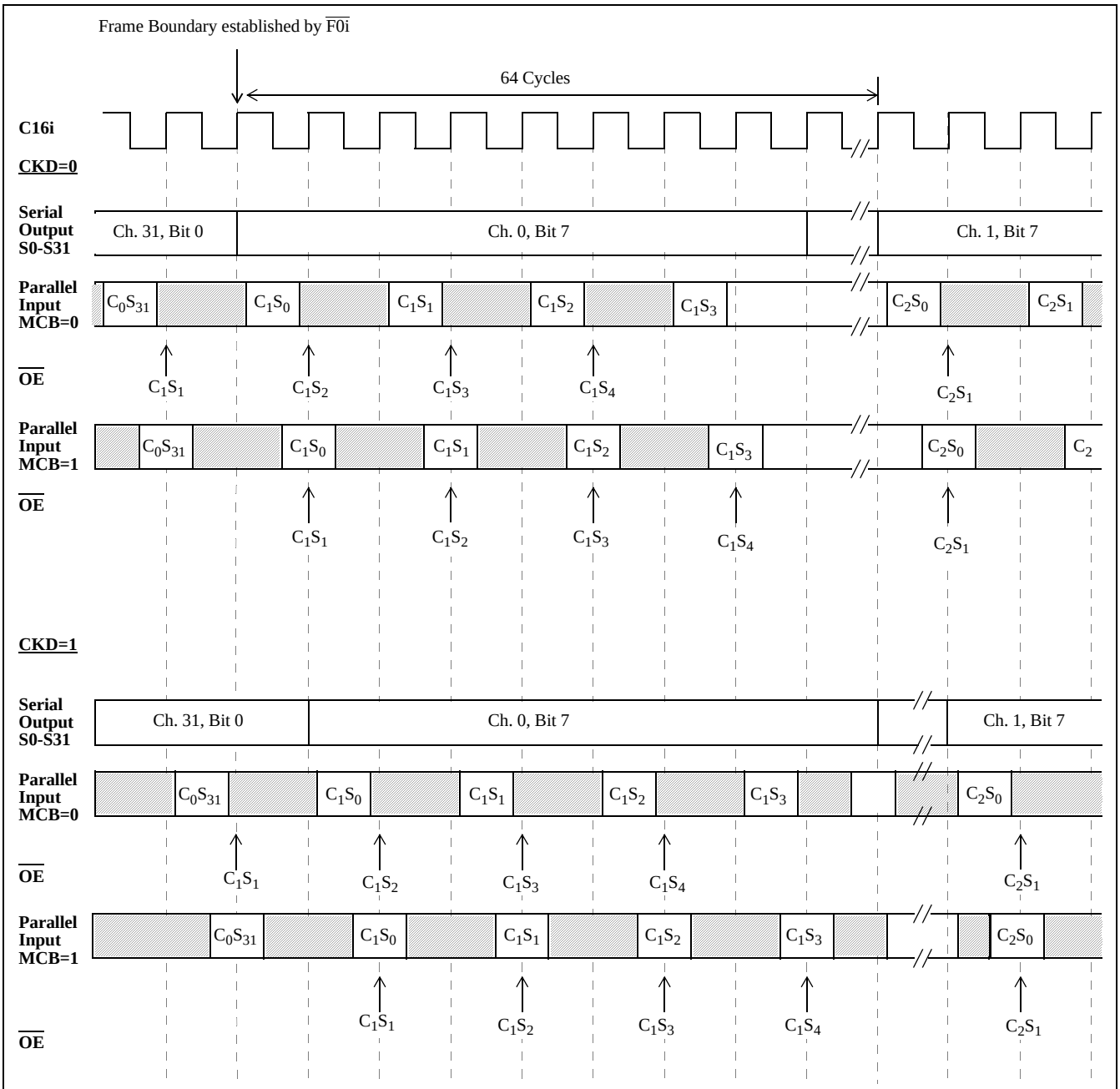


Figure 5 - Channel and Frame Alignment (CKD = 1)



Notes:

C_XS_Y - on t

Arrows in the row marked $\overline{OE}$ indicate the clock edge which latches in the state of the $\overline{OE}$ pin. C_XS_Y written below the arrow indicates the serial output channel affected by the $\overline{OE}$ signal. For example, the level on $\overline{OE}$ clocked in with edge marked C_1S_1 will enable or disable the serial output drivers for stream 1 during channel 1.

Figure 6 - Functional Data I/O Timing in Parallel to Serial Mode (MCA = 1)

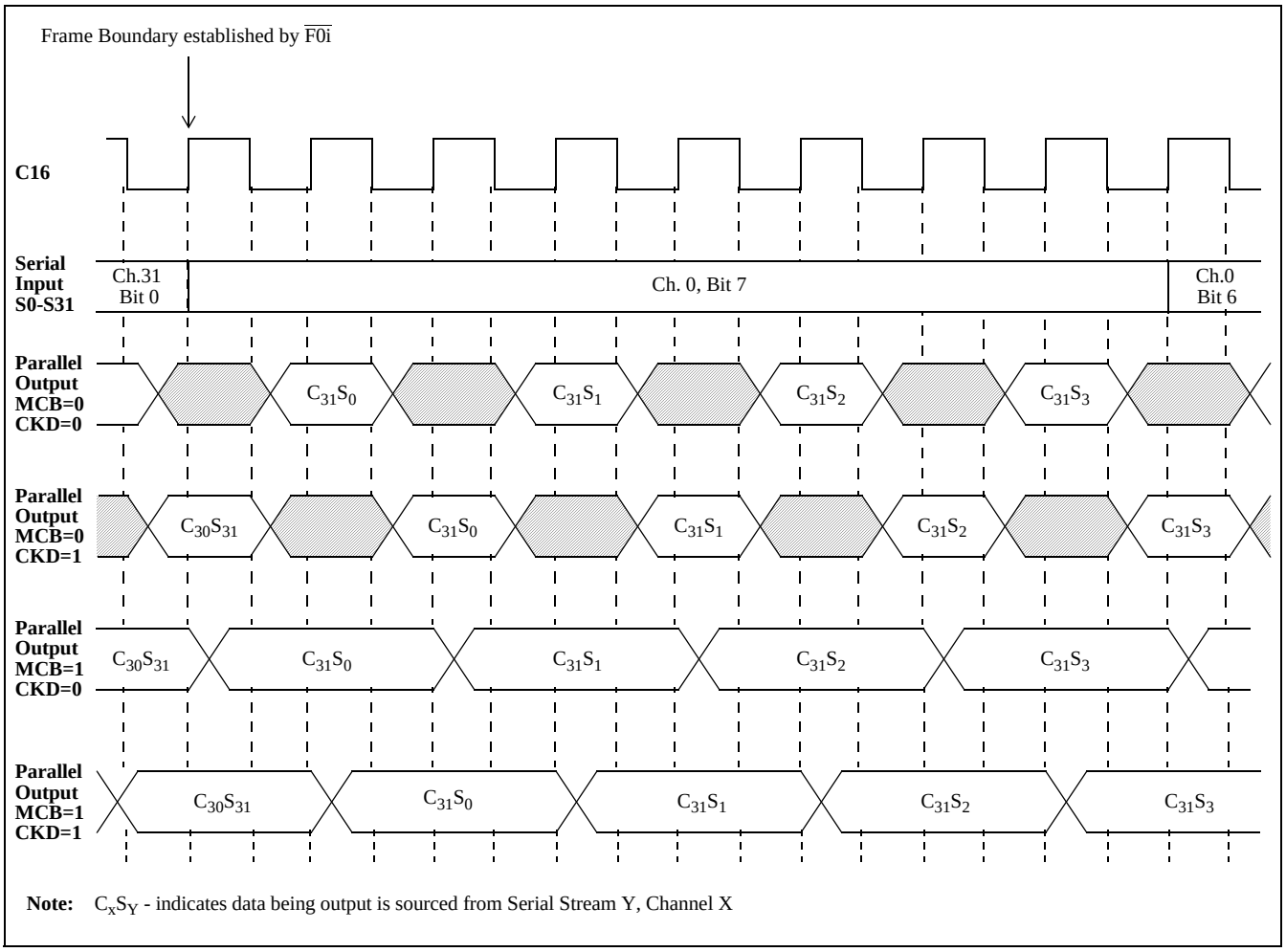


Figure 7 - Functional Data I/O Timing in Serial to Parallel Mode (MCA = 0)

Functional Description

The MT9085 Parallel Access Circuit (PAC) is a 68 pin monolithic device. It interfaces a parallel 8 bit, time division, multiplexed bus to 32 or 16 time division multiplexed serial streams. The device can be configured to perform either parallel to serial conversion or serial to parallel conversion. A single PAC device can handle 1024 channels. The data on the parallel bus is in a format suitable for interfacing with the Zarlink MT9080 Switch Matrix Module (SMX). The data rate on the serial streams can be selected to be 2.048 or 4.096 Mbit/s.

The serial input/output format conforms to the ST-BUS requirements when the data rate is 2.048 Mbit/s (see Figure 3). The ST-BUS is a time-division, multiplexed serial bus with 32, eight bit channels per frame. Frame boundaries are delineated by the frame pulse. Data on the serial streams is clocked in and out with the C16i clock.

When the device is configured for 4.096 Mbit/s data rate operation, the first 16 (S0-S15) of the 32 serial streams are used. Each of the 16 time-division multiplexed serial streams is made up of 64 channels. Data is clocked in or out with the C16i clock.

Parallel To Serial Conversion

The MT9085 can be configured to perform parallel to serial conversion by tying the MCA input high.

Data on the eight bit parallel bus (P0-P7) is clocked into the device with the C16i clock. It is clocked out on the serial streams at either 2.048 Mbit/s ($\overline{2}$/4S =0) or at 4.096 Mbit/s ($\overline{2}$/4S=1). See Figures 16, 17 and 19 for timing information.

Contiguous channels clocked into the device are output on the serial streams in an interleaved manner on each of the serial outputs. For example when the device is configured for 2.048 Mbit/s data rate, the first 32 parallel channels clocked into the device will be clocked out during channel 0 on serial streams 0 to 31. Channel 1 on serial streams 0 to 31 will contain data from the next 32 timeslots. On any single serial stream, consecutive output channels are sourced from every 32nd parallel input channel (see Figures 6 and 8). When the device is configured for 4.096 Mbit/s serial output operation, contiguous channels on the serial streams are sourced from every 16th parallel input channel.

Data on the eight bit parallel bus is clocked into the device with the C16 clock. The level asserted on the MCB input specifies whether the data is clocked into the device on the falling edge or the rising edge of C16. The relative phase of the critical edge with respect to the system frame boundary is defined by the level asserted on the CKD pin as illustrated in Figure 16. The flexibility in input timing permits the PAC to be easily interfaced to the SMX in 1024 and 2048 switching applications. Refer to the applications section of this data sheet for more details.

The delay through the PAC is approximately one ST-BUS channel time when the device is operated in 2.048 Mbit/s mode, i.e., any specific channel clocked into the device will be clocked out one ST-BUS channel later. In the 4.096 Mbit/s mode, the delay is equal to eight C4 clock cycles.

Serial output channel timeslots can be tri-stated by setting $\overline{OE}$ high during a specific parallel channel timeslot. The timing for $\overline{OE}$ is described in Figures 6 and 21. Note that the level asserted on MCB affects the operation of $\overline{OE}$.

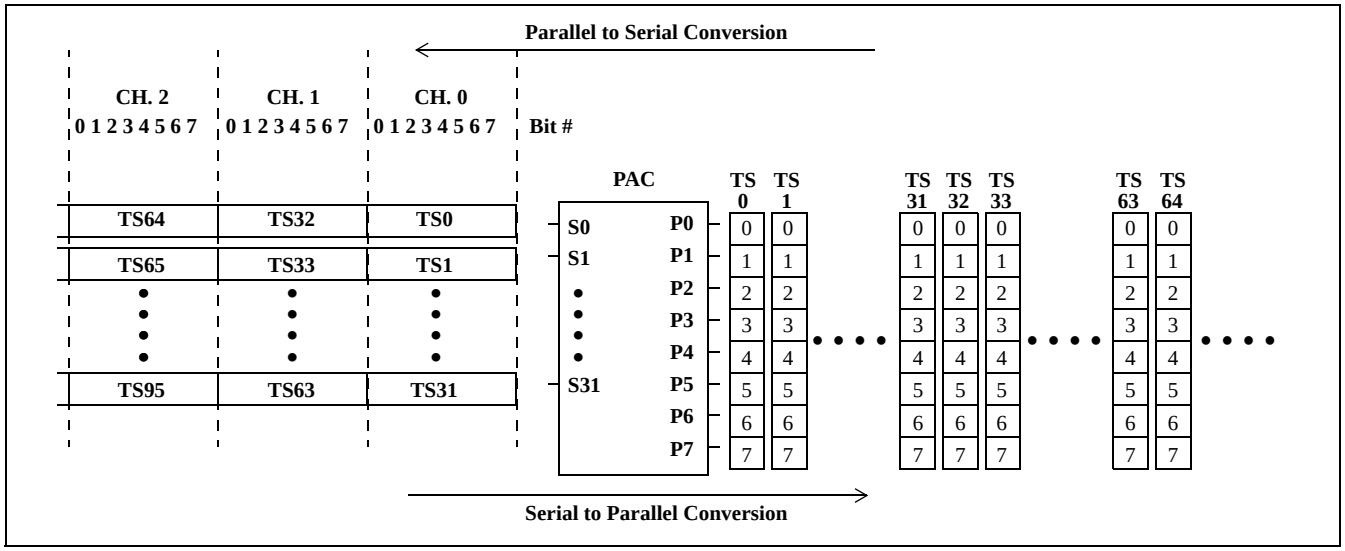


Figure 8 - PAC Operation at 2.048 Mbit/s

Serial to Parallel Conversion

The MT9085 can be configured to perform serial to parallel conversion by tying the MCA pin low. A single PAC will accept 1024 channels on the 32 or 16 serial streams and output the data onto the parallel bus as illustrated in Figure 8.

The data on the serial input streams can be clocked in at 2.048 Mbit/s or at 4.096 Mbit/s by setting the appropriate level on the 2/4S pin. See Figures 16 and 17 for timing details.

Data is clocked out on the parallel bus with the C16 clock (see Figure 18 for timing details). The parallel output bus will be actively driven for two C16 clock periods when MCB is tied high. Data is output with every second rising clock edge. Setting MCB low will enable the output drivers for only one C16 clock period in any specific parallel channel timeslot. The actual phase relationship between the system frame boundary and the parallel output timeslots is affected by the level asserted on the CKD input (see Figure 7). The flexibility in output timing permits the PAC to be easily interfaced to the SMX in 1024 and 2048 channel configurations. Refer to the applications section of this data sheet for more information.

The delay through the PAC is approximately one ST-BUS channel when the device is configured for 2.048 Mbit/s serial rate. In the 4.096 Mbit/s mode, the delay is equal to approximately eight C4 clock cycles.

Timing and Framing Signals

The PAC requires two clock signals. A 16.384 MHz master clock (C16) is used to clock data in and out of the device on the parallel bus. A 4.096 MHz clock (C4i), phase locked to C16i, clocks in the frame pulse. The positive C16i edge immediately after the C4i falling edge which clocks in F0i defines the internal frame boundary. The two separate clock inputs permit synchronization of the MT9085 to system timing in which the frame pulse is derived from a 4.096 MHz clock.

The PAC generates all framing signals necessary to construct a 1024 channel or a 2048 channel switch matrix using the SMX. The DFPo signal is used as a framing signal for the SMXs operated as the Data Memory. The CFPo is used to synchronize Connect Memory timing in a typical 1K or 2K switch application (refer to the application section in this data sheet for more information). The timing of both DFPo and CFPo signals is affected by the level asserted on the CKD input as shown in Figure 15.

The PAC outputs ST-BUS timing signals, F0o, C2o and C4o derived from C16i. The phase relationship between the frame boundary established by F0i and F0o is illustrated in Figures 4 and 5.

Applications

1024 Channel Digital Time-Space Switch

A 1024 channel serial time-space digital switch design is illustrated in Figure 9.

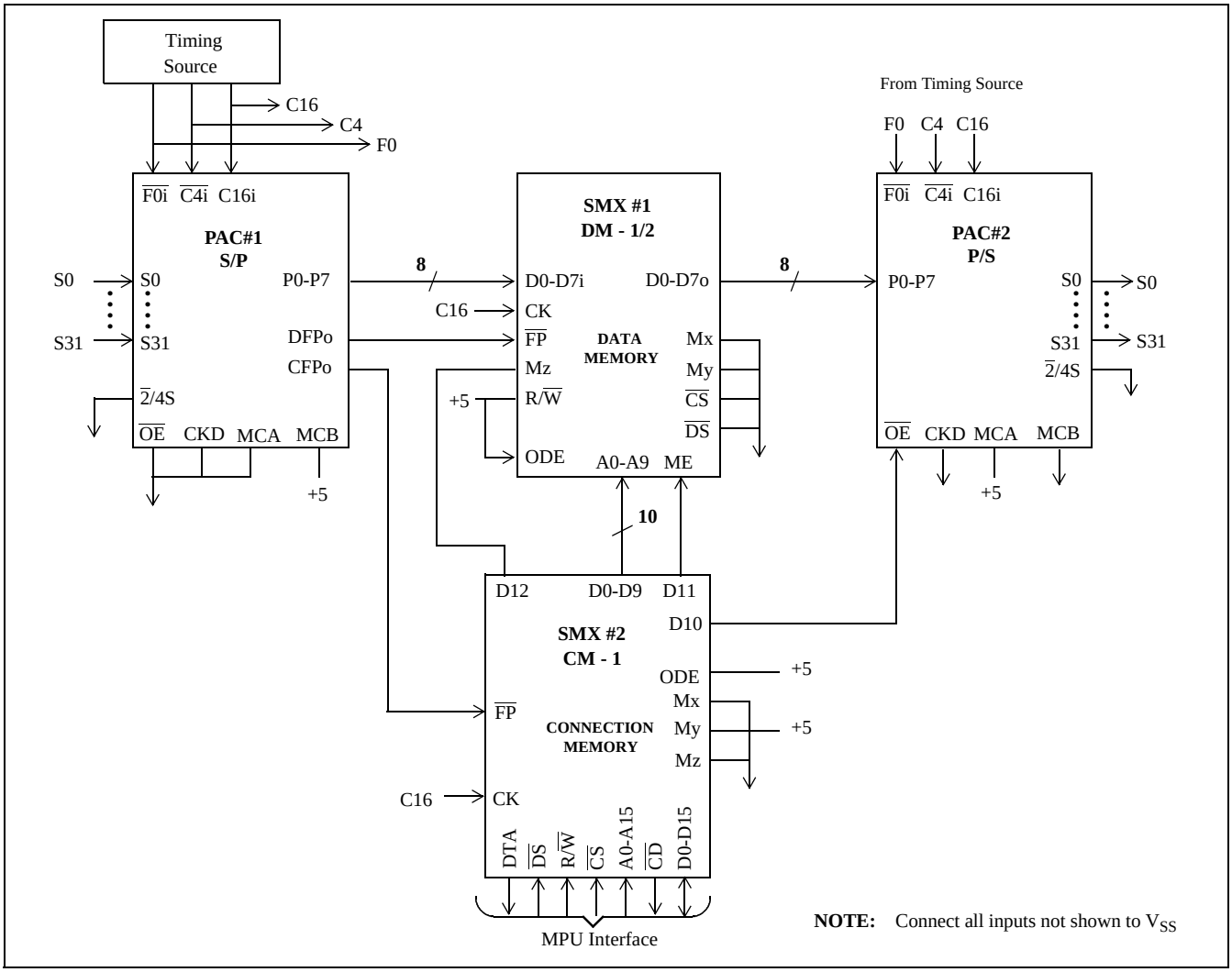


Figure 9 - 1024 Channel Switch Matrix Using the PAC and SMX

The main switching function is accomplished using two MT9080s (SMXs). One SMX is operated in the Data Memory mode and the second serves as the Connection Memory. Refer to the SMX data sheet for more information on this configuration. The serial to parallel conversion function is provided by a PAC configured for 2.048 Mbit/s operation ($\overline{2}$/4S = 0). The MCB input in this PAC is tied high to ensure data output by the PAC meets SMX input setup and hold requirement. PAC #2 performs the parallel to serial function; MCA is set high. The MCB input in this device is set low to allow data to be clocked in with the falling edge of C16.

The main timing source generates a 16.384 MHz clock phase locked to a 4.096 MHz clock. The framing signal input to PAC#1 at $\overline{F0i}$ should meet the requirements specified in Figure 13 of this data sheet. In some applications where a master 16.384 MHz oscillator is used for system timing, the $\overline{C4i}$ and $\overline{F0i}$ clocks could be derived directly from it. In applications where a 4.096 MHz clock signal is available, the 16.384 MHz clock can be generated using a phase-lock loop.

Framing signals for both the SMXs are generated by PAC #1. DFPo is connected to $\overline{FP}$ input of the Data Memory. CFPo is connected to the FP input of the Connection Memory. PAC #2 is configured to perform parallel to serial conversion.

The DFPo and CFPo signals ensure that all timing requirements necessary to interface the SMXs with the PACs are met while input and output serial frames are aligned.

The maximum delay through the switch is approximately one frame plus two serial channels when SMX#1 is operated in Data Memory Mode-1. When the SMX is operated in Data Memory Mode-2, the maximum delay is two frames. In this case, the channels are double buffered; frame integrity is maintained for all switching configurations.

In the example configuration shown in Figure 9 the $\overline{OE}$ pin of PAC #2 is connected to D10 on the Connection Memory. Setting bit 10 high in the Connection Memory location corresponding to a serial channel timeslot will result in the output driver for the specific stream being disabled during that serial channel timeslot. D11 is connected to the ME input of SMX1 and D12 is connected to a mode select pin (Mz). Consequently, the levels on these outputs can be set high or low by writing to the appropriate memory location corresponding to the selected output channel. The mapping of the control functions on to Connection Memory data bits is illustrated in Figure 10.

The data on the PAC serial streams is byte interleaved as described in the Functional Description section in this data sheet. The SMX channel number corresponding to the channel on the serial streams can be determined directly by specifying the serial channel and stream number in binary as shown in Figure 11. For example, serial channel 4, stream 2 corresponds to SMX channel number Hex 0082. In order to program the matrix for switching, the input channel address is written to the Connection Memory address corresponding to the serial output channel. The bits controlling features such as $\overline{OE}$, ME, and Mz should be set or reset accordingly at the same time. For example. if channel 4 on stream 2 is to be switched to channel 10 on stream 1, the following binary word is written to Connection Memory address corresponding to the output channel (Hex 0141):

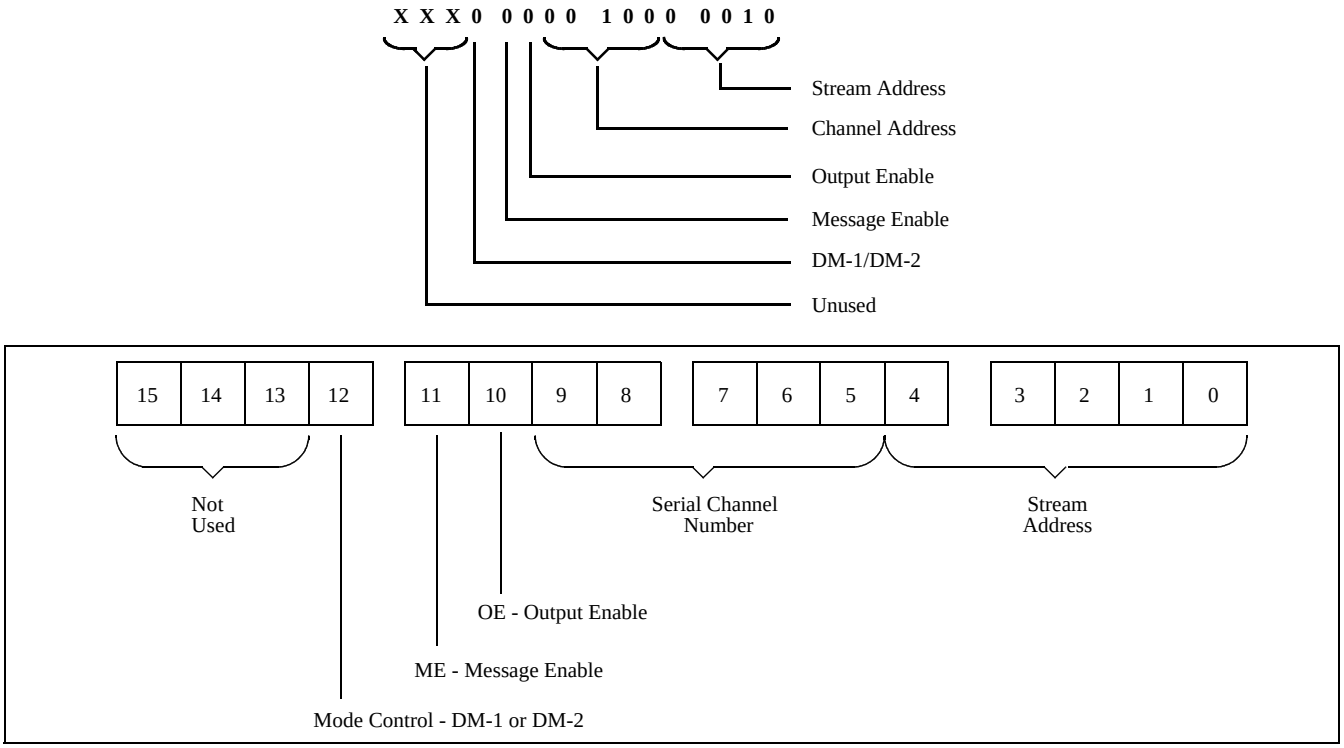


Figure 10 - Mapping of Data Memory and PAC Control Functions on Connection Memory Data Bits

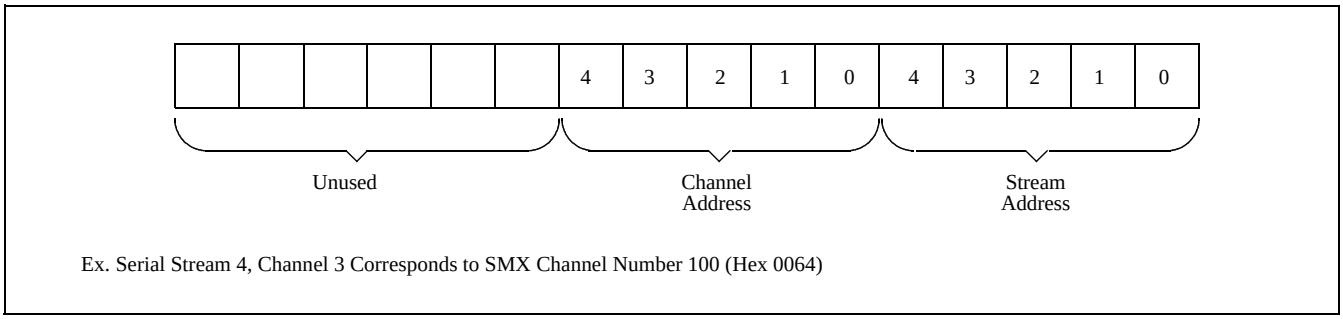


Figure 11 - Decoding SMX Channel Number from Serial Stream & Channel Address 1024 Switch Configuration

2048 Channel Digital Space-Time Switch Application

A 2048 channel serial time-space digital switch design is illustrated in Figure 12.

The main switching function is accomplished using three MT9080s (SMXs). Two SMXs function as the data memory, while the third is operated in Connect Memory mode. Refer to the SMX data sheet for more information on this configuration. The Serial to parallel conversion for 2048 channels is handled by two PACs. PAC #1a and PAC #1b. Both are configured for 2.048 Mbit/s operation ($\overline{2}$/4S=0). The MCB input is tied low in both devices. The parallel data bus on each of the devices will be actively driven for one C16 clock period. The CKD input is set low in one of the devices and set high in the other. This will cause the output timing of the two PACs to be off set by one C16 clock period. Consequently, the parallel output of one device will be disabled while the other is active.

The parallel to serial conversion is also accomplished with two PACs. Data from the common SMX parallel bus is clocked into each PAC in alternate clock periods.

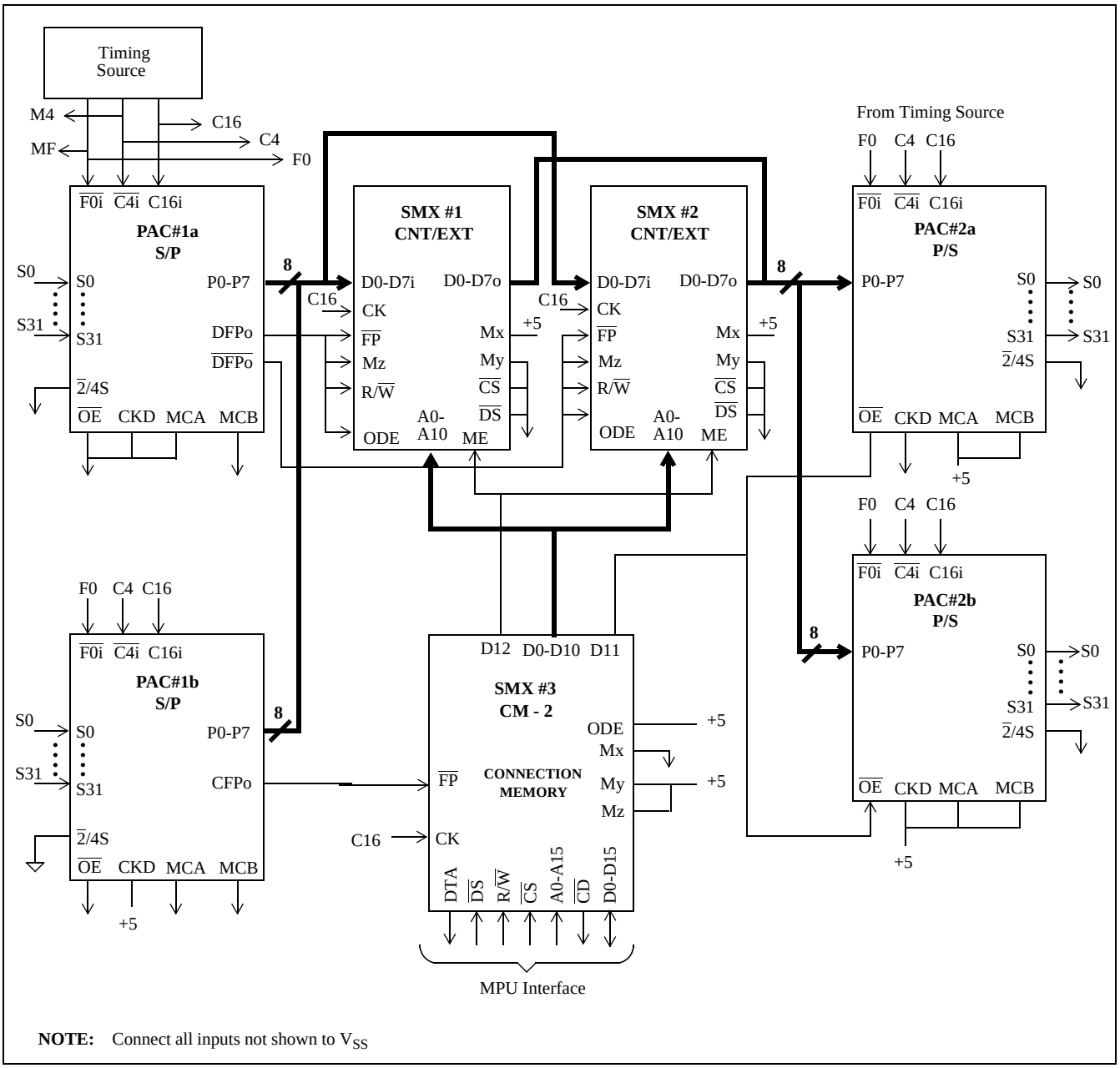
The timing source generates a 16.384 MHz clock phase locked to a 4.096 MHz clock. The framing signal input to PAC #1a at $\overline{F0i}$ should meet the requirements specified in this data sheet. In some applications where a master 16.384 MHz oscillator is used for system timing, the $\overline{C4i}$ and $\overline{F0i}$ clocks could be derived directly from it.

The DFPo and $\overline{DFPo}$ generated by PAC #1a are used to switch the mode of operation of the Data Memory SMXs between Counter and External modes and also serve as the frame pulse for the two SMXs. Because DFPo and $\overline{DFPo}$ are complementary signals, one of the two SMXs is operated in the Counter mode while the second one is operated in the External mode. The states of the other control inputs, R/$\overline{W}$ and ODE, are changed accordingly.

The SMX configured as the Connection Memory, is fed a frame pulse from PAC #1b. The phase alignment of CFPo with respect to DFPo ensures that timing requirements for proper operation of the SMXs are met. Refer to the SMX data sheet for more information on the timing requirements.

The maximum delay through the switch is two frames. Channels are double buffered and frame integrity is maintained for all switching configurations.

For more information, see Zarlink's Application Note MSAN-135, *"Design of Large Digital Switching Matrices using the SMX/PAC"* (in this data book) and Application Sheet MSAS-62 *"16.384 MHz Clock Generation for SMX/PAC"* (available from Zarlink).



NOTE: Connect all inputs not shown to V_{SS}

Figure 12 - 2048 Channel Switch Matrix Using the PAC and SMX

Absolute Maximum Ratings* - Voltages are with respect to Ground (V_{SS}) unless otherwise stated.

	Parameter	Symbol	Min.	Max.	Units
1	V_{DD}-V_{SS}		-0.3	7	V
2	Voltage on Digital Inputs	V_I	V_{SS}-0.3	V_{DD}+0.3	V
3	Voltage on Digital Outputs	V_O	V_{SS}-0.3	V_{DD}+0.3	V
4	Current at Digital Outputs	I_O		40	mA
5	Storage Temperature	T_S	-40	125	°C
6	Package Power Dissipation	P_D		2	W

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to Ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max	Units	Test Conditions
1	Operating Temperature	T_{OP}	-40		70	°C	
2	Positive Supply	V_{DD}	4.5		5.5	V	
3	Input Voltage	V_I	0		V_{DD}	V	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Voltages are with respect to Ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	INPUTS	Supply Current	I_{DD}			50	mA	Outputs unloaded
2		Input High Voltage - all pins except $\overline{C4i}$, $\overline{F0i}$, S0-S31	V_{IH}	$0.7V_{DD}$			V	
3		Input Low Voltage - all pins except $\overline{C4i}$, $\overline{F0i}$, S0-S31	V_{IL}	0		$0.3V_{DD}$	V	
4		Input High Voltage - $\overline{C4i}$, $\overline{F0i}$, S0-S31	V_{IH}	2.0			V	
5		Input Low Voltage - $\overline{C4i}$, $\overline{F0i}$, S0-S31	V_{IL}			0.8	V	
6		Input Leakage Current	I_{IL}			±10	µA	

DC Electrical Characteristics - Voltages are with respect to Ground (V_{SS}) unless otherwise stated.

7	OUTPUTS	Output Low Current S0-S31	I_{OL}	8			mA	V_{OL}=0.4V
8		Output Low Current all outputs except S0-S31	I_{OL}	8			mA	V_{OL}=0.3V_{DD}
9		Output High Current S0-S31	I_{OH}	8			mA	V_{OH}=2.4V
10		Output High Current all outputs except S0-S3	I_{OH}	8			mA	V_{OH}=0.7V_{DD}
11		High Impedance Leakage	I_{OZ}			10	µA	
12		Input Pin Capacitance	C_i			10	pF	
13		Output Pin Capacitance	C_o		10		pF	V_{DD}=5.0V ±10%

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Input Frame Pulse and Clock Timing (See Figure 13) - Voltages are with respect to Ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	C16 Clock Period	t_{C16P}	60	61	62	ns	
2	C4 Clock Period	t_{C4P}	219	244	269	ns	
3	C16 Pulse Width Low	t_{C16L}	25			ns	
4	C16 Pulse Width High	t_{C16H}	25			ns	
5	C4 Setup Time	t_{C4S}	-10		25	ns	
6	Frame Pulse Setup Time	t_{FPS}	5		200	ns	
7	Frame Pulse Hold Time	t_{FPH}	5			ns	

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

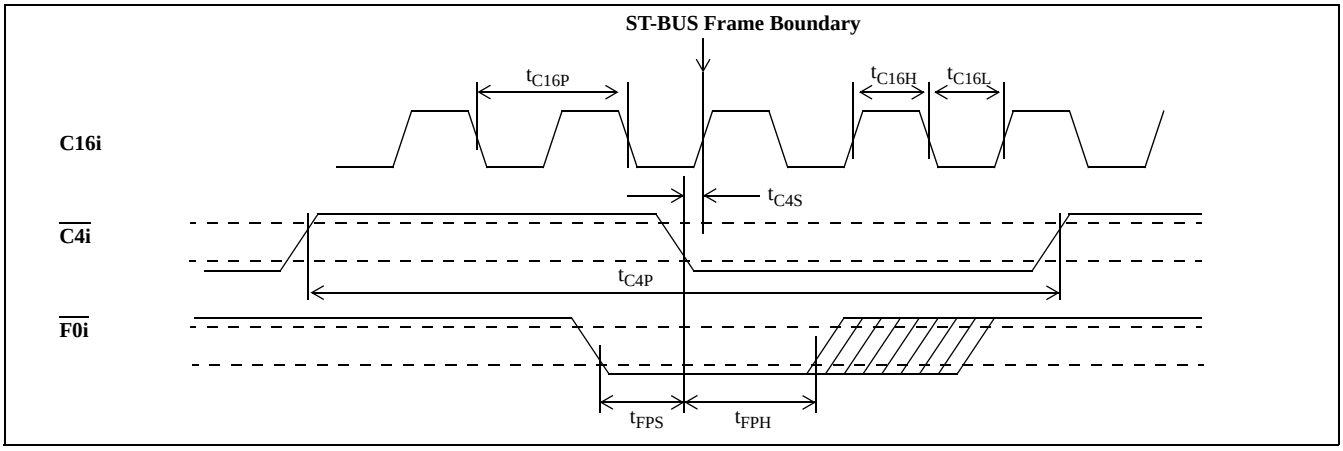


Figure 13 - ST-BUS Frame Pulse and Clock Timing

AC Electrical Characteristics† - Output Clocks and Frame Pulse Timing (See Figure 14) - Voltages are with respect to Ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Frame Pulse Delay	t_{FPD}	0		31	ns	C_L=85pF
2	C4 Clock Delay	t_{C4D}	0		28	ns	C_L=85pF
3	C2 Clock Delay	t_{C2D}	0			ns	C_L=85pF

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

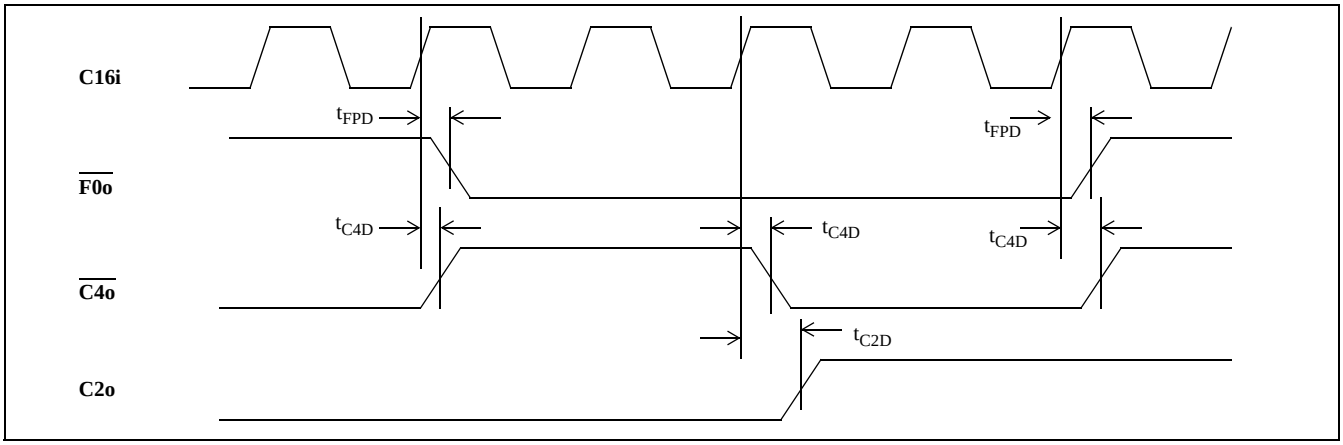


Figure 14 - $\overline{F0o}$, $\overline{C4o}$ and C2o Output Clock Timing

AC Electrical Characteristics† - Data Memory and Connect Memory Frame Pulse (See Figure 15) - Voltages are with respect to Ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Data - Memory Frame Pulse Delay	t_{DFPo}	0		37	ns	C_L=85 pF
2	Connection - Memory Frame Pulse Delay	t_{CFPo}	0		30	ns	C_L=85 pF

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

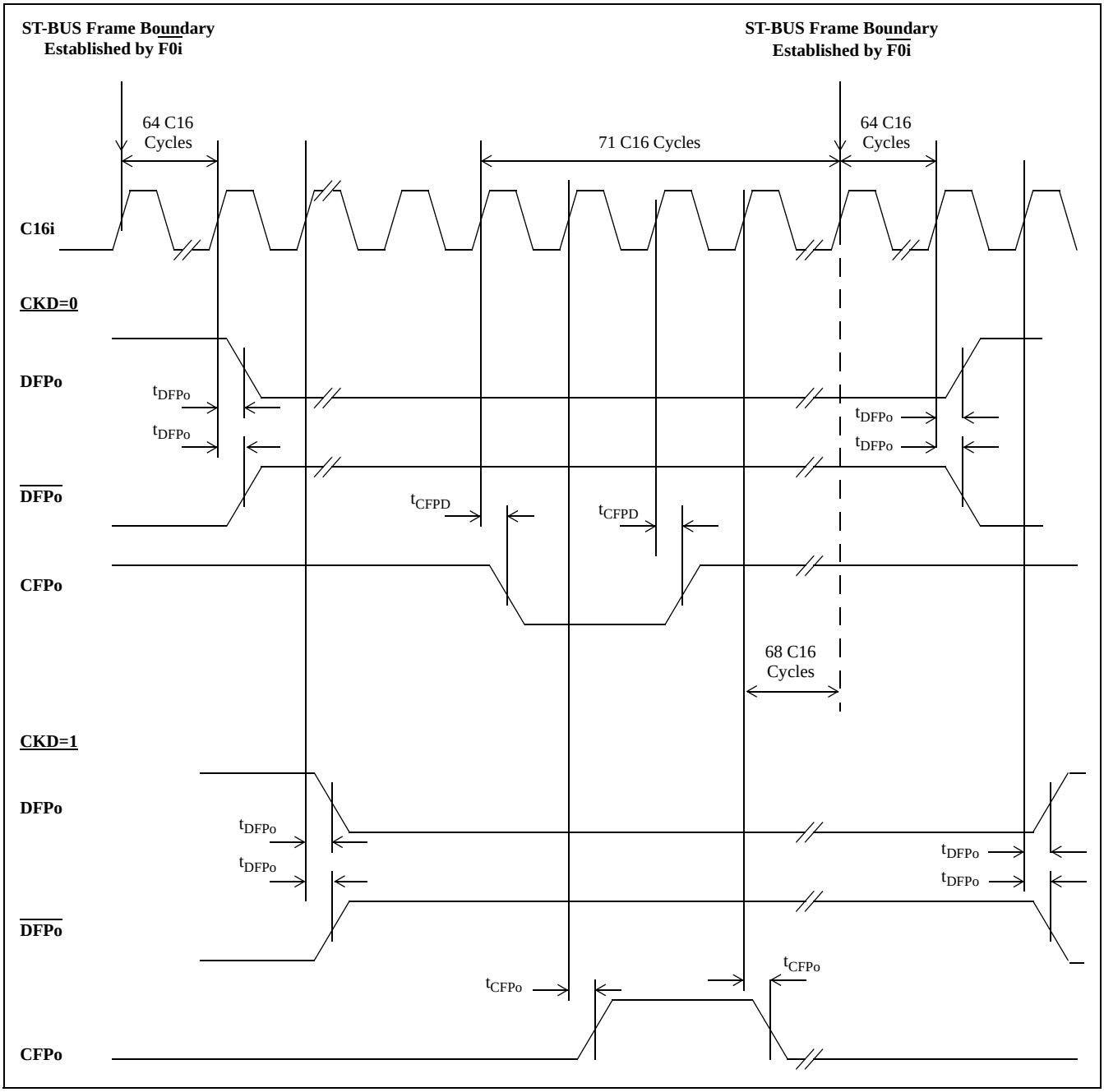


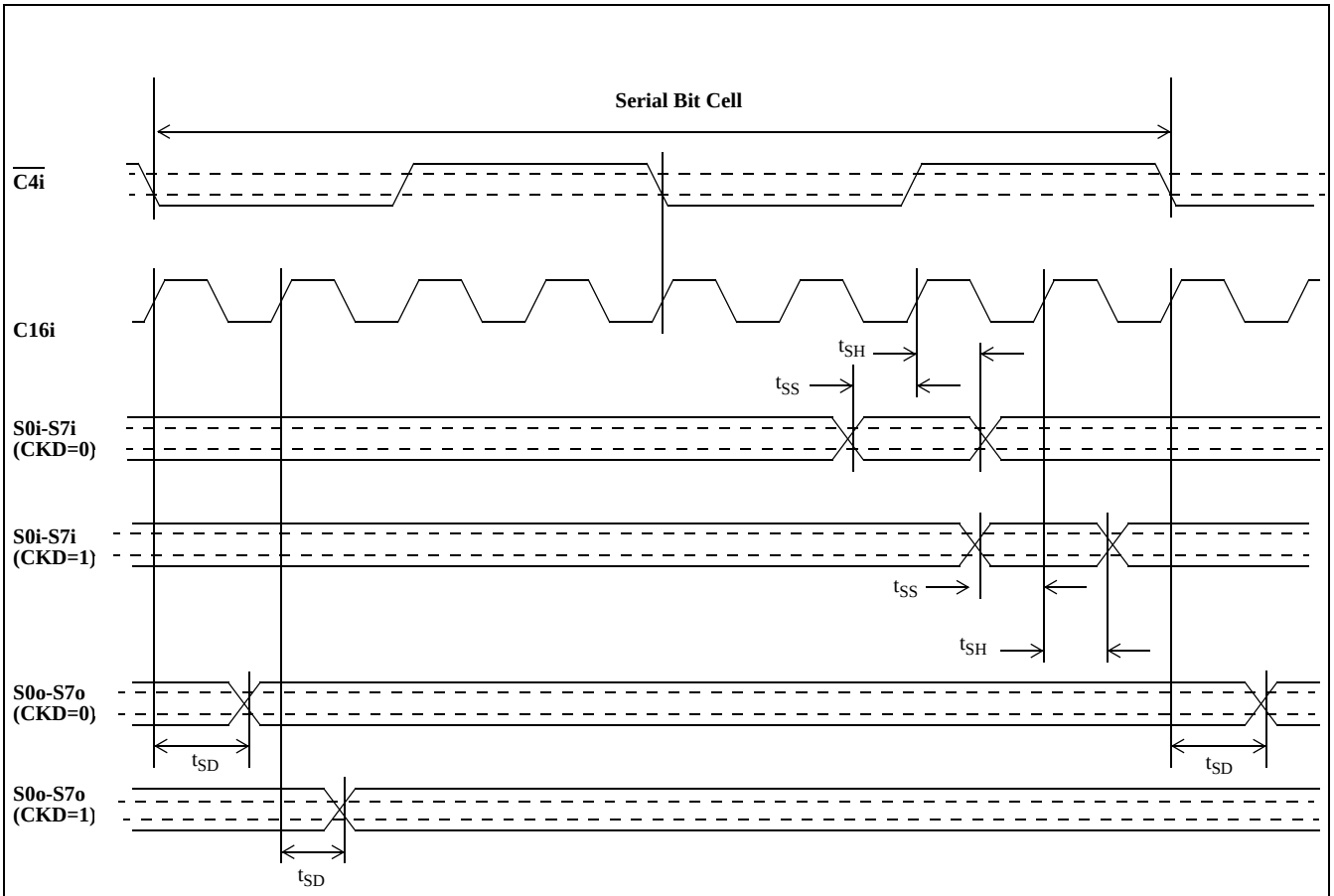
Figure 15 - $\overline{\text{DFPo}}$ and CFPo Output Timing

AC Electrical Characteristics† - Serial Input and Output Timing in 2 MHz Mode ($\overline{2}$/4S=0) (See Figure 16) -
Voltages are with respect to Ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Serial Input Setup Time	t_{SS}	0			ns	
2	Serial Input Hold Time	t_{SH}	24			ns	
3	Serial Output Delay	t_{SD}					
	Active to Active				47	ns	C_L=150pF
	High Impedance to Active				47	ns	C_L=150pF
	Active to High Impedance				44	ns	C_L=150pF

‡ Timing is over recommended temperature & power supply voltages

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.



Note: 1) The phase relationship of $\overline{C4i}$ and C16i depends on the user's timing source (see Fig. 13 for device related constraints).

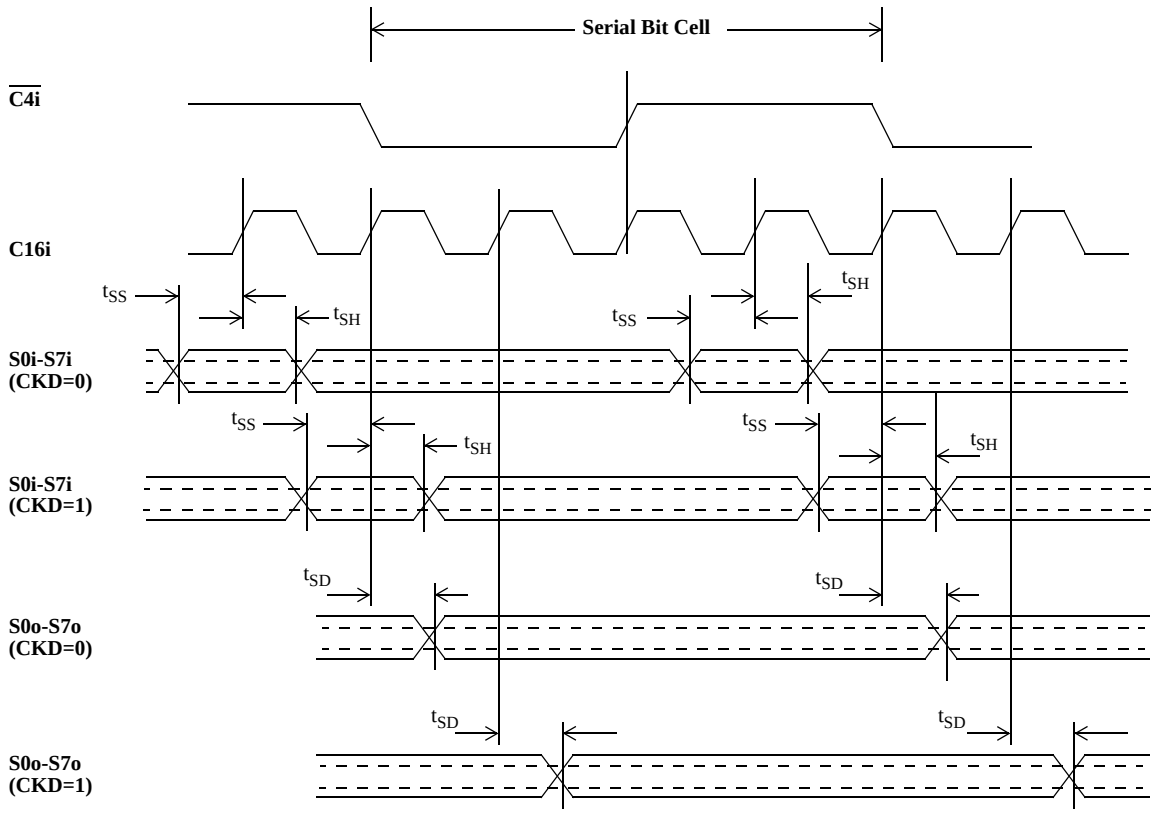
2) Timing measurements for inputs are referenced to/from a low voltage of 0.8V and a high voltage of 2.0V. Measurements for outputs are referenced to/from a low voltage of 0.4V to a high voltage of 2.4V

Figure 16 - Serial Input and Output Timing in 2 Mbit/s Mode ($\overline{2}$/4S=0)

AC Electrical Characteristics† - Serial Input and Output Timing in 4 MHz Mode ($\overline{2}$/4S=1) (See Figure 17) - Voltages are with respect to Ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Serial Input Setup Time	t_{SS}	0			ns	
2	Serial Input Hold Time	t_{SH}	24			ns	
3	Serial Output Delay	t_{SD}					
	Active to Active				47	ns	C_L=150pF
	High Impedance to Active				47	ns	C_L=150pF
	Active to High Impedance				44	ns	C_L=150pF

† Timing is over recommended temperature & power supply voltages
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.



Note: 1) The phase relationship of $\overline{C4i}$ and C16i depends on the user's timing source (see Fig. 13 for device related constraints).

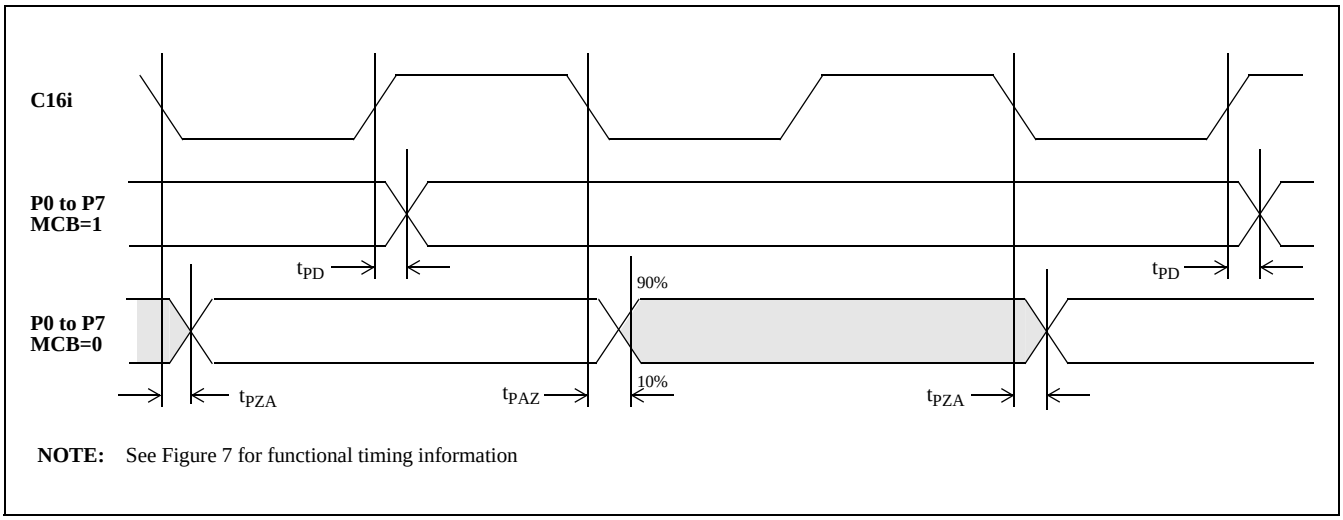
2) Timing measurements for inputs are referenced to/from a low voltage of 0.8 V and a high voltage of 2.0 V. Measurements for outputs are referenced to/from a low voltage of 0.4 V to a high voltage of 2.4 V

Figure 17 - Serial Input and Output Timing in 4 Mbit/s Mode ($\overline{2}$/4S=1)

AC Electrical Characteristics† - Parallel Output Timing (See Figure 18) - Voltages are with respect to Ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Parallel Output Delay	t_{PD}			28	ns	C_L=85pF
2	Parallel Output Delay High Impedance to Active	t_{PZA}			28	ns	C_L=85pF
3	Parallel Output Delay Active to High Impedance	t_{PAZ}			28	ns	C_L=85pF

† Timing is over recommended temperature & power supply voltages
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.



NOTE: See Figure 7 for functional timing information

Figure 18 - Parallel Output Timing

AC Electrical Characteristics† - Parallel Input Timing (See Figure 19) - Voltages are with respect to Ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Parallel Input Setup Time	t_{PS}	0			ns	
2	Parallel Input Hold Time	t_{PH}	5			ns	

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

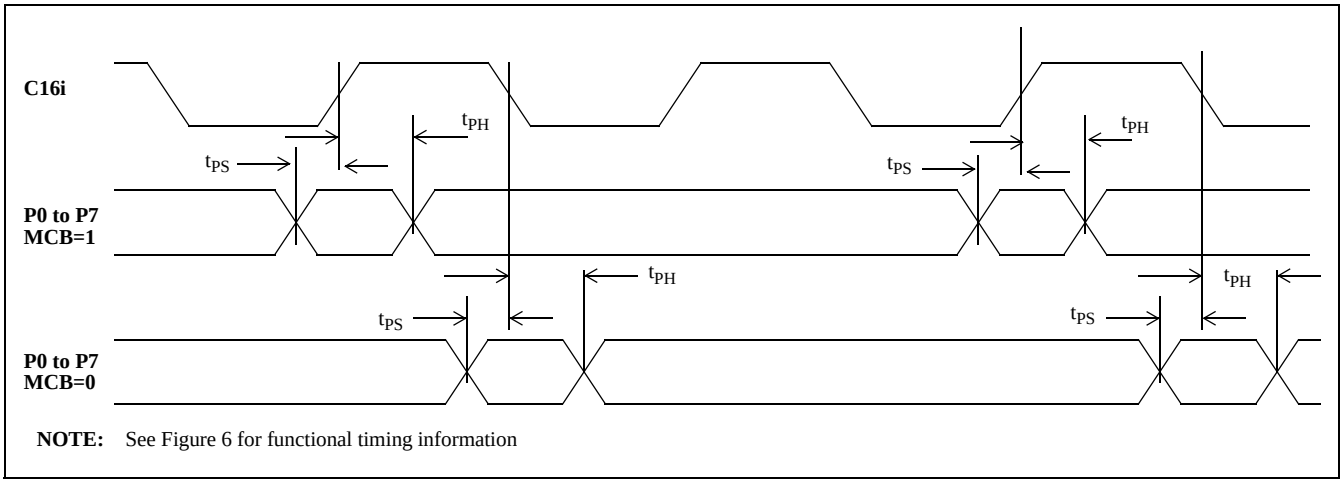


Figure 19 - Parallel Input Timing

AC Electrical Characteristics† - Output Enable Timing, Serial to Parallel Mode (See Figure 20) - Voltages are with respect to Ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Parallel Output Delay Active to High Impedance	t_{PAZ}			23	ns	C_L=85pF
2	Parallel Output Delay High Impedance to Active	t_{PZA}			25	ns	C_L=85pF

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

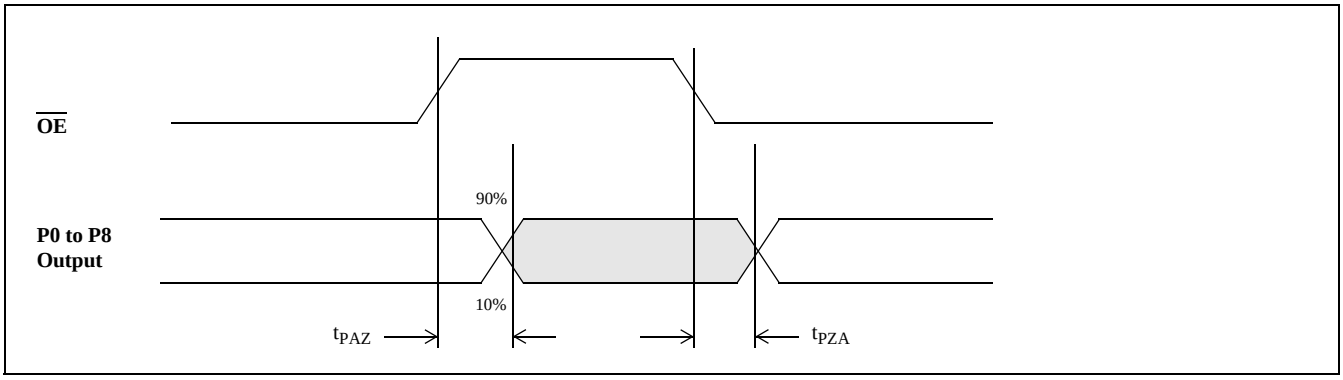


Figure 20 - $\overline{OE}$ Timing in Serial to Parallel Mode

AC Electrical Characteristics† - Output Enable ($\overline{OE}$) Timing, in Parallel to Serial Mode (See Figure 21) - Voltages are with respect to Ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	$\overline{OE}$ Setup Time	t_{OES}	2			ns	
2	$\overline{OE}$ Hold Time	t_{OEH}	10			ns	

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

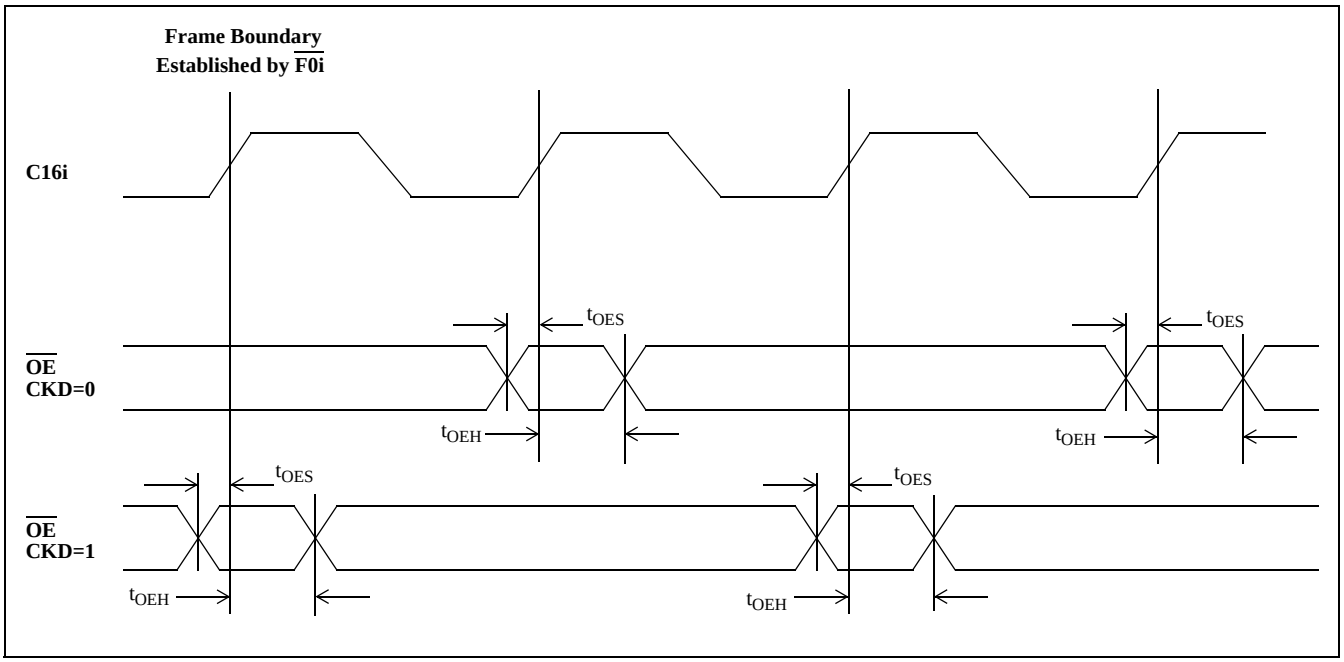


Figure 21 - $\overline{OE}$ Timing in Parallel to Serial Mode

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