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Highly-Integrated, Fully-Featured 6-Port DS3/E3/STS-1 Line Interface Unit with Digital Jitter-Attenuator and STS-1 to DS3/E3 Desynchronizer

M28356

This highly-integrated, low-power solution is designed for transmission applications including add/drop multiplexers, routers, ATM multi-service switches, digital cross connects and DS3 to STS-1 mappers. The M28356 incorporates six independent receivers, transmitters and jitter-attenuators in a single 27 mm BGA package. Each channel of the M28356 can be independently configured to operate in DS3 (44.736MHz), E3 (34.368 MHz) or STS-1 (51.84 MHz) rates. Each channel of the transmitter can be turned off and tri-stated for redundancy support and power conservation.

The M28356 adaptive receive equalizer provides high noise interference margin and it is capable of receiving the data over 1350 feet of cable with 25 dB of flat loss.

The M28356 includes transmit monitoring features that determine the integrity of the signals and continuously monitor the quality of the connections in both receive and transmit directions. It incorporates clock rate adapter (CLAD) in generating the independent line rate clocks for DS3, E3 and STS-1. The internal clock management scheme includes an internal crystal oscillator using a common 19.44 MHz external passive crystal.

The M28356 supports local, remote and digital loop-backs. It also contains an on-chip PRBS generation and detection with the capability to insert and detect single bit error.

The embedded digital jitter-attentuator (DJAT) technology leverages Mindspeed's advance digital signal processing techniques, along with extensive knowledge of analog mixed signal design, to provide a complete solution of its kind to adapt and fully smooth an STS-1 clock (with overhead gaps) to a network compliant signal level 3 (DS3) line clock.

KEY FEATURES

- Programmable pulse shape adjustability
- High density: up to 6 independent XMT and RCV LIUs with digital jitter-attenuator and desynchronizer for DS3, E3 and STS-1 in one package
- Complies with Telcordia GR-253, GR-499, ETSI TBR-24, ANSI T1.105.03b, as well as ITU-T G.703, G.751, G.755, G.783 and G.823 standards
- Automatic adaptive equalizer capable of recovering data with up to 1350 feet of cable with 25 dB of flat loss
- On-chip clock rate adapters (CLADs) providing DS3, E3 and STS-1 clock rates from a single 19.44 MHz crystal
- RLOS receive loss of signal indicator compliant with ITU G.775
- Supports local, remote and analog (RCV to XMT) loop-backs
- PRBS generator/detector per channel

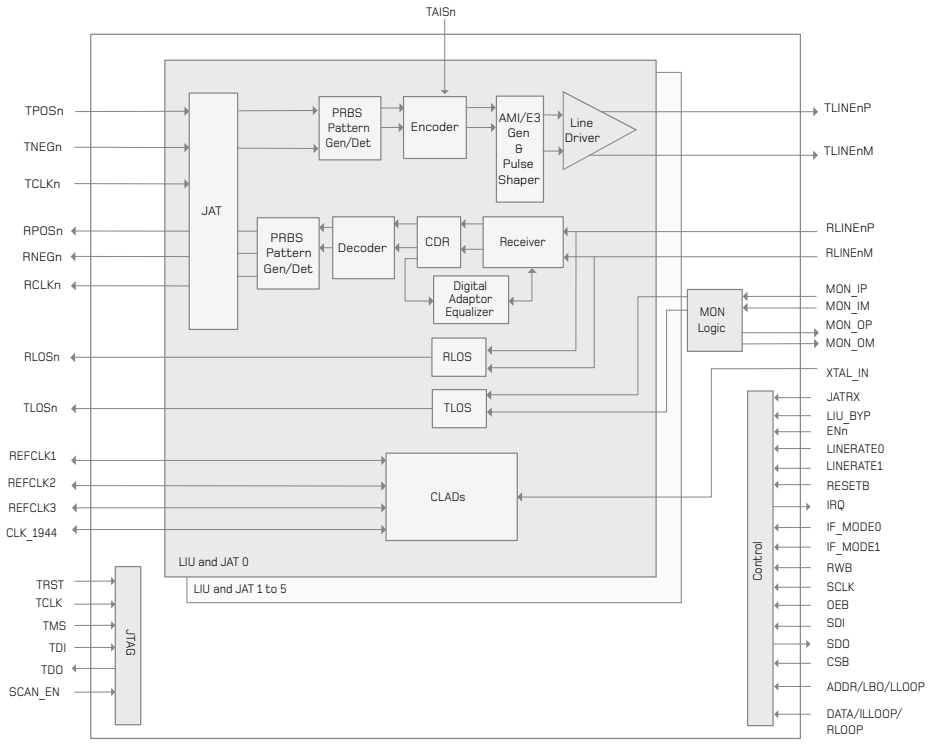
The M28356 complies with Telcordia GR-253, GR-499, ETSI TBR-24, ANSI T1.105.03b, as well as ITU G.751, G.755, G.783 and G.823 standards. For Category I interfaces, the M28356 DJAT technology smooths the inherent jitter due to mapping/demapping, bit stuffing and pointer adjustments in DS3 or E3 payloads extracted from STS-1 frames, generating a network compliant clock.

The M28356 seamlessly interfaces with Mindspeed's CX2834x (multi-port DS3/E3 framers) and CX28365 (12-port T3/E3 framer ATM TC) —providing a complete solution for high density DS3/E3 line cards.

Digital Jitter–Attenuator and Desynchronizer

DJAT smooths the phase differences of clock signals due to phase variations between STRATUM clocks, bit stuffing and pointer adjustments caused by frequency differences and demapping of STS-1 payloads.

There are two modes of operations for the embedded DJAT. The first involves attenuating jitter from a clock signal of DS3, E3 or STS-1 data rates. This is typically referred to as a Category II interface. Clock jitter on this interface is also referred to as line timing jitter. The second mode of operation, for a Category I interface, involves extracting a DS3 or E3 payload from a STS-1 frame. Clock jitter on this interface is also referred to as demapping jitter.



M28356 block diagram

Microprocessor Interface

In hardware mode, the M28356 device requires little or no control and may be statically configured. The M28356 device also supports a 4-signal serial and the parallel 8-bit microprocessor interface that allows access to extended features such as the PRBS generators and biit error rate (BER) counters. Control and status registers are memory mapped.

Product Features

- **High density: up to 6 independent XMT and RCV LIUs with digital jitter–attenuator and desynchronizer for DS3, E3 and STS–1 in one package**
- **Independent and configurable per–channel jitter attenuator compliant with jitter transfer template outlined in ITU G.751, G.752, G.755, GR–253 and GR–499–CORE**
- **Meets ETSI TBR–24 jitter transfer requirements**
- **Automatic adaptive equalizer capable of recovering data with up to 1350 feet of cable with 25 dB of flat loss**
- **On–chip Clock Rate Adapters (CLADs) providing DS3, E3, and STS–1 clock rates from a single 19.44 MHz crystal**
- **Programmable pulse shape adjustability**
- **Fully compliant with ITU–T G.703 pulse template requirements for E3**
- **DC continuity check of receive inputs**
- **RLOS receive loss of signal indicator compliant with ITU G.775**
- **Supports Transmit Clock with duty cycle of 30–70%**
- **Selectable settings for the recovered receive data while the RLOS condition is declared**
  - **Three–state on RLOS**
  - **All ones on RLOS**
  - **All zeros (squelch) on RLOS**
- **24–bit receive counters per port for LCV, EXZ and BPV**
- **Programmable FIFO depth optimal for SONET/SDH**
- **Crystal–less jitter attenuation**
- **Programmable clocking of both inputs and outputs on either edge**
- **PRBS generator/detector per channel**
- **Supports local, remote and analog (RCV to XMT) loopbacks**
- **One–second timer for event latching**
- **Hardware, SPI and parallel microprocessor interface**
- **Power–down control for each channel**
- **27 mm BGA package**
- **–40C to 85C industrial temperature range**
- **1.8 and 3.3 V supply**

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28356-BRF-001-A M02-0701

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