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x12/x6/x4 T3/E3 Framers with ATM Transmission Convergence

CX28365/28366/28364

High-Density ATM UNI and NNI Interfaces for up to OC-12 Density Line Cards

Mindspeed Technologies™ offers 12-, six- and four-port T3/E3 framers with Transmission Convergence. These high-density, low-power solutions are designed for ATM and multiservice line cards for T3 and E3 lines. Each device supports ANSI, ETSI, ITU-T and Bellcore standards for T3 and E3 framing, as well as ATM Forum standards for the Transmission Convergence Sublayer defined for T3 and E3 transmission types. The framers interface seamlessly with Mindspeed's 12-port line interface unit (LIU), the M28335, and the triple and dual LIUs, the CX28333 and CX28332.

KEY FEATURES

- High density: Up to 12 independent T3/E3 framers in one package
- Low power: < 190 mW maximum per port
- CX28365TAP software includes mature API and rich performance- and fault-monitoring feature set in addition to driver
- PLCP or direct framing selectable per port
- One-second event latching reduces software overhead
- Each port independently configurable as ATM UNI/NNI, T3/E3 framer only, or ATM Transmission Convergence PHY only
- Forms complete T3/E3 solutions with Mindspeed's CX28333 and M28335 LIUs

T3/E3 Framers

The devices leverage the proven framer design of Mindspeed's successful CX2834x family of multiport T3/E3 framers. The CX28365 provides framing recovery for M13, M23, C-bit parity, G.751, and G.832-formatted signals. They permit easy configuration while providing maximum flexibility to support the transmission and recovery of industry-standard formats. A flexible overhead-bit generation method is provided to source overhead bits on an individual framer.

ATM Transmission Convergence

A modified Transmission Convergence Sublayer block provides ATM cell delineation. This block, used in many other Mindspeed products, has been upgraded for T3 and E3 rates to include Physical Layer Convergence Protocol (PLCP) framing as defined in the ATM Forum's Cell-Based Transmission Convergence Sublayer specification (af-phy-0043.000), DS3 Physical Layer Interface specification (af-phy-0054.000, ITU-T G.804) and E3 Public User Network Interface (UNI) specification (af-phy-0034.000, ETS 300-214). System designers benefit from the highest integration density and lowest cost for T3 and E3 UNI and NNI ATM interfaces. To design a complete solution for interfacing cells from a standard UTOPIA Level 2 system interface to the physical line connections, designers only need to add a single M28335 12-port LIU or four CX28333 triple LIUs and a microprocessor for configuration and control. The CX28365 delivers new economies of scale with low power consumption, high port density and the integration of framer and ATM functions in one package.

Automatic Maintenance and Alarms

The device offers T1.231-compliant support for network performance monitoring and alarming. It includes on-chip TDL (LAPD) channels with 128-byte transmit and receive FIFOs, a FEAC channel controller with automatic message decoding, and a FIFO containing the three most recent, decoded, distinct FEAC messages. All error counters are 16 bits wide, except for the LCV counter, which is 24 bits wide.

Loopbacks

A set of local and remote loopbacks is available, including source and line loopbacks for diagnostics, maintenance and troubleshooting for each channel. The source loopbacks loop the host (ATM layer) data back to itself. The line loopbacks loop the receive data back towards the T3/E3 line. Integrated in-band loopback code generation and detection are also supported.

Microprocessor Interface

A standard eight-bit parallel microprocessor interface is provided. Real-time events may be latched immediately or synchronized to a one-second timer derived from a T3/E3 line or separate input.

Software Drivers

A portable, OS-independent software driver is available. It implements all user access to the device's configuration, performance-monitoring and fault-monitoring features.

Bypass Capabilities

ATM cell delineation and processing functions may be bypassed on a per-port basis. Each T3/E3 framer may also be bypassed on a per-port basis to provide separate data and overhead insertion at up to 52 Mbps line rates. This gives OEMs the flexibility to provide different services on a single line card (e.g., TDM and Frame Relay) using a common physical-layer framing and line interface.

What is Framing?

Framing is a means of recovering one or more additional layers of timing information from a received data stream. This timing information enables the transport of multiplexed data channels, whether the bit rate of the channel is derived from the data stream bit rate (synchronous), is unrelated to the data stream (asynchronous), or is indirectly related to the data stream bit rate (plesiochronous).

What is T3?

T-carrier Level 3 is a standard for data transmission at 44. 736 Mbps using the B3ZS (bipolar with three-zero substitution) line coding technique. The framing format for data carried over a T3 connection is referred to as DS3, and the two terms are often used interchangeably. A two-stage bit-interleaved framing technique was initially defined, but this has since been replaced by the more common C-bit parity framing format.

What is E3?

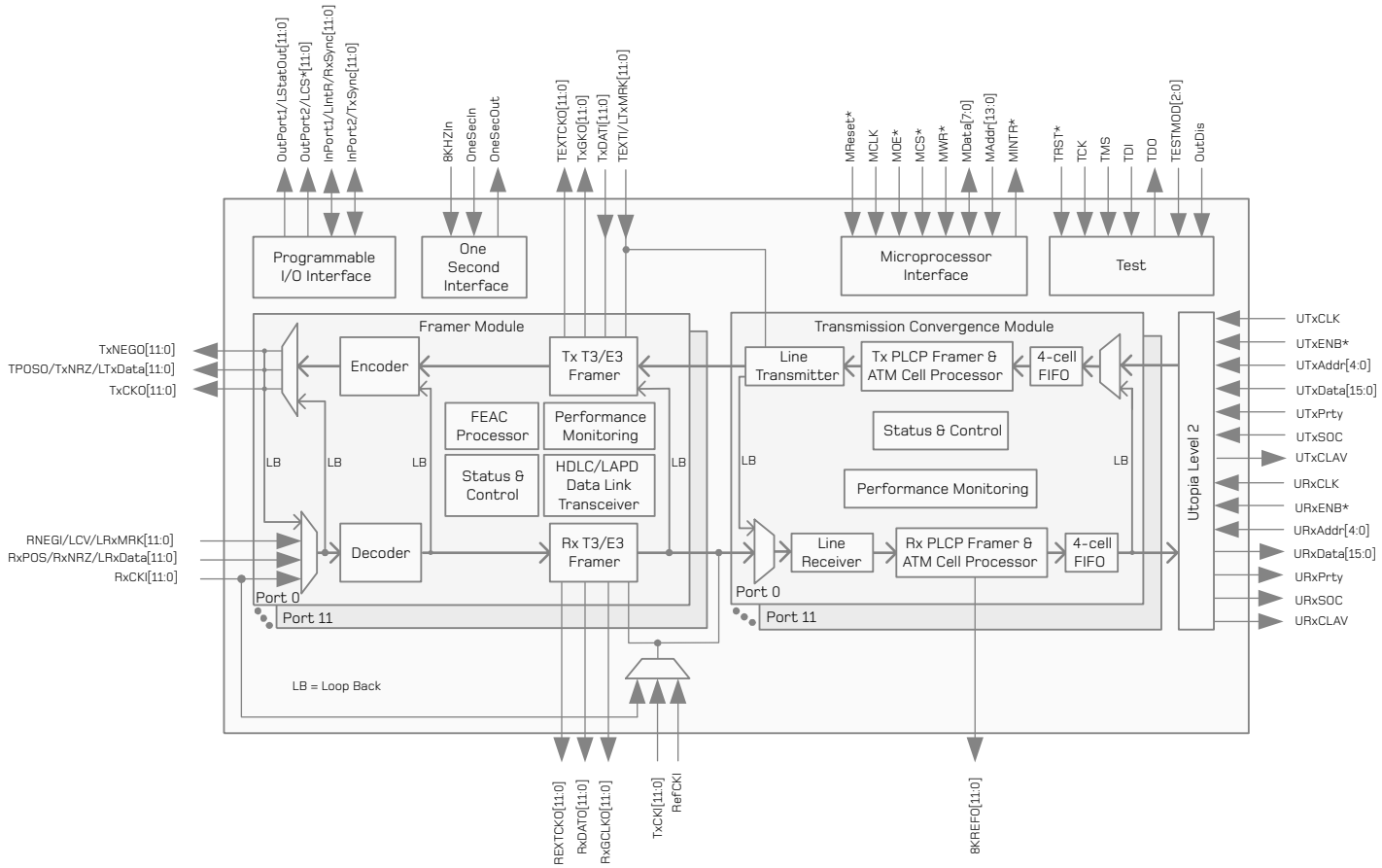
E3 is a standard enabling data transmission at 34. 368 Mbps. E3 employs a modified AMI line coding called HDB3 (high density bipolar 3), which is similar to but incompatible with T3's B3ZS. It was defined by European standards committees to allow for the multiplexing of E1 (2. 048 Mbps) and E2 (8. 448 Mbps) signals. E3 implements two incompatible framing types: G.751 (bit-aligned frames, similar in principle to the M13 format of DS3 frames) and the newer G.832 (byte-aligned frames, similar to C-bit parity framing in DS3).

What is ATM?

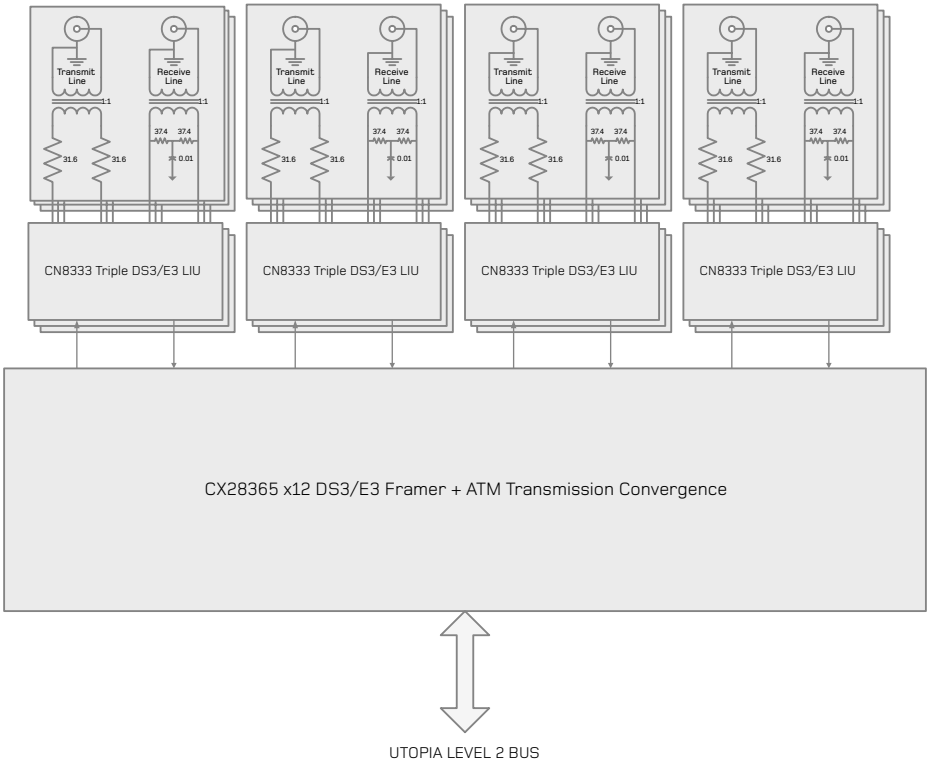
Asynchronous Transfer Mode (ATM) is a transport method that uses cells (packets of a fixed size) to transport all data traffic types, including conventional telephony, video and data traffic, across LANs, MANs and WANs (local, metropolitan and wide area networks, respectively). The ITU-T and ANSI selected ATM for broadband ISDN. SONET/SDH as specified by the ITU-T is intended to be the primary transport mechanism for ATM

cells in WANs. ATM also plays an important role as an access technology for wireless and high-speed Internet connections. The ADSL Forum and Universal ADSL Working Group chose ATM as the network-layer protocol for G.lite and G.DMT ADSL.

An ATM physical-layer (PHY) device adapts ATM cells to and from a wide range of transmission rates including T1/E1, T3/E3, 155 Mbps and higher. The standard ATM interface to the PHY is the UTOPIA bus. The PHY device performs ATM cell functions such as cell delineation, scrambling/descrambling, cell header processing and cell buffering for rate decoupling. The PHY device also defines various cell-mapping functions for specific line-interface types, as well as the ability to multiplex cells from a single UTOPIA bus to multiple, separate, physical connections.



Functional Block Diagram



Typical Application: 12-Port DS3 ATM Line Card

Product Highlights

- Twelve-, six- or four-port ATM UNI/NNI in a single package with each port independently configurable for T3 or E3 transmission rates
- Each internal T3/E3 framer may be individually configured to bypass the ATM cell delineator for operation solely as a framer
- Each internal T3/E3 framer may be individually bypassed to support external connections to the ATM cell delineator for line transmissions up to 52 Mbps
- Complete T3/E3 solution with Mindspeed's CX2833x and M28335 DS3/E3/STS-1 LIUs
- Line coding supported:
  - DS3: B3ZS, NRZ, AMI
  - E3: HDB3, NRZ, AMI
- Framing supported:
  - DS3: M13, M23, C-bit parity
  - E3: G. 751, G.832
- Inserts and extracts opportunity bits
- FEAC and TDL channel supported
- Performance monitoring support per T1. 231
- Supplies integral transmit and receive HDLC controllers with 128-byte FIFO buffers
- Glueless interfaces to the following devices:
  - DS3/E3/STS-1 LIUs: CX28335/3/2/1 (x12, x3, x2, x1 ports)
  - SAR interfaces: Bt8233/RS8234
  - Network processors: CX27440/ CX27460
  - HDLC controllers: CX23500
- An eight-bit microprocessor interface for configuration, control and status monitoring
- PLCP or direct cell mapping selectable per port
- Recovers 8 kHz clock from PLCP frame for source synchronization
- ATM Transmission Convergence
  - ATM direct-cell mapping according to ITU-T G.804
  - Passes or rejects idle cells or selected cells based on header register configuration
  - Recovers cell alignment from HEC
  - Performs single-bit HEC error correction and multiple-bit detection
  - Generates cell status bits, cell counts and error counts
  - Reads cell data from the UTOPIA FIFO
  - Inserts idle cells when no traffic is available
  - ITU I.432-compliant
- UTOPIA Level 2 multi-PHY eight- or 16-bit interface
- Provides for source, line and payload loopbacks
- Power supplies and power consumption
  - I/O 3.3 V, input 5 V-tolerant; core 1.8 V
  - Low-power operation (< 190 mW max. per port)
- Mindspeed's CX28365TAP software includes mature API and rich performance and fault monitoring feature set in addition to driver
- IEEE 1149. 1 JTAG boundary scan support
- Rated for industrial temperature operation
- Available in high-density, 456-pin, 35 mm x 35 mm PBGA package

Applications

- Digital cross-connect systems
- Optical transport equipment
- Access concentrators
- ATM switches
- Frame Relay equipment
- Routers

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