ZL30236
Dual Channel Universal Clock Generator
Short Form Data Sheet

April 2010

Features

- Operates from a single crystal resonator, clock oscillator or voltage controlled oscillator
- Two independently programmable clock synthesizers generate any clock rate from 1 kHz to 720 MHz
- Precision synthesizers generate clocks with jitter below 0.7 ps RMS for 10 G PHYs
- Supports programmable frequency offsets for clock margining; or for use as a digitally controlled oscillator
- Eight LVPECL outputs; max rate 720 MHz
- Four LVCMOS outputs; max rate 160 MHz
- Dynamically Configurable via SPI/I2C interface

Ordering Information

ZL30236GGG	100 Pin CABGA	Trays
ZL30236GGG2	100 Pin CABGA*	Trays

*Pb Free Tin/Silver/Copper

-40°C to +85°C

Applications

- Timing for NPUs, FPGAs, Ethernet switches and PCIe switches
- Timing for 10 Gigabit CDRs, Rapid-IO, PCIe, Serial MII, Star Fabric, Fibre Channel, XAUI
- Processor clock, Processor bus clock, SDRAM clock, DDR clock

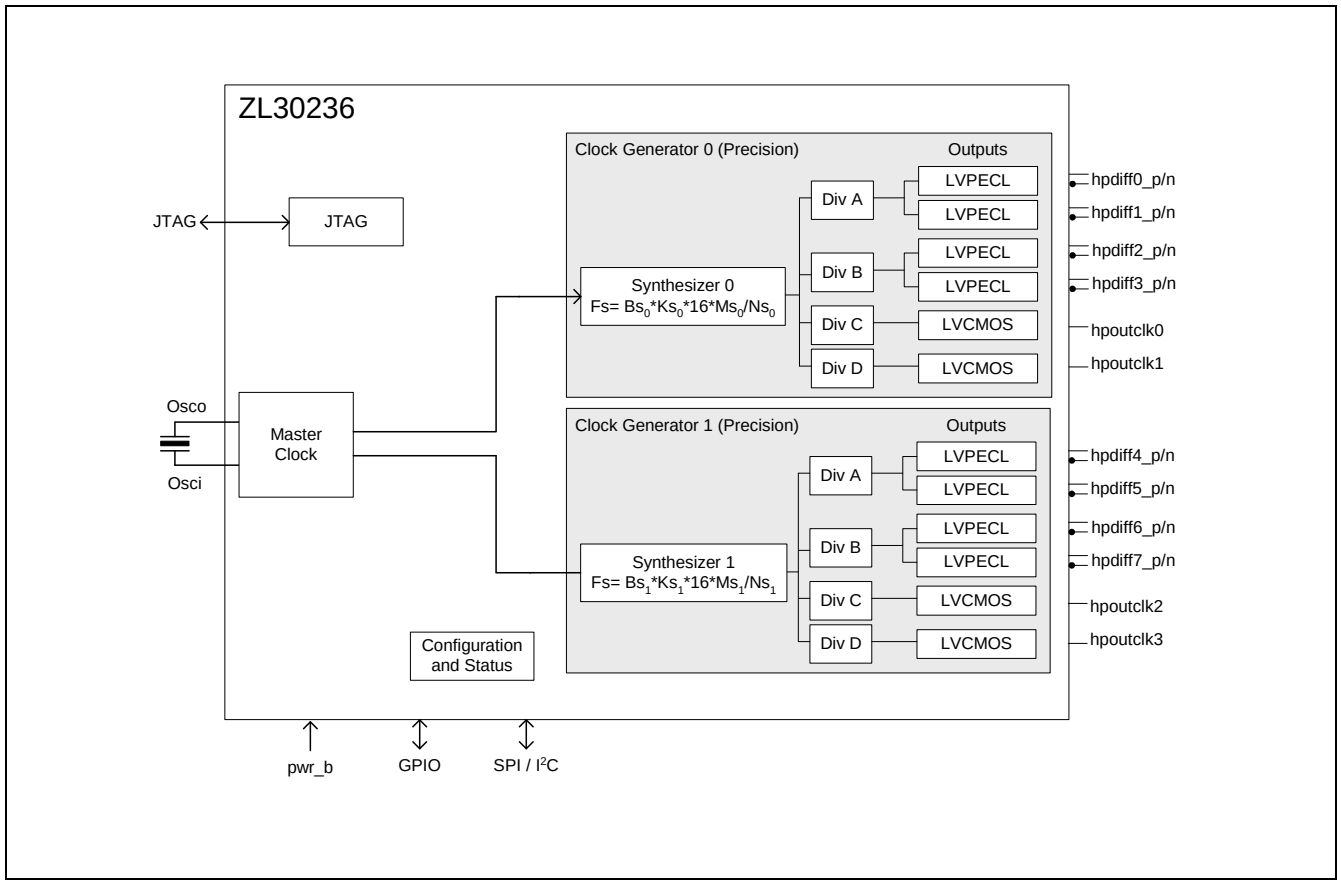

Figure 1 - Functional Block Diagram

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Description

The ZL30236 Dual Channel Universal Clock Generator, part of Zarlink's ClockCenter platform of Free Run Clock devices, delivers industry leading performance for a range of free run applications. The free run synchronization solution allows designers to replace multiple, costly components with a highly integrated and programmable, single-chip solution.

The ZL30236 device generates up to 12 clocks from a single crystal, allowing designers to replace numerous oscillators traditionally used to provide timing for various components with one chip.

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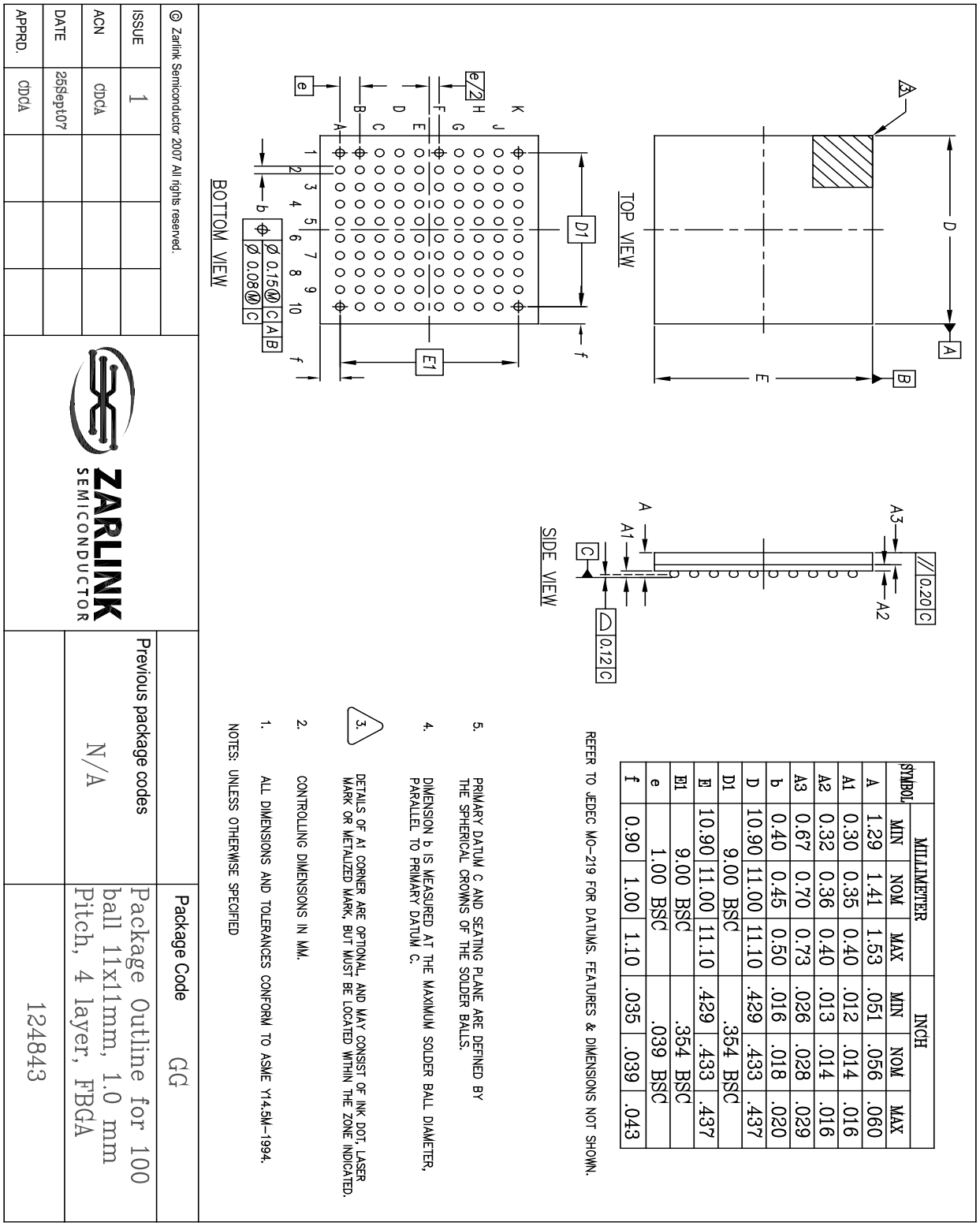
Mechanical Drawing



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.29	1.41	1.53	.051	.056	.060
A1	0.30	0.35	0.40	.012	.014	.016
A2	0.32	0.36	0.40	.013	.014	.016
A3	0.67	0.70	0.73	.026	.028	.029
b	0.40	0.45	0.50	.016	.018	.020
D	10.90	11.00	11.10	.429	.433	.437
D1		9.00 BSC			.354 BSC	
E	10.90	11.00	11.10	.429	.433	.437
E1		9.00 BSC			.354 BSC	
e		1.00 BSC			.039 BSC	
f	0.90	1.00	1.10	.035	.039	.043

REFER TO JEDEC MO-219 FOR DATUMS. FEATURES & DIMENSIONS NOT SHOWN.

5. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
3. DETAILS OF A1 CORNER ARE OPTIONAL AND MAY CONSIST OF INK DOT, LASER MARK OR METALIZED MARK, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
2. CONTROLLING DIMENSIONS IN MM.
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

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ACN	CDCA			
DATE	26Sept07			
APPRD.	CDCA			

ZARLINK SEMICONDUCTOR

Previous package codes: N/A

Package Code: GG

Package Outline for 100 ball 11x11mm, 1.0 mm Pitch, 4 layer, FBGA

124843

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