

A full Design Manual is available to qualified customers. To register, please send an email to TimingandSync@Zarlink.com

Features

- Supports the requirements of ITU-T G.8262 for synchronous Ethernet Equipment slave Clocks (EEC option 1 and 2)
 - Supports the requirements of Telcordia GR-1244 Stratum 3 and GR-253, ITU-T G.812 and ITU-T G.813
 - Supports ITU-T G.823, G.824 and G.8261 for 2048 kbit/s and 1544 kbit/s interfaces
 - Frequency, Phase and Time Synchronization over IP, MPLS and Ethernet Packet Networks
 - Frequency accuracy performance for WCDMA-FDD, GSM, LTE-FDD and femtocell applications, with target performance less than ± 15 ppb.
 - Frequency performance for ITU-T G.823 and G.824 synchronization interface, as well as G.8261 PNT EEC, PNT PEC and CES interface specifications.
 - Phase Synchronization performance for WCDMA-TDD, Mobile WiMAX, TD-SCDMA and CDMA2000 applications with target performance less than $\pm 1 \mu\text{s}$ phase alignment.
 - Time Synchronization for UTC-traceability and GPS replacement.
- Meets the SONET/SDH jitter generation requirements up to OC-48/STM-16
 - Synchronizes to telecom reference clocks (2 kHz, N*8 kHz up to 77.76 MHz, 155.52 MHz) or to Ethernet reference clocks (25 MHz, 50 MHz, 62.5 MHz, 125 MHz)
 - Programmable output synthesizers (P0, P1) generate telecom clock frequencies from any multiple of 8 kHz up to 100 MHz
 - Generates standard SONET/SDH clock rates (e.g., 19.44 MHz, 38.88 MHz, 77.76 MHz, 155.52 MHz, 622.08 MHz) or Ethernet clock rates (e.g., 25 MHz, 50 MHz, 125 MHz, 156.25 MHz, 312.5 MHz) for synchronizing Gigabit Ethernet PHYs
 - DPLL that is configurable through a serial interface
 - Client reference switching between multiple Servers
 - Client holdover when Server packet connectivity is lost

Ordering Information

ZL30342GGG	64 Pin CABGA	Trays
ZL30342GGG2	64 Pin CABGA*	Trays

*Pb Free Tin/Silver/Copper

-40°C to +85°C

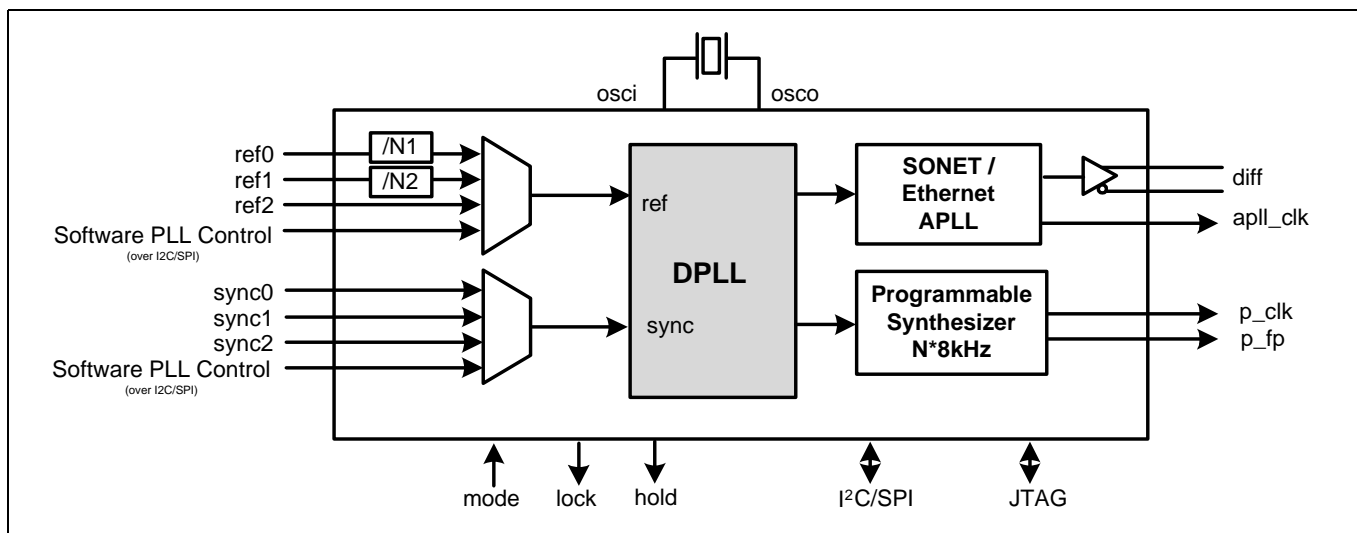


Figure 1 - Functional Block Diagram

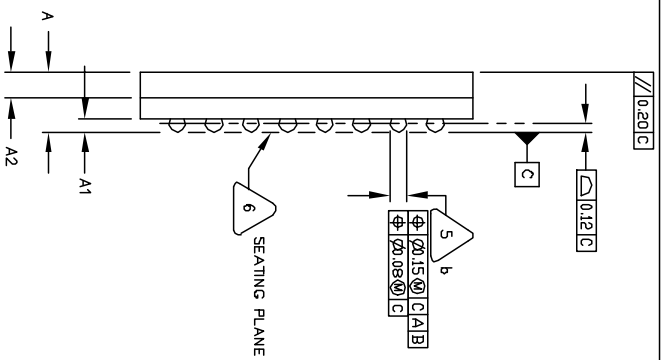
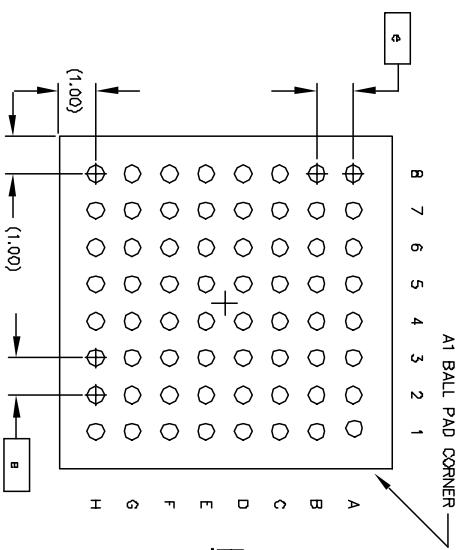
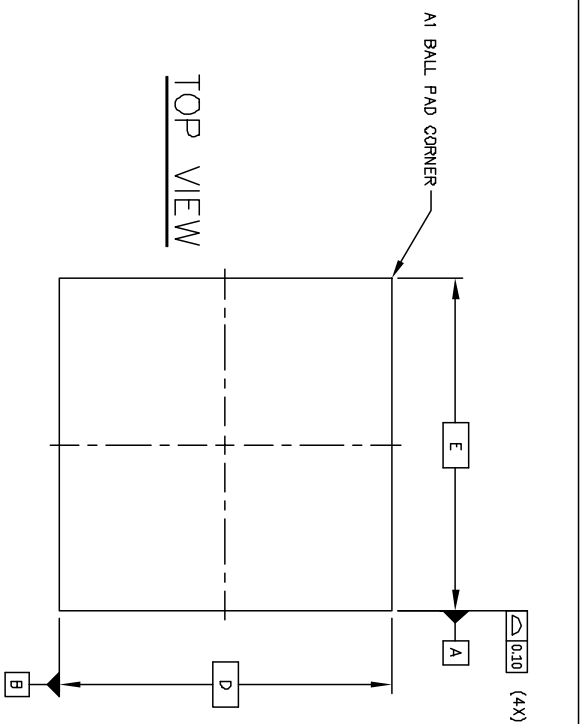
Applications

- ITU-T G.8262 System Timing Cards which support 1 GbE and 10 GbE interfaces
- Telcordia GR-253 Carrier Grade SONET/SDH Stratum 3 System Timing Cards
- System Timing Cards which supports ITU-T G.781 SETS (SDH Equipment Timing Source)
- Integrated basestation reference clock for air interface for GSM, WCDMA, LTE and WiMAX macro, micro or femtocells
- Mobile Backhaul NID, edge router or access aggregation node
- EPON/GE-PON & GPON OLT
- EPON/GE-PON & GPON ONU/OLT
- DSLAM and RT-DSLAM

Description

The ZL30342 is a member of a family of footprint-compatible devices offering the full range of features required for timing and synchronization across packet networks. These devices focus on the Clock Recovery, Servo Mechanism and Clock Generation for Synchronization using IEEE-1588. They work seamlessly with Time Stamp solutions from all the major Switch/PHY NPU/CPU vendors.

These are the only commercially available single chip devices to offer both packet timing using IEEE-1588 Precision Time Protocol (PTP) and Synchronous Ethernet (SyncE) capable of driving the physical layer clock with the required very low jitter. The ZL30342 offers a full Stratum 3 DPLL, ideal for Timing Card applications and supports clock recovery over L2 and L3 networks for all wireless applications.



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.52	1.62	1.72
A1	0.31	0.36	0.41
A2	0.65	0.70	0.75
b	0.46 TYP.		
D	9.00 REF.		
E	9.00 Ref.		
e	1.0 Ref		
n	64		

6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
 DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.
 2. THE BASIC SOLDER BALL GRID PITCH IS 1.00mm.
 3. Not to Scale.
 4. THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS IS 64.
- NOTES: UNLESS OTHERWISE SPECIFIED

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ISSUE	1		
ACN	CDCA		
DATE	15Apr105		
APPRD.			



Previous package codes

N/A

Package Code GG

Package Outline for 64ball 9x9mm, 1.0 mm Pitch, 4 layer, CABGA

111039



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