ZL30347

IEEE 1588-2008 Synchronization PLL

Data Sheet

June 2011

A full Design Manual is available to qualified customers. To register, please send an email to TimingandSynch@Zarlink.com.

Features

- Frequency, Phase and Time Synchronization over IP, MPLS and Ethernet Packet Networks
  - Frequency accuracy performance for WCDMA-FDD, GSM, LTE-FDD and femtocell applications, with target performance less than ± 15 ppb.
  - Frequency performance for ITU-T G.823 and G.824 synchronization interface, as well as G.8261 PNT EEC, PNT PEC and CES interface specifications.
  - Phase Synchronization performance for WCDMA-TDD, Mobile WiMAX, TD-SCDMA and CDMA2000 applications with target performance less than ± 1 μs phase alignment.
  - Time Synchronization for UTC-traceability and GPS replacement.
- Meets the SONET/SDH jitter generation requirements up to OC-48/STM-16

Ordering Information

ZL30347GGG	100 Pin CABGA	Trays
ZL30347GGG2	100 Pin CABGA*	Trays

*Pb Free Tin/Silver/Copper

-40°C to +85°C

- Programmable output synthesizers (P0, P1) generate telecom clock frequencies from any multiple of 8 kHz up to 100 MHz
- Generates standard SONET/SDH clock rates (e.g., 19.44 MHz, 38.88 MHz, 77.76 MHz, 155.52 MHz, 622.08 MHz) or Ethernet clock rates (e.g., 25 MHz, 50 MHz, 125 MHz, 156.25 MHz, 312.5 MHz) for synchronizing Gigabit Ethernet PHYs
- Client reference switching between multiple Servers
- Client holdover when Server packet connectivity is lost

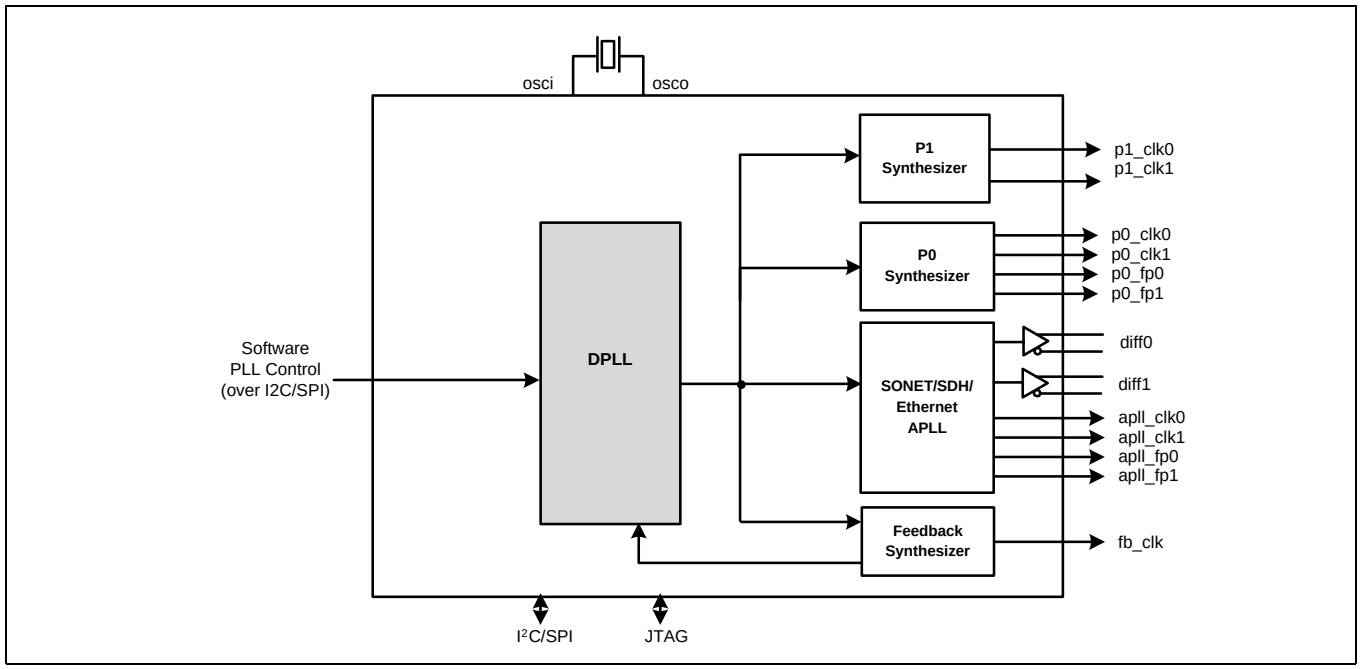


Figure 1 - Functional Block Diagram

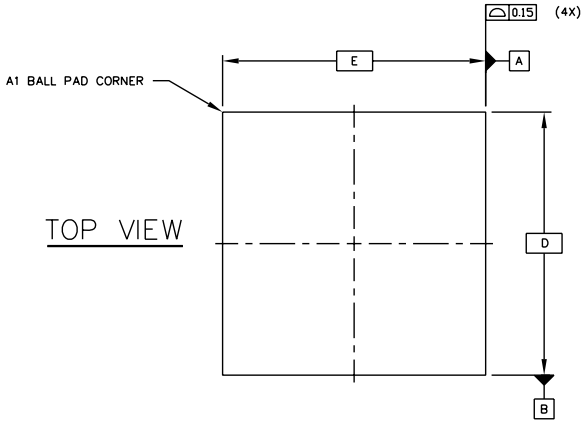
Applications

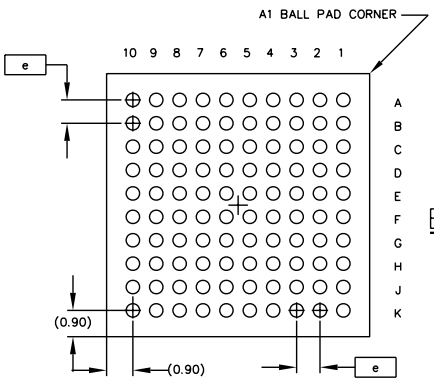
- Integrated basestation reference clock for air interface for GSM, WCDMA, LTE and WiMAX macro, micro or femtocells
- Mobile Backhaul NID, edge router or access aggregation node
- EPON/GE-PON & GPON OLT
- EPON/GE-PON & GPON ONU/OLT
- DSLAM and RT-DSLAM

Description

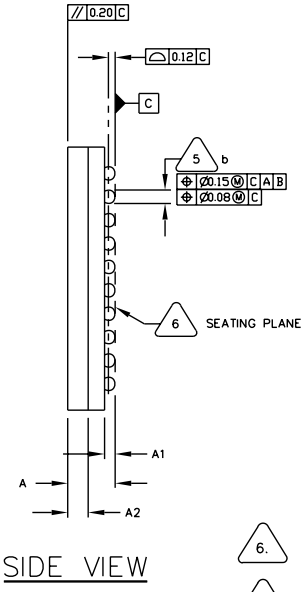
The ZL30347 is a member of a family of footprint-compatible devices offering the full range of features required for timing and synchronization across packet networks. These devices focus on the Clock Recovery, Servo Mechanism and Clock Generation for Synchronization using IEEE-1588. They work seamlessly with Time Stamp solutions from all the major Switch/PHY NPU/CPU vendors.

These are the only commercially available single chip devices to offer both packet timing using IEEE-1588 Precision Time Protocol (PTP) and Synchronous Ethernet (SyncE) capable of driving the physical layer clock with the required very low jitter. The ZL30347 offers a full Stratum 3 DPLL, ideal for Timing Card applications and supports clock recovery over L2 and L3 networks for all wireless applications.





BOTTOM VIEW
100 SOLDER BALLS



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.52	1.62	1.72
A1	0.31	0.36	0.41
A2	0.65	0.70	0.75
b		0.46 Typ.	
D	8.85	9.00	9.15
E	8.85	9.00	9.15
e		0.8 Ref	
n		100	

6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

5. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.

4. THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS IS 100.

3. Not to Scale.

2. THE BASIC SOLDER BALL GRID PITCH IS 0.8mm.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

ISSUE	1	2	3	
ACN	CDCA	CDCA	CDCA	
DATE	15April05	24Aug05	26Oct06	
APPRD.				

ZARLINK SEMICONDUCTOR

Package Code GG

Previous package codes
N/A

Package Outline for 100ball 9x9mm, 0.8 mm Pitch, 4 layer, CABGA

111040

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www.zarlink.com