![ZARLINK SEMICONDUCTOR logo]

ZL30160
Four Channel Universal Clock Translator
Short Form Data Sheet

April 2010

Features

- Four independent clock channels

- Programmable synthesizers generate any clock-rate from 1 kHz to 720 MHz

- Two precision synthesizers generate clocks with jitter below 0.7 ps RMS for 10 G PHYs

- Two general purpose synthesizers generate a wide range of digital bus clocks

- Programmable digital PLLs synchronize to any clock rate from 1 kHz to 720 MHz

- Flexible two-stage architecture translates between arbitrary data rates, line coding rates and FEC rates

- Digital PLLs filter jitter from 14 Hz, 28 Hz, 56 Hz, 112 Hz, 224 Hz, 448 Hz or 896 Hz

- Automatic hitless reference switching and digital holdover on reference fail

- Four reference inputs configurable as single ended or differential

- Eight LVPECL outputs and four LVCMOS outputs

Ordering Information		
ZL30160GGG	100 Pin CABGA	Trays
ZL30160GGG2	100 Pin CABGA*	Trays

*Pb Free Tin/Silver/Copper
-40°C to +85°C

- Eight outputs configurable as LVCMOS or LVDS/LVPECL/HCSL

- Operates from a single crystal resonator or clock oscillator

- Configurable via SPI/I2C interface

Applications

- 10 Gigabit linecards

- Synchronous Ethernet, 10GBASE-R and 10 GBASE-W

- OTN multiplexers and transponders
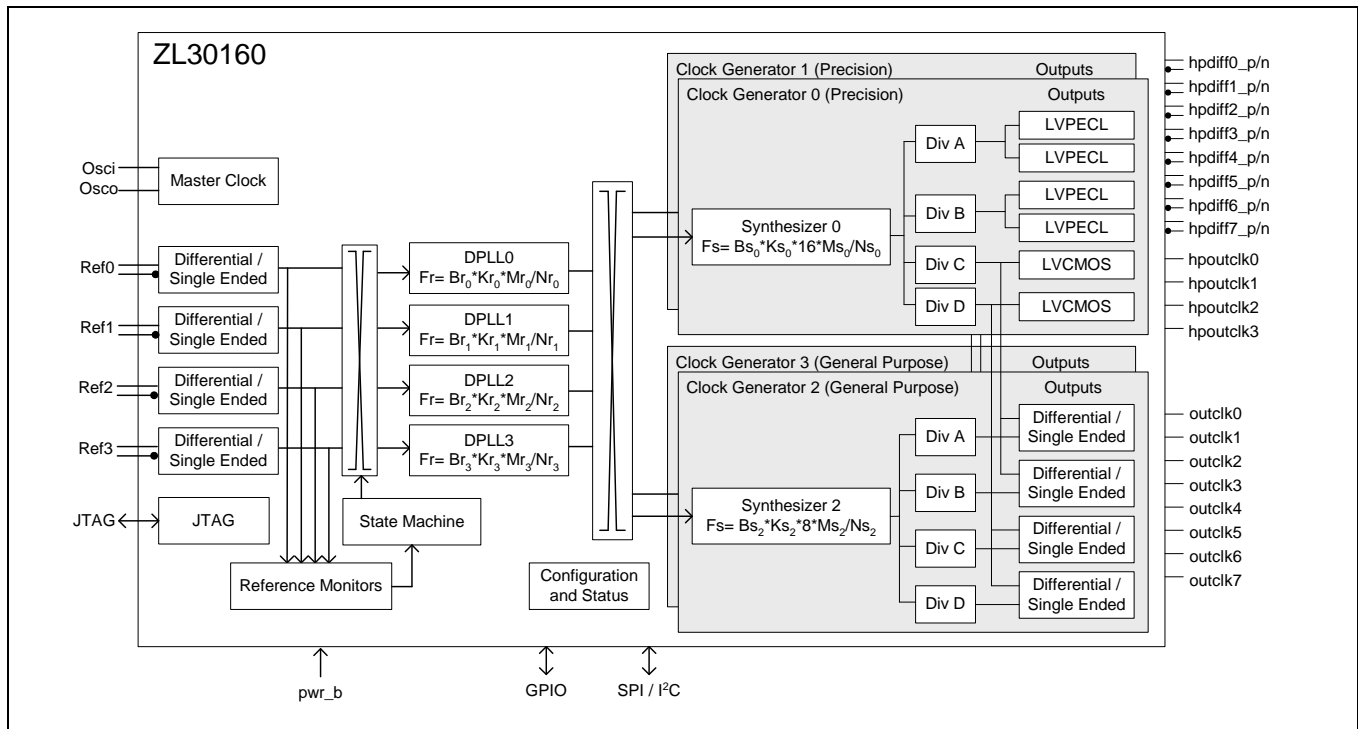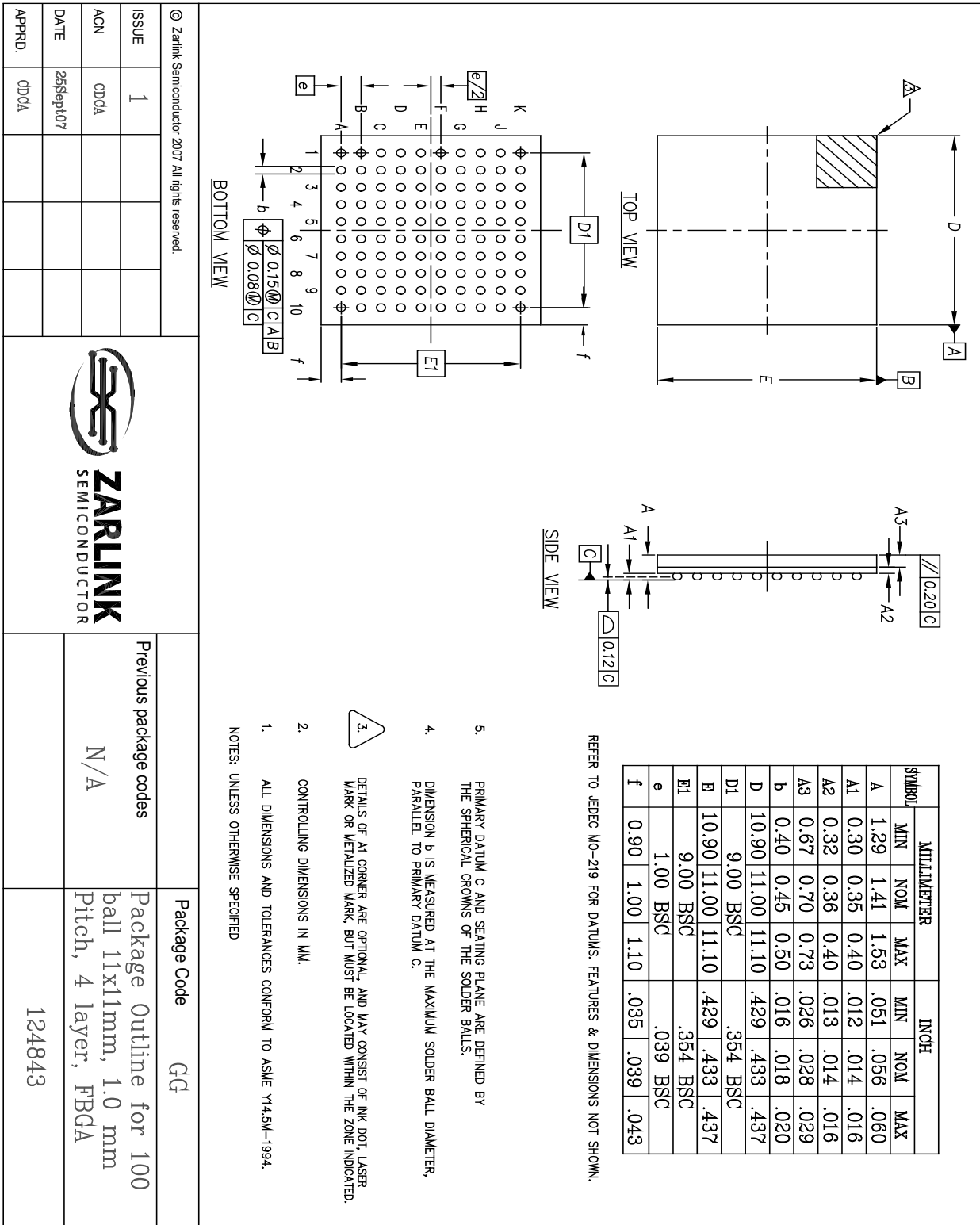
- SONET/SDH, Fibre Channel, XAUI

Figure 1 - Functional Block Diagram

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Description

The ZL30160 Four Channel Universal Clock Translator, part of Zarlink's ClockCenter platform of Synchronous Clock devices, delivers industry leading synchronization performance for high-speed, complex applications. The highly integrated and programmable solution provides translation from any input reference frequency to any output clock frequency with jitter performance that can directly drive 10 G PHY devices.

The ZL30160 integrates 4 independent digital PLLs, accepts 4 input references and generates 20 programmable clock outputs. The highly integrated solution allows designers to replace multiple components with a single chip, simplifying design and reducing component count and power.

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Mechanical Drawing

TOP VIEW

BOTTOM VIEW

SIDE VIEW

SYMBOL	MILLIMETER MIN	MILLIMETER NOM	MILLIMETER MAX	INCH MIN	INCH NOM	INCH MAX
A	1.29	1.41	1.53	.051	.056	.060
A1	0.30	0.35	0.40	.012	.014	.016
A2	0.32	0.36	0.40	.013	.014	.016
A3	0.67	0.70	0.73	.026	.028	.029
b	0.40	0.45	0.50	.016	.018	.020
D	10.90	11.00	11.10	.429	.433	.437
D1	9.00 BSC			.354 BSC		
E	10.90	11.00	11.10	.429	.433	.437
E1	9.00 BSC			.354 BSC		
e	1.00 BSC			.039 BSC		
f	0.90	1.00	1.10	.035	.039	.043

REFER TO JEDEC MO-219 FOR DATUMS, FEATURES & DIMENSIONS NOT SHOWN.

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

2. CONTROLLING DIMENSIONS IN MM.

3. DETAILS OF A1 CORNER ARE OPTIONAL, AND MAY CONSIST OF INK DOT, LASER MARK OR METALIZED MARK, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

4. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.

5. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

Package Code	GG
	Package Outline for 100 ball 11x11mm, 1.0 mm Pitch, 4 layer, FBGA
Previous package codes	N/A
	124843

ZARLINK SEMICONDUCTOR

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Zarlink Semiconductor Inc.

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