ZL30152
Universal Rate Adapting Synchronous Clock Generator
Short Form Data Sheet

January 2011

Features

- Programmable synthesizers generate any clock-rate from 1 kHz to 720 MHz
- Precision synthesizers generate clocks with jitter below 0.7 ps RMS for 10 G PHYs
- Programmable digital PLL synchronize to any clock rate from 1 kHz to 720 MHz
- Flexible two-stage architecture translates between arbitrary data rates, line coding rates and FEC rates
- Digital PLL filter jitter from 14 Hz, 28 Hz, 56 Hz, 112 Hz, 224 Hz, 448 Hz or 896 Hz
- Automatic hitless reference switching and digital holdover on reference fail
- Two reference inputs configurable as single ended or differential
- Four LVPECL outputs and two LVCMOS outputs
- Operates from a single crystal resonator or clock oscillator
- Configurable via SPI/I2C interface

Ordering Information

ZL30152GGG	64 Pin CABGA	Trays
ZL30152GGG2	64 Pin CABGA*	Trays

*Pb Free Tin/Silver/Copper

-40°C to +85°C

Applications

- Clock Generation for Physical Line Interface:
  - SONET/SDH, OC-192/OC-48
  - SONET/SDH with FEC
  - 10G Base X, R and W
  - 100 BaseX, GE, Fibre channel
- Clock Generation and Distribution for back plane Interface:
  - TDM, Telecom Bus, Utopia, SBI
- Rapid-IO, PCI-Express, serial MII, Star Fabric, XAUI

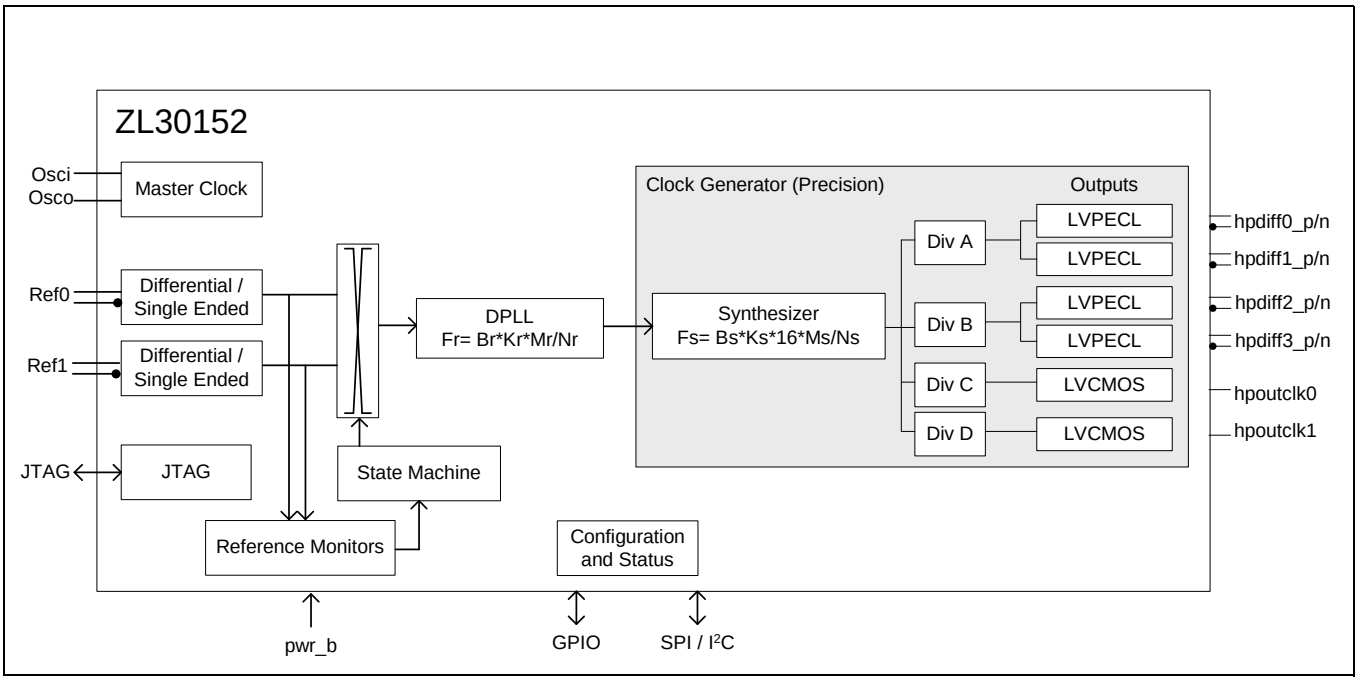

Figure 1 - Functional Block Diagram

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Description

The ZL30152 Universal Clock Translator, part of Zarlink's ClockCenter platform of Synchronous Clock devices, delivers industry leading synchronization performance for high-speed complex applications. The highly integrated and programmable solution provides translation from any input reference frequency to any output clock frequency with jitter performance that can directly drive 10 G PHY devices.

The ZL30152 accepts 2 single ended or differential input references and generates 6 high performance programmable clock outputs. The highly integrated solution allows designers to replace multiple components with a single chip, simplifying design and reducing component count and power.

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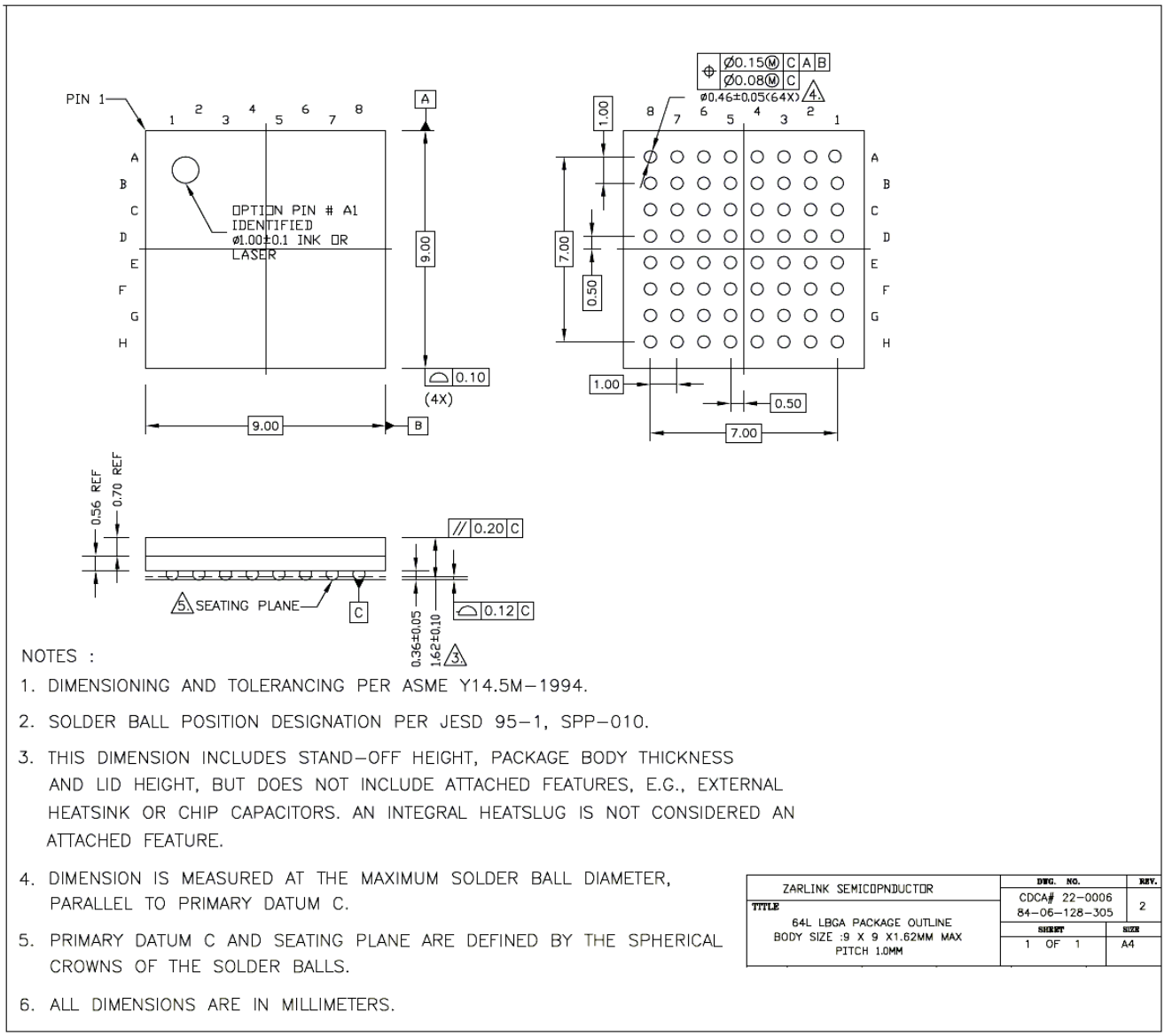
Mechanical Drawing



NOTES :

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. SOLDER BALL POSITION DESIGNATION PER JESD 95–1, SPP–010.
3. THIS DIMENSION INCLUDES STAND–OFF HEIGHT, PACKAGE BODY THICKNESS AND LID HEIGHT, BUT DOES NOT INCLUDE ATTACHED FEATURES, E.G., EXTERNAL HEATSINK OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AN ATTACHED FEATURE.
4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
5. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. ALL DIMENSIONS ARE IN MILLIMETERS.

ZARLINK SEMICONDUCTOR	DWG. NO.	REV.
TITLE: 64L LBGA PACKAGE OUTLINE BODY SIZE :9 X 9 X1.62MM MAX PITCH 1.0MM	CDCA# 22–0006 84–06–128–305	2
	SHEET 1 OF 1	SIZE A4

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