

Features

- Two independent clock channels
- Programmable synthesizers generate any clock-rate from 1 kHz to 720 MHz
- Two precision synthesizers generate clocks with jitter below 0.7 ps RMS for 10 G PHYs
- Programmable digital PLLs synchronize to any clock rate from 1 kHz to 720 MHz
- Flexible two-stage architecture translates between arbitrary data rates, line coding rates and FEC rates
- Digital PLLs filter jitter from 14 Hz, 28 Hz, 56 Hz, 112 Hz, 224 Hz, 448 Hz or 896 Hz
- Automatic hitless reference switching and digital holdover on reference fail
- Four reference inputs configurable as single ended or differential
- Four reference inputs configurable as single ended or differential
- Eight LVPECL outputs and four LVCMOS outputs

Ordering Information

ZL30155GGG	100 Pin CABGA	Trays
ZL30155GGG2	100 Pin CABGA*	Trays

*Pb Free Tin/Silver/Copper
-40°C to +85°C

- Operates from a single crystal resonator or clock oscillator
- Configurable via SPI/I2C interface

Applications

- 10 Gigabit linecards
- Synchronous Ethernet, 10GBASE-R and 10 GBASE-W
- OTN multiplexers and transponders
- SONET/SDH, Fibre Channel, XAUI

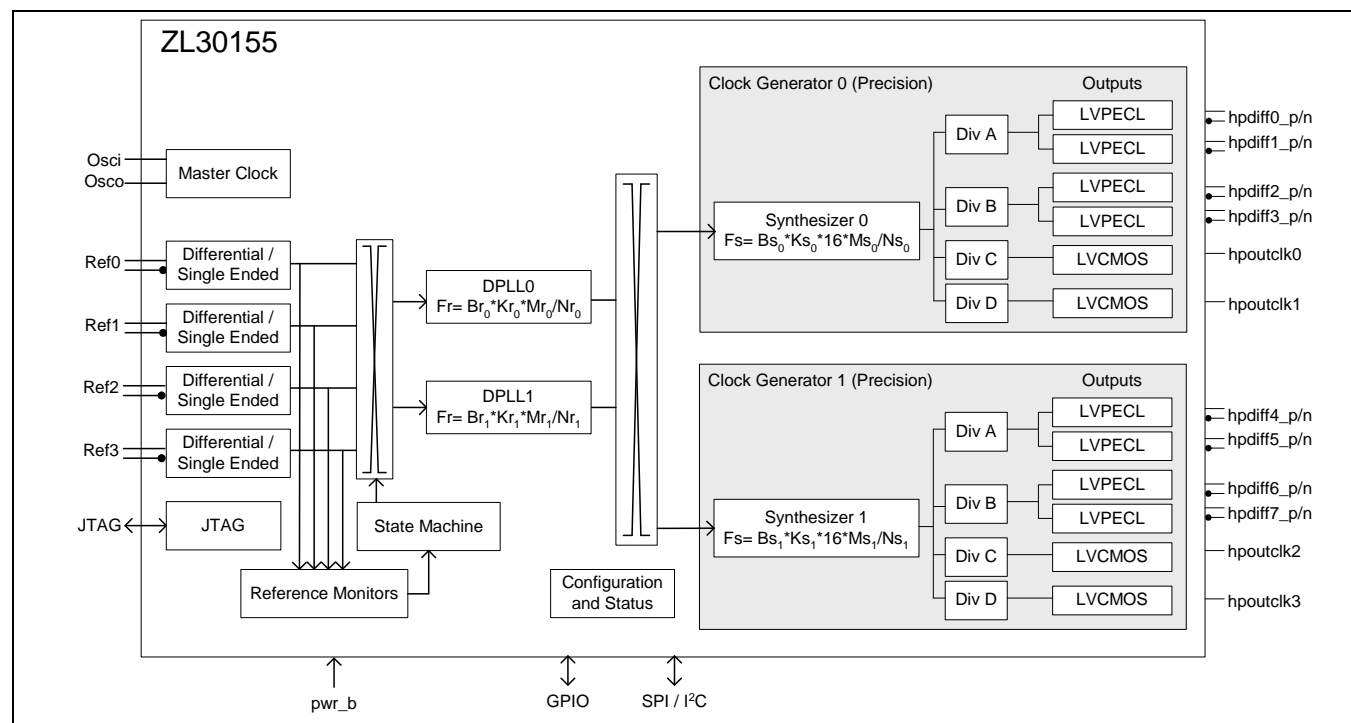


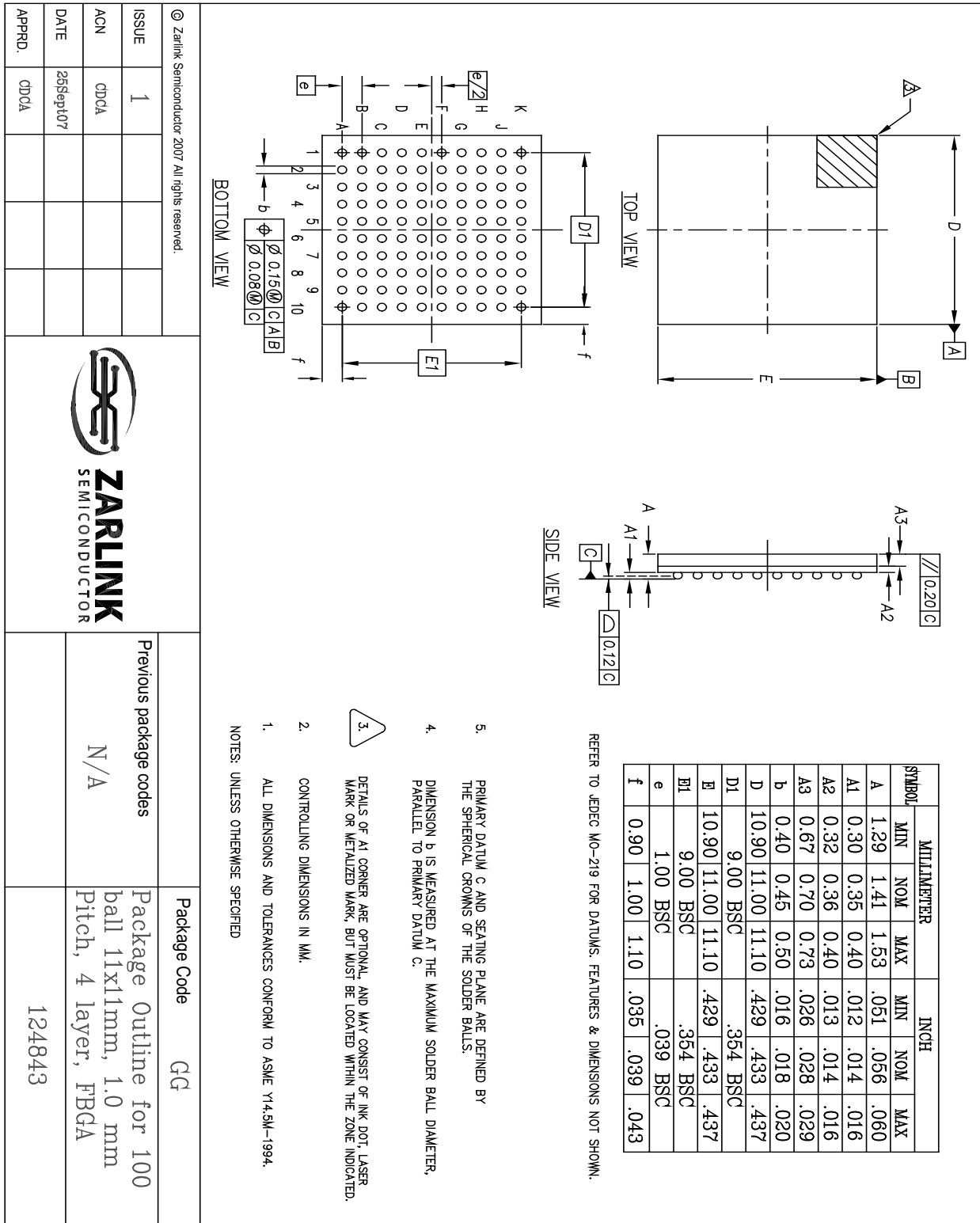
Figure 1 - Functional Block Diagram

Description

The ZL30155 Dual Channel Universal Clock Translator, part of Zarlink's ClockCenter platform of Synchronous Clock devices, delivers industry leading synchronization performance for high-speed complex applications. The highly integrated and programmable solution provides translation from any input reference frequency to any output clock frequency with jitter performance that can directly drive 10G PHY devices.

The ZL30155 integrates 2 independent digital PLLs, accepts 4 input references and generates 12 programmable clock outputs. The highly integrated solution allows designers to replace multiple components with a single chip, simplifying design and reducing component count and power.

Mechanical Drawing





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