ZL30145

SyncE (10 GbE) SONET/SDH Rate Conversion and Jitter Attenuator PLL

Short Form Data Sheet

February 2009

Features

- Can be used in systems to support the requirements of ITU-T G.8262 for synchronous Ethernet Equipment slave Clocks (EEC option 1 and 2)
- Meets jitter generation requirements of Telcordia GR-253-CORE for OC-192, OC-48, OC-12 and OC-3 rates
- Meets jitter generation requirements of ITU-T G.813 for STM-64, STM-16, STM-4 and STM-1 rates
- Synchronizes to standard telecom or Ethernet clock and provides jitter filtered output clock for SONET/SDH and Synchronous Ethernet line cards
- Synchronizes to telecom reference clocks (2 kHz, N*8 kHz up to 77.76 MHz, 155.52 MHz) or to Ethernet reference clocks (25 MHz, 50 MHz, 62.5 MHz, 125 MHz)
- Generates standard SONET/SDH clock rates (e.g., 19.44 MHz, 38.88 MHz, 77.76 MHz, 155.52 MHz, 622.08 MHz) or Ethernet clock rates (e.g., 25 MHz, 50 MHz, 125 MHz, 156.25 MHz, 312.5 MHz) for synchronizing Ethernet PHYs
- Selectable loop bandwidth of 14 Hz, 28 Hz, or 890 Hz

Ordering Information

ZL30145GGG	64 Pin CABGA	Trays
ZL30145GGG2	64 Pin CABGA*	Trays

*Pb Free Tin/Silver/Copper

-40°C to +85°C

- Configurable through a serial interface (SPI or I^2C)
- DPLL can be configured to provide synchronous or asynchronous clock outputs
- Supports IEEE 1149.1 JTAG Boundary Scan

Applications

- ITU-T G.8262 Line Cards which support 1 GbE and 10 GbE interfaces
- SONET line cards up to OC-192
- SDH line cards up to STM-64

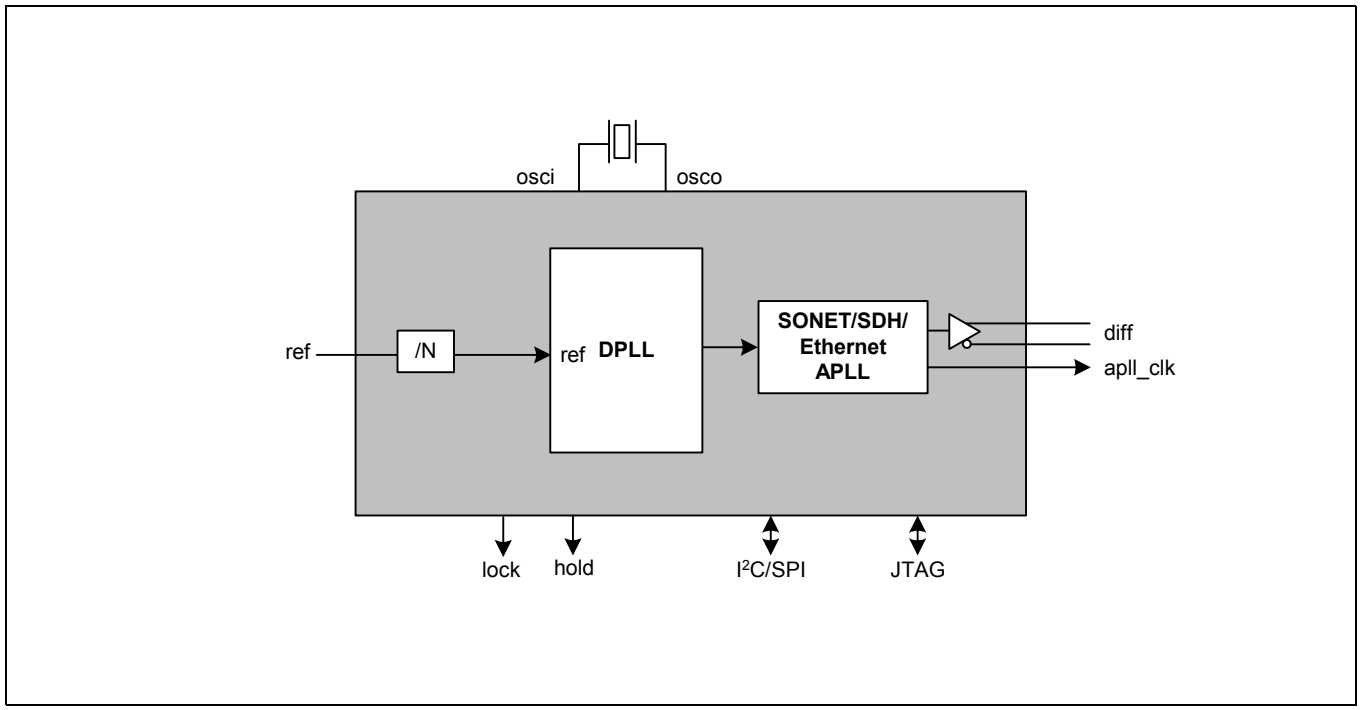
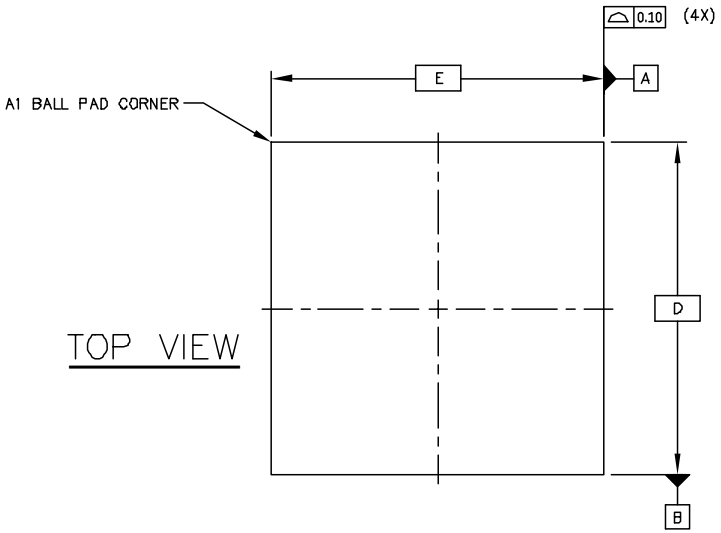


Figure 1 - Simplified Functional Block Diagram

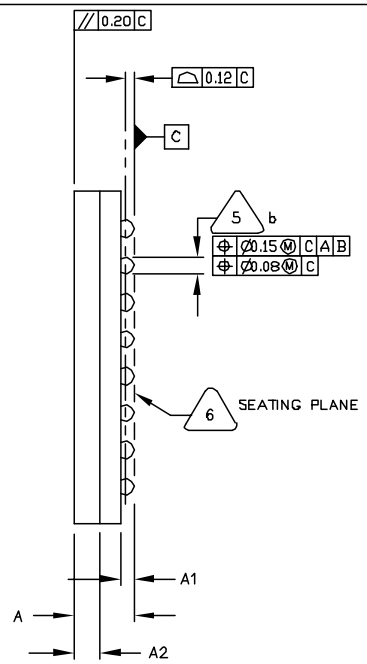
1.0 High Level Overview

The ZL30145 is a highly integrated device that provides timing for line cards. The DPLL automatically locks to one input reference and provides two synchronized output clocks for synchronizing SONET/SDH and Synchronous Ethernet line cards.

The ZL30145 has a on-chip digital phase-locked loop (DPLL) designed to provide rate conversion and jitter attenuation for Synchronous Ethernet, (SyncE), Synchronous Digital Hierarchy (SDH) and Synchronous Optical Network (SONET) networking equipment. The ZL30145 generates very low jitter clocks that meet the jitter requirements of ITU-T G.8262, Telcordia GR-253-CORE OC-48, OC-12, OC-3, OC-1 rates and ITU-T G.813 STM-16, STM-4 and STM-1 rates.

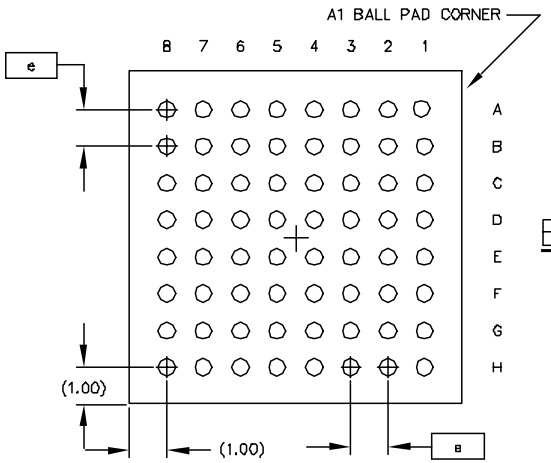


TOP VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.52	1.62	1.72
A1	0.31	0.36	0.41
A2	0.65	0.70	0.75
b	0.46 Typ.		
D	9.00 REF.		
E	9.00 Ref.		
e	1.0 Ref		
n	64		



BOTTOM VIEW

64 SOLDER BALLS

6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

5. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.

4. THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS IS 64.

3. Not to Scale.

2. THE BASIC SOLDER BALL GRID PITCH IS 1.00mm.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

ISSUE	1			
ACN	CDCA			
DATE	15April05			
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

N/A

Package Code GG

Package Outline for 64ball 9x9mm, 1.0 mm Pitch, 4 layer, CABGA

111039

For more information about all Zarlink products visit our Web Site at

www.zarlink.com