ZL30146

# SyncE SONET/SDH Line Card PLL

Short Form Data Sheet

February 2009

## Features

- Synchronizes to standard telecom or Ethernet backplane clocks and provides jitter filtered output clocks for SONET/SDH, PDH and Ethernet network interface cards
- Supports the requirements of ITU-T G.8262 for synchronous Ethernet Equipment slave Clocks
- Meets the SONET/SDH jitter generation requirements up to OC-192/STM-64
- Two independent DPLLs provides timing for the transmit path (backplane to line rate) and the receive path (recovered line rate to backplane)
- Synchronizes to telecom reference clocks (2 kHz, N*8 kHz up to 77.76 MHz, 155.52 MHz) or to Ethernet reference clocks (25 MHz, 50 MHz, 62.5 MHz, 125 MHz)
- Selectable loop bandwidth of 14 Hz, 28 Hz, 890 Hz, 3.5 Hz, 1.7 Hz, or 0.1 Hz
- Supports automatic hitless reference switching and short term holdover during loss of reference inputs
- Generates standard SONET/SDH clock rates (e.g., 19.44 MHz, 38.88 MHz, 77.76 MHz, 155.52 MHz, 622.08 MHz) or Ethernet clock rates (e.g., 25 MHz, 50 MHz, 125 MHz, 156.25 MHz, 312.5 MHz) for synchronizing Ethernet PHYs

**Ordering Information**

| | | |
|---|---|---|
| ZL30146GGG | 64 Pin CABGA | Trays |
| ZL30146GGG2 | 64 Pin CABGA* | Trays |

*Pb Free Tin/Silver/Copper

**-40°C to +85°C**

- Programmable output synthesizer to generate telecom clock frequencies from any multiple of 8 kHz up to 100 MHz (e.g., T1/E1, DS3/E3)
- Generates several styles of output frame pulse with selectable pulse width, polarity, and frequency
- Configurable input to output delay and output to output phase alignment
- Configurable through a serial interface (SPI or $I^2C$)
- DPLLs can be configured to provide synchronous or asynchronous clock outputs

## Applications

- ITU-T G.8262 Line Cards which support 1 GbE and 10 GbE interfaces
- SONET/SDH line cards up to OC-192/STM-64

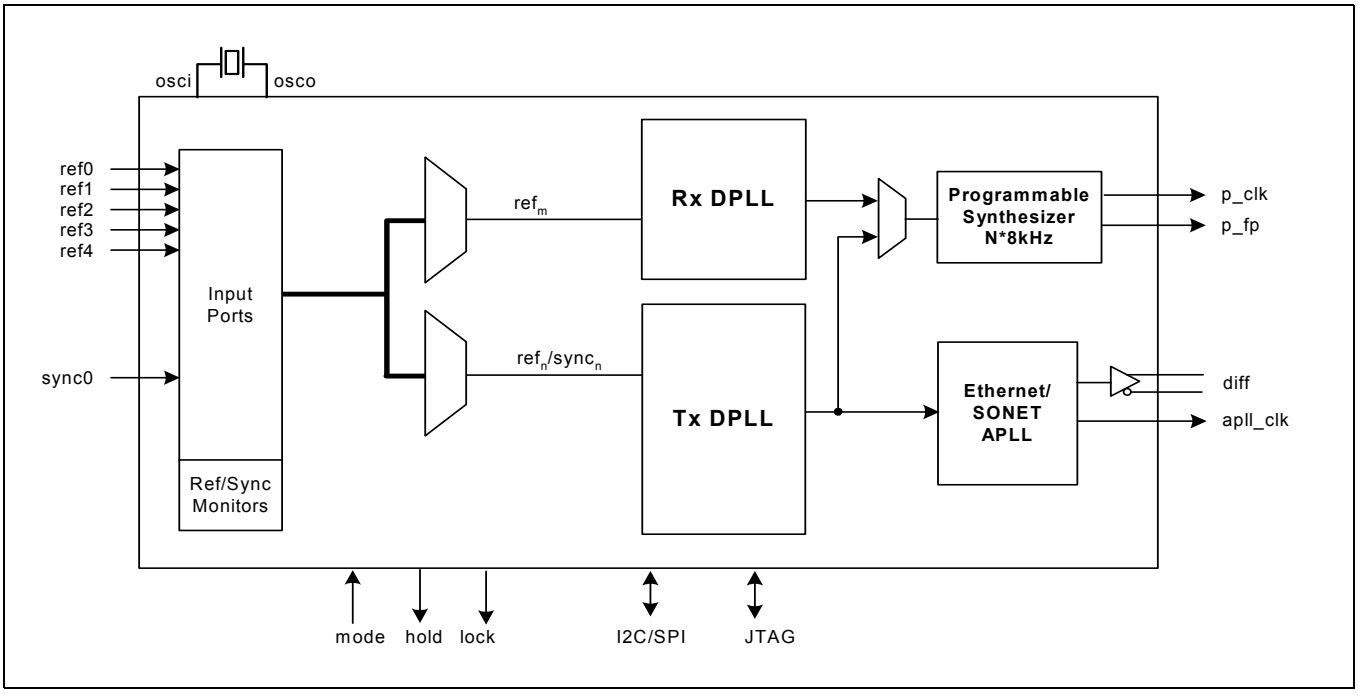



**Figure 1 - Functional Block Diagram**

## 1.0 Functional Description

The ZL30146 OC-192/STM-64 PDH/SONET/SDH/Synchronous Ethernet Network Interface Synchronizer is a highly integrated device that provides timing for both PDH/SONET/SDH and Ethernet network interface cards. A functional block diagram is shown in Figure 1.

This device is ideally suited for designs that require both a transmit timing path (backplane to PHY) and a receive timing path (PHY to backplane). Each path is controlled with separate DPLLs (Tx DPLL, Rx DPLL) which are both independently configurable through the serial interface (SPI or $I^2C$). A typical application of the ZL30146 is shown in Figure 2. In this application, the ZL30146 translates the 19.44 MHz clock from the telecom rate backplane (system timing bus), translates the frequency to 622.08 MHz or 156.25 MHz for the PHY Tx clock, and filters the jitter to ensure compliance with the related standards. On the receive path, the Rx DPLL and the programmable synthesizer translate the line recovered clock (8 kHz or 25 MHz) from the PHY to the 19.44 MHz telecom backplane (line recovered timing) for the central timing cards. The ZL30146 allows easy integration of Ethernet line rates with today's telecom backplanes.

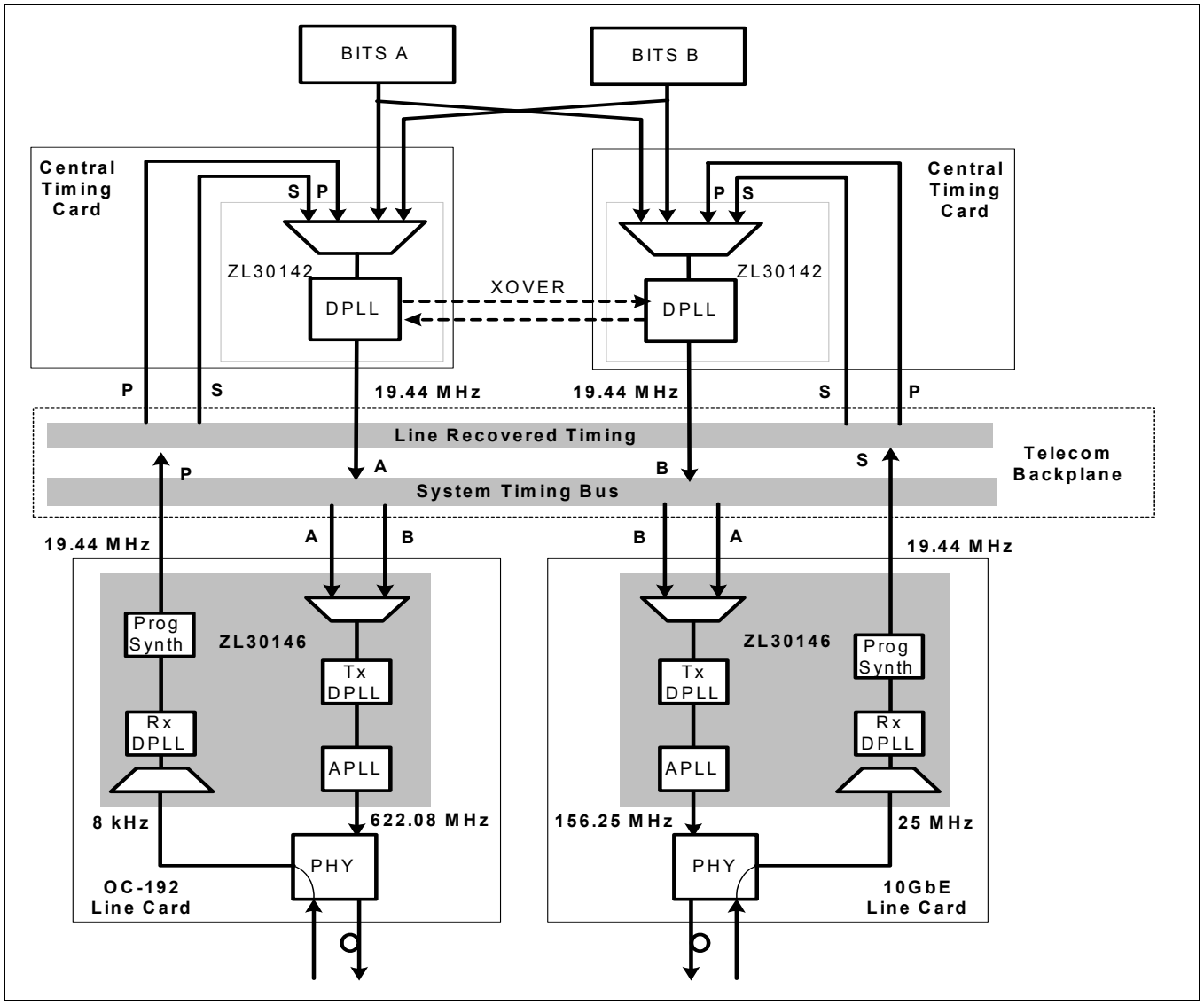
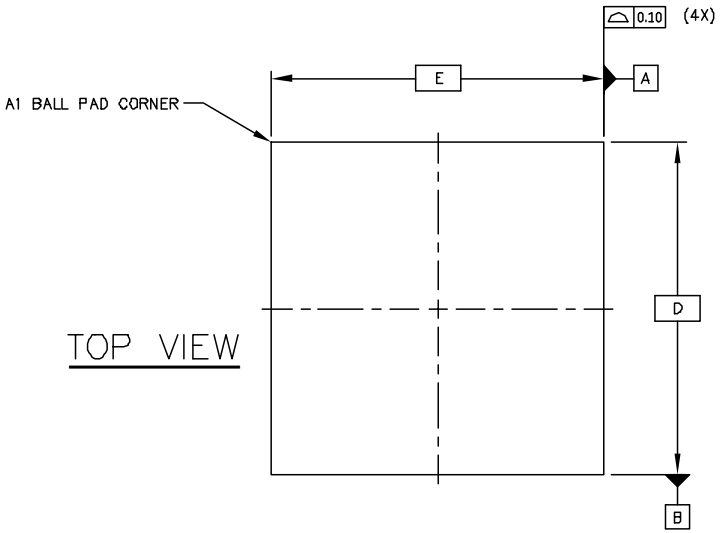
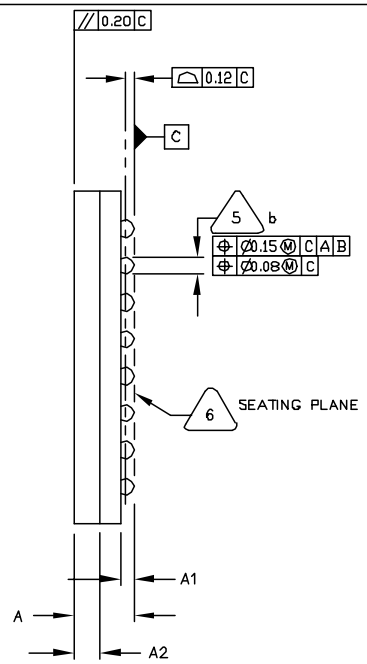



**Figure 2 - Typical Application of the ZL30146**

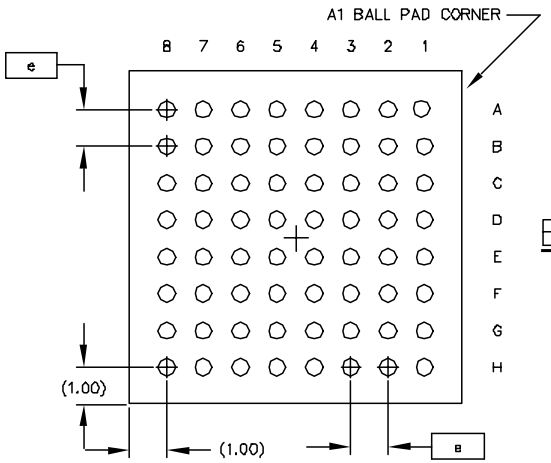



TOP VIEW




SIDE VIEW

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 1.52 | 1.62 | 1.72 |
| A1 | 0.31 | 0.36 | 0.41 |
| A2 | 0.65 | 0.70 | 0.75 |
| b | 0.46 Typ. | | |
| D | 9.00 REF. | | |
| E | 9.00 Ref. | | |
| e | 1.0 Ref | | |
| n | 64 | | |




BOTTOM VIEW

64 SOLDER BALLS

6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

5. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.

4. THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS IS 64.

3. Not to Scale.

2. THE BASIC SOLDER BALL GRID PITCH IS 1.00mm.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED



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|---|---|---|---|---|
| ISSUE | 1 | | | |
| ACN | CDCA | | | |
| DATE | 15April05 | | | |
| APPRD. | | | | |

ZARLINK SEMICONDUCTOR

Previous package codes

N/A

Package Code GG

Package Outline for 64ball 9x9mm, 1.0 mm Pitch, 4 layer, CABGA

111039

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**www.zarlink.com**