ZL30143

SyncE SONET/SDH G.8262/Stratum3 System Synchronizer/SETS

Short Form Data Sheet

February 2009

Features

- Supports the requirements of ITU-T G.8262 for synchronous Ethernet Equipment slave Clocks (EEC option 1 and 2)
- Supports the requirements of Telcordia GR-1244 Stratum 3 and GR-253, ITU-T G.813, and G.781 SETS
- Supports ITU-T G.823, G.824 and G.8261 for 2048 kbit/s and 1544 kbit/s interfaces
- Meets the SONET/SDH jitter generation requirements up to OC-48/STM-16
- Synchronizes to telecom reference clocks (2 kHz, N*8 kHz up to 77.76 MHz, 155.52 MHz) or to Ethernet reference clocks (25 MHz, 50 MHz, 62.5 MHz, 125 MHz)
- Supports composite clock inputs (64 kHz, 64 kHz + 8 kHz, 64kHz + 8 kHz + 400 Hz)
- Generates standard SONET/SDH clock rates (e.g., 19.44 MHz, 38.88 MHz, 77.76 MHz, 155.52 MHz, 622.08 MHz) or Ethernet clock rates (e.g., 25 MHz, 50 MHz, 125 MHz, 156.25 MHz, 312.5 MHz) for synchronizing Gigabit Ethernet PHYs
- Programmable output synthesizers (P0, P1) generate telecom clock frequencies from any multiple of 8 kHz up to 100 MHz
- Generates several styles of telecom frame pulses with selectable pulse width, polarity and frequency
- Provides two DPLLs which are independently configurable through a serial interface

Ordering Information

ZL30143GGG	100 Pin CABGA	Trays
ZL30143GGG2	100 Pin CABGA*	Trays

*Pb Free Tin/Silver/Copper

-40°C to +85°C

- Internal state machine automatically controls mode of operation (free-run, locked, holdover)
- Flexible input reference monitoring automatically disqualifies references based on frequency and phase irregularities
- Provides automatic reference switching and holdover during loss of reference input
- Supports master/slave configuration and dynamic input to output delay compensation for AdvancedTCA™
- Configurable input to output delay and output to output phase alignment

Applications

- ITU-T G.8262 System Timing Cards which support 1 GbE and 10 GbE interfaces
- Telcordia GR-253 Carrier Grade SONET/SDH Stratum 3 System Timing Cards
- System Timing Cards which supports ITU-T G.781 SETS (SDH Equipment Timing Source)

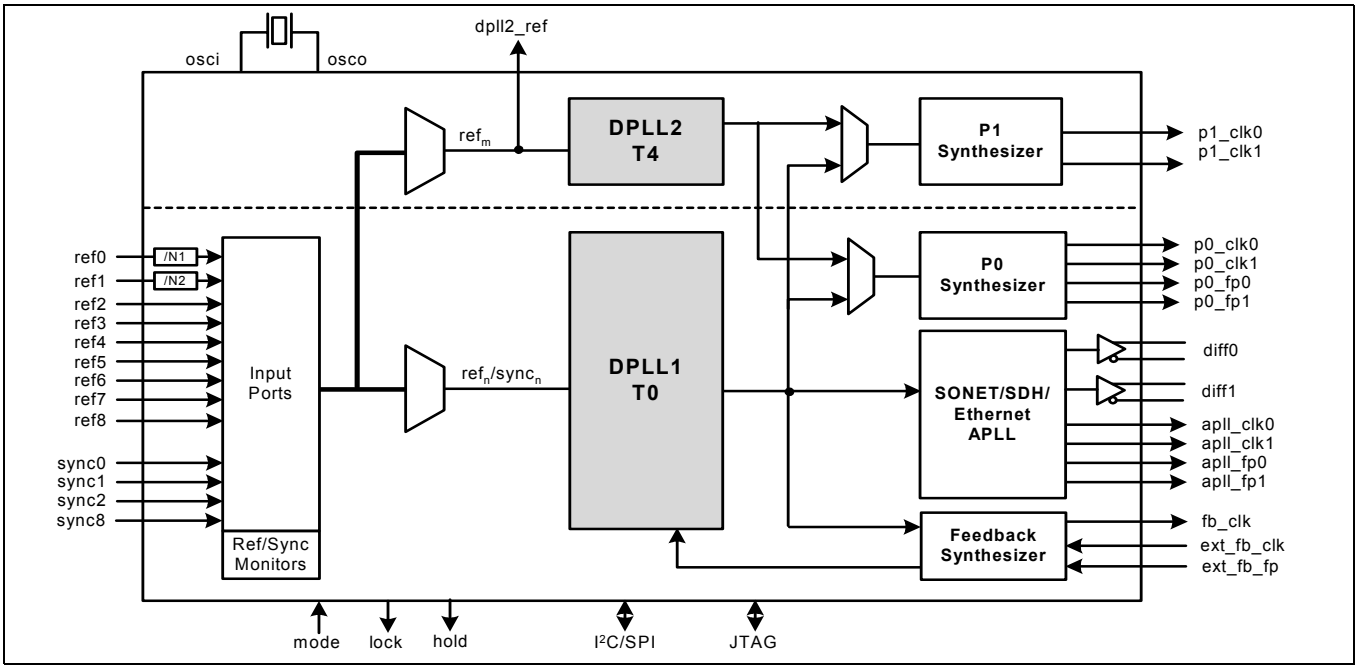


Figure 1 - Functional Block Diagram

1.0 Overview

The ZL30143 System Synchronizer and SETS device is a highly integrated device that provides all of the functionality that is required for a central timing card in carrier grade network equipment. The basic functions of a central timing card include:

- Input reference monitoring for both frequency accuracy and phase irregularities
- Automatic input reference selection
- Support of both external timing and line timing modes
- Hitless reference switching
- Wander and jitter filtering
- Master/slave crossover for minimizing phase alignment between redundant timing cards
- Independent derived output timing path for support of the SETS functionality

In a typical application, the main timing path uses DPLL1 to synchronize to either an external BITS source or to a recovered line timed source. DPLL1 monitors all references and automatically selects the best available reference based on configurable priority and revertive properties. DPLL1 provides the wander filtering function and the P0 synthesizer generates a jitter filtered clock and frame pulse for the system timing bus which supplies all line cards with a common timing reference. The APLL is used to generate a reference clock for an Ethernet PHY which can be used to synchronize remote equipment. A derived output timing path using DPLL2 is available to support the SETS function. In this case DPLL2 uses a filter above 10 Hz to prevent it from filtering wander.

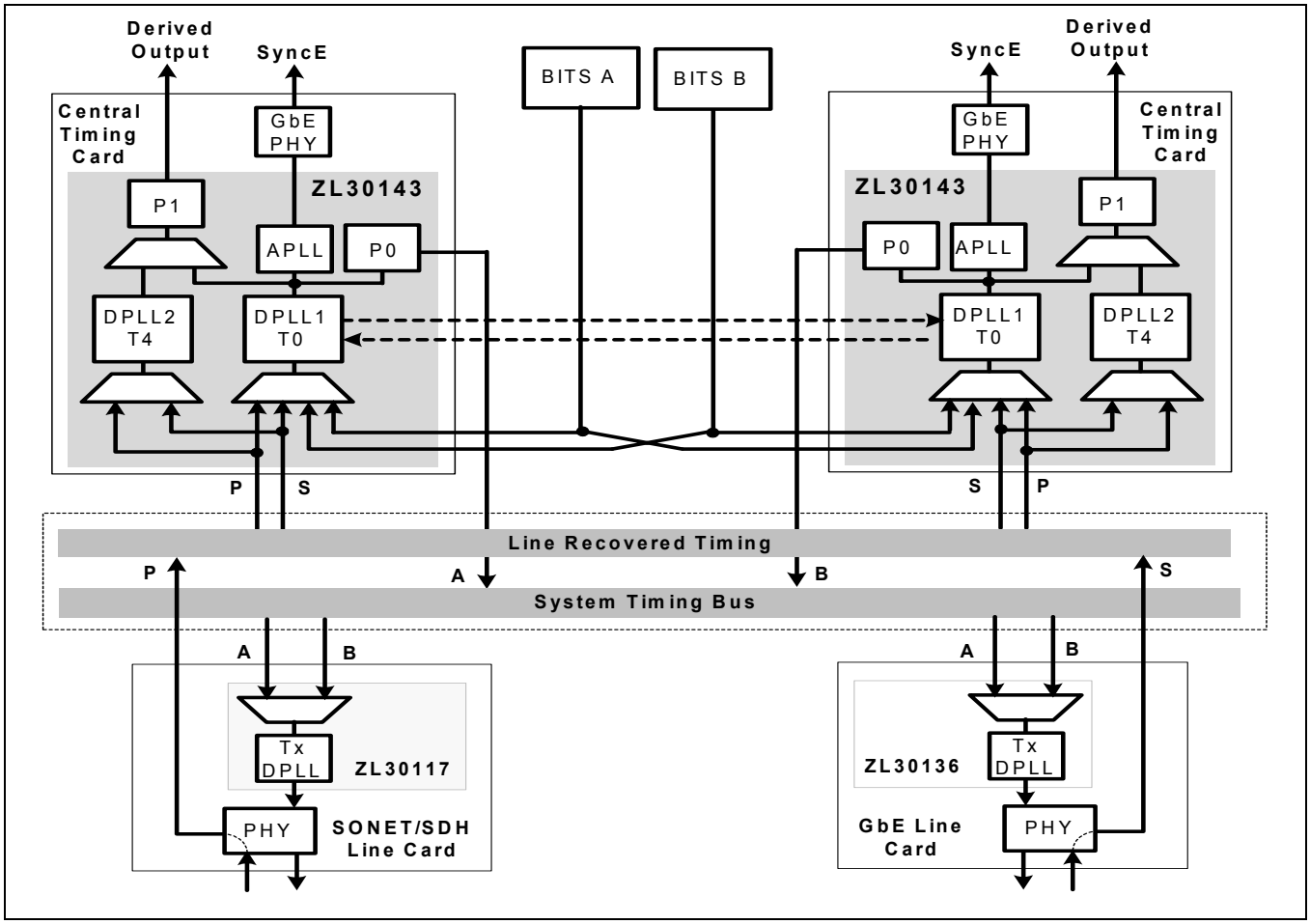
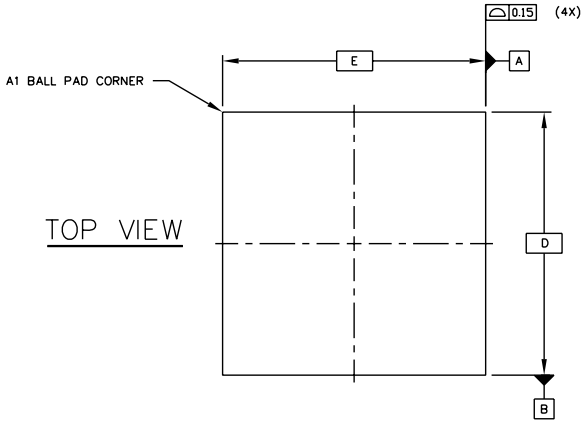
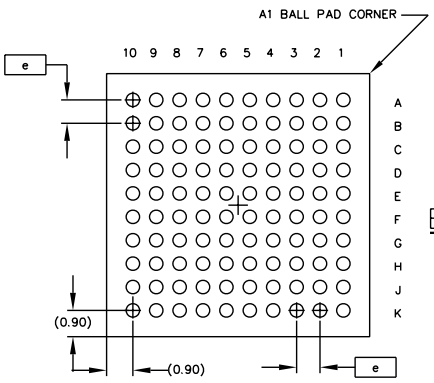
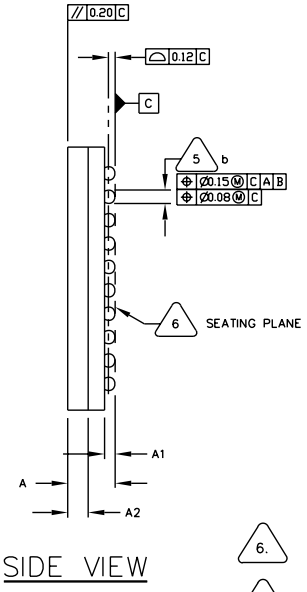


Figure 2 - Typical Application of the ZL30143





BOTTOM VIEW
100 SOLDER BALLS



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.52	1.62	1.72
A1	0.31	0.36	0.41
A2	0.65	0.70	0.75
b		0.46 Typ.	
D	8.85	9.00	9.15
E	8.85	9.00	9.15
e		0.8 Ref	
n		100	

6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

5. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.

4. THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS IS 100.

3. Not to Scale.

2. THE BASIC SOLDER BALL GRID PITCH IS 0.8mm.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

ISSUE	1	2	3	
ACN	CDCA	CDCA	CDCA	
DATE	15April05	24Aug05	26Oct06	
APPRD.				

ZARLINK SEMICONDUCTOR

Package Code GG

Previous package codes
N/A

Package Outline for 100ball 9x9mm, 0.8 mm Pitch, 4 layer, CABGA

111040

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www.zarlink.com