ZARLINK SEMICONDUCTOR

ZL30108
SONET/SDH Network Interface DPLL

Data Sheet

March 2006

Features

- Supports output wander and jitter generation specifications for GR-253-CORE OC-3 and G.813 STM-1 SONET/SDH interfaces
- Accepts two input references and synchronizes to any combination of 2 kHz, 8 kHz, 1.544 MHz, 2.048 MHz, 8.192 MHz, 16.384 MHz or 19.44 MHz inputs
- Provides a 19.44 MHz (SONET/SDH) clock output
- Provides an 8 kHz framing pulse and a 2 kHz multi-frame pulse
- Provides automatic entry into Holdover and return from Holdover
- Hitless reference switching between any combination of valid input reference frequencies
- Provides lock and accurate reference fail indication
- Loop filter bandwidth of 29 Hz or 14 Hz
- Less than 24 ps_{rms} intrinsic jitter on the 19.44 MHz output clock, compliant with GR-253-CORE OC-3 and G.813 STM-1 specifications
- Less than 0.5 ns_{pp} intrinsic jitter on output frame pulses
- External master clock source: clock oscillator or crystal
- Simple hardware control interface

Ordering Information

ZL30108LDA	32 Pin QFN	Tubes
ZL30108LDE1	32 Pin QFN*	Tubes, Bake & Drypack
	*Pb Free Matte Tin	

-40°C to +85°C

Applications

- Line card synchronization for SONET/SDH systems

Description

The ZL30108 SONET/SDH network interface digital phase-locked loop (DPLL) provides timing and synchronization for SONET/SDH network interface cards.

The ZL30108 generates a SONET/SDH clock and framing signals that are phase locked to one of two backplane or network references. It helps ensure system reliability by monitoring its references for frequency accuracy and stability and by maintaining tight phase alignment between the input reference clock and clock outputs.

The ZL30108 output clock's wander and jitter generation are compliant with GR-253-CORE OC-3 and G.813 STM-1 specifications.

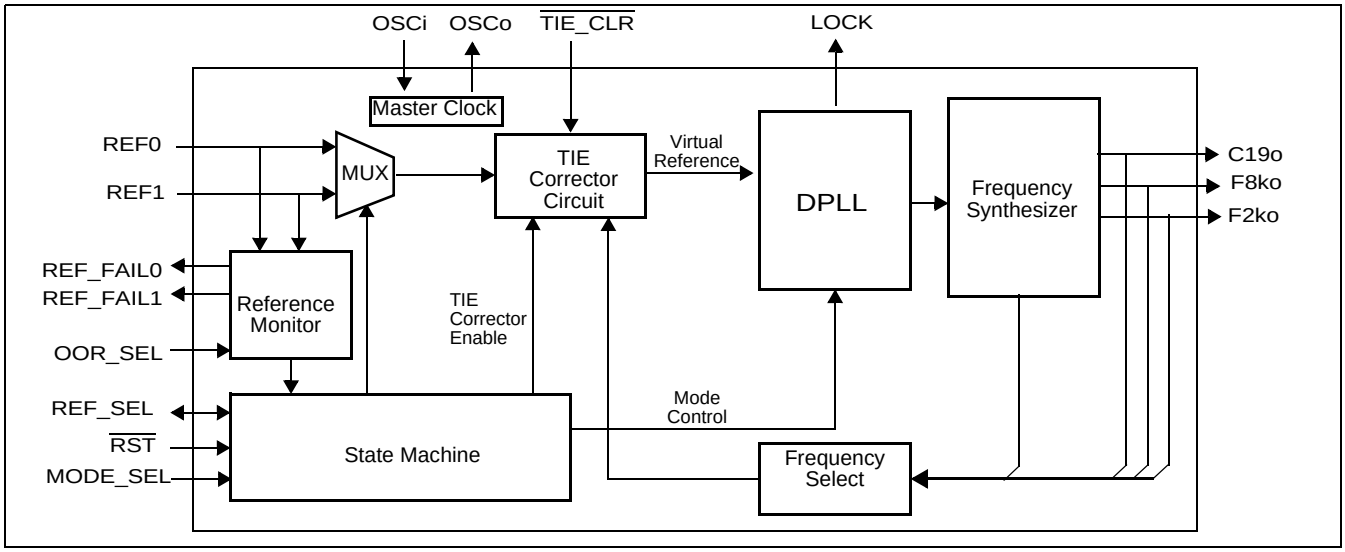

Figure 1 - Functional Block Diagram

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List of Figures

1.0 Change Summary

Changes from November2005 Issue to March 2006 Issue. Page, section, figure and table numbers refer to this current issue.

Page	Item	Change
1		Updated Ordering Information.

Changes from July 2005 Issue to October 2005 Issue. Page, section, figure and table numbers refer to this current issue.

Page	Item	Change
1	Features	Changed description for hitless reference switching.
18	Section 7.1	Removed power supply decoupling circuit and included reference to synchronizer power supply decoupling application note.

Changes from October 2004 Issue to July 2005 Issue. Page, section, figure and table numbers refer to this issue.

Page	Item	Change
6	$\overline{\text{RST}}$ pin	Specified clock and frame pulse outputs forced to high impedance.
20	Section 7.4	Corrected time-constant of example reset circuit.
21	Table “DC Electrical Characteristics*“	Corrected Schmitt trigger levels.
25	Table “Performance Characteristics* - Functional“	Specified $\overline{\text{TIE\_CLR}}$=1 in Lock Time conditions.

2.0 Physical Description

2.1 Pin Connections

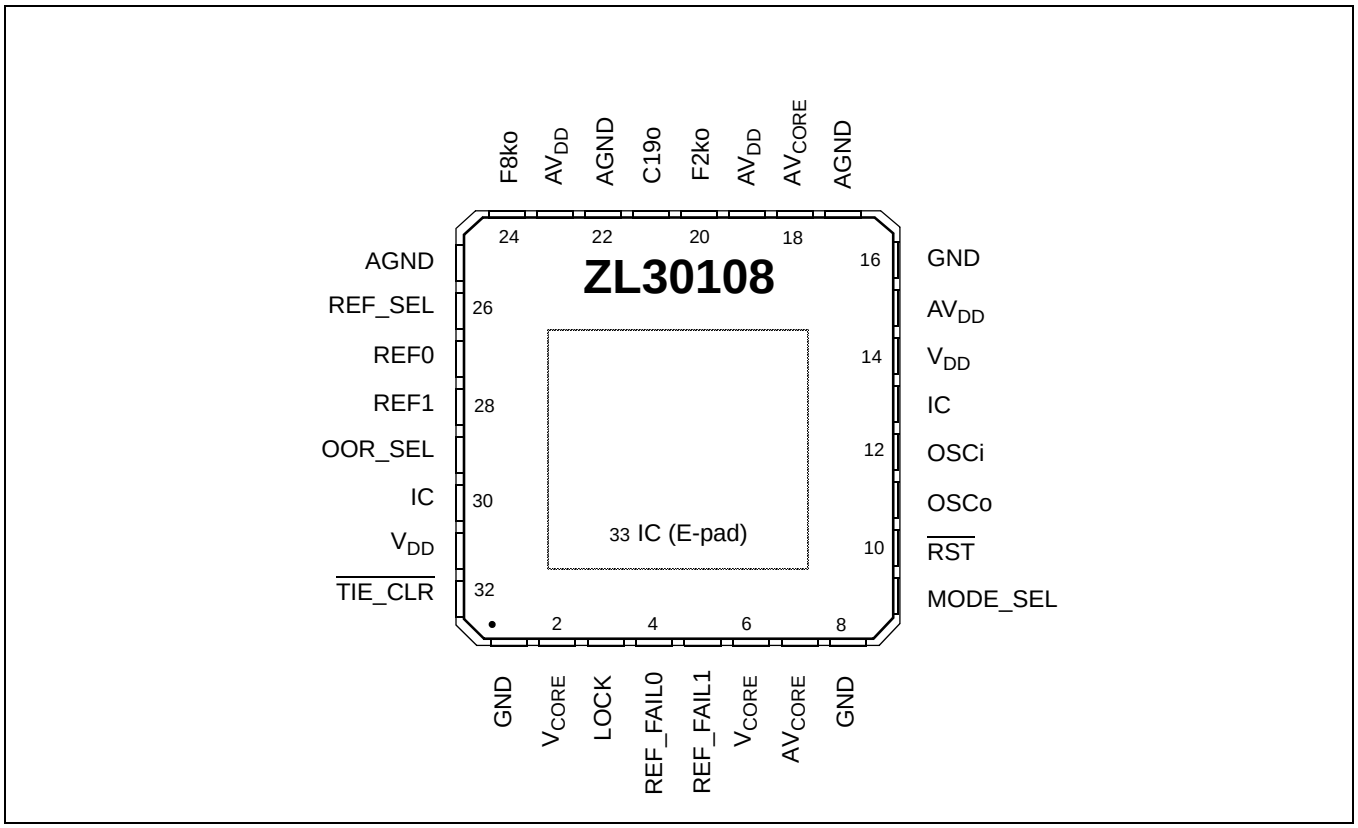


Figure 2 - Pin Connections (32 pin 5 mm X 5 mm QFN)

3.0 Pin Description

Pin #	Name	Description
1	GND	**Ground.** 0 V
2	V_{CORE}	**Positive Supply Voltage.** +1.8 V_{DC} nominal
3	LOCK	**Lock Indicator (Output).** This output goes to a logic high when the PLL is frequency locked to the selected input reference.
4	REF_FAIL0	**Reference 0 Failure Indicator (Output).** A logic high at this pin indicates that the REF0 reference frequency has exceeded the out-of-range limit set by the OOR_SEL pin or that it is exhibiting abrupt phase or frequency changes.
5	REF_FAIL1	**Reference 1 Failure Indicator (Output).** A logic high at this pin indicates that the REF1 reference frequency has exceeded the out-of-range limit set by the OOR_SEL pin or that it is exhibiting abrupt phase or frequency changes.
6	V_{CORE}	**Positive Supply Voltage.** +1.8 V_{DC} nominal.
7	AV_{CORE}	**Positive Analog Supply Voltage.** +1.8 V_{DC} nominal.
8	GND	**Ground.** 0 V
9	MODE_SEL	**Mode Select (Input).** This input determines the mode of operation: See Table 3. 0: Normal mode (device locked to input reference) 1: Freerun mode
10	$\overline{RST}$	**Reset (Input).** A logic low at this input resets the device. On power up, the $\overline{RST}$ pin must be held low for a minimum of 300 ns after the power supply pins have reached the minimum supply voltage. When the $\overline{RST}$ pin goes high, the device will transition into a Reset state for 3 ms. In the Reset state all clock and frame pulse outputs will be forced into high impedance.
11	OSCo	**Oscillator Master Clock (Output).** For crystal operation, a 20 MHz crystal is connected from this pin to OSCi. This output is not suitable for driving other devices. For clock oscillator operation, this pin must be left unconnected.
12	OSCi	**Oscillator Master Clock (Input).** For crystal operation, a 20 MHz crystal is connected from this pin to OSCo. For clock oscillator operation, this pin must be connected to a clock source.
13	IC	**Internal Connection.** Connect this pin to VDD.
14	V_{DD}	**Positive Supply Voltage.** +3.3 V_{DC} nominal
15	AV_{DD}	**Positive Analog Supply Voltage.** +3.3 V_{DC} nominal
16	GND	**Ground.** 0 V
17	AGND	**Analog Ground.** 0 V
18	AV_{CORE}	**Positive Analog Supply Voltage.** +1.8 V_{DC} nominal
19	AV_{DD}	**Positive Analog Supply Voltage.** +3.3 V_{DC} nominal
20	F2ko	**Multi Frame Pulse (Output).** This is a CMOS 2 kHz active high 51 ns framing pulse, which marks the beginning of a multi frame. This clock output pad includes a Schmitt triggered input which serves as a PLL feedback path; proper transmission-line termination should be applied to maintain reflections below Schmitt trigger levels.

Pin #	Name	Description
21	C19o	**Clock 19.44 MHz (Output).** This CMOS output is used in SONET/SDH applications. This clock output pad includes a Schmitt input which serves as a PLL feedback path; proper transmission-line termination should be applied to maintain reflections below Schmitt trigger levels.
22	AGND	**Analog Ground.** 0 V
23	AV_{DD}	**Positive Analog Supply Voltage.** +3.3 V_{DC} nominal
24	F8ko	**Frame Pulse (Output).** This is an CMOS 8 kHz active high 31 ns framing pulse, which marks the beginning of a 125 μs frame. This clock output pad includes a Schmitt input which serves as a PLL feedback path; proper transmission-line termination should be applied to maintain reflections below Schmitt trigger levels.
25	AGND	**Analog Ground.** 0 V
26	REF_SEL	**Reference Select 0 (Input/Output).** As an input REF_SEL selects the reference input that is used for synchronization; See Table 4. 0: REF0 1: REF1 This pin is internally pulled down to GND.
27	REF0	**Reference (Input).** This is one of two (REF0 and REF1) input reference sources used for synchronization. One of seven possible frequencies may be used: 2 kHz, 8 kHz, 1.544 MHz, 2.048 MHz, 8.192 MHz,16.384 MHz or 19.44 MHz. This pin is internally pulled down to GND.
28	REF1	**Reference (Input).** See REF0 pin description.
29	OOR_SEL	**Out Of Range Selection (Input).** This input selects the frequency acceptance limits of the reference monitor: See Table 2. 0: 40 - 52 ppm 1: 64 - 83 ppm
30	IC	**Internal Connection.** Connect this pin to GND.
31	V_{DD}	**Positive Supply Voltage.** +3.3 V_{DC} nominal.
32	$\overline{\text{TIE\_CLR}}$	**TIE Circuit Reset (Input).** A logic low at this input resets the Time Interval Error (TIE) correction circuit resulting in a realignment of input phase with output phase.
33	IC	**Internal Connection.** Package E-pad, this pin is internally connected to device GND, it can be left unconnected or it can be connected to GND.

4.0 Functional Description

The ZL30108 is a SONET/SDH Network Interface DPLL, providing timing (clock) and synchronization (frame) signals to SONET/SDH network interface cards. Figure 1 is a functional block diagram which is described in the following sections.

4.1 Reference Select Multiplexer (MUX)

The ZL30108 accepts two simultaneous reference input signals and operates on their rising edges. One of two, the primary reference (REF0) or the secondary reference (REF1) signal is selected as input to the TIE Corrector Circuit based on the Reference Selection (REF_SEL) input.

4.2 Reference Monitor

The input references are monitored by two independent reference monitor blocks, one for each reference. The block diagram of a single reference monitor is shown in Figure 3. For each reference clock, the frequency is detected and the clock is continuously monitored for three independent criteria that indicate abnormal behavior of the reference signal, for example; long term drift from its nominal frequency or excessive jitter. To ensure proper operation of the reference monitor circuit, the minimum input pulse width restriction of 15 nsec must be observed.

- **Reference Frequency Detector (RFD)**: This detector determines whether the frequency of the reference clock is 2 kHz, 8 kHz, 1.544 MHz, 2.048 MHz 8.192 MHz, 16.384 MHz or 19.44 MHz and provides this information to the various monitor circuits and the phase detector circuit of the DPLL.
- **Precise Frequency Monitor (PFM)**: This circuit determines whether the frequency of the reference clock is within the applicable accuracy range defined by the OOR_SEL pin, see Figure 5, Figure 6 and Table 2. It will take the precise frequency monitor up to 10 s to qualify or disqualify the input reference.
- **Coarse Frequency Monitor (CFM)**: This circuit monitors the reference over intervals of approximately 30 µs to quickly detect large frequency changes.
- **Single Cycle Monitor (SCM)**: This detector checks the period of a single clock cycle to detect large phase hits or the complete loss of the clock.

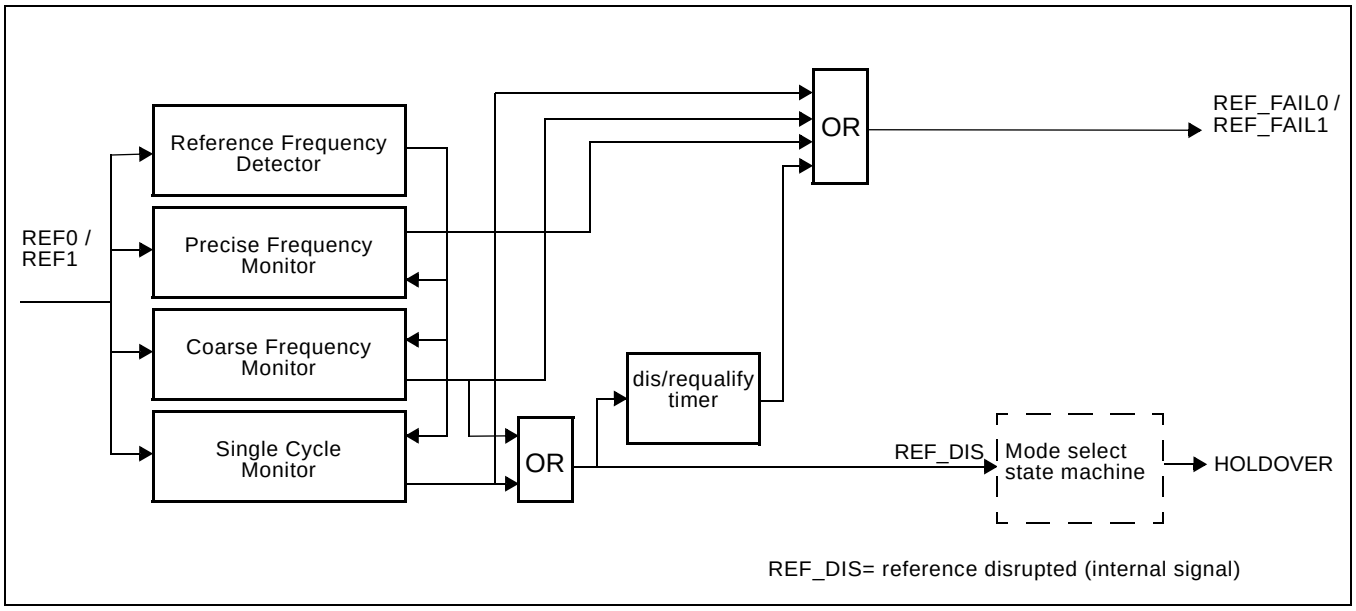


Figure 3 - Reference Monitor Circuit

Exceeding the threshold of any of the monitors forces the corresponding REF_FAIL pin to go high. The single cycle and coarse frequency failure flags force the DPLL into Holdover mode and feed a timer that disqualifies the reference input signal when the failures are present for more than 2.5 s. The single cycle and coarse frequency failures must be absent for 10 s to let the timer requalify the input reference signal as valid. Multiple failures of less than 2.5 s each have an accumulative effect and will disqualify the reference. This is illustrated in Figure 4.

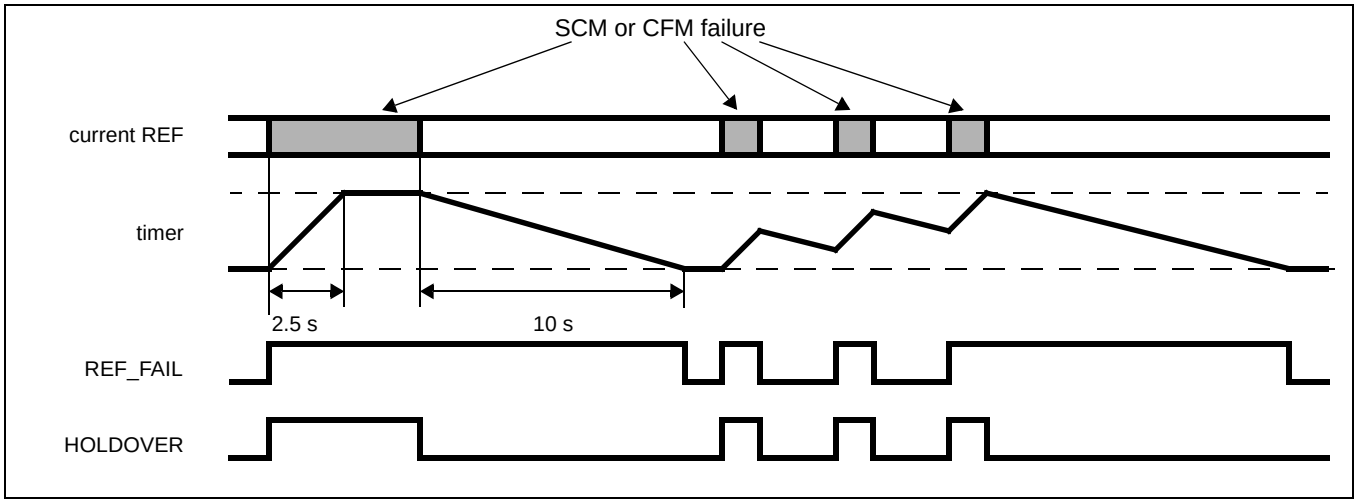


Figure 4 - Behavior of the Dis/Requalify Timer

When the incoming signal returns to normal (REF_FAIL=0), the DPLL returns to Normal mode with the output signal locked to the input signal. Each of the monitors has a built-in hysteresis to prevent flickering of the REF_FAIL status pin at the threshold boundaries. The precise frequency monitor and the timer do not affect the mode (Holdover/Normal) of the DPLL.

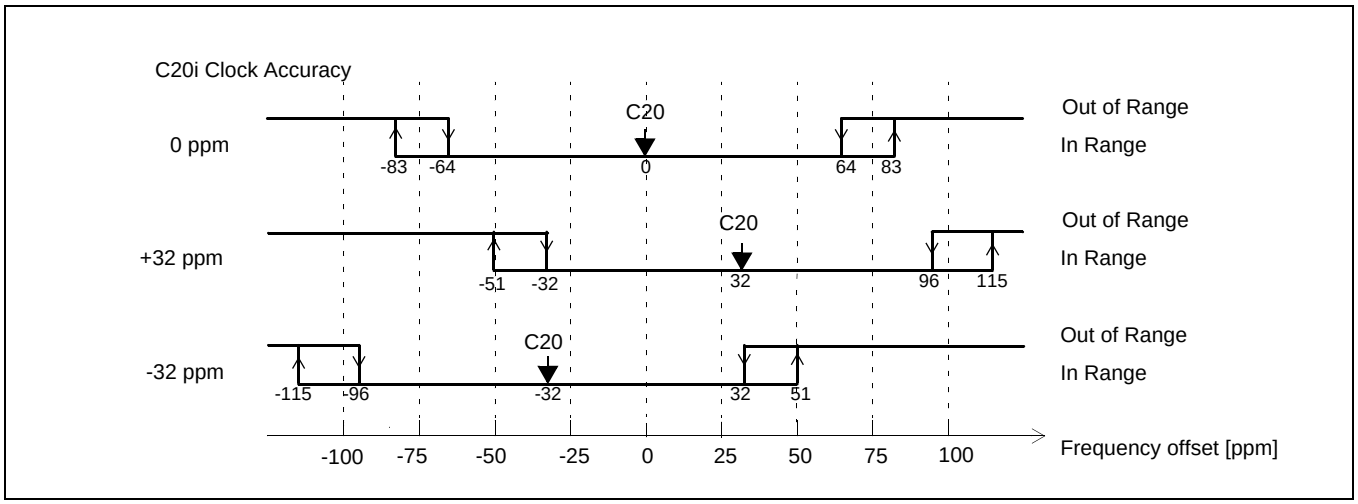


Figure 5 - Out-of-Range Thresholds for OOR_SEL=1

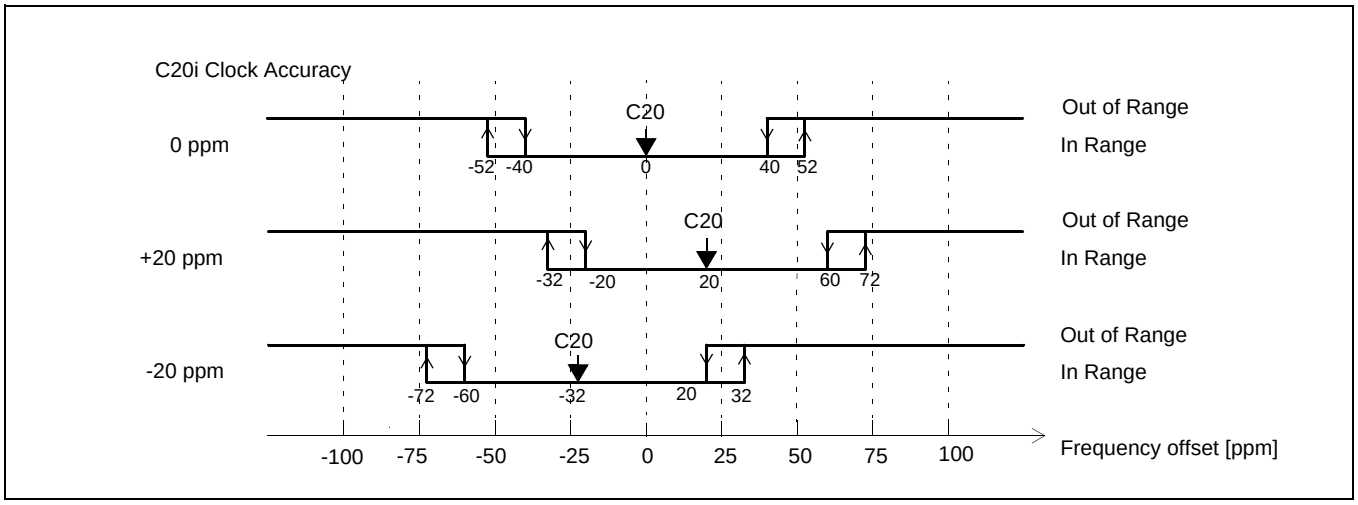


Figure 6 - Out-of-Range Thresholds for OOR_SEL=0

4.3 Time Interval Error (TIE) Corrector Circuit

The TIE Corrector Circuit eliminates phase transients on the output clock that may occur in the course of recovery from Automatic Holdover mode to Normal mode.

On recovery from Automatic Holdover mode or when switching to another reference input, the TIE corrector circuit measures the phase delay between the current phase (feedback signal) and the phase of the selected reference signal. This delay value is stored in the TIE corrector circuit. This circuit creates a new virtual reference signal that is at the same phase position as the feedback signal. By using the virtual reference, the PLL minimizes the phase transient it experiences when it switches to another reference input or recovers from Automatic Holdover mode.

The delay value can be reset by setting the TIE Corrector Circuit Clear pin ($\overline{\text{TIE\_CLR}}$) low for at least 15 ns. This results in a phase alignment between the input reference signal and the output clocks and frame pulses as shown in Figure 14 and Figure 15. The speed of the phase alignment correction is limited by the loop filter bandwidth. Convergence is always in the direction of least phase travel. $\overline{\text{TIE\_CLR}}$ can be kept low continuously. In that case the output clocks will always align with the selected input reference. This is illustrated in Figure 7.

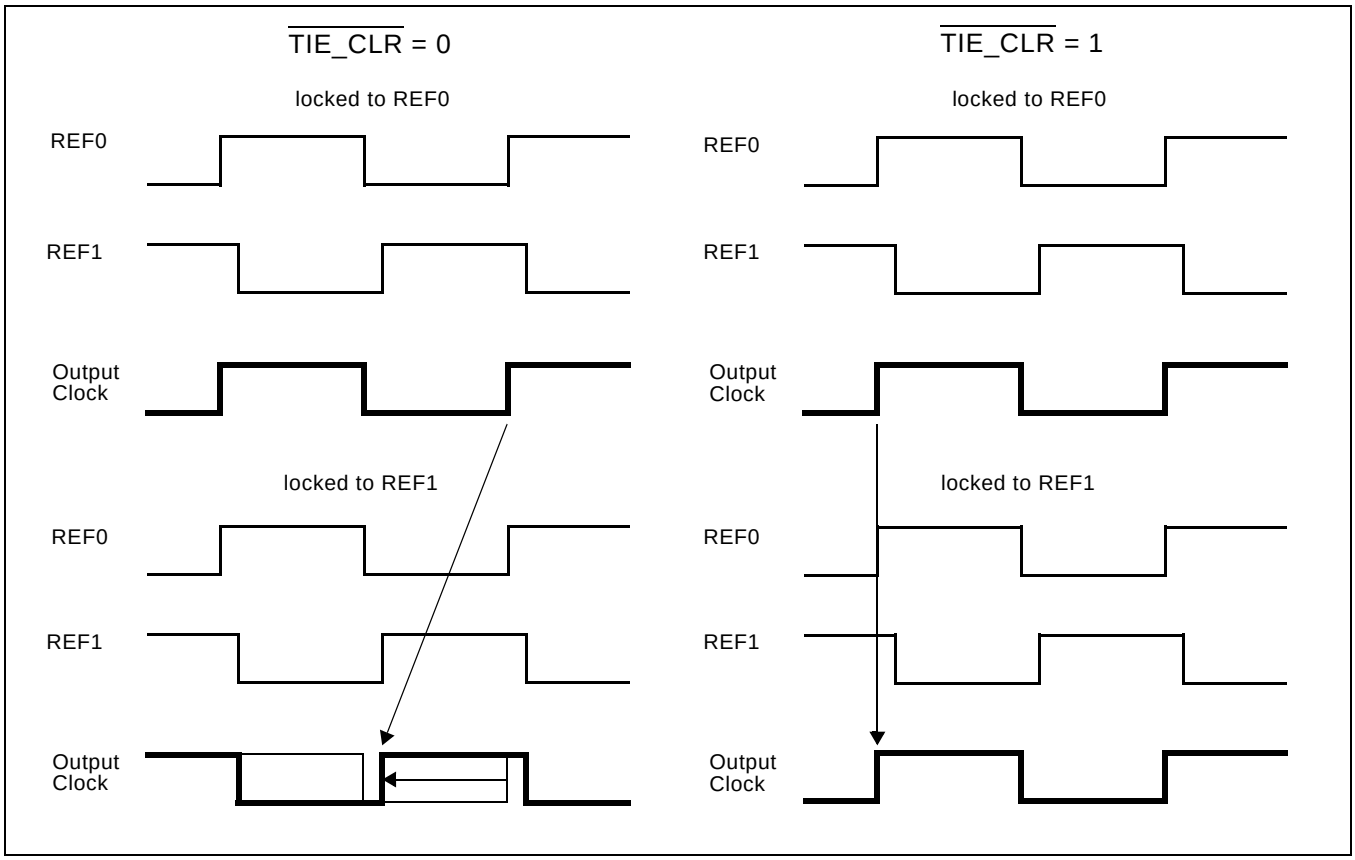


Figure 7 - Timing Diagram of Hitless Reference Switching

4.4 Digital Phase Lock Loop (DPLL)

The DPLL of the ZL30108 consists of a phase detector, an integrated on-chip loop filter, and a digitally controlled oscillator as shown in Figure 8. The data path from the phase detector to the filter is tapped and routed to the lock indicator that provides a lock indication which is output at the LOCK pin.

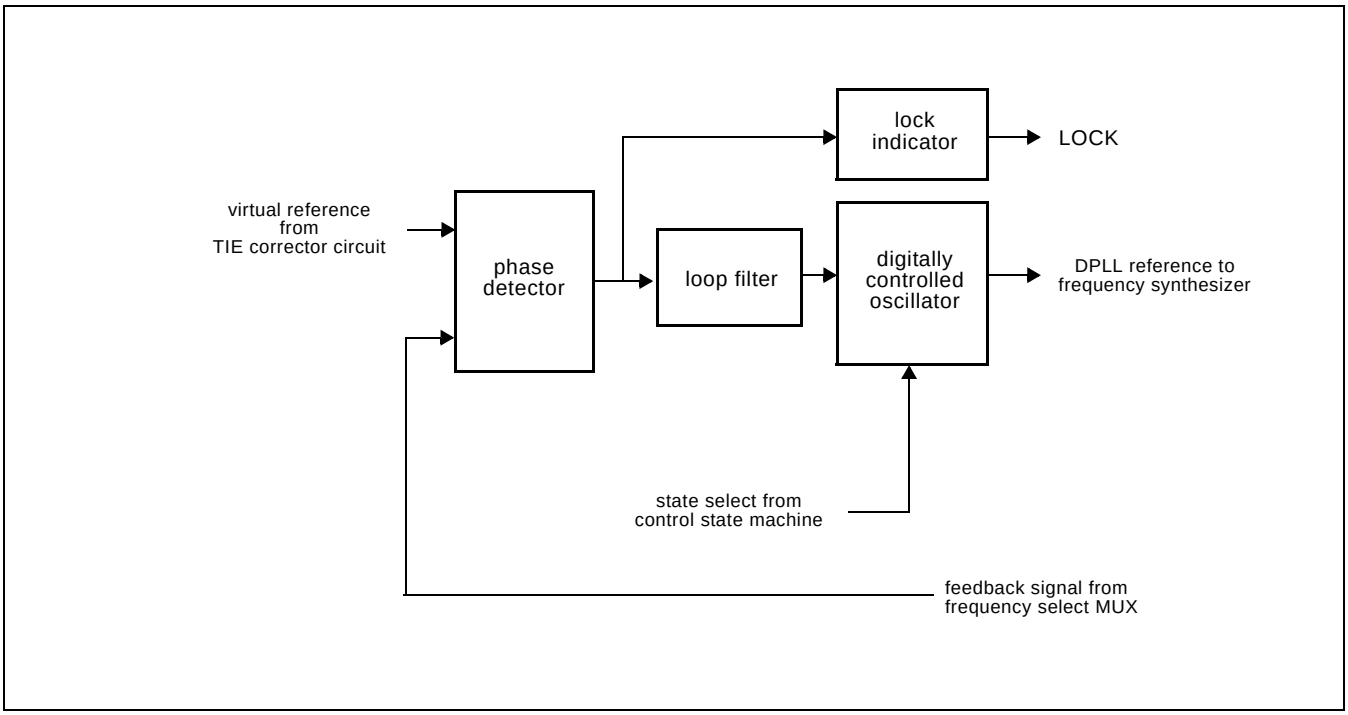


Figure 8 - DPLL Block Diagram

Phase Detector - the phase detector compares the virtual reference signal from the TIE corrector circuit with the feedback signal and provides an error signal corresponding to the phase difference between the two. This error signal is passed to the loop filter circuit.

Loop Filter - the loop filter is similar to a first order low pass filter with bandwidth of 29 Hz, suitable to provide timing and synchronization for SONET/SDH network interface cards.

Detected REF Frequency	Loop Filter Bandwidth
2 kHz	14 Hz
8 kHz, 1.544 MHz, 2.048 MHz, 8.192 MHz, 16.384 MHz, 19.44 MHz	29 Hz

Table 1 - Loop Filter Bandwidth Settings

Digitally Controlled Oscillator (DCO) - the DCO receives the limited and filtered signal from the Loop Filter, and based on its value, generates a corresponding digital output signal. The synchronization method of the DCO is dependent on the state of the ZL30108.

In Normal Mode, the DCO provides an output signal which is frequency and phase locked to the selected input reference signal.

In the Automatic Holdover mode, the DCO is free running at a frequency equal to the frequency that the DCO was generating in Normal Mode. The frequency in the Automatic Holdover mode is calculated from frequency samples stored 26 ms to 52 ms before the ZL30108 entered the Automatic Holdover mode. This ensures that the coarse frequency monitor and the single cycle monitor have time to disqualify a bad reference before it corrupts the holdover frequency.

In Freerun Mode, the DCO is free running with an accuracy equal to the accuracy of the OSCi 20 MHz source.

Lock Indicator - the lock detector monitors if the output value of the phase detector is within the phase-lock-window for a certain time. The selected phase-lock-window guarantees the stable operation of the LOCK pin with maximum network jitter and wander on the reference input. If the DPLL goes into the Automatic Holdover mode, the LOCK pin will initially stay high for 0.1 s. If at that point the DPLL is still in the Automatic Holdover mode, the LOCK pin will go low. In Freerun mode the LOCK pin will go low immediately.

4.5 Frequency Synthesizers

The output of the DCO is used by the frequency synthesizers to generate the output clocks and frame pulses which are synchronized to one of the input references (REF0 or REF1).

The frequency synthesizer uses digital techniques to generate output clocks and advanced noise shaping techniques to minimize the output jitter. The clock and frame pulse outputs have limited drive capability and should be buffered when driving high capacitance loads.

4.6 State Machine

As shown in Figure 1, the state machine controls the TIE Corrector Circuit and the DPLL. The control of the ZL30108 is based on the input MODE_SEL.

4.7 Master Clock

The ZL30108 can use either a clock or crystal as the master timing source. For recommended master timing circuits, see the Applications - Master Clock section.

5.0 Control and Modes of Operation

5.1 Out of Range Selection

The frequency out of range limits for the precise frequency monitoring in the reference monitors are selected by the OOR_SEL pin, see Table 2.

OOR_SEL	Out Of Range Limits
0	40 - 52 ppm
1	64 - 83 ppm

Table 2 - Out of Range Limits Selection

5.2 Modes of Operation

The ZL30108 has two possible manual modes of operation; Normal and Freerun. These modes are selected with mode select pins MODE_SEL as is shown in Table 3. Transitioning from one mode to the other is controlled externally.

MODE_SEL	Mode
0	Normal (with automatic Holdover)
1	Freerun

Table 3 - Operating Modes

5.2.1 Freerun Mode

Freerun mode is typically used when an independent clock source is required, or immediately following system power-up before network synchronization is achieved.

In Freerun mode, the ZL30108 provides timing and synchronization signals which are based on the master clock frequency (supplied to OSCi pin) only, and are not synchronized to the reference input signals.

The accuracy of the output clock is equal to the accuracy of the master clock (OSCi). So if a ±32 ppm output clock is required, the master clock must also be ±32 ppm. See Applications - Section 7.2, “Master Clock“.

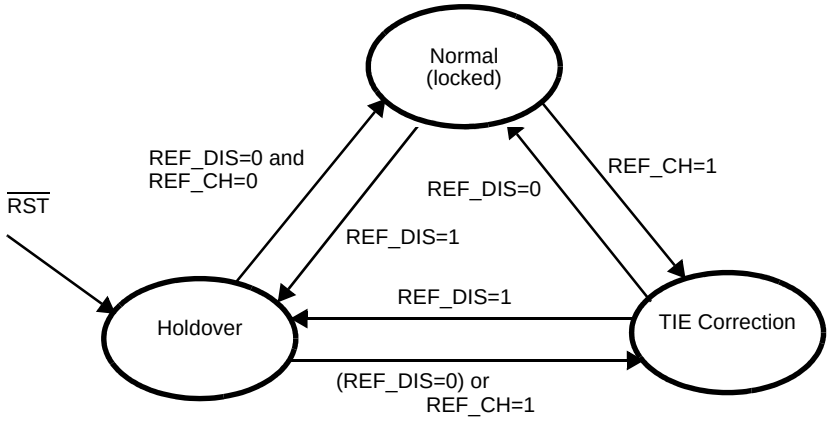
5.2.2 Normal Mode

Normal mode is typically used when a system clock source, synchronized to the network or a backplane is required. In Normal mode, the ZL30108 provides timing and frame synchronization signals, which are synchronized to one of two reference inputs (REF0 or REF1). The input reference signal may have a nominal frequency of 2 kHz, 8 kHz, 1.544 MHz, 2.048 MHz, 8.192 MHz, 16.384 MHz or 19.44 MHz. The frequency of the reference inputs are automatically detected by the reference monitors.

When the Normal mode is selected through the MODE_SEL pin, the ZL30108 will automatically go into the Automatic Holdover mode if the currently selected reference is disrupted (see Figure 9). After the power up reset, the ZL30108 will initially go into the Automatic Holdover mode, generating clocks with the same accuracy as it would be in the Freerun mode. If the currently selected reference is not disrupted (see Figure 3), the state machine takes the DPLL out of the Automatic Holdover mode. The transition is done through the TIE correction state and the current phase offset of the output signals to the input reference is maintained.

If the current reference experiences an disruption while the device is in Normal mode, the device will go automatically into Automatic Holdover mode. It will return to Normal mode as soon as the reference is valid again.

If the reference selection changes because the value of the REF_SEL pin change the ZL30108 goes into Automatic Holdover mode and returns to Normal mode through the TIE correction state.



REF_DIS=1: Current selected reference disrupted (see Figure 3)

REF_CH= 1: Reference change, a transition in the reference selection (a change in the REF_SEL pin).

Figure 9 - Mode Switching in Normal Mode

Automatic Holdover Mode

Automatic Holdover mode is typically used for short durations while system synchronization is temporarily disrupted.

In Automatic Holdover mode, the ZL30108 provides timing and synchronization signals, which are not locked to an external reference signal, but are based on storage techniques. The storage value is determined while the device is in Normal Mode and locked to an external reference signal.

When in Normal Mode, and locked to the input reference signal, a numerical value corresponding to the ZL30108 output reference frequency is stored alternately in two memory locations every 26 ms. When the device is switched into Automatic Holdover mode, the value in memory from between 26 ms and 52 ms is used to set the output frequency of the device. The frequency accuracy of Automatic Holdover mode is 0.01 ppm.

Two factors affect the accuracy of Automatic Holdover mode. One is drift on the master clock while in Automatic Holdover mode, drift on the master clock directly affects the Automatic Holdover mode accuracy. Note that the absolute master clock (OSCi) accuracy does not affect Holdover accuracy, only the *change* in OSCi accuracy while in Holdover. For example, a ±32 ppm master clock may have a temperature coefficient of ±0.1 ppm per °C. So a ±10 °C change in temperature, while the ZL30108 is in the Automatic Holdover mode may result in an additional offset (over the 0.01 ppm) in frequency accuracy of ±1 ppm, which is much greater than the 0.01 ppm of the ZL30108. The other factor affecting the accuracy is large jitter on the reference input prior (26 ms to 52 ms) to the mode switch.

5.3 Reference Selection

The active reference input (REF0 or REF1) is selected by the REF_SEL pin as shown in Table 4. If the logic value of the REF_SEL pin is changed when the DPLL is in Normal mode, the ZL30108 will perform a hitless reference switch.

REF_SEL (input pin)	**Input Reference Selected**
0	REF0
1	REF1

Table 4 - Manual Reference Selection

When the REF_SEL inputs are used to force a change from the currently selected reference to another reference, the action of the LOCK output will depend on the relative frequency and phase offset of the old and new references. Where the new reference has enough frequency offset and/or TIE-corrected phase offset to force the output outside the phase-lock-window, the LOCK output will de-assert, the lock-qualify timer is reset, and LOCK will stay de-asserted for the full lock-time duration. Where the new reference is close enough in frequency and TIE-corrected phase for the output to stay within the phase-lock-window, the LOCK output will remain asserted through the reference-switch process.

6.0 Measures of Performance

The following are some PLL performance indicators and their corresponding definitions.

6.1 Jitter Generation (Intrinsic Jitter)

Timing jitter is defined as the high frequency variation of the clock edges from their ideal positions in time. Wander is defined as the low-frequency variation of the clock edges from their ideal positions in time. High and low frequency variation imply phase oscillation frequencies relative to some demarcation frequency. (Often 10 Hz or 20 Hz for DS1 or E1, higher for SONET/SDH clocks.) Jitter parameters given in this data sheet are total timing jitter numbers, not cycle-to-cycle jitter.

6.2 Jitter Tolerance

Jitter tolerance is a measure of the ability of a PLL to operate properly (i.e., remain in lock and or regain lock in the presence of large jitter magnitudes at various jitter frequencies) when jitter is applied to its reference. The applied jitter magnitude and jitter frequency depends on the applicable standards.

6.3 Jitter Transfer

Jitter transfer or jitter attenuation refers to the magnitude of jitter at the output of a device for a given amount of jitter at the input of the device. Input jitter is applied at various amplitudes and frequencies, and output jitter is measured with various filters depending on the applicable standards. For the ZL30108, the internal low pass loop filter determines the jitter attenuation.

Since intrinsic jitter is always present, jitter attenuation will appear to be lower for small input jitter signals than for large ones. Consequently, accurate jitter transfer function measurements are usually made with large input jitter signals (for example 75% of the specified maximum tolerable input jitter).

6.4 Frequency Accuracy

Frequency accuracy is defined as the absolute accuracy of an output clock signal when it is not locked to an external reference, but is operating in a free running mode. For the ZL30108, the Freerun accuracy is equal to the master clock (OSCi) accuracy.

6.5 Holdover Accuracy

Holdover accuracy is defined as the absolute frequency accuracy of an output clock signal, when it is not locked to an external reference signal, but is operating using storage techniques. For the ZL30108, the storage value is determined while the device is in Normal Mode and locked to an external reference signal.

6.6 Capture Range

Also referred to as pull-in range. This is the input frequency range over which the PLL must be able to pull into synchronization. The ZL30108 capture range is equal to ±130 ppm minus the accuracy of the master clock (OSCi). For example, a +32 ppm master clock results in a capture range of +162 ppm on one side and -98 ppm on the other side of frequency range.

6.7 Lock Range

This is the input frequency range over which the synchronizer must be able to maintain synchronization. The lock range is equal to the capture range for the ZL30108.

6.8 Time Interval Error (TIE)

TIE is the time delay between a given timing signal and an ideal timing signal.

6.9 Maximum Time Interval Error (MTIE)

MTIE is the maximum peak to peak delay between a given timing signal and an ideal timing signal within a particular observation period.

6.10 Phase Continuity

Phase continuity is the phase difference between a given timing signal and an ideal timing signal at the end of a particular observation period. Usually, the given timing signal and the ideal timing signal are of the same frequency. Phase continuity applies to the output of the PLL after a signal disturbance due to a reference switch or a mode change. The observation period is usually the time from the disturbance, to just after the synchronizer has settled to a steady state.

6.11 Phase Lock Time

This is the time it takes the PLL to phase lock to the input signal. Phase lock occurs when the input signal and output signal are aligned in phase with respect to each other within a certain phase distance (not including jitter). Lock time is affected by many factors which include:

- initial input to output phase difference
- initial input to output frequency difference
- PLL loop filter bandwidth
- in-lock phase distance

The presence of input jitter makes it difficult to define when the PLL is locked as it may not be able to align its output to the input within the required phase distance, dependent on the PLL bandwidth and the input jitter amplitude and frequency.

Although a short lock time is desirable, it is not always possible to achieve due to other synchronizer requirements. For instance, better jitter transfer performance is achieved with a lower frequency loop filter which increases lock time. See Section 8.2, “Performance Characteristics“ for Maximum Phase Lock Time.

7.0 Applications

This section contains ZL30108 application specific details for power supply decoupling, clock and crystal operation, reset operation,and control operation.

7.1 Power Supply Decoupling

Jitter levels on the ZL30108 output clocks may increase if the device is exposed to excessive noise on its power pins. For optimal jitter performance, the ZL30108 device should be isolated from noise on power planes connected to its 3.3 V and 1.8 V supply pins. For recommended common layout practices, refer to Zarlink Application Note ZLAN-178.

7.2 Master Clock

The ZL30108 can use either a clock or crystal as the master timing source. Zarlink Application Note ZLAN-68 lists a number of applicable oscillators and crystals that can be used with the ZL30108.

7.2.1 Clock Oscillator

When selecting a Clock Oscillator, numerous parameters must be considered. These includes absolute frequency, frequency change over temperature, output rise and fall times, output levels, duty cycle and phase noise.

1	Frequency	20 MHz
2	Tolerance	As required
3	Rise & Fall Time	<10 ns
4	Duty Cycle	40% to 60%

Table 5 - Typical Clock Oscillator Specification

The output clock should be connected directly (not AC coupled) to the OSCi input of the ZL30108 and the OSCo output should be left open as shown in Figure 10.

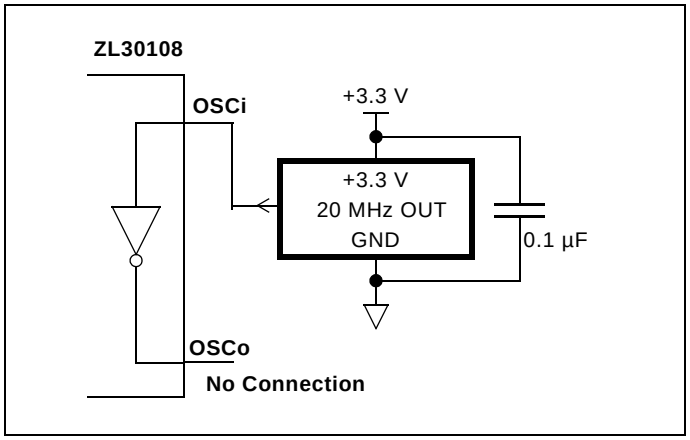


Figure 10 - Clock Oscillator Circuit

7.2.2 Crystal Oscillator

Alternatively, a Crystal Oscillator may be used. A complete oscillator circuit made up of a crystal, resistor and capacitors is shown in Figure 11.

The accuracy of a crystal oscillator depends on the crystal tolerance as well as the load capacitance tolerance. Typically, for a 20 MHz crystal specified with a 32 pF load capacitance, each 1 pF change in load capacitance contributes approximately 9 ppm to the frequency deviation. Consequently, capacitor tolerances and stray capacitances have a major effect on the accuracy of the oscillator frequency.

The crystal should be a fundamental mode type - not an overtone. The fundamental mode crystal permits a simpler oscillator circuit with no additional filter components and is less likely to generate spurious responses. The crystal specification is as follows.

1	Frequency	20 MHz
2	Tolerance	As required
3	Oscillation Mode	Fundamental
4	Resonance Mode	Parallel
5	Load Capacitance	As required
6	Maximum Series Resistance	50 Ω

Table 6 - Typical Crystal Oscillator Specification

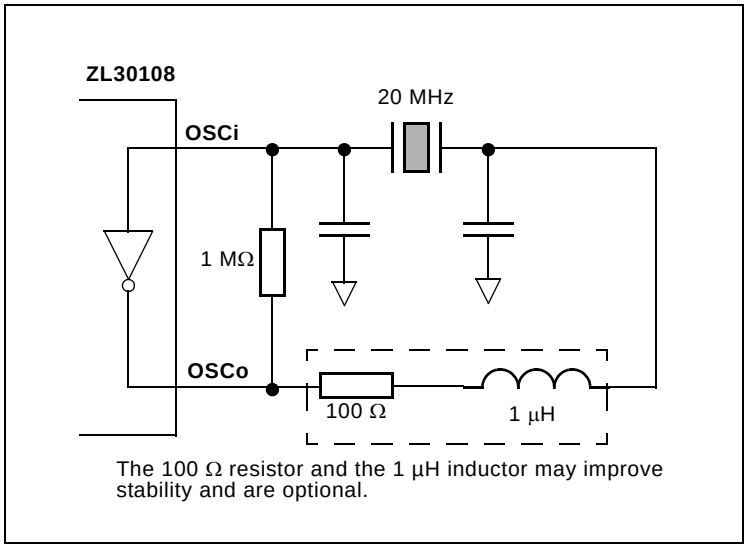


Figure 11 - Crystal Oscillator Circuit

7.3 Power Up Sequence

The ZL30108 requires that the 3.3 V is not powered after the 1.8 V. This is to prevent the risk of latch-up due to the presence of parasitic diodes in the IO pads.

Two options are given:

1. Power-up 3.3 V first, 1.8 V later
2. Power up 3.3 V and 1.8 V simultaneously ensuring that the 3.3 V power is never lower than 1.8 V minus a few hundred millivolts (e.g., by using a schottky diode or controlled slew rate)

7.4 Reset Circuit

A simple power up reset circuit with about a 60 µs reset low time is shown in Figure 12. Resistor R_P is for protection only and limits current into the $\overline{RST}$ pin during power down conditions. The reset low time is not critical but should be greater than 300 ns.

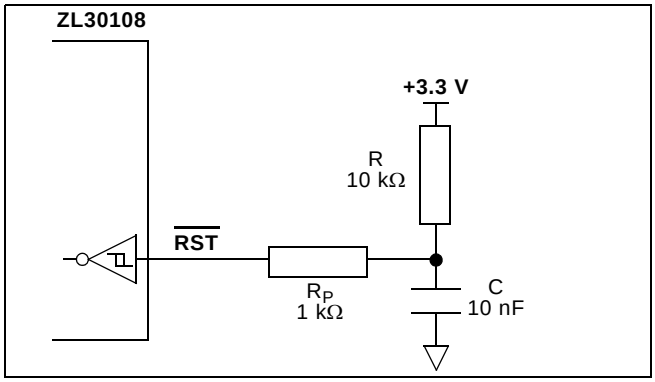


Figure 12 - Power-Up Reset Circuit

8.0 Characteristics

8.1 AC and DC Electrical Characteristics

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Supply voltage	V_{DD_R}	-0.5	4.6	V
2	Core supply voltage	V_{CORE_R}	-0.5	2.5	V
3	Voltage on any digital pin	V_{PIN}	-0.5	6	V
4	Voltage on OSCi and OSCo pin	V_{OSC}	-0.3	V_{DD} + 0.3	V
5	Current on any pin	I_{PIN}		30	mA
6	Storage temperature	T_{ST}	-55	125	°C
7	Package power dissipation	P_{PD}		195	mW
8	ESD rating	V_{ESD}		2k	V

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
* Voltages are with respect to ground (GND) unless otherwise stated.

Recommended Operating Conditions*

	Characteristics	Sym.	Min.	Typ.	Max.	Units
1	Supply voltage	V_{DD}	2.97	3.30	3.63	V
2	Core supply voltage	V_{CORE}	1.62	1.80	1.98	V
3	Operating temperature	T_A	-40	25	85	°C

* Voltages are with respect to ground (GND) unless otherwise stated.

DC Electrical Characteristics*

	Characteristics	Sym.	Min.	Max.	Units	Notes
1	Supply current with: OSCi = 0 V	I_{DDS}	2.5	7.0	mA	outputs loaded with 30 pf
2	OSCi = Clock	I_{DD}		43	mA	Outputs unloaded
3	Core supply current with: OSCi = 0 V	I_{CORES}		20	uA	
4	OSCi = Clock	I_{CORES}		18	mA	
5	Schmitt trigger Low to High threshold point	V_{CIH}	1.43	1.85	V	All device inputs are Schmitt trigger type.
6	Schmitt trigger High to Low threshold point	V_{CIL}	0.8	1.1	V	
7	Input leakage current	I_{IL}	-105	105	µA	V_I=V_{DD} or 0 V

DC Electrical Characteristics*

	Characteristics	Sym.	Min.	Max.	Units	Notes
8	High-level output voltage	V_{OH}	2.4		V	I_{OH} = 8 mA for clock and frame-pulse outputs, 4 mA for status outputs
9	Low-level output voltage	V_{OL}		0.4	V	I_{OL} = 8 mA for clock and frame-pulse outputs, 4 mA for status outputs

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Voltages are with respect to ground (GND) unless otherwise stated.

AC Electrical Characteristics* - Timing Parameter Measurement Voltage Levels (see Figure 13).

	Characteristics	Sym.	CMOS	Units
1	Threshold Voltage	V_T	1.5	V
2	Rise and Fall Threshold Voltage High	V_{HM}	2.0	V
3	Rise and Fall Threshold Voltage Low	V_{LM}	0.8	V

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Voltages are with respect to ground (GND) unless otherwise stated.

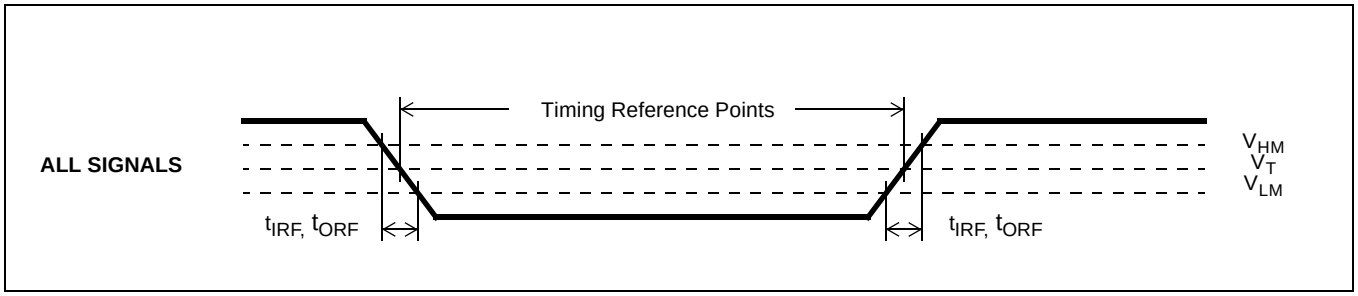


Figure 13 - Timing Parameter Measurement Voltage Levels.

AC Electrical Characteristics* - Input timing for REF0 and REF1 references (see Figure 14).

	Characteristics	Symbol	Min.	Typ.	Max.	Units
1	2 kHz reference period	t_{REF2kP}	483	500	516	µs
2	8 kHz reference period	t_{REF8kP}	120	125	128	µs
3	1.544 MHz reference period	$t_{REF1.5P}$	338	648	950	ns
4	2.048 MHz reference period	t_{REF2P}	263	488	712	ns
5	8.192 MHz reference period	t_{REF8P}	63	122	175	ns
6	16.384 MHz reference period	t_{REF16P}	38	61	75	ns
7	19.44 MHz reference period	t_{REF8kP}	38	51	75	ns
8	reference pulse width high or low	t_{REFW}	15			ns

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Period Min/Max values are the limits to avoid a single-cycle fault detection. Short-term and long-term average periods must be within Out-of-Range limits.

AC Electrical Characteristics* - Input to output timing for REF0 and REF1 references (see Figure 14).

	Characteristics	Symbol	Min.	Max.	Units
1	2 kHz reference input to F2ko delay	t_{REF2kD}	0	1.2	ns
2	2 kHz reference input to F8ko delay	t_{REF2k_F8kD}	-27.2	-26.5	ns
3	8 kHz reference input to F8ko delay	t_{REF8kD}	-0.3	2	ns
4	1.544 MHz reference input to F8ko delay	$t_{REF1.5\_F8kD}$	-1.1	0.9	ns
5	2.048 MHz reference input to F8ko delay	t_{REF2_F8kD}	-1.1	0.9	ns
6	8.192 MHz reference input to F8ko delay	t_{REF8_F8kD}	-0.6	0.8	ns
7	16.384 MHz reference input to F8ko delay	t_{REF16_F8kD}	29.0	30.6	ns
8	19.44 MHz reference input to C19o delay	t_{REF19D}	0.2	1.1	ns
9	19.44 MHz reference input to F8ko delay	t_{REF19_F8kD}	-1.7	1	ns

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

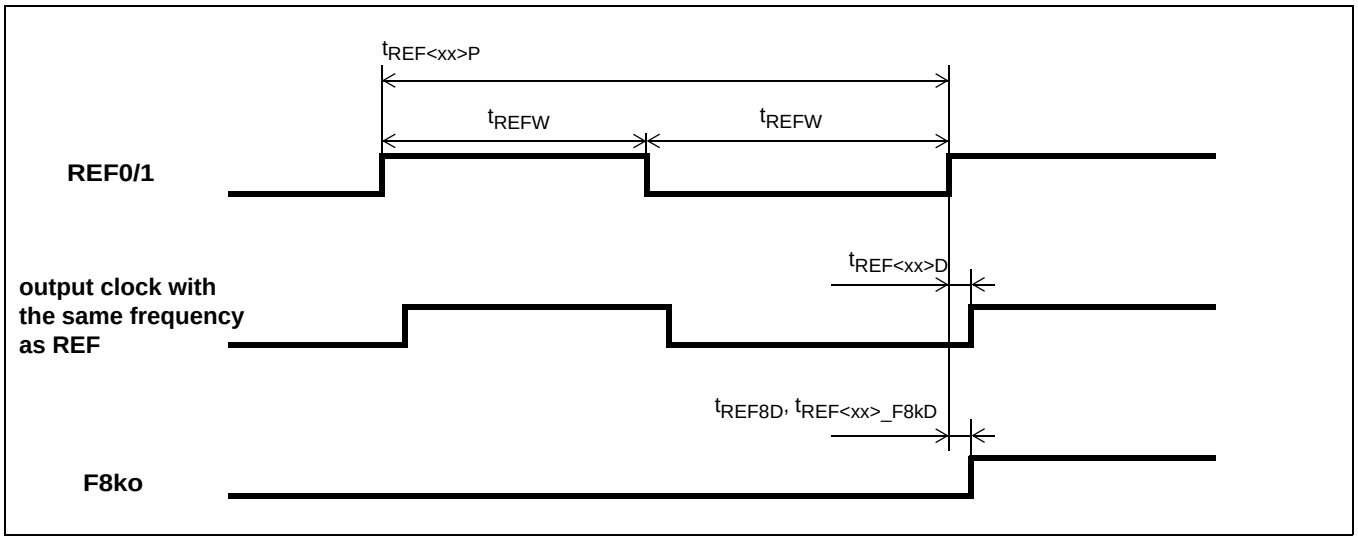


Figure 14 - Input to Output Timing

AC Electrical Characteristics* - Output Timing (see Figure 15).

	Characteristics	Sym.	Min.	Max.	Units
1	C19o delay	t_{C19D}	-1.0	0.5	ns
2	C19o pulse width low	t_{C19L}	25.0	25.8	ns
3	F2ko delay	t_{F2kD}	25.0	26.6	ns
4	F2ko pulse width high	t_{F2kH}	51.1	52	ns
5	F8ko pulse width high	t_{F8kH}	30.0	31.8	ns
7	Output clock and frame pulse rise or fall time (with 30 pF load)	t_{ORF}	1.1	2.3	ns

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

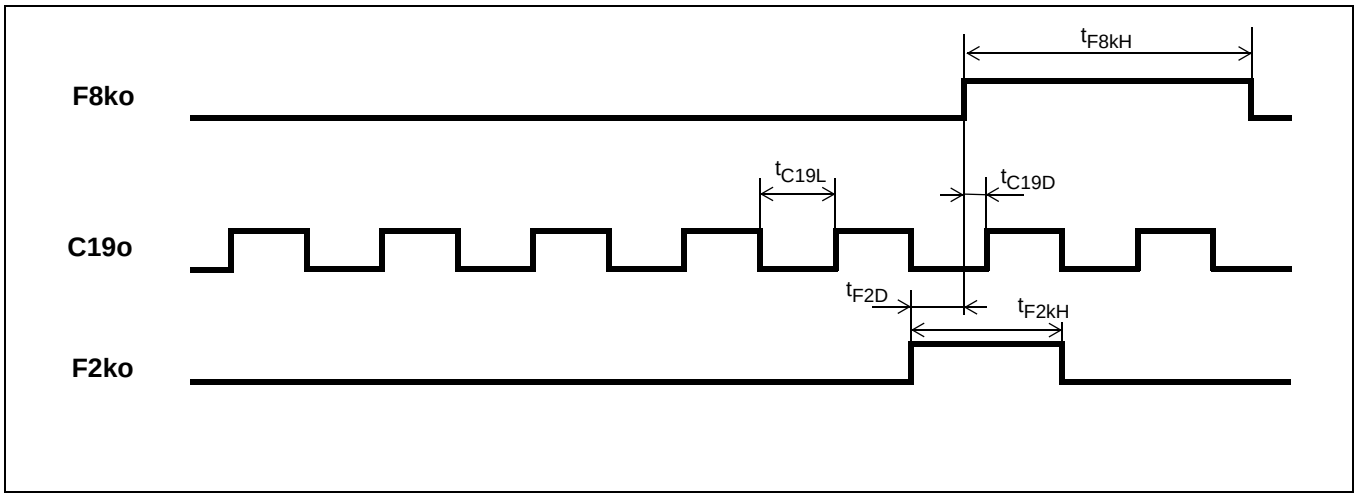


Figure 15 - SONET/SDH Output Timing Referenced to F8ko

AC Electrical Characteristics* - OSCi 20 MHz Master Clock Input

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Oscillator Tolerance		-20		+20	ppm	OOR_SEL=0
2			-32		+32	ppm	OOR_SEL=1
4	Duty cycle		40		60	%	
5	Rise time				10	ns	
6	Fall time				10	ns	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

8.2 Performance Characteristics

Performance Characteristics* - Functional

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Holdover accuracy		0.01		ppm	
2	Holdover stability		NA		ppm	Determined by stability of the 20 MHz Master Clock oscillator
3	Capture range	-130		+130	ppm	The 20 MHz Master Clock oscillator set at 0.ppm
4	Reference Out of Range Threshold (including hysteresis)	-64 -83		+64 +83	ppm	The 20 MHz Master Clock oscillator set at 0 ppm and OOR_SEL=1
6		-40 -52		+40 +52	ppm	The 20 MHz Master Clock oscillator set at 0 ppm and OOR_SEL=0
Lock Time						
7	14 Hz Filter			1.5	s	input reference = 2 kHz, ±100 ppm frequency offset, TIE_CLR=1
8	29 Hz Filter			1	s	input reference ≠ 2 kHz, ±100 ppm frequency offset, TIE_CLR=1
Output Phase Continuity (MTIE)						
11	Reference switching		13		ns	
12	Switching from Normal mode to Automatic Holdover mode		0		ns	
13	Switching from Automatic Holdover mode to Normal mode		13		ns	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

Performance Characteristics*: Measured Output Jitter - GR-253-CORE and T1.105.03 conformance

	Signal	Telcordia GR-253-CORE and ANSI T1.105.03 Jitter Generation Requirements			ZL30108 Maximum Jitter Generation	Units
		Jitter Measurement Filter	Limit in UI (1 UI = 6.4 ns)	Equivalent limit in time domain		
OC-3 Interface						
1	C19o	65 kHz to 1.3 MHz	0.15 UI_{pp}	0.96	0.22	ns_{pp}
2		12 kHz to1.3 MHz (Category II)	0.1 UI_{pp}	0.64	0.22	ns_{pp}
			0.01 UI_{rms}	64	24	ps_{rms}
3		500 Hz to 1.3 MHz	1.5 UI_{pp}	9.65	0.22	ns_{pp}

* Supply voltage and operating temperature are as per Recommended Operating Conditions

Performance Characteristics*: Measured Output Jitter - G.813 conformance (Option 1 and Option 2

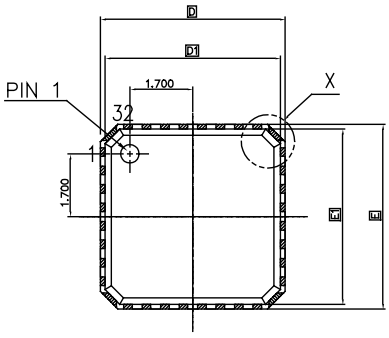
	Signal	ITU-T G.813 Jitter Generation Requirements			ZL30108 Maximum Jitter Generation	Units
		Jitter Measurement Filter	Limit in UI (1 UI = 6.4 ns)	Equivalent limit in time domain		
STM-1 Option 1 Interface						
1	C19o	65 kHz to 1.3 MHz	0.1 UI_{pp}	0.64	0.22	ns_{pp}
2		500 Hz to 1.3 MHz	0.5 UI_{pp}	3.22	0.22	ns_{pp}
STM-1 Option 2 Interface						
3	C19o	12 kHz to1.3 MHz	0.1 UI_{pp}	0.64	0.22	ns_{pp}

* Supply voltage and operating temperature are as per Recommended Operating Conditions

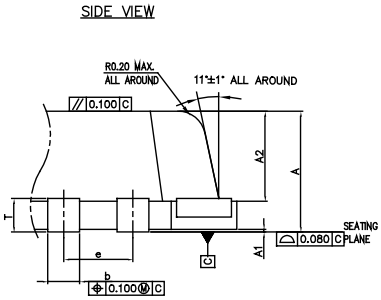
Performance Characteristics* - Unfiltered Intrinsic Jitter

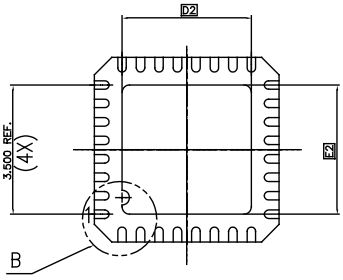
	Signal	Max. [ns_{pp}]	Notes
1	C19o (19.44 MHz)	0.5	
2	F8ko (8 kHz)	0.5	
3	F2ko (2 kHz)	0.5	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.



TOP VIEW

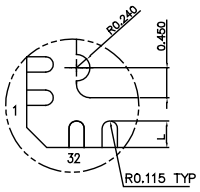




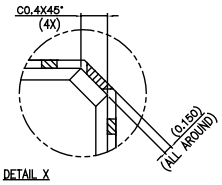
BOTTOM VIEW

S/N	SYM	DIMENSIONS	REMARKS
1	A	0.850±0.050	OVERALL HEIGHT
2	A1	0.025±0.020	STANDOFF
3	A2	0.650±0.050	CAVITY THICKNESS
4	D	5.000±0.100	PKG. LENGTH
5	D1	4.750±0.100	CAVITY LENGTH
6	D2	3.500±0.050	EXPOSED PAD LENGTH
7	E	5.000±0.100	PKG. WIDTH
8	E1	4.750±0.100	CAVITY WIDTH
9	E2	3.500±0.050	EXPOSED PAD WIDTH
10	L	0.400±0.100	FOOT LENGTH
11	T	0.190~0.245	FRAME THICKNESS
12	b	0.230 $^{+0.070}_{-0.050}$	LEAD WIDTH
13	e	0.500 BASE	LEAD PITCH

COMPLIANT TO JEDEC STANDARD: MO-220



DETAIL B



DETAIL X

NOTES:

1. DIMENSIONS & TOLERANCES CONFORM TO ASME Y14.5M, – 1994
2. PIN 1 IDENTIFIER MUST BE ON THE TOP SURFACE OF THE PACKAGE USING AN INDENTATION OR OTHER FEATURE OF THE PACKAGE BODY
3. ALL DIMENSIONS ARE IN MILLIMETERS.
4. PACKAGE WARPAGE MAX 0.08 mm.
5. NOT TO SCALE.
6. DRAWING DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION

ISSUE	1	2	3	
ACN	CDCA	CDCA	CDCA	
DATE	30-01-2004	15-08-2005	22-08-2005	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

Package Code LD

Package Outline for Stamped 32 lead QFN (5 x 5mm), 3.7mm DAP (Die Attach Pad)

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