

## M21408/M21418/M21428 SD, HD/SD and 2xHD-SDI Cable Drivers

The M21408, M21418 and M21428 are high-speed, low-power, low-jitter cable drivers. They are designed to drive serial digital video data through 75Ω coaxial cable typically used in SMPTE and DVB-ASI video applications. The M21428 cable driver is optimized for performance from 143 Mbps up to 2970 Mbps, the M21418 cable driver is optimized for performance from 143 Mbps up to 1485 Mbps. Both the M21428 and M21418 have selectable slew rates for SD-SDI and HD-SDI applications. The M21408 cable driver is optimized for performance from 143 Mbps up to 540 Mbps with SD-SDI slew rates.

The typical output rise/fall time of the M21428 is 100 ps for HD and 2xHD rates, the typical output rise/fall time of the M21418 is 100 ps for HD rates. All devices have a typical set slew rate of 600 ps at SD rates. The default output voltage swing is compliant with SMPTE 292M, 259M, 344M and 424M using a 750Ω ±1% resistor. The M21408, M21418 and M21428 are pin compatible, with the exception that the M21408 has no SD/HD control pin. M21408/M21418/M21428 support a maximum single ended output swing of 1600 mVp-p, when configured appropriately.

All devices are packaged in a new high performance 3x3 mm MLF package to simplify the PCB and reduce package parasitics with resulting improvements in Output Return Loss (ORL). Both devices are available in an RoHS compliant package, that is backwards compatible with standard JEDEC SnPb processes.

### Applications

- Serial Routing Switchers,
- Production/Master Control Switchers
- Distribution Amplifiers
- Video Tape Recorders, ENG Edit decks, Cameras
- Broadcast video applications
- NLE's, MPEG Encoders/Decoders, format convertors etc.

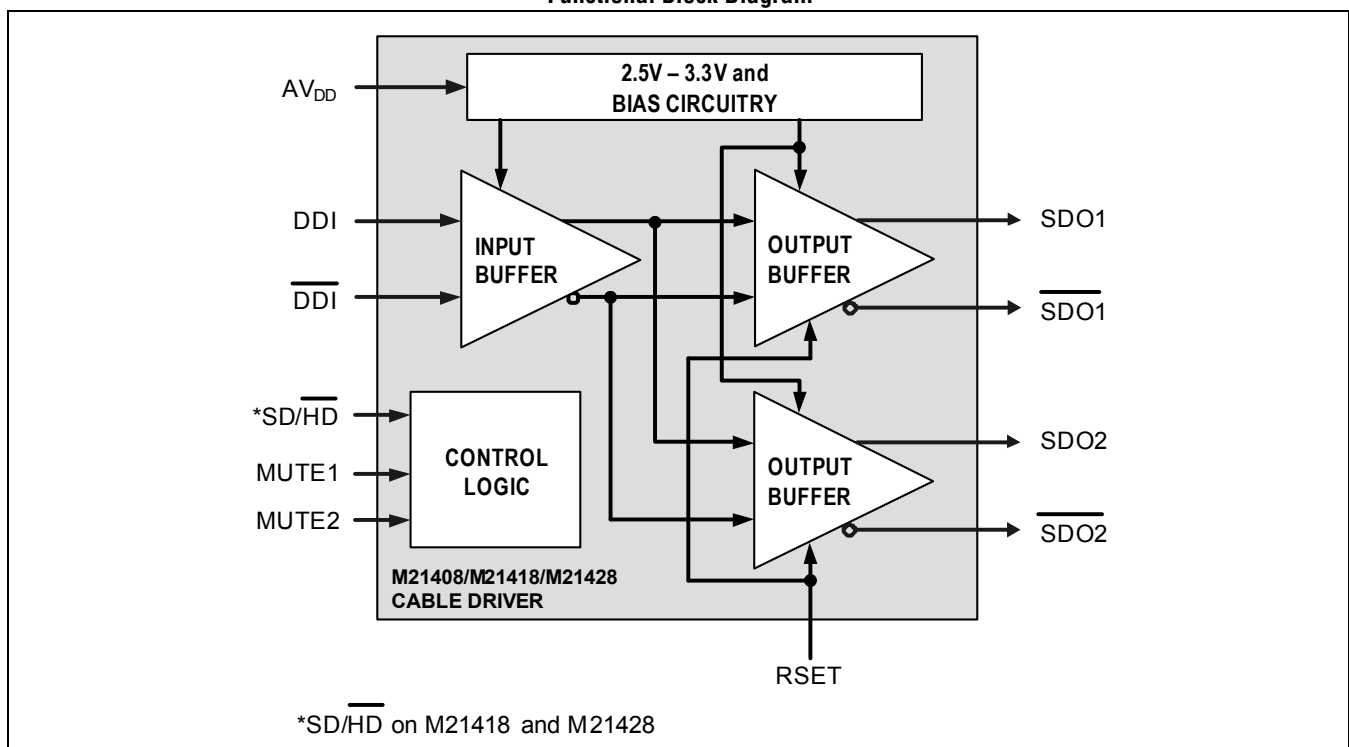
### Standards Compliance

- SMPTE 292M, 259M, 344M, 424M (only M21428 complies with 424M)
- DVB-ASI

### Features

- 2xHD, HD and SD operation (M21428),
- HD and SD operation (M21418)
- SD operation (M21408)
- Dual Differential outputs, with individual mute control
- 800 mVp-p single ended output swing (typical)
- 1600 mVp-p maximum single ended output swing
- SD/HD Slew Rate control
- 2.5V or 3.3V Supply
- Low P<sub>DISS</sub> (122 mW @ 2.5V, 144 mW @ 3.3V)
- Extended temp. range: -10 to 85°C
- RoHS package

Functional Block Diagram



## Ordering Information

| Part Number | Data Rates Supported | Package                            | Operating Temperature |
|-------------|----------------------|------------------------------------|-----------------------|
| M21408G-xx* | 143–540 Mbps         | 3x3 mm MLF—16pins (RoHS compliant) | -10 °C to 85 °C       |
| M21418G-xx* | 143–1485 Mbps        | 3x3 mm MLF—16pins (RoHS compliant) | -10 °C to 85 °C       |
| M21428G-xx* | 143–2970 Mbps        | 3x3 mm MLF—16pins (RoHS compliant) | -10 °C to 85 °C       |

**NOTES:**

\* Consult the price list for exact part number when ordering.

\* The letter 'G' designator after the part number indicates a RoHS-compliant package. Refer to [www.mindspeed.com](http://www.mindspeed.com) for additional information.

## Revision History

| Revision | Level   | Date          | Description   |
|----------|---------|---------------|---|
| D        | Release | May 2007      | Modified text in <a href="#">Section 1.1.2</a> to indicate that RSET must be used.<br>SD/HD changed to pull-up in <a href="#">Table 1-5</a> . |
| C        | Release | February 2007 | Updated ordering information.<br>Minor updates to <a href="#">Tables 2-3, 2-6, 2-7, and 2-8</a> .   |
| B        | Release | February 2007 | Production Release<br>M21428 added.<br>Characterization data added to <a href="#">Tables 2-3, 2-6, 2-7, and 2-8</a> .                         |
| A        | Advance | April 2006    | Initial Release.  |



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# 1.0 Functional Description

## 1.1 Features

### 1.1.1 HD-SDI and SD-SDI Slew-rate Selection

The output slew rate of the M21418 and M21428 are selectable to conform with the different SD-SDI and HD-SDI specifications, in the case of the M21428 this includes 2xHD-SDI. With  $\overline{\text{SD/HD}}$  = Low, rise/fall time is typically 100 ps. The slew rate will vary depending on the output matching network and connector used.

With  $\overline{\text{SD/HD}}$  = High, for standard definition (143 to 540 Mbps) applications, the rise/fall time is typically 600 ps, which is compliant with SMPTE 259M and SMPTE 344M. The M21408 has no control over the slew rate, this is set at the SD requirement.

### 1.1.2 Output Amplitude Adjustment

For SMPTE compliance, an external  $750\Omega \pm 1\%$  resistor at **RSET** to **A<sub>VDD</sub>** is recommended for a swing level of 800mV within a tolerance that is less than  $\pm 10\%$  which meets SMPTE requirements. The output amplitude can also be adjusted to range from 500 to 1600 mVpp single ended using the following formula:

$$\text{Output Swing} = (600/\text{RSET}) [\text{RSET in k}\Omega] \text{ (in mVpp, Single Ended)}$$

The actual swing is set as a function of the IC supply voltage, the external termination voltage and the limitations are shown in [Table 1-1](#). For a 2.5V minimum termination voltage, the IC can be SMPTE compliant for all supply voltages. In applications where a lossy matching or splitting networks are used, the M21408/M21418/M21428 offers additional gain of up to 1600 mVpp swings, so the output after the lossy network can be SMPTE compliant.

**Table 1-1. Output Swing vs. Supply and Termination Voltage**

| <b>A<sub>VDD</sub> (V)</b> | <b>A<sub>VDDTERM</sub> (V)</b> | <b>Maximum Swing<br/>(Single-ended mVp-p)</b> | <b>Minimum Swing<br/>(Single-ended mVp-p)</b> |
|----------------------------|--------------------------------|---|---|
| 2.5–3.3V                   | 3.3V                           | 1200 mV                                       | 500 mV  |
| 2.5–3.3V                   | 5.0V                           | 1600 mV                                       | 500 mV  |

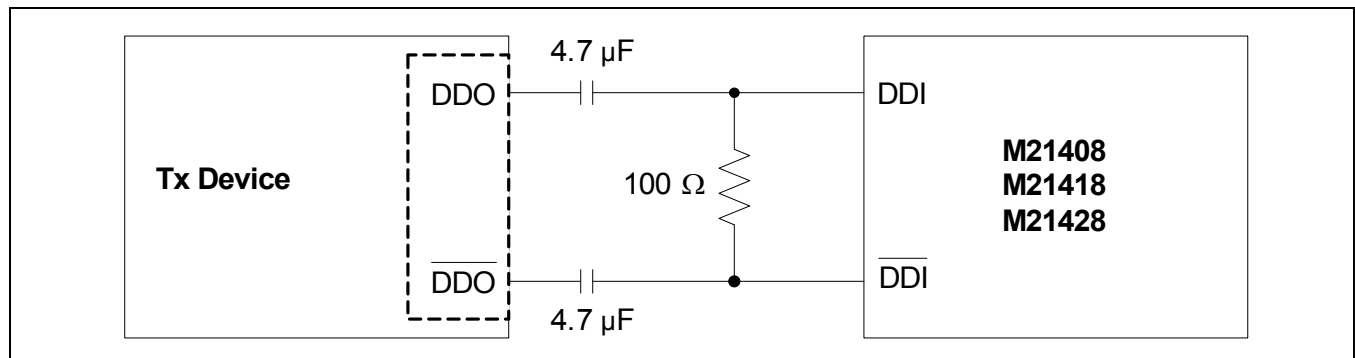
## 1.2 Pin Definitions

### 1.2.1 High-speed Inputs

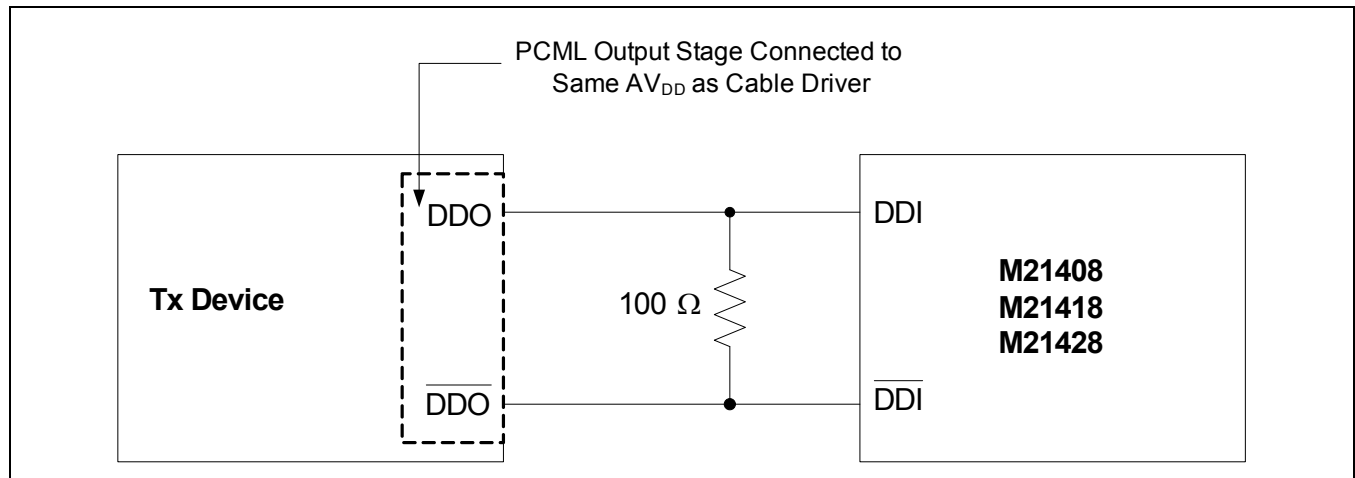
The M21408/M21418/M21428 are designed to be operated with input signals as low as 100 mV or up to 2000 mV differential peak to peak. The M21408/M21418/M21428 uses external 50Ω input termination resistors to match 100Ω differential impedance transmission lines for improved system level performance. The M21408/M21418/M21428 recommended input circuits are shown in [Figure 1-1](#).

Note that AC coupling is not required when the M21408/M21418/M21428 are driven by Mindspeed Broadcast video devices.

**Figure 1-1. Typical Input Circuit—AC Coupled**



**Figure 1-2. Typical Input Circuit—DC Coupled**

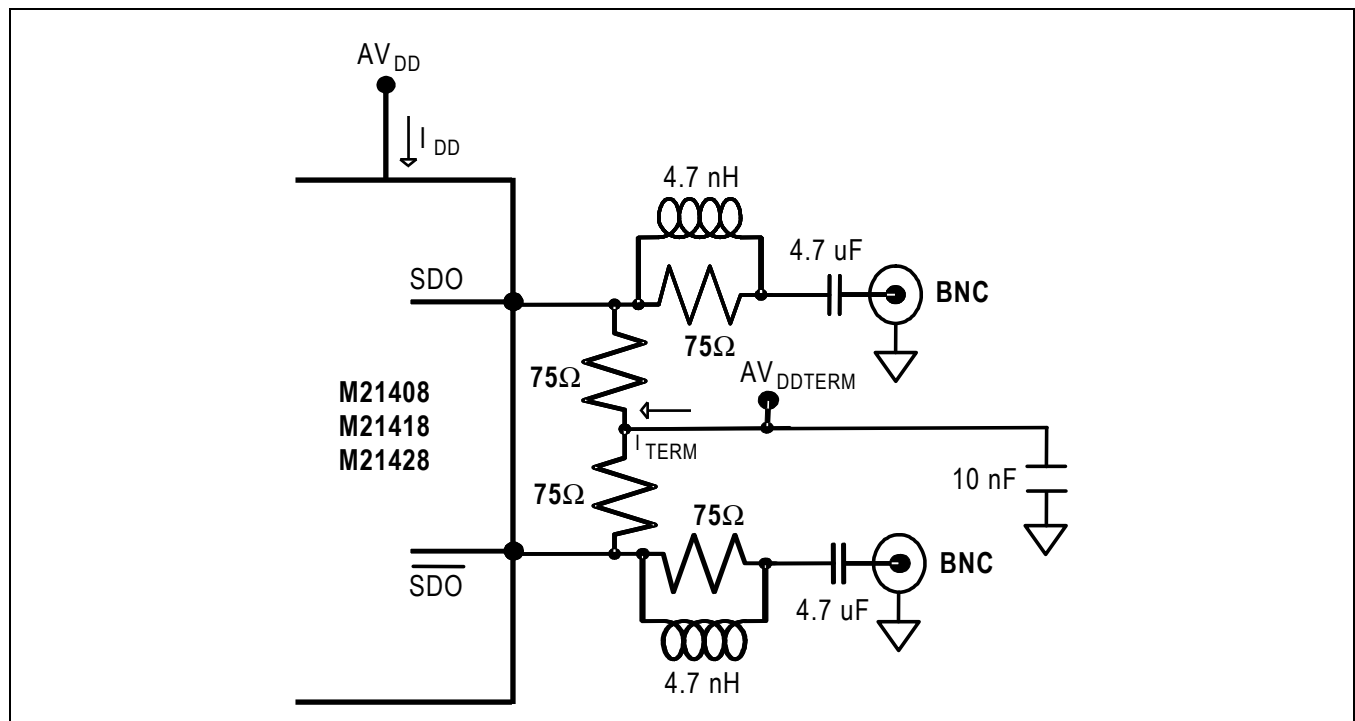


### 1.2.2 High-speed Outputs

The M21408/M21418/M21428 output buffer is an open collector buffer that is designed for a return loss of 15 dB at SD and HD rates and 10 dB at 2xHD rates, using standard through-hole BNC connectors as typically employed in broadcast video equipment. A typical output matching circuit is shown in Figure 1-3. The Output Return Loss (ORL) is dependent on many factors such as the value and type of components used, PCB layout, PCB trace lengths, and type of PCB di-electric, therefore, the recommendations in the figure below should be used as starting guidelines only. Different output matching network topologies and different component values will result in different ORL performance.

The M21408/M21418/M21428 has SD-SDI and HD-SDI rise/fall times that are typically faster than the legacy cable driver devices but within the relevant SMPTE specification for additional margin in most designs. The faster output slew rate results in a more open eye. The actual maximum output of the part depends on the applied IC voltage as well as the external termination voltage for the load termination. The limitations are discussed in Section 1.1.

Figure 1-3. Typical Output Matching/Back-termination Circuit





### 1.2.3 M21408/M21418/M21428 Pin List

**Table 1-2. Interface Pins**

| Pin Name | Pin # | Function  | Default | Type         |
|----------|-------|---|---------|--------------|
| RSET     | 5     | Input control signal for setting the single-ended output swing amplitude. Higher output swing levels or reduced variations with a ±1% tolerance external resistor. For 800mV <sub>p-p</sub> single-ended, a 750Ω ±1% resistor to AV <sub>DD</sub> is recommended. | —       | Analog Input |

**Table 1-3. Power Pins**

| Pin Name         | Pin #    | Function   | Type  |
|------------------|----------|--|-------|
| AV <sub>SS</sub> | 3, 8, 15 | Chip Ground  | Power |
| AV <sub>DD</sub> | 2, 7     | Positive Supply  | Power |
| NC               | 4        | Not Connected. Leave these pins floating. Do not connect to any supply, ground or logic level. | NC    |

**Table 1-4. High-speed Signal Pins**

| Pin Name           | Pin #  | Function   | Default | Type         |
|--------------------|--------|--|---------|--------------|
| DDI/DD $\bar{I}$   | 16, 1  | Non-inverting and Inverting serial externally terminated inputs.               | —       | I—High-speed |
| SD02/SD $\bar{O}2$ | 11, 10 | Non-inverting and inverting serial unterminated data outputs to coaxial cable. | —       | O—High-speed |
| SD01/SD $\bar{O}1$ | 13, 12 | Non-inverting and inverting serial unterminated data outputs to coaxial cable. | —       | O—High-speed |

**Table 1-5. Control Pins**

| Pin Name                                    | Pin # | Function  | Default   | Type   |
|---|-------|---|-----------|--------|
| MUTE2                                       | 6     | A high mutes SD02/SD $\bar{O}2$ outputs, low enables SD02/SD $\bar{O}2$ .   | Pull-up   | I—CMOS |
| MUTE1                                       | 14    | A high mutes SD01/SD $\bar{O}1$ outputs, low enables SD01, SD $\bar{O}1$ .  | Pull-down | I—CMOS |
| SD/ $\bar{H}D$<br>*(M21418 and M21428 only) | 9     | Input control signal to change the output slew rate.<br>SD/ $\bar{H}D$ = High: Slow output slew rate for SD-SDI rate (143–540 Mbps).<br>SD/ $\bar{H}D$ = Low: Fast output slew rate for HD and 2xHD-SDI rate (1485 Mbps). | Pull-up   | I—CMOS |

**NOTES:**

Internal pull-ups/pull-downs are 100 kΩ.

\* On the M21408 this pin is a NC.



## 2.0 Product Specification

### 2.1 Absolute Maximum Ratings

Table 2-1. Absolute Maximum Ratings

| Symbol       | Parameter                             | Minimum         | Maximum          | Units |
|--------------|---------------------------------------|-----------------|------------------|-------|
| $V_{DD}$     | Power                                 | $AV_{SS} - 0.5$ | $AV_{SS} + 3.47$ | V     |
| $V_{IOAM}$   | Any I/O Pin                           | $AV_{SS} - 0.5$ | $AV_{DD} + 0.5$  | V     |
| $T_{STORE}$  | Storage Temperature                   | -65             | +150             | °C    |
| $ESD_{HBML}$ | Human Body Model (low-speed)          | 2000            | —                | V     |
| $ESD_{HBMH}$ | Human Body Model (high-speed outputs) | 2000            | —                | V     |
| $ESD_{CDM}$  | Charge Device Model                   | 500             | —                | V     |

**NOTE:**  
1. No Damage.

### 2.2 Recommended Operating Conditions

Table 2-2. Recommended Operating Conditions

| Symbol          | Parameter                              | Notes                           | Minimum | Typical | Maximum | Units |
|-----------------|--|---------------------------------|---------|---------|---------|-------|
| $AV_{DD}$       | $AV_{DD}$ Power                        | 1                               | —       | 2.5/3.3 | —       | V     |
| $AV_{SS}$       | $AV_{SS}$ Ground                       | —                               | —       | 0       | —       | V     |
| $T_A$           | Ambient Temperature                    | —                               | -10     | —       | +85     | °C    |
| $\theta_{JA}$   | Junction to ambient Thermal Resistance | 2, 3                            | —       | 75      | —       | °C/W  |
| $AV_{DD\_TERM}$ | 75 $\Omega$ Output Termination Voltage | See <a href="#">Table 1-1</a> . |         |         |         |       |

**NOTES:**  
1.  $\pm 5\%$  is allowed from nominal supply.  
2. Solder exposed underbody paddle with an array of thermal vias to optimize junction to ambient thermal resistance. Refer to Amkor Application Note (see [Section A.2.1](#)).  
3. Mounted on a multi layer board ( $\geq 4$  layers), airflow = 0.0 m/s.

## 2.3 DC Electrical Specifications

**Table 2-3. Power DC Electrical Specifications**

| Symbol         | Parameter  | Notes      | Minimum | Typical | Maximum | Units |
|----------------|--|------------|---------|---------|---------|-------|
| $I_{DD}$       | Supply Current (one output enabled)                        | 1, 2       | —       | 27      | —       | mA    |
| $I_{DD}$       | Supply Current (two outputs enabled)                       | 1, 2       | —       | 48      | —       | mA    |
| $I_{DDTERM}$   | Current in external termination resistors                  | 1, 2, 3    | —       | 22      | —       | mA    |
| $P_{DISSINT1}$ | Power dissipation ( $AV_{DD} = 2.5V, AV_{DDTERM} = 3.3V$ ) | 1, 2, 4, 7 | —       | 122     | —       | mW    |
| $P_{DISSINT2}$ | Power dissipation ( $AV_{DD} = 2.5V, AV_{DDTERM} = 3.3V$ ) | 1, 2, 5, 7 | —       | 156     | —       | mW    |
| $P_{DISSINT1}$ | Power dissipation ( $AV_{DD} = 2.5V, AV_{DDTERM} = 5.0V$ ) | 1, 2, 4, 7 | —       | 159     | —       | mW    |
| $P_{DISSINT2}$ | Power dissipation ( $AV_{DD} = 2.5V, AV_{DDTERM} = 5.0V$ ) | 1, 2, 5, 7 | —       | 194     | —       | mW    |
| $P_{DISSINT1}$ | Power dissipation ( $AV_{DD} = 3.3V, AV_{DDTERM} = 3.3V$ ) | 1, 2, 4, 7 | —       | 144     | —       | mW    |
| $P_{DISSINT2}$ | Power dissipation ( $AV_{DD} = 3.3V, AV_{DDTERM} = 3.3V$ ) | 1, 2, 5, 7 | —       | 195     | —       | mW    |
| $P_{DISSINT1}$ | Power dissipation ( $AV_{DD} = 3.3V, AV_{DDTERM} = 5.0V$ ) | 1, 2, 4, 7 | —       | 181     | —       | mW    |
| $P_{DISSINT2}$ | Power dissipation ( $AV_{DD} = 3.3V, AV_{DDTERM} = 5.0V$ ) | 1, 2, 5, 7 | —       | 232     | —       | mW    |
| $P_{DISSTOT1}$ | Power dissipation ( $AV_{DD} = 2.5V, AV_{DDTERM} = 3.3V$ ) | 1, 2, 4, 6 | —       | 140     | —       | mW    |
| $P_{DISSTOT2}$ | Power dissipation ( $AV_{DD} = 2.5V, AV_{DDTERM} = 3.3V$ ) | 1, 2, 5, 6 | —       | 193     | —       | mW    |
| $P_{DISSTOT1}$ | Power dissipation ( $AV_{DD} = 2.5V, AV_{DDTERM} = 5.0V$ ) | 1, 2, 4, 6 | —       | 177     | —       | mW    |
| $P_{DISSTOT2}$ | Power dissipation ( $AV_{DD} = 2.5V, AV_{DDTERM} = 5.0V$ ) | 1, 2, 5, 6 | —       | 230     | —       | mW    |
| $P_{DISSTOT1}$ | Power dissipation ( $AV_{DD} = 3.3V, AV_{DDTERM} = 3.3V$ ) | 1, 2, 4, 6 | —       | 162     | —       | mW    |
| $P_{DISSTOT2}$ | Power dissipation ( $AV_{DD} = 3.3V, AV_{DDTERM} = 3.3V$ ) | 1, 2, 5, 6 | —       | 231     | —       | mW    |
| $P_{DISSTOT1}$ | Power dissipation ( $AV_{DD} = 3.3V, AV_{DDTERM} = 5.0V$ ) | 1, 2, 4, 6 | —       | 199     | —       | mW    |
| $P_{DISSTOT2}$ | Power dissipation ( $AV_{DD} = 3.3V, AV_{DDTERM} = 5.0V$ ) | 1, 2, 5, 6 | —       | 268     | —       | mW    |

**NOTES:**

1. Recommended operating conditions—see [Table 2-2](#).
2. 800 mV standard SMPTE swing, terminated as in [Figure 1-3](#).
3. A portion of the power will be dissipated in the external 750Ω termination ( $P_{EXT} = V_{OD} \times I_{TERM}$ ).
4. One Output Enabled.
5. Two Outputs Enabled.
6.  $P_{DISSTOT} = AV_{DD} \times I_{DD} + AV_{DDTERM} \times I_{TERM}$ .
7.  $P_{DISSINT} = P_{DISSTOT} - P_{EXT}$ .

## 2.4 Input/Output Level Specifications

**Table 2-4. CMOS Input Electrical Specifications**

| Symbol   | Parameter                  | Notes | Minimum               | Typical | Maximum               | Units   |
|----------|----------------------------|-------|-----------------------|---------|-----------------------|---------|
| $V_{IH}$ | Input Logic High Voltage   | 1     | $0.75 \times AV_{DD}$ | —       | $AV_{DD} + 0.3$       | V       |
| $V_{IL}$ | Input Logic Low Voltage    | 1     | 0                     | —       | $0.25 \times AV_{DD}$ | V       |
| $I_{IH}$ | Input Current (logic High) | 1     | -100                  | —       | 100                   | $\mu A$ |
| $I_{IL}$ | Input Current (logic Low)  | 1     | -100                  | —       | 100                   | $\mu A$ |

**NOTE:**  
 1. Specified at recommended operating condition—see [Table 2-2](#).

**Table 2-5. High-Speed Input Electrical Specifications**

| Symbol    | Parameter                                 | Notes   | Minimum | Typical | Maximum         | Units     |
|-----------|---|---------|---------|---------|-----------------|-----------|
| $DR_{IN}$ | Input Bit Rate (M21408)                   | 1, 2    | 0       | —       | 540             | Mbps      |
| $DR_{IN}$ | Input Bit Rate (M21418)                   | 1, 2    | 0       | —       | 1485            | Mbps      |
| $DR_{IN}$ | Input Bit Rate (M21428)                   | 1, 2    | 0       | —       | 2970            | Mbps      |
| $V_{ID}$  | Input Differential Voltage (peak to peak) | 1, 3, 4 | 100     | —       | 2000            | mV        |
| $V_{CM}$  | Input Common-Mode Voltage                 | 1       | 1200    | —       | $AV_{DD}$       | mV        |
| $V_{IH}$  | Maximum Input High Voltage                | 1       | —       | —       | $AV_{DD} + 400$ | mV        |
| $V_{IL}$  | Minimum Input Low Voltage                 | 1       | 1.2     | —       | —               | V         |
| $R_{IN}$  | Single-ended input impedance              | 1       | —       | 13.33   | 20              | $k\Omega$ |

**NOTES:**  
 1. Specified at recommended operation conditions—see [Table 2-2](#).  
 2. Part is DC coupled at the input.  
 3. Example  $1200 \text{ mV}_{pp}$  differential =  $600 \text{ mV}_{pp}$  for each single-ended terminal.  
 4. Minimum input level defined as  $BER \leq 10^{-12}$ .

**Table 2-6. Cable Driver Output Electrical Specifications M21408 (SD only)**

| Symbol                           | Parameter  | Notes      | Minimum | Typical | Maximum | Units |
|----------------------------------|--|------------|---------|---------|---------|-------|
| DR <sub>OUT</sub>                | Output Bit Rates   | 1, 5       | —       | —       | 540     | Mbps  |
| t <sub>r</sub> /t <sub>f</sub>   | SD Rise/Fall Time (20–80%)   | 1, 3       | 400     | 600     | 800     | ps    |
| t <sub>r</sub> /t <sub>fMM</sub> | Rise/fall mismatch   | 1, 2       | —       | 40      | 100     | ps    |
| V <sub>OD</sub>                  | Single-ended voltage swing range p–p   | 1, 2, 4, 5 | 500     | 800     | 1600    | mV    |
| V <sub>ODTOL</sub>               | Swing Level output variation at 800 mVpp<br>[RSET = 750ohm ±1%] (Single-Ended) | 1, 2, 3    | -7      | —       | +7      | %     |
| V <sub>OS</sub>                  | Overshoot/Undershoot   | 1, 2       | -8      | —       | +8      | %     |
| JAO <sub>PP</sub>                | Additive Output Jitter   | 1, 8       | —       | 40      | 60      | ps    |
| DCD                              | Duty Cycle Distortion  | 1, 2, 6, 8 | —       | 20      | 70      | ps    |
| S <sub>22</sub>                  | Output Return Loss (5 MHz to 600MHz)   | 1, 2, 7    | 15      | —       | —       | dB    |

**NOTES:**

1. Entire table specified at recommended operating condition with 400 mV<sub>p-p</sub> differential input—see [Table 2-2](#).
2. Specification verified at 800 mVpp output with 1m cable.
3. Rated at nominal SMPTE 800 mV output swing level (using a 750Ω ±1% resistor at RSET).
4. Output stage is an open collector differential pair, actual swing dependant on IC supply voltage and external termination voltage.
5. Into 75Ω back termination and 75Ω load and appropriate external termination voltage.
6. Duty Cycle Distortion (DCD) is defined as the difference in the intrinsic jitter at the 50% voltage level and the intrinsic jitter at the rising/falling edge crossing point. If the rising/falling edge crossing point is at the 50% voltage level, then DCD = 0.
7. Measured under DC conditions that simulate AC coupling, V<sub>T</sub> = 3.3V.
8. Measured using a “1010” data pattern.

**Table 2-7. Cable Driver Output Electrical Specifications M21418 (SD/HD)**

| Symbol                           | Parameter  | Notes      | Minimum | Typical | Maximum | Units |
|----------------------------------|--|------------|---------|---------|---------|-------|
| DR <sub>OUT</sub>                | Output Bit Rates   | 1, 5       | —       | —       | 1485    | Mbps  |
| t <sub>r</sub> /t <sub>f</sub>   | SD Rise/Fall Time (20–80%)   | 1, 3       | 400     | 600     | 800     | ps    |
|                                  | HD Rise/Fall Time (20–80%)   | 1, 3       | —       | 100     | 180     | ps    |
| t <sub>r</sub> /t <sub>rMM</sub> | Rise/fall mismatch (HD Rate)   | 1, 2       | —       | 10      | 30      | ps    |
|                                  | Rise/fall mismatch (SD Rate)   | 1, 2       | —       | 40      | 100     | ps    |
| V <sub>OD</sub>                  | Single-ended voltage swing range p–p   | 1, 2, 4, 5 | 500     | 800     | 1600    | mV    |
| V <sub>ODTOL</sub>               | Swing Level output variation at 800 mVpp<br>[RSET = 750ohm ±1%] (Single-Ended) | 1, 2, 3    | -7      | —       | +7      | %     |
| V <sub>OS</sub>                  | Overshoot/Undershoot   | 1, 2       | -8      | —       | +8      | %     |
| JAO <sub>pp</sub>                | Additive Output Jitter (HD rate 1010 pattern)                                  | 1, 8       | —       | 20      | 30      | ps    |
|                                  | Additive Output Jitter (SD rate 1010 pattern)                                  | 1, 8       | —       | 40      | 60      | ps    |
| DCD <sub>0</sub>                 | Duty Cycle Distortion (HD Rate)  | 1, 2, 6, 8 | —       | 15      | 30      | ps    |
|                                  | Duty Cycle Distortion (SD Rate)  | 1, 2, 6, 8 | —       | 20      | 70      | ps    |
| S <sub>22</sub>                  | Output Return Loss (5 MHz to 1.5 GHz)  | 1, 2, 7    | 15      | —       | —       | dB    |

**NOTES:**

- Entire table specified at recommended operating condition with 400 mV<sub>p-p</sub> differential input—see [Table 2-2](#).
- Specification verified at 800 mVpp output with 1m cable on MSPD test board. System results may vary.
- Rated at nominal SMPTE 800 mV output swing level (using a 750Ω ±1% resistor at RSET).
- Output stage is an open collector differential pair, actual swing dependant on IC supply voltage and external termination voltage.
- Into 75Ω back termination and 75Ω load and appropriate external termination voltage.
- Duty Cycle Distortion (DCD) is defined as the difference in the intrinsic jitter at the 50% voltage level and the intrinsic jitter at the rising/falling edge crossing point. If the rising/falling edge crossing point is at the 50% voltage level, then DCD = 0.
- Measured under DC conditions that simulate AC coupling, V<sub>T</sub> = 3.3V.
- Measured using a “1010” data pattern.

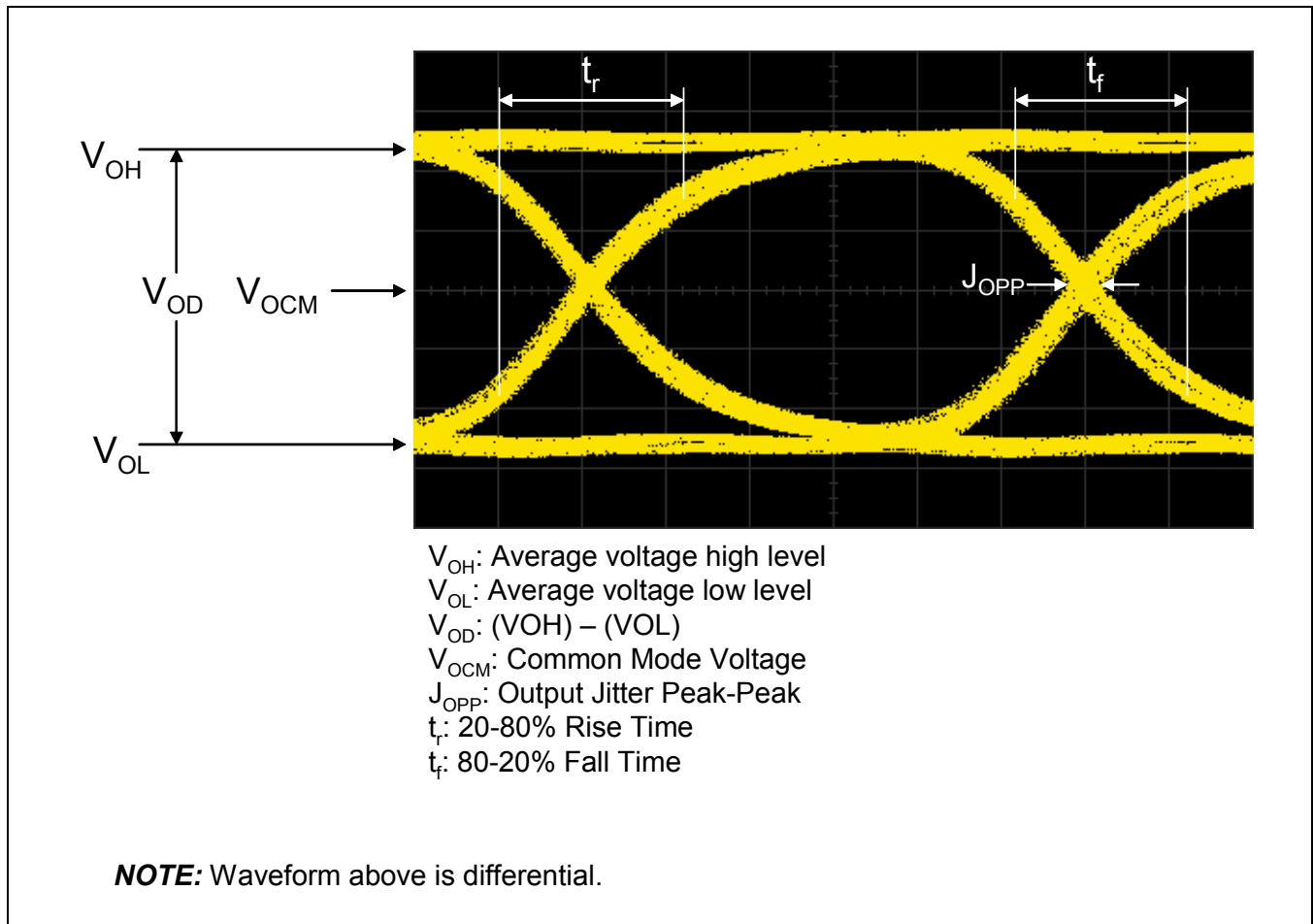
**Table 2-8. Cable Driver Output Electrical Specifications M21428 (SD/HD/2xHD)**

| Symbol                           | Parameter  | Notes         | Minimum | Typical | Maximum | Units |
|----------------------------------|--|---------------|---------|---------|---------|-------|
| DR <sub>OUT</sub>                | Output Bit Rates   | 1, 5          | —       | —       | 2970    | Mbps  |
| t <sub>r</sub> /t <sub>f</sub>   | SD Rise/Fall Time (20–80%)   | 1, 3, 5       | 400     | 600     | 800     | ps    |
|                                  | HD/2xHD Rise/Fall Time (20–80%)  | 1, 3, 5       | —       | 100     | 180     | ps    |
| t <sub>r</sub> /t <sub>rMM</sub> | Rise/fall mismatch (HD/2xHD Rate)  | 1, 2, 5       | —       | 10      | 30      | ps    |
|                                  | Rise/fall mismatch (SD Rate)   | 1, 2, 5       | —       | 40      | 100     | ps    |
| V <sub>O</sub>                   | Single-ended voltage swing range p–p   | 1, 2, 4, 5    | 500     | 800     | 1600    | mV    |
| V <sub>OTOL</sub>                | Swing Level output variation at 800 mVpp<br>[RSET = 750ohm ±1%] (Single-Ended) | 1, 2, 3, 5    | -7      | —       | +7      | %     |
| V <sub>OS</sub>                  | Overshoot/Undershoot   | 1, 2, 5       | -8      | —       | +8      | %     |
| JAO <sub>PP</sub>                | Additive Output Jitter (HD/2xHD rate)  | 1, 5, 8       | —       | 20      | 30      | ps    |
|                                  | Additive Output Jitter (SD rate)   | 1, 5, 8       | —       | 40      | 60      | ps    |
| DCD <sub>O</sub>                 | Duty Cycle Distortion (HD/2xHD Rate)   | 1, 2, 5, 6, 8 | —       | 15      | 30      | ps    |
|                                  | Duty Cycle Distortion (SD Rate)  | 1, 2, 5, 6, 8 | —       | 20      | 70      | ps    |
| S <sub>22</sub>                  | Output Return Loss (5 MHz to 1.5 GHz)  | 1, 2, 5, 7    | 15      | —       | —       | dB    |
| S <sub>22</sub>                  | Output Return Loss (5 MHz to 3.0 GHz)  | 1, 2, 5, 7    | 10      | —       | —       | dB    |

**NOTES:**

- Entire table specified at recommended operating condition with 400 mV<sub>p-p</sub> differential input—see [Table 2-2](#).
- Specification verified at 800 mVpp output with 1m cable on MSPD test board. System results may vary.
- Rated at nominal SMPTE 800 mV output swing level (using a 75Ω ±1% resistor at RSET).
- Output stage is an open collector differential pair, actual swing dependant on IC supply voltage and external termination voltage.
- Into 75Ω back termination and 75Ω load and appropriate external termination voltage, see [Table 1-1](#), [Figure 1-3](#).
- Duty Cycle Distortion (DCD) is defined as the difference in the intrinsic jitter at the 50% voltage level and the intrinsic jitter at the rising/falling edge crossing point. If the rising/falling edge crossing point is at the 50% voltage level, then DCD = 0.
- Measured under DC conditions that simulate AC coupling, V<sub>T</sub> = 3.3V.
- Measured using a “1010” data pattern.

Figure 2-1. Output Symbols Definition





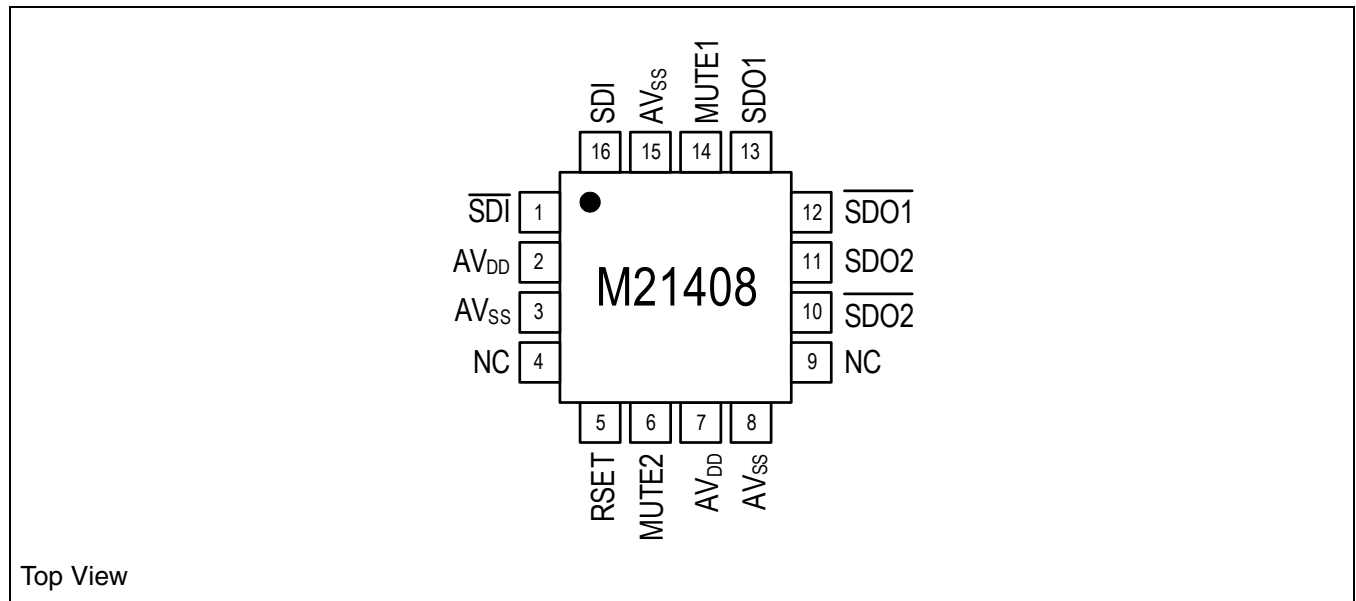
## 2.5 Package Specification

### 2.5.1 Mechanical Description

#### 2.5.1.1 Package Information

The M21408/M21418/M21428 are available in a 16 pin 3x3mm MLF IC package. The pin out is shown in [Figure 2-2](#) and the package drawing in [Figure 2-4](#).

**Figure 2-2. M21408 Pin Out**



**Figure 2-3. M21418/M21428 Pin Out**

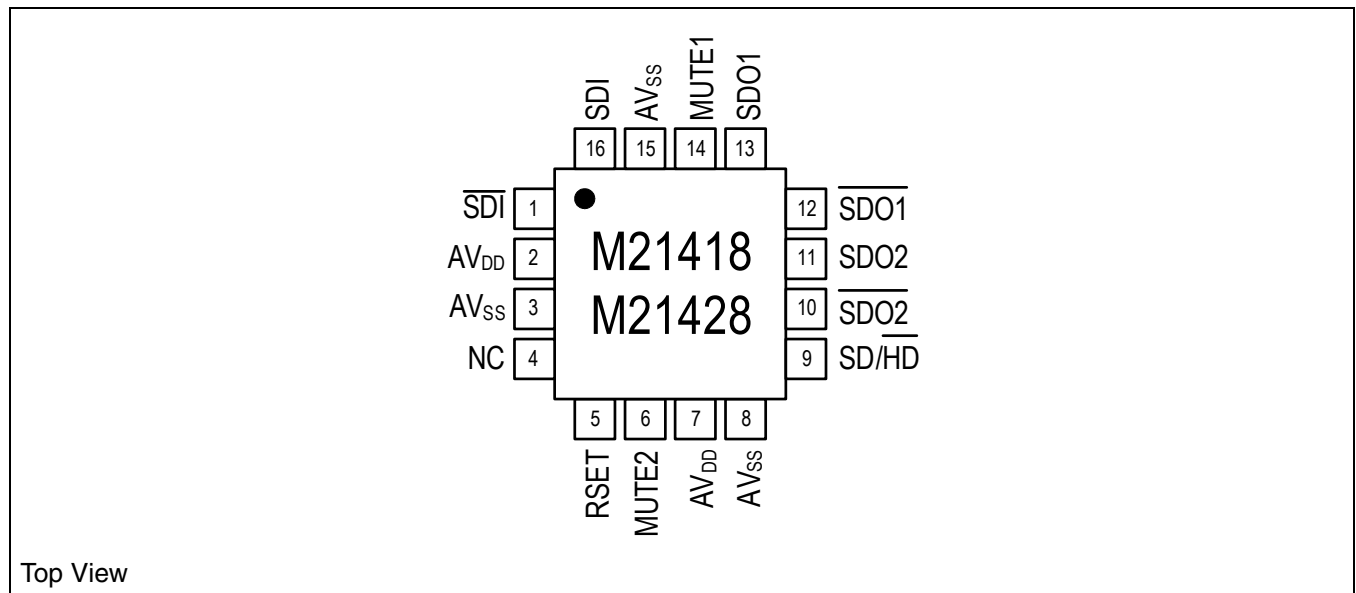
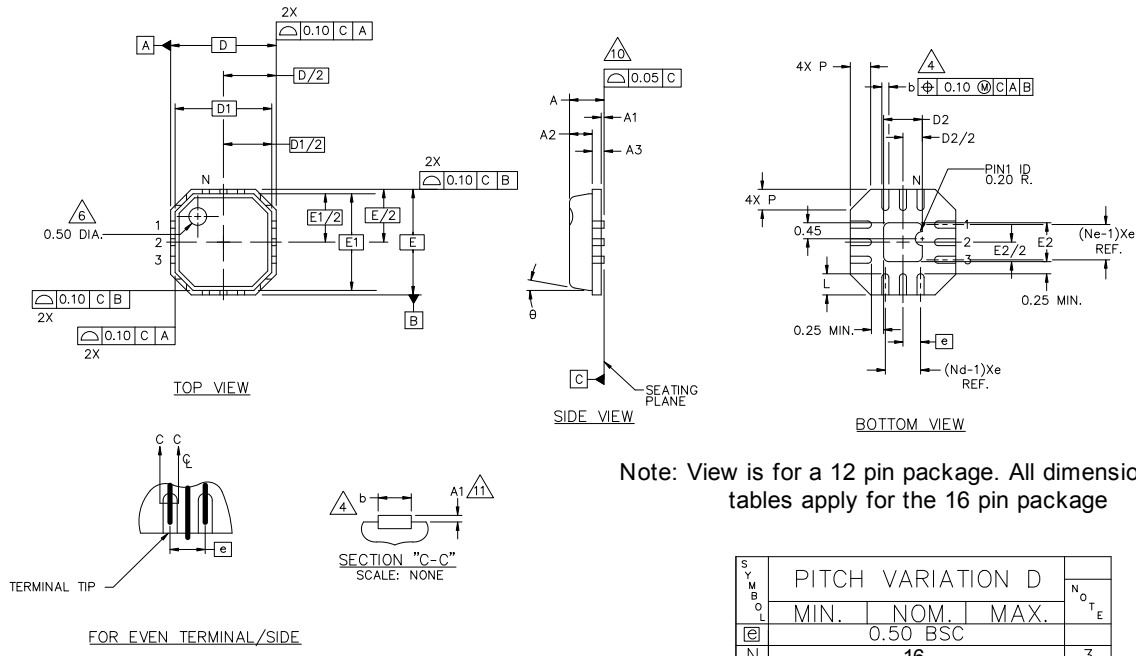


Figure 2-4. Package Drawing (3x3 mm MLF Package)<sup>1</sup>



Note: View is for a 12 pin package. All dimensions in the tables apply for the 16 pin package

FOR EVEN TERMINAL/SIDE

| SYMBOL | PITCH VARIATION D |      |      | NOTE |
|--------|-------------------|------|------|------|
|        | MIN.              | NOM. | MAX. |      |
| Ⓜ      | 0.50 BSC          |      |      |      |
| N      | 16                |      |      | 3    |
| Nd     | 4                 |      |      | 3    |
| Ne     | 4                 |      |      | 3    |
| L      | 0.30              | 0.40 | 0.50 |      |
| b      | 0.18              | 0.23 | 0.30 | 4    |
| D2     | 1.35              | 1.50 | 1.65 |      |
| E2     | 1.35              | 1.50 | 1.65 |      |

| SYMBOL | COMMON DIMENSIONS |      |      | NOTE |
|--------|-------------------|------|------|------|
|        | MIN.              | NOM. | MAX. |      |
| A      | -                 | 0.85 | 0.90 |      |
| A1     | 0.00              | 0.01 | 0.05 | 11   |
| A2     | -                 | 0.65 | 0.70 |      |
| A3     | 0.20 REF.         |      |      |      |
| D      | 3.00 BSC          |      |      |      |
| D1     | 2.75 BSC          |      |      |      |
| E      | 3.00 BSC          |      |      |      |
| E1     | 2.75 BSC          |      |      |      |
| θ      | 12°               |      |      |      |
| P      | 0.24              | 0.42 | 0.60 |      |

NOTES:

2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS.  
Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &  
Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. PACKAGE WARPAGE MAX 0.05mm.
10. APPLIED FOR EXPOSED PAD AND TERMINALS.  
EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
11. APPLIED ONLY FOR TERMINALS.

1. Please see Amkor's Application Note for PCB footprint (referenced in Section 3.2.1).

## 2.6 Manufactureability

The values shown in this section may change; however, these are standard requirements.

### 2.6.1 Electrostatic Discharge

Tested per JESD22-A114. This device passes 2000V of ESD Human Body Model (HBM) testing.

Tested per JESD22-C101. This device passes 500V of ESD Charged Device Model (CDM) testing.

Tested per EIA/JESD78. This device passes 150mA of trigger current at 85°C during Latchup testing.

### 2.6.2 Peak Reflow Temperature

M21408/M21418/M21428G (RoHS compliant package): Peak reflow temperature is 260°C per JEDEC standards.

### 2.6.3 Moisture Sensitivity Level (MSL)

All versions of this device (standard Pb-type and RoHS compliant packages) are Moisture Sensitivity Level (MSL) 3 per J-STD-020B and J-STD-033.

## 2.7 Design Considerations

See Digital Video Interfacing Application Note (212xx-APP-001-A) for guidance on the following:

- Component Placement and Layout
- Routing Considerations and Thermal Considerations

The M21408/M21418/M21428 consumes less power than legacy devices, therefore the M21408/M21418/M21428 will contribute less thermal energy resulting in a lower operating temperature.



# Appendix

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## A.1 Glossary of Terms/Acronyms

|       |  |
|-------|--|
| BER   | Bit Error Rate                                     |
| CD    | Cable Driver                                       |
| CDA   | Cable Distribution Amplifier                       |
| CML   | Current Mode Logic                                 |
| CMOS  | Complementary Metal Oxide Semiconductor            |
| DPLL  | Digital Phase Locked Loop                          |
| DTV   | Digital Television                                 |
| DVB   | Digital Video Broadcast                            |
| EMI   | Electro Magnetic Interference                      |
| EQ    | Equalizer or Equalization                          |
| GREEN | Environmentally friendly                           |
| HD    | High Definition                                    |
| HW    | Hardware   |
| IC    | Integrated Circuit                                 |
| ID    | Identifier   |
| I/O   | Input/Output                                       |
| MLF   | Micro Lead Frame package (also called QFN)         |
| PCB   | Printed Circuit Board                              |
| ORL   | Output Return Loss                                 |
| RoHS  | Restriction of Hazardous Substances                |
| SD    | Standard Definition                                |
| SDI   | Serial Digital Input                               |
| SDO   | Serial Digital Output                              |
| SE    | Single Ended                                       |
| SMPTE | Society of Motion Picture and Television Engineers |

## **A.2 Reference Documents**

### **A.2.1 External**

The following external documents were referenced in this data sheet.

- Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages
- Amkor Technology Thermal Test Report TT-00-06 (See <http://www.amkor.com> for detailed information)
- SMPTE 292M, SMPTE 259M, SMPTE 344M
- ESI TR101 891 DVB Asynchronous Serial Interface (ASI)

[www.mindspeed.com](http://www.mindspeed.com)

General Information:  
Telephone: (949) 579-3000  
Headquarters - Newport Beach  
4000 MacArthur Blvd., East Tower  
Newport Beach, CA 92660

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