M21353

4.25 Gbps Twelve-Channel Backplane Equalizer and Driver with 12x12 Crosspoint Switch

The M21353 is a twelve channel device designed to enable the transmission of multi-gigabit serial data through the most challenging environments. The device features twelve independent, programmable equalizers that equalize data at rates up to 4.25 Gbps. Control of the M21353 is provided through an I^2C compatible software control interface. The M21353 can also self-configure from an external EEPROM without the need for a host processor. For compatibility with PCI-Express and S-ATA/SAS systems, the M21353 is designed with an electrical idle pass-through function to drive the differential output to the common mode level during OOB signaling. Boundary scan is provided for high-speed input and output pins, and the device is available in a 12x12 mm, 88 pin MLF package.

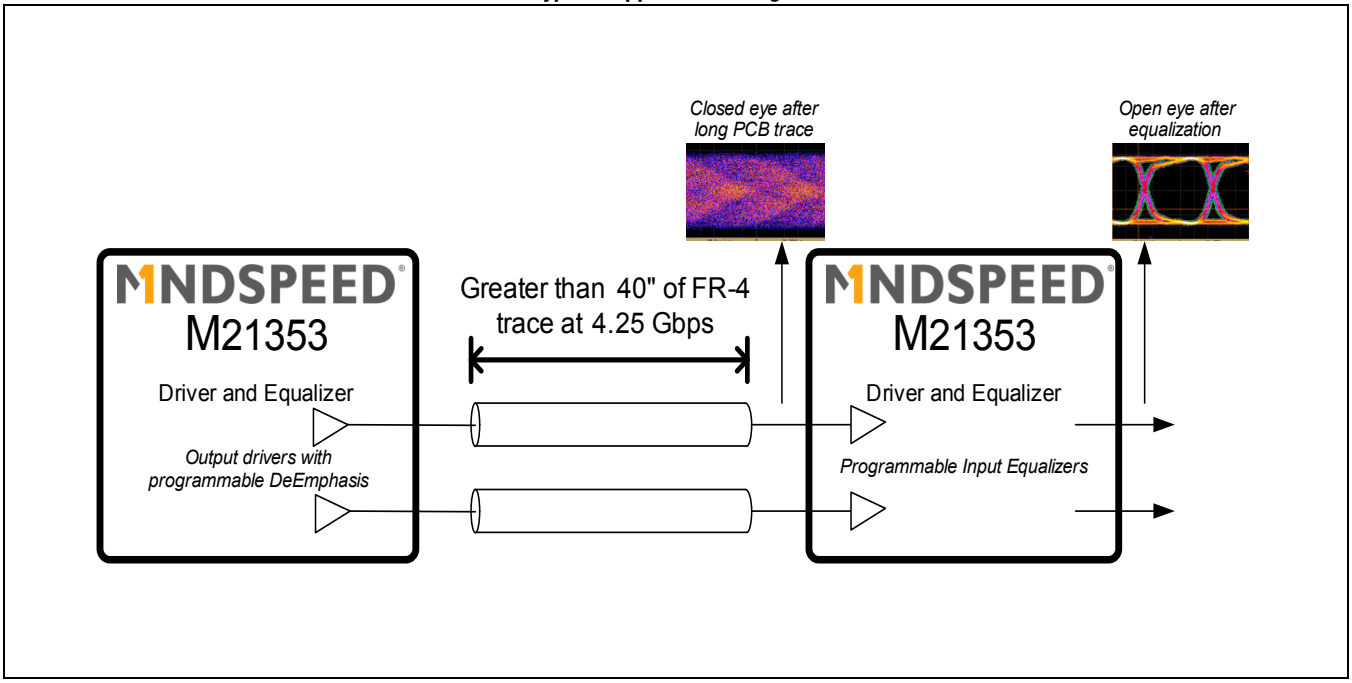
Features

- Programmable Equalization for greater than 40" of FR-4 PCB trace at 4.25 Gbps
- Supports electrical idle signaling for PCIe and OOB signaling for S-ATA/SAS
- Twelve channel programmable equalizer for data rates up to 4.25 Gbps
- Low power dissipation: 110 mW per channel, 1.3 W total power at 1.2V
- Up to 16 dB of input equalization and 6 dB of output de-emphasis
- 12x12 mm, 88 pin MLF package
- Extended case temperature range (-20 °C to 85 °C)
- Integrated 12x12 Crosspoint Switch Matrix

Applications

XAUI	3.125 Gbps	—	—
S-ATA/SAS	1.5 Gbps	3.0 Gbps	—
PCIe	2.5 Gbps	—	—
Fibre Channel	1.0625 Gbps	2.125 Gbps	4.25 Gbps
Infiniband	2.5 Gbps	—	—
SDI Video	270 Mbps	1.485 Gbps 1.485/1.001 Gbps	2.97 Gbps 2.97/1.001 Gbps

Typical Application Diagram



Ordering Information

Part Number	Package	Operating Case Temperature
M21353G-13	12x12 mm, 88 pin MLF package	-20 °C to 85 °C
The M21353 is RoHS compliant. Refer to **http://www.mindspeed.com/web/support/environment/index.html** for additional information. Mindspeed RoHS compliant devices are backwards compatible with 225 °C reflow profiles.		

Revision History

Revision	Level	Date	Description
B	Released	January 2009	Updated for production release. The following specifications were modified in Table 1-3 and Table 1-4: - Power Consumption - Input Launch Amplitude - Rise/Fall Time - Deterministic Jitter - Random Jitter - Propagation Delay Values for input equalization and output de-emphasis dynamic range were removed from Table 1-4. Channel to Channel skew was added to Table 1-4. Figure 2-1 through Figure 2-11 were added. Default value of registers 41h-4Ch were modified to reflect the new default state. (Output buffers powered-down by default in M21453G-13.) Removed description of register address 04h - Register 04h is now a MSPD internal register. Removed support for programmable interrupt pulse widths for xALARM signal in register 00h[3:0]. Support for SDI video was added, see Section 5.8 for details. Additional information on how to configure the crosspoint switch core was added in Section 5.9. Added etails on boundary scan support were in Section 5.11. Added details on how to compute the correct seed value for the checksum register (address 01h) when using MIC mode in Section 5.13.
A	Advance	May 2008	Initial release.

1.0 Electrical Characteristics

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
AVDDIO	Analog I/O power supply voltage	—	2.1	V
AVDDCORE/ DVDDCORE	Core power supply voltage	—	1.5	V
DVDDIO	Digital I/O power supply voltage	—	3.6	V
Tst	Storage Temperature	–65	150	°C
Vesd	Electrostatic discharge voltage (HBM)	—	2000	V
Vesd	Electrostatic discharge voltage (CDM)	—	500	V

NOTES:

Exposure of the device beyond the minimum/maximum limits may cause permanent damage.

Limits listed in the above table are stress limits only, and do not imply functional operation within these limits.

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
AVDDIO	Analog I/O power supply voltage	1.14	1.2, 1.8	1.89	V
AVDDCORE/ DVDDCORE	Core power supply voltage	1.14	1.2	1.26	V
DVDDIO	Digital I/O power supply voltage	1.14	1.2, 1.8, 2.5, 3.3	3.47	V
Tc	Operating Case Temperature	–20	—	85	°C

Table 1-3. Power Consumption Specifications

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
AIDDIO	Analog I/O power supply current (AVDDIO = 1.2V)	1	—	210	240	mA
AIDDIO	Analog I/O power supply current (AVDDIO = 1.8V)	2	—	390	475	mA
AIDDCORE	Analog core power supply current (AVDDIO = 1.2V)	1	—	850	1000	mA
AIDDCORE	Analog core power supply current (AVDDIO = 1.8V)	2	—	925	1200	mA
DIDDIO	Digital I/O power supply current	—	—	2	—	mA
DVDDCORE	Digital core power supply current	—	—	3	—	mA
Pdiss	Total power dissipation (AVDDIO=1.2V)	1, 3	—	1.3	1.6	W
Pdiss	Total power dissipation (AVDDIO=1.8V)	2, 3	—	1.8	2.4	W

NOTES:

1. Valid with nominal (800 mVppd) output swing for all channels.
2. Valid with maximum (1500 mVppd) output swing for all channels.
3. Typical calculated with nominal current and voltage. Maximum calculated with maximum current and 5% over voltage.

Unless noted otherwise, specifications in this section are valid with AVDDIO = 1.8V, 25 °C case temperature, 800 mV differential input data swing, nominal (800 mVppd) output data swing, PRBS 2^{15} – 1 test pattern at 4.25 Gbps, R_L = 50Ω, short cables and/or traces.

Table 1-4. Input/Output Electrical Characteristics (1 of 2)

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
DR	NRZ Data Rate	—	100	—	4250	Mbps
Vin	Input differential voltage swing (AC-Coupled), voltage measured at the device input	—	200	—	2000	mV
VI	Input launch amplitude (Voltage used to drive a signal across 40" of FR-4 trace)	—	500	—	—	mVppd
VI	Input launch amplitude (Voltage used to drive a signal across 40" of FR-4 trace, pathological video pattern)	—	700	—	—	mVppd
Rt	PCML differential input impedance termination	—	80	100	120	Ω
Voh	PCML single ended output logic-high	—	AVDDIO - 0.05	—	AVDDIO	V
Vod	PCML p-p differential output swing	1,2,3,6	350	—	1750	mV
Tr/Tf	PCML output rise/fall time (20–80%)	6	—	60	—	ps
DJ	Deterministic output jitter	4	—	0.1	0.2	UI
RJ	Random output jitter (RMS)	4	—	6	9	mUI RMS
Tprop	Propagation delay	—	—	1	—	ns
Tskew	Channel to channel skew	—	—	300	—	ps
V_{IH}	CMOS Input logic high	—	0.85 x DVDDIO	—	—	V
V_{IF}	CMOS input logic floating state	—	0.25 x DVDDIO	—	0.75 x DVDDIO	V
V_{IL}	CMOS input logic low	—	—	—	0.15 x DVDDIO	V

Table 1-4. Input/Output Electrical Characteristics (2 of 2)

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
V_{OH}	CMOS output logic high	5	0.85 x DVDDIO	—	—	V
V_{OL}	CMOS output logic low	5	—	—	0.15 x DVDDIO	V

NOTES:

1. AVDDIO must be 1.8V to achieve higher than 800 mV output swing.
2. Output swing is specified with output de-emphasis disabled.
3. Six output swing levels can be selected. Output swing increases by approximately 200 mV with each setting. See Figure 2-6 for typical swing levels.
4. Additive output jitter with minimal media length
5. Two-wire serial interface can drive 500 pF at 100 kHz and 400 kHz, 100 pF at 3.4 MHz.
6. Measured using a CID pattern with a minimum CID length of 10 bits.

2.0 Typical Performance Characteristics

Unless noted otherwise, test conditions in this section are: AVDDIO = 1.8V, 25 °C case temperature, 800 mVppd input data swing, nominal (800 mVppd) output data swing PRBS 2^{15} - 1 test pattern at 4.25 Gbps, $R_L = 50\Omega$, short traces and/or cables.

Figure 2-1. Eye Diagram at 3.125 Gbps

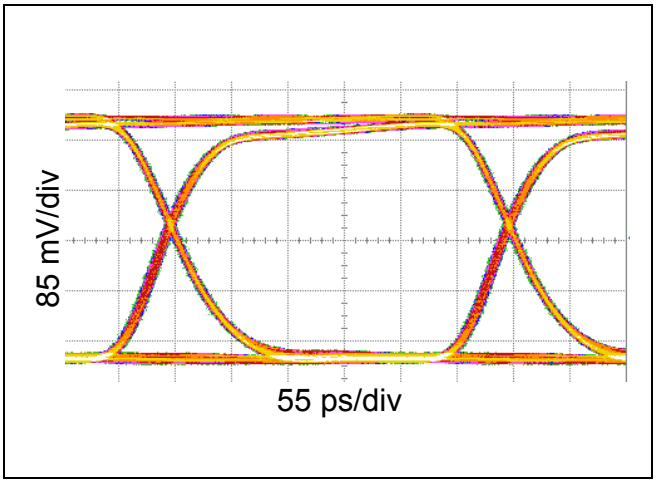


Figure 2-2. Eye Diagram at 4.25 Gbps

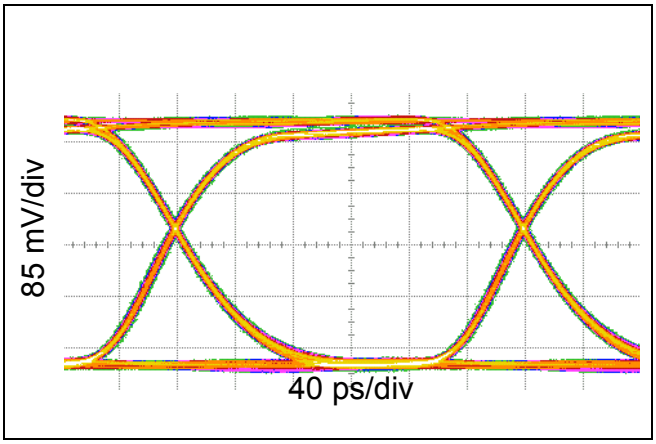


Figure 2-3. Output Waveform With COMWAKE OOB Signal

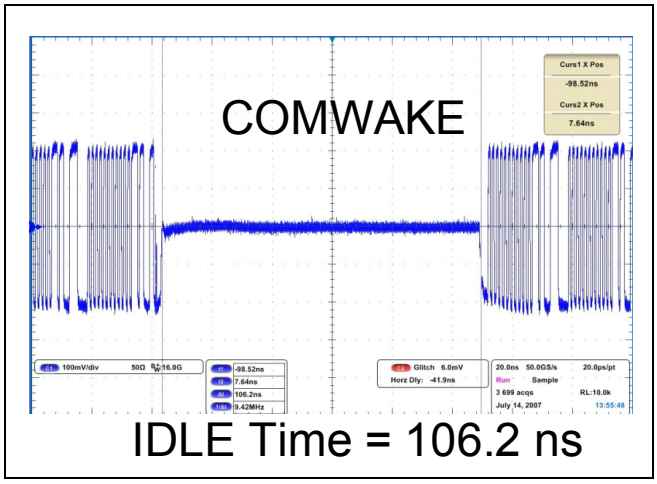


Figure 2-4. Deterministic Jitter vs. Data Rate as a Function of Trace Length

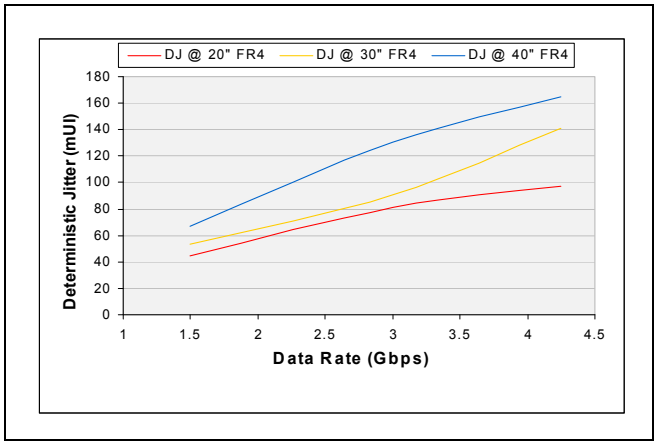


Figure 2-5. Eye Diagram After 40" of FR-4 Trace

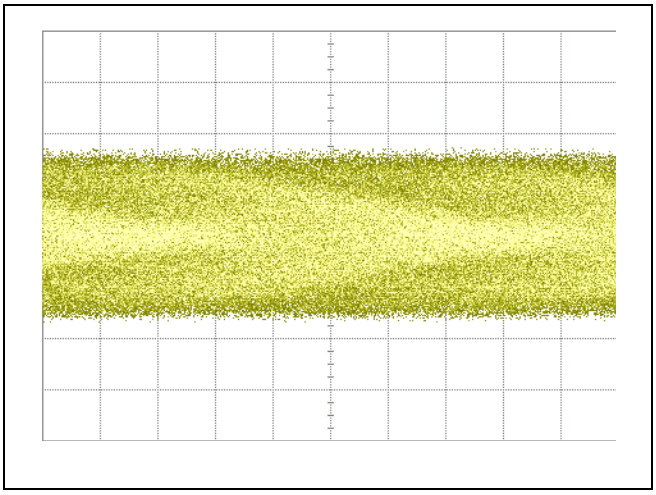


Figure 2-6. Differential Output Swing vs. OutctrIN[7:5] Setting as a Function of AVDDIO

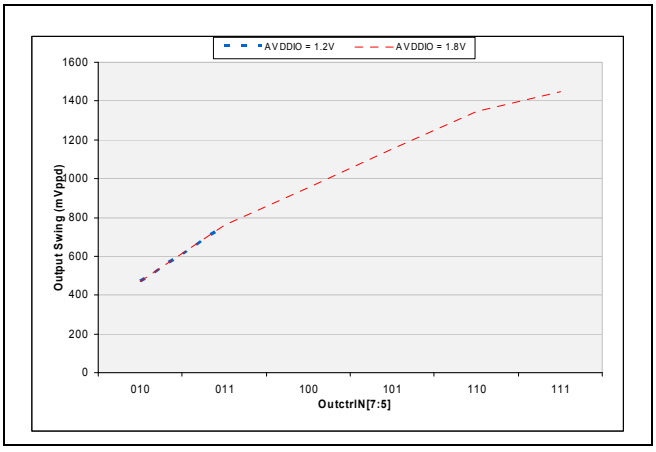


Figure 2-7. Eye Diagram after Equalizing 40" of FR-4 trace at 4.25 Gbps

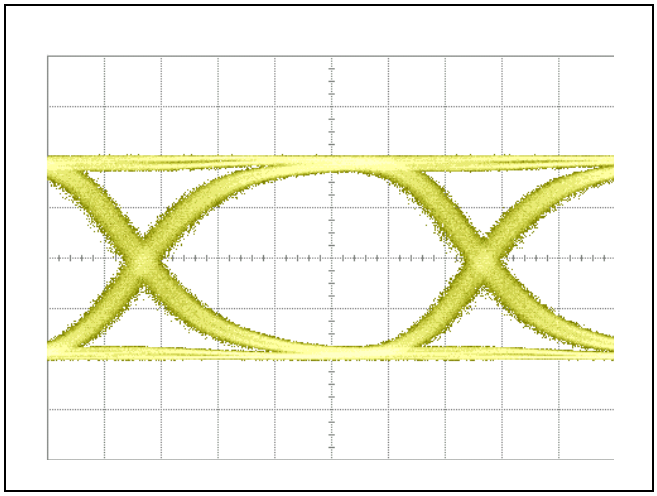


Figure 2-8. Random Jitter Distribution

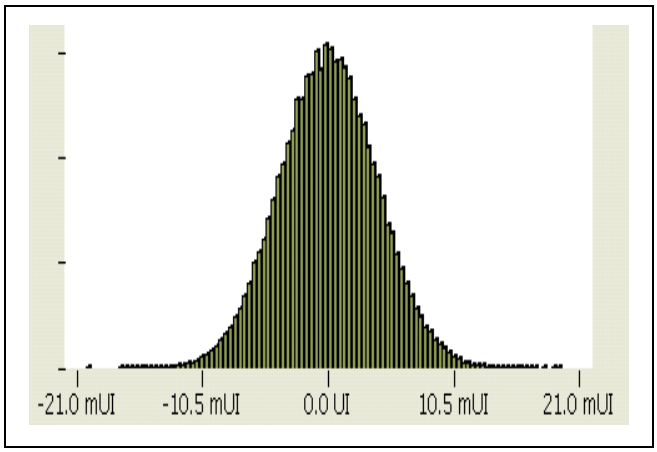


Figure 2-9. Deterministic Jitter vs. Launch Amplitude as a Function of Data Rate (Input EQ Optimized for 30" FR-4 trace)

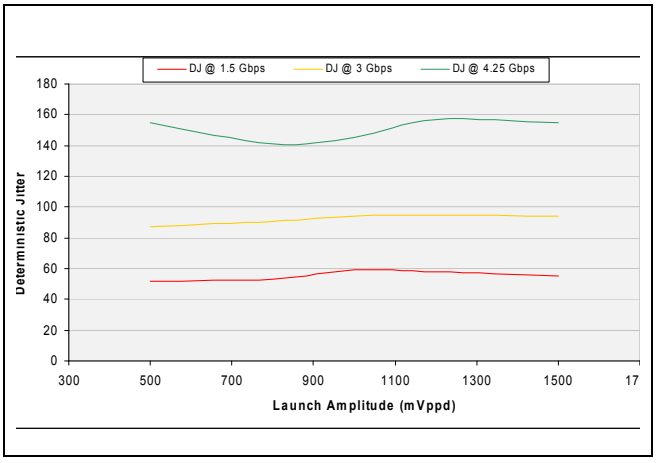


Figure 2-10. Bathtub Curve

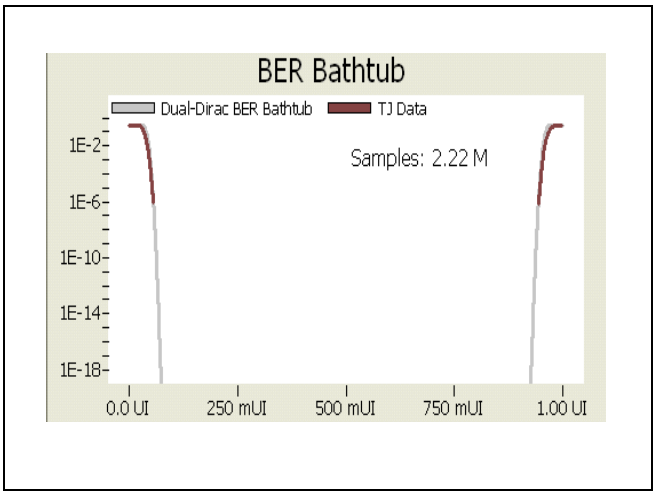


Figure 2-11. Typical LOS Assert/De-Assert Behavior

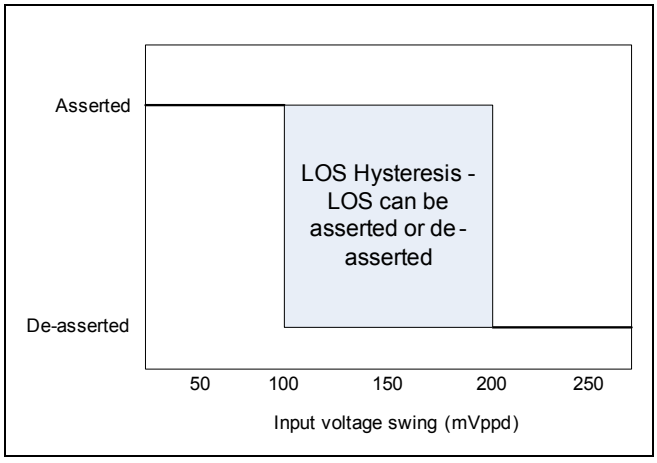
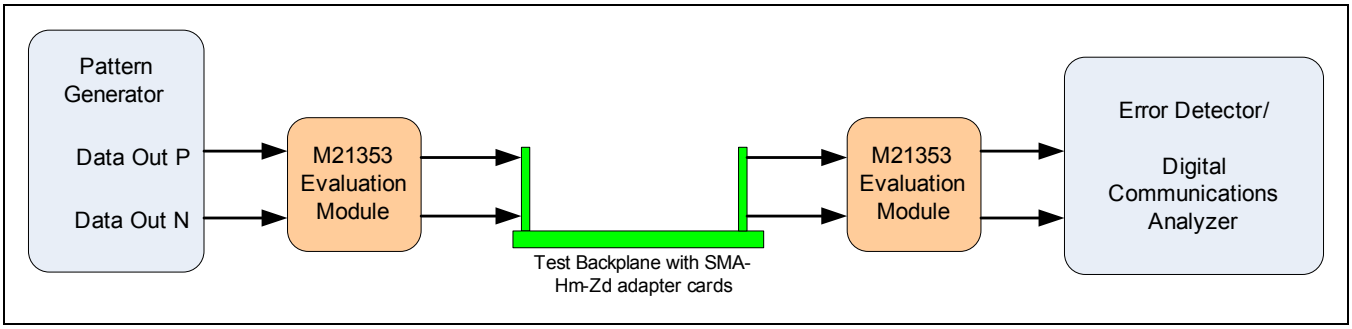


Figure 2-12. Input Equalization Test Setup Test Backplane



3.0 Package Description and Package Outline Drawing

The M21353 is assembled in 12x12 mm, 88 pin MLF packages. The package paddle should be soldered to the ground plane to provide a GND connection and a thermal path for the device.

Figure 3-1. Package Outline Drawing

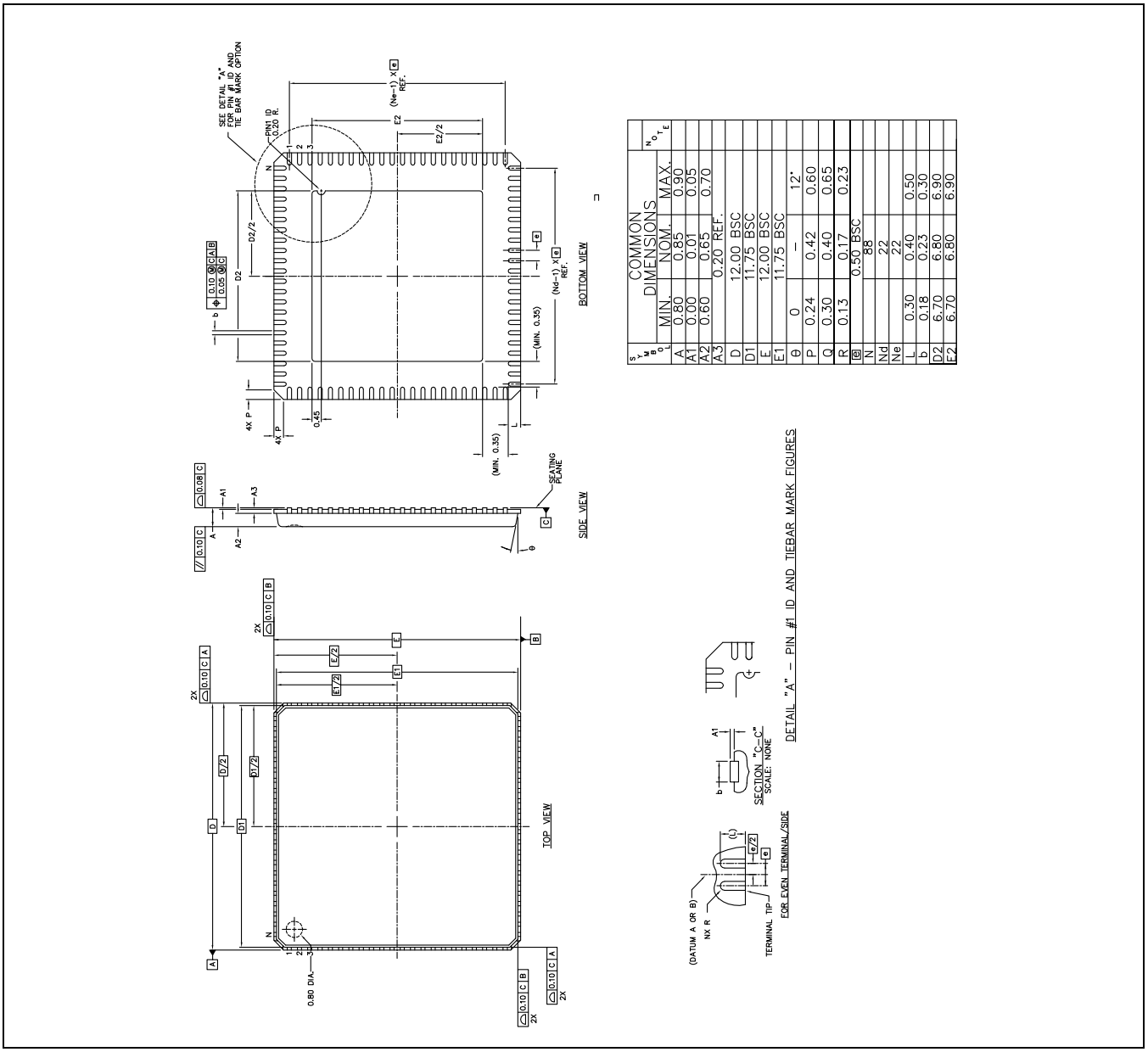


Figure 3-2. Pinout Diagram - Top View

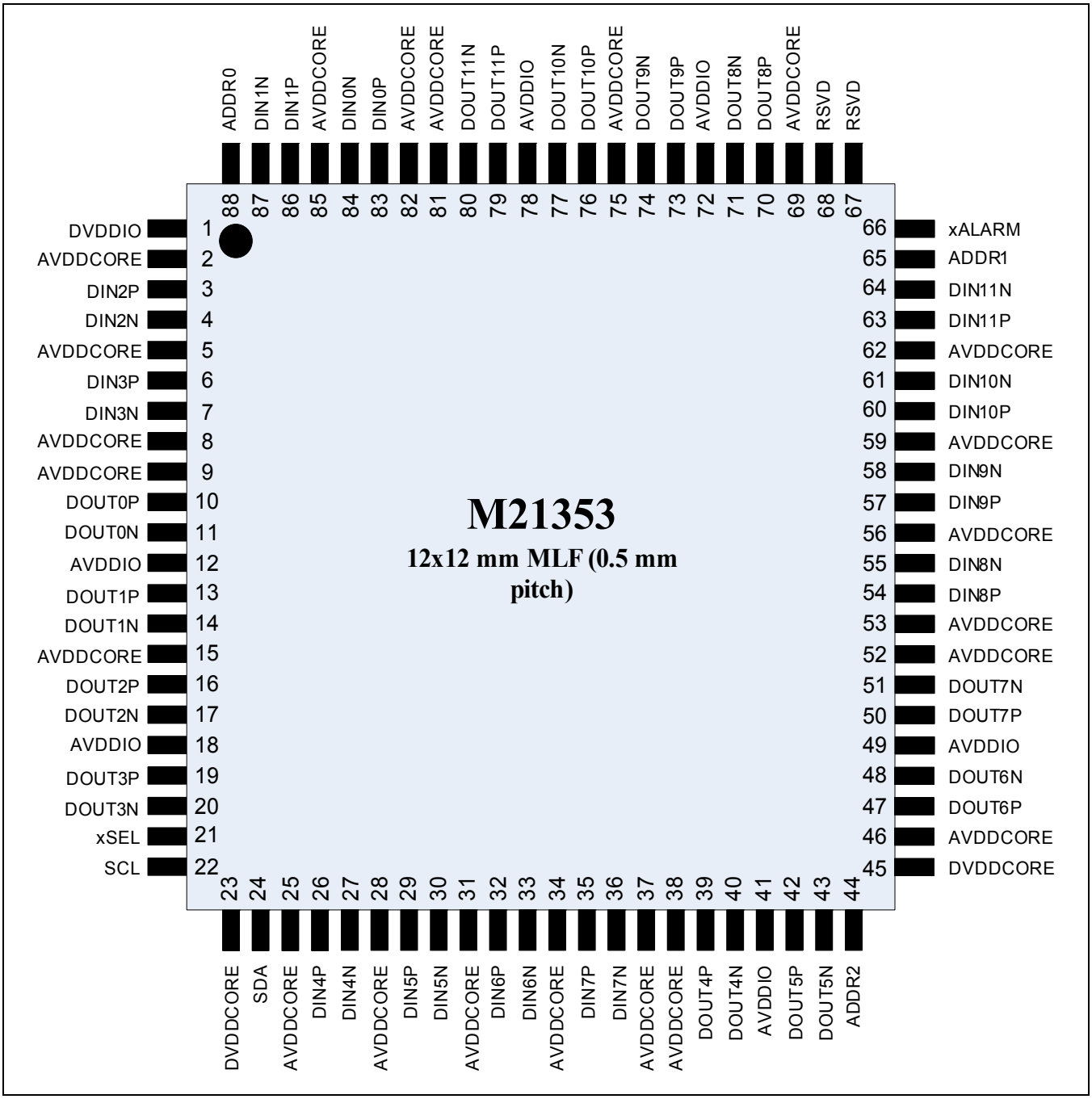


Table 3-1. M21353 Pin Descriptions (1 of 2)

Pin Name	Pin Number(s)	Pin Function	Pin Type
AVDDIO	12,18,41, 49, 72, 78,	Analog IO Voltage Supply	Power
DVDDIO	1	Digital IO Voltage Supply	Power
AVDDCORE	2, 5, 8, 9, 15, 25, 28, 31, 34, 37, 38, 46, 52, 53, 56, 59, 62, 69, 75, 81, 82, 85	Analog Core Voltage Supply	Power
DVDDCORE	23, 45	Digital Core Voltage Supply	Power
GND	Exposed pad on bottom of package	Device ground	Ground
xSEL	21	Hardware Strobe Pin	Control
SCL	22	2 wire interface SCL pin	Control
SDA	24	2 wire interface SDA pin	Control
ADDR2	44	2 wire interface address select pin	Control
ADDR1	65	2 wire interface address select pin	Control
ADDR0	88	2 wire interface address select pin	Control
xALARM (1)	66	Alarm output pin (1)	Status - Open Drain
RSVD	67, 68	Do not connect for M21353 (2)	Mindspeed Reserved
DIN0P	83	Channel 0 Input P	High-Speed Input
DIN0N	84	Channel 0 Input N	High-Speed Input
DIN1P	86	Channel 1 Input P	High-Speed Input
DIN1N	87	Channel 1 Input N	High-Speed Input
DIN2P	3	Channel 2 Input P	High-Speed Input
DIN2N	4	Channel 2 Input N	High-Speed Input
DIN3P	6	Channel 3 Input P	High-Speed Input
DIN3N	7	Channel 3 Input N	High-Speed Input
DIN4P	26	Channel 4 Input P	High-Speed Input
DIN4N	27	Channel 4 Input N	High-Speed Input
DIN5P	29	Channel 5 Input P	High-Speed Input
DIN5N	30	Channel 5 Input N	High-Speed Input
DIN6P	32	Channel 6 Input P	High-Speed Input
DIN6N	33	Channel 6 Input N	High-Speed Input
DIN7P	35	Channel 7 Input P	High-Speed Input
DIN7N	36	Channel 7 Input N	High-Speed Input
DIN8P	54	Channel 8 Input P	High-Speed Input
DIN8N	55	Channel 8 Input N	High-Speed Input
DIN9P	57	Channel 9 Input P	High-Speed Input
DIN9N	58	Channel 9 Input N	High-Speed Input
DIN10P	60	Channel 10 Input P	High-Speed Input
DIN10N	61	Channel 10 Input N	High-Speed Input

Table 3-1. M21353 Pin Descriptions (2 of 2)

Pin Name	Pin Number(s)	Pin Function	Pin Type
DIN11P	63	Channel 11 Input P	High-Speed Input
DIN11N	64	Channel 11 Input N	High-Speed Input
DOUT0P	10	Channel 0 Output P	High-Speed Output
DOUT0N	11	Channel 0 Output N	High-Speed Output
DOUT1P	13	Channel 1 Output P	High-Speed Output
DOUT1N	14	Channel 1 Output N	High-Speed Output
DOUT2P	16	Channel 2 Output P	High-Speed Output
DOUT2N	17	Channel 2 Output N	High-Speed Output
DOUT3P	19	Channel 3 Output P	High-Speed Output
DOUT3N	20	Channel 3 Output N	High-Speed Output
DOUT4P	39	Channel 4 Output P	High-Speed Output
DOUT4N	40	Channel 4 Output N	High-Speed Output
DOUT5P	42	Channel 5 Output P	High-Speed Output
DOUT5N	43	Channel 5 Output N	High-Speed Output
DOUT6P	47	Channel 6 Output P	High-Speed Output
DOUT6N	48	Channel 6 Output N	High-Speed Output
DOUT7P	50	Channel 7 Output P	High-Speed Output
DOUT7N	51	Channel 7 Output N	High-Speed Output
DOUT8P	70	Channel 8 Output P	High-Speed Output
DOUT8N	71	Channel 8 Output N	High-Speed Output
DOUT9P	73	Channel 9 Output P	High-Speed Output
DOUT9N	74	Channel 9 Output N	High-Speed Output
DOUT10P	76	Channel 10 Output P	High-Speed Output
DOUT10N	77	Channel 10 Output N	High-Speed Output
DOUT11P	79	Channel 11 Output P	High-Speed Output
DOUT11N	80	Channel 11 Output N	High-Speed Output

Note:

1. xALARM is an open-drain output, and should be connected to an external pull-up resistor in system designs.
2. These pins are used for the REFCLK connection in the M21363. Mindspeed recommends that system PCBs for the M21353 include a refclk circuit if feasible to allow for the use of the M21363 on the same PCB.

4.0 Control Registers Map and Descriptions

4.1 Control Registers Map

Table 4-1. M21353 Register Summary Table (1 of 4)

Address	Register Name	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0	Default (Lane/ Group mode)	R/W
00h	Alarm Mode	MSPD				xALARM mode control	MSPD			00h/00h	R/W
01h	Checksum	Seed value for MIC checksum								55h/55h	R/W
02h	MIC Control	MSPD				Identifies number of devices in MIC mode				00h/00h	R/W
03h	Gen Config	Standby	MSPD	Group Switch	Clear Alarm	Strobe Mode	MSPD	Set Squelch Level		2Bh/2Bh	R/W
05h	Strobe	ICL Select	xSel Mode	Software Strobe						00h/00h	R/W
06h	Polarity Invert	MSPD				Input 11 Polarity	Input 10 Polarity	Input 9 Polarity	Input 8 Polarity	00h/00h	R/W
07h	Polarity Invert	Input 7 Polarity	Input 6 Polarity	Input 5 Polarity	Input 4 Polarity	Input 3 Polarity	Input 2 Polarity	Input 1 Polarity	Input 0 Polarity	00h/00h	R/W
*08h**	Active Switch Config	Configuration for Output 11				Configuration for Output 10				BAh/00h	R/W
*09h**	Active Switch Config	Configuration for Output 9				Configuration for Output 8				98h/00h	R/W
*0Ah**	Active Switch Config	Configuration for Output 7				Configuration for Output 6				32h/00h	R/W
*0Bh**	Active Switch Config	Configuration for Output 5				Configuration for Output 4				10h/00h	R/W
0Ch	Active Switch Config	Configuration for Output 3				Configuration for Output 2/Group 2				76h/02h	R/W
0Dh	Active Switch Config	Configuration for Output 1/Group 1				Configuration for Output 0/Group 0				54h/01h	R/W
*0Eh**	Intermediate Switch Config #1	Configuration for Output 11				Configuration for Output 10				BAh/00h	R/W
*0Fh**	Intermediate Switch Config #1	Configuration for Output 9				Configuration for Output 8				98h/00h	R/W
*10h**	Intermediate Switch Config #1	Configuration for Output 7				Configuration for Output 6				32h/00h	R/W

Table 4-1. M21353 Register Summary Table (2 of 4)

Address	Register Name	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0	Default (Lane/ Group mode)	R/W
*11h**	Intermediate Switch Config #1	Configuration for Output 5				Configuration for Output 4				10h/00h	R/W
12h	Intermediate Switch Config #1	Configuration for Output 3				Configuration for Output 2/Group 2				76h/02h	R/W
13h	Intermediate Switch Config #1	Configuration for Output 1/Group 1				Configuration for Output 0/Group 0				54h/01h	R/W
*14h**	Intermediate Switch Config #2	Configuration for Output 11				Configuration for Output 10				32h/00h	R/W
*15h**	Intermediate Switch Config #2	Configuration for Output 9				Configuration for Output 8				10h/00h	R/W
*16h**	Intermediate Switch Config #2	Configuration for Output 7				Configuration for Output 6				76h/00h	R/W
*17h**	Intermediate Switch Config #2	Configuration for Output 5				Configuration for Output 4				54h/00h	R/W
18h	Intermediate Switch Config #2	Configuration for Output 3				Configuration for Output 2/Group 2				BAh/00h	R/W
19h	Intermediate Switch Config #2	Configuration for Output 1/Group 1				Configuration for Output 0/Group 0				98h/12h	R/W
*1Ah**	Input Config A	Input 11 Configuration		Input 10 Configuration		Input 9 Configuration		Input 8 Configuration		FFh/00h	R/W
*1Bh**	Input Config A	Input 7 Configuration		Input 6 Configuration		Input 5 Configuration		Input 4 Configuration		FFh/00h	R/W
1Ch	Input Config A	Input 3 Configuration		Input 2/Group 2 Configuration		Input 1/Group 1 Configuration		Input 0/Group 0 Configuration		FFh/3Fh	R/W
*1Dh**	Input 11 Equalization	Input 11 Equalization								37h/00h	R/W
*1Eh**	Input 10 Equalization	Input 10 Equalization								37h/00h	R/W
*1Fh**	Input 9 Equalization	Input 9 Equalization								37h/00h	R/W
*20h**	Input 8 Equalization	Input 8 Equalization								37h/00h	R/W
*21h**	Input 7 Equalization	Input 7 Equalization								37h/00h	R/W
*22h**	Input 6 Equalization	Input 6 Equalization								37h/00h	R/W
*23h**	Input 5 Equalization	Input 5 Equalization								37h/00h	R/W

Table 4-1. M21353 Register Summary Table (3 of 4)

Address	Register Name	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0	Default (Lane/ Group mode)	R/W
*24h**	Input 4 Equalization	Input 4 Equalization								37h/00h	R/W
*25h**	Input 3 Equalization	Input 3 Equalization								37h/00h	R/W
26h	Input 2 Equalization	Input/Group 2 Equalization								37h/37h	R/W
27h	Input 1 Equalization	Input/Group 1 Equalization								37h/37h	R/W
28h	Input 0 Equalization	Input/Group 0 Equalization								37h/37h	R/W
*35h**	Input 11 Config B	MSPD		In11 LOS Enable	MSPD		Input11 Squelch	MSPD	Input11 EBI Enable	C0h/00h	R/W
*36h**	Input 10 Config B	MSPD		In10 LOS Enable	MSPD		Input10 Squelch	MSPD	Input10 EBI Enable	C0h/00h	R/W
*37h**	Input 9 Config B	MSPD		In9 LOS Enable	MSPD		Input9 Squelch	MSPD	Input9 EBI Enable	C0h/00h	R/W
*38h**	Input 8 Config B	MSPD		In8 LOS Enable	MSPD		Input8 Squelch	MSPD	Input8 EBI Enable	C0h/00h	R/W
*39h**	Input 7 Config B	MSPD		In7 LOS Enable	MSPD		Input7 Squelch	MSPD	Input7 EBI Enable	C0h/00h	R/W
*3Ah**	Input 6 Config B	MSPD		In6 LOS Enable	MSPD		Input6 Squelch	MSPD	Input6 EBI Enable	C0h/00h	R/W
*3Bh**	Input 5 Config B	MSPD		In5 LOS Enable	MSPD		Input5 Squelch	MSPD	Input5 EBI Enable	C0h/00h	R/W
*3Ch**	Input 4 Config B	MSPD		In4 LOS Enable	MSPD		Input4 Squelch	MSPD	Input4 EBI Enable	C0h/00h	R/W
*3Dh**	Input 3 Config B	MSPD		In3 LOS Enable	MSPD		Input3 Squelch	MSPD	Input3 EBI Enable	C0h/00h	R/W
3Eh	Input 2 Config B	MSPD		In/Group2 LOS Enable	MSPD		Input/Group2 Squelch	MSPD	Input2 EBI Enable	C0h/C0h	R/W
3Fh	Input 1 Config B	MSPD		In/Group1 LOS Enable	MSPD		Input/Group1 Squelch	MSPD	Input1 EBI Enable	C0h/C0h	R/W
40h	Input 0 Config B	MSPD		In/Group0 LOS Enable	MSPD		Input/Group0 Squelch	MSPD	Input0 EBI Enable	C0h/C0h	R/W
*41h**	Output 11 Config	Output 11 Swing			MSPD	Output 11 De-Emphasis			MSPD	00h/00h	R/W
*42h**	Output 10 Config	Output 10 Swing			MSPD	Output 10 De-Emphasis			MSPD	00h/00h	R/W
*43h**	Output 9 Config	Output 9 Swing			MSPD	Output 9 De-Emphasis			MSPD	00h/00h	R/W
*44h**	Output 8 Config	Output 8 Swing			MSPD	Output 8 De-Emphasis			MSPD	00h/00h	R/W

Table 4-1. M21353 Register Summary Table (4 of 4)

Address	Register Name	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0	Default (Lane/ Group mode)	R/W
*45h**	Output 7 Config	Output 7 Swing			MSPD	Output 7 De-Emphasis			MSPD	00h/00h	R/W
*46h**	Output 6 Config	Output 6 Swing			MSPD	Output 6 De-Emphasis			MSPD	00h/00h	R/W
*47h**	Output 5 Config	Output 5 Swing			MSPD	Output 5 De-Emphasis			MSPD	00h/00h	R/W
*48h**	Output 4 Config	Output 4 Swing			MSPD	Output 4 De-Emphasis			MSPD	00h/00h	R/W
*49h**	Output 3 Config	Output 3 Swing			MSPD	Output 3 De-Emphasis			MSPD	00h/00h	R/W
4Ah	Output 2 Config	Output/Group 2 Swing			MSPD	Output/Group 2 De-Emphasis			MSPD	00h/00h	R/W
4Bh	Output 1 Config	Output/Group 1 Swing			MSPD	Output/Group 1 De-Emphasis			MSPD	00h/00h	R/W
4Ch	Output 0 Config	Output/Group 0 Swing			MSPD	Output/Group 0 De-Emphasis			MSPD	00h/00h	R/W
C3h	LOS Alarm	MSPD				Input11 LOS	Input10 LOS	Input9 LOS	Input8 LOS	N/A	R
C4h	LOS Alarm	Input7 LOS	Input6 LOS	Input5 LOS	Input4 LOS	Input 3 LOS	Input 2 LOS	Input 1 LOS	Input 0 LOS	N/A	R
FCh	MIC Checksum	Computed Checksum Value								00h	R
FDh	Chip Code	M21353 Chip Code								20h	R
FEh	Chip Revision	M21353 Revision Number								---**	R
FFh	Master Reset	Chip Reset								00h	R/W

* Registers noted with a * are only used when the device is in Lane Switch Mode, which is enabled by setting address 03h[5] to 0b.
** See register description for details on the contents of the chip revision register (register address FEh).

4.2 Control Registers Descriptions

Register Address: 00h
Register Name: Alarm Mode
Description: Controls the behavior of the xAlarm pin when an alarm is asserted.

Bit	Bit Description	Default	R/W
7:4	Reserved, set to 0000b	0000b	R/W
3	1: xALARM is static high or low depending on Alarm condition 0: xALARM toggles once with an interrupt pulse when asserted	0b	R/W
2:0	Reserved, set to 000b	000b	R/W

Register Address: 01h
Register Name: Checksum
Description: Used with MIC mode. The sum of the value of registers from 00h-4Ch must be equal to 2Eh for to compute a valid checksum after the EEPROM download..

Bit	Bit Description	Default	R/W
7:0	Checksum seed value	55h	R/W

Register Address: 02h
Register Name: MIC Control
Description: Identifies the number of devices on the serial bus when MIC programming mode is used.

Bit	Bit Description	Default	R/W
7:4	Reserved, set to 0000b	0000b	R/W
3:0	0000: No other devices on the serial bus 0001: 1 other device on the serial bus ⋮ 1101: 13 other devices on the serial bus (maximum number supported)	0000b	R/W

Register Address: 03h
Register Name: General Config
Description: Used to power up/power down device circuitry, configure crosspoint switching modes, clear alarms, and select squelch mode.

Bit	Bit Description	Default	R/W
7	0: Power up mode, normal operation 1: Power down mode	0b	R/W
6	Reserved, set to 0b	0b	R/W
5	0: Lane Switch Mode 1: Group Switch Mode	1b	R/W
4	0: Normal operation 1: Clear global alarms	0b	R/W
3	0: Switch setting updated with software strobe (address 05h) 1: Switch setting updated with hardware xSel pin	1b	R/W
2	Reserved, set to 0b	0b	R/W
1:0	00: Do not squelch 01: Output logic high on squelch 10: Output logic low on squelch 11: Output EBI level (common-mode) on squelch (recommended for AC coupled outputs)	11b	R/W

Register Address: 05h
Register Name: Strobe
Description: Configures the switch core setting changes.

Bit	Bit Description	Default	R/W
7	0: Selects ISC#1 as the active switch state upon a HW/SW strobe 1: Selects ISC#2 as the active switch state upon a HW/SW strobe	0b	R/W
6	0: When the device is configured for HW strobe mode (address 03h, bit 3), ISC#1 becomes active switch setting when xSEL pin is H, ISC#2 becomes the active switch setting when xSEL pin is L 1: When the device is configured for HW strobe mode (address 03h, bit 3), A transition from H to L on xSEL pin updates the active switch setting (ISC#1 or ISC#2 as determined by bit 7 of address 05h)	0b	R/W
5:0	000000: Normal operation 010101: When the device is configured for SW strobe mode (address 03h, bit 3), Software strobe to update the active switch setting (ISC#1 or ISC#2 as determined by bit 7 of address 05h)	000000b	R/W

Register Address: 06h, 07h
Register Name: Polarity Invert
Description: Inverts the polarity of the high-speed inputs.

Bit	Bit Description	Default	R/W
7	0: Reserved, set to 0b (address 06h), normal polarity for input 7 (address 07h) 1: Not Used (address 06h), inverted polarity for input 7 (address 07h)	0b	R/W
6	0: Reserved, set to 0b (address 06h), normal polarity for input 6 (address 07h) 1: Not Used (address 06h), inverted polarity for input 6 (address 07h)	0b	R/W
5	0: Reserved, set to 0b (address 06h), normal polarity for input 5 (address 07h) 1: Not Used (address 06h), inverted polarity for input 5 (address 07h)	0b	R/W
4	0: Reserved, set to 0b (address 06h), normal polarity for input 4 (address 07h) 1: Not Used (address 06h), inverted polarity for input 4 (address 07h)	0b	R/W
3	0: Normal polarity for input 11 (address 06h), input 3 (address 07h) 1: Inverted polarity for input 11 (address 06h), input 3 (address 07h)	0b	R/W
2	0: Normal polarity for input 10 (address 06h), input 2 (address 07h) 1: Inverted polarity for input 10 (address 06h), input 2 (address 07h)	0b	R/W
1	0: Normal polarity for input 9 (address 06h), input 1 (address 07h) 1: Inverted polarity for input 9 (address 06h), input 1 (address 07h)	0b	R/W
0	0: Normal polarity for input 8 (address 06h), input 0 (address 07h) 1: Inverted polarity for input 8 (address 06h), input 0 (address 07h)	0b	R/W

Register Address: 08h, 09h, 0Ah, 0Bh, 0Ch, 0Dh
Register Name: Active Switch Configuration (ASC)
Description: Contains the active crosspoint switch configuration for output channels. In group switch mode, only addresses 0Ch and 0Dh are used.

Bit	Bit Description	Default (Group Switch Mode)	Default (Lane Switch Mode)	R/W
7:4	Address 08h - Selects the input for output 11 (lane switch mode) Address 09h - Selects the input for output 9 (lane switch mode) Address 0Ah - Selects the input for output 7 (lane switch mode) Address 0Bh - Selects the input for output 5 (lane switch mode) Address 0Ch - Selects the input for output 3 (lane switch mode) Address 0Dh - Selects the input for output 1 (lane switch mode) or group 1 (group switch mode)	Address 08h - 0000 Address 09h - 0000 Address 0Ah - 0000 Address 0Bh - 0000 Address 0Ch - 0000 Address 0Dh - 0000 (Input group 0)	Address 08h - 1011 (Input 11) Address 09h - 1001 (Input 9) Address 0Ah - 0011 (Input 3) Address 0Bh - 0001 (Input 1) Address 0Ch - 0111 (Input 7) Address 0Dh - 0101 (Input 5)	R/W
3:0	Address 08h - Selects the input for output 10 (lane switch mode) Address 09h - Selects the input for output 8 (lane switch mode) Address 0Ah - Selects the input for output 6 (lane switch mode) Address 0Bh - Selects the input for output 4 (lane switch mode) Address 0Ch - Selects the input for output 2 (lane switch mode) or group 2 (group switch mode) Address 0Dh - Selects the input for output 0 (lane switch mode) or group 0 (group switch mode)	Address 08h - 0000 Address 09h - 0000 Address 0Ah - 0000 Address 0Bh - 0000 Address 0Ch - 0010 (Input group 2) Address 0Dh - 0001 (Input group 1)	Address 08h - 1010 (Input 10) Address 09h - 1000 (Input 8) Address 0Ah - 0010 (Input 2) Address 0Bh - 0000 (Input 0) Address 0Ch - 0110 (Input 6) Address 0Dh - 0100 (Input 4)	R/W

Register Address: 0Eh, 0Fh, 10h, 11h, 12h, 13h
Register Name: Intermediate Switch Configuration #1 (ISC #1)
Description: Contains ISC #1 for output channels. In group switch mode, only addresses 12h and 13h are used.

Bit	Bit Description	Default (Group Switch Mode)	Default (Lane Switch Mode)	R/W
7:4	Address 0Eh - Selects the input for output 11 (lane switch mode) Address 0Fh - Selects the input for output 9 (lane switch mode) Address 10h - Selects the input for output 7 (lane switch mode) Address 11h - Selects the input for output 5 (lane switch mode) Address 12h - Selects the input for output 3 (lane switch mode) Address 13h - Selects the input for output 1 (lane switch mode) or group 1 (group switch mode)	Address 0Eh - 0000 Address 0Fh - 0000 Address 10h - 0000 Address 11h - 0000 Address 12h - 0000 Address 13h - 0000 (Input group 0)	Address 0Eh - 1011 (Input 11) Address 0Fh - 1001 (Input 9) Address 10h - 0011 (Input 3) Address 11h - 0001 (Input 1) Address 12h - 0111 (Input 7) Address 13h - 0101 (Input 5)	R/W
3:0	Address 0Eh - Selects the input for output 10 (lane switch mode) Address 0Fh - Selects the input for output 8 (lane switch mode) Address 10h - Selects the input for output 6 (lane switch mode) Address 11h - Selects the input for output 4 (lane switch mode) Address 12h - Selects the input for output 2 (lane switch mode) or group 2 (group switch mode) Address 13h - Selects the input for output 0 (lane switch mode) or group 0 (group switch mode)	Address 0Eh - 0000 Address 0Fh - 0000 Address 10h - 0000 Address 11h - 0000 Address 12h - 0010 (Input group 2) Address 13h - 0001 (Input group 1)	Address 0Eh - 1010 (Input 10) Address 0Fh - 1000 (Input 8) Address 10h - 0010 (Input 2) Address 11h - 0000 (Input 0) Address 12h - 0110 (Input 6) Address 13h - 0100 (Input 4)	R/W

Register Address: 14h, 15h, 16h, 17h, 18h, 19h
Register Name: Intermediate Switch Configuration #2 (ISC #2)
Description: Contains ISC #2 for output channels. In group switch mode, only addresses 18h and 19h are used.

Bit	Bit Description	Default (Group Switch Mode)	Default (Lane Switch Mode)	R/W
7:4	Address 14h - Selects the input for output 11 (lane switch mode) Address 15h - Selects the input for output 9 (lane switch mode) Address 16h - Selects the input for output 7 (lane switch mode) Address 17h - Selects the input for output 5 (lane switch mode) Address 18h - Selects the input for output 3 (lane switch mode) Address 19h - Selects the input for output 1 (lane switch mode) or group 1 (group switch mode)	Address 14h - 0000 Address 15h - 0000 Address 16h - 0000 Address 17h - 0000 Address 18h - 0000 Address 19h - 0000 (Input group 0)	Address 14h - 0011 (Input 3) Address 15h - 0001 (Input 1) Address 16h - 0111 (Input 7) Address 17h - 0101 (Input 5) Address 18h - 1011 (Input 11) Address 19h - 1001 (Input 9)	R/W
3:0	Address 14h - Selects the input for output 10 (lane switch mode) Address 15h - Selects the input for output 8 (lane switch mode) Address 16h - Selects the input for output 6 (lane switch mode) Address 17h - Selects the input for output 4 (lane switch mode) Address 18h - Selects the input for output 2 (lane switch mode) or group 2 (group switch mode) Address 19h - Selects the input for output 0 (lane switch mode) or group 0 (group switch mode)	Address 14h - 0000 Address 15h - 0000 Address 16h - 0000 Address 17h - 0000 Address 18h - 0010 (Input group 2) Address 19h - 0001 (Input group 1)	Address 14h - 0010 (Input 2) Address 15h - 0000 (Input 0) Address 16h - 0110 (Input 6) Address 17h - 0100 (Input 4) Address 18h - 1010 (Input 10) Address 19h - 1000 (Input 8)	R/W

Register Address: 1Ah, 1Bh, 1Ch
Register Name: Input configuration A
Description: Configures buffers for high-speed inputs. In group switch mode, only address 1Ch is used.

Bit	Bit Description	Default	R/W
7:6	00: Input 11 (address 1Ah), input 7 (address 1Bh), input 3 (address 1Ch) powered down with high impedance (>100 kΩ single ended, 100Ω differential) termination 01: Input 11 (address 1Ah), input 7 (address 1Bh), input 3 (address 1Ch) powered down with source 50Ω single-ended (100Ω differential) termination 10: Input 11 (address 1Ah), input 7 (address 1Bh), input 3 (address 1Ch) powered on with high impedance (>100 kΩ single ended, 100Ω differential) termination 11: Input 11 (address 1Ah), input 7 (address 1Bh), input 3 (address 1Ch) powered on with source 50Ω single-ended (100Ω differential) termination	11	R/W
5:4	00: Input 10 (address 1Ah), input 6 (address 1Bh), input 2 (address 1Ch) powered down with high impedance (>100 kΩ single ended, 100Ω differential) termination 01: Input 10 (address 1Ah), input 6 (address 1Bh), input 2 (address 1Ch) powered down with source 50Ω single-ended (100Ω differential) termination 10: Input 10 (address 1Ah), input 6 (address 1Bh), input 2 (address 1Ch) powered on with high impedance (>100 kΩ single ended, 100Ω differential) termination 11: Input 10 (address 1Ah), input 6 (address 1Bh), input 2 (address 1Ch) powered on with source 50Ω single-ended (100Ω differential) termination	11	R/W
3:2	00: Input 9 (address 1Ah), input 5 (address 1Bh), input 1 (address 1Ch) powered down with high impedance (>100 kΩ single ended, 100Ω differential) termination 01: Input 9 (address 1Ah), input 5 (address 1Bh), input 1 (address 1Ch) powered down with source 50Ω single-ended (100Ω differential) termination 10: Input 9 (address 1Ah), input 5 (address 1Bh), input 1 (address 1Ch) powered on with high impedance (>100 kΩ single ended, 100Ω differential) termination 11: Input 9 (address 1Ah), input 5 (address 1Bh), input 1 (address 1Ch) powered on with source 50Ω single-ended (100Ω differential) termination	11	R/W
1:0	00: Input 8 (address 1Ah), input 4 (address 1Bh), input 0 (address 1Ch) powered down with high impedance (>100 kΩ single ended, 100Ω differential) termination 01: Input 8 (address 1Ah), input 4 (address 1Bh), input 0 (address 1Ch) powered down with source 50Ω single-ended (100Ω differential) termination 10: Input 8 (address 1Ah), input 4 (address 1Bh), input 0 (address 1Ch) powered on with high impedance (>100 kΩ single ended, 100Ω differential) termination 11: Input 8 (address 1Ah), input 4 (address 1Bh), input 0 (address 1Ch) powered on with source 50Ω single-ended (100Ω differential) termination	11	R/W

Register Address: 1Dh, 1Eh, 1Fh, 20h, 21h, 22h, 23h, 24h, 25h, 26h, 27h, 28h
Register Name: Input Equalization
Description: Sets the equalization for input 11 (address 1Dh), input 10 (address 1Eh), input 9 (address 1Fh), input 8 (address 20h), input 7 (address 21h), input 6 (address 22h), input 5 (address 23h), input 4(address 24h), input 3 (address 25h), input 2/Group 2 (address 26h), input 1/Group 1 (address 27h), input 0/Group 0 (address 28h). In group mode, only addresses 26h, 27h, and 28h are used.

Bit	Bit Description	Default	R/W
7:0	00h: Equalization level 1—Minimum Equalization 20h: Equalization level 2 11h: Equalization level 3 21h: Equalization level 4 31h: Equalization level 5 A1h: Equalization level 6 29h: Equalization level 7 33h: Equalization level 8 37h: Equalization level 9 45h: Equalization level 10 59h: Equalization level 11 5Eh: Equalization level 12 6Eh: Equalization level 13 7Fh: Equalization level 14 FAh: Equalization level 15 FFh: Equalization level 16—Maximum Equalization	37h	R/W

Register Address: 35h, 36h, 37h, 38h, 39h, 3Ah, 3Bh, 3Ch, 3Dh, 3Eh, 3Fh, 40h
Register Name: Input configuration B
Description: Configures the LOS, squelch, and EBI functionality for input 11 (address 35h), input 10 (address 36h), input 9 (address 37h), input 8 (address 38h), input 7 (address 39h), input 6 (address 3Ah), input 5 (address 3Bh), input 4 (address 3Ch), input 3 (address 3Dh), input 2/group (address 3Eh), input 1/group (address 3Fh), input 0/group (address 40h). In group switch mode, only addresses 3Eh, 3Fh, and 40h are used.

Bit	Bit Description	Default	R/W
7:6	Reserved, set to 11b	11b	R/W
5	0: LOS Enabled 1: LOS Disabled	0b	R/W
4:3	Reserved, set to 00b	00b	R/W
2	0: Normal operation 1: Force squelch on input channel	0b	R/W
1	Reserved, set to 0b	0b	R/W
0	0: Disable EBI pass through mode 1: Enable EBI pass through mode	0b	R/W

Register Address: 41h, 42h, 43h, 44h, 45h, 46h, 47h, 48h, 49h, 4Ah, 4Bh, 4Ch
Register Name: Output configuration
Description: Configures the output swing and de-emphasis for output 11 (address 41h), output 10 (address 42h), output 9 (address 43h), output 8

(address 44h), output 7 (address 45h), output 6 (output 46h), output 5 (address 47h), output 4 (address 48h), output 3 (address 49h), output 2/Group 2 (address 4Ah), output 1/Group 1 (address 4Bh), output 0/Group 0 (address 4Ch). In group switch mode, only addresses 4Ah, 4Bh, and 4Ch are used.

Bit	Bit Description	Default	R/W
7:5	00X: Power down 010: Minimum output swing 011: Nominal output swing ⋮ 111: Maximum output swing	000b	R/W
4	Reserved, set to 0b	0b	R/W
3:2	00: Output de-emphasis disabled 01: Approximately 2 dB output de-emphasis 10: Approximately 4 dB output de-emphasis 11: Approximately 6 dB output de-emphasis	00b	R/W
1	0: Nominal de-emphasis time constant 1: Higher de-emphasis time constant	0b	R/W
0	Reserved, set to 0b	0b	R/W

Register Address: C3h, C4h
Register Name: LOS Alarm Status
Description: Monitors the LOS alarm status for input channels. LOS alarms are latched into this register once asserted. This register is cleared by setting bit 4 of address 03h to "1" and then back to "0"

Bit	Bit Description	Default	R/W
7	0: Reserved (address C3h), No LOS on input 7 (address C4h) 1: Reserved (address C3h), LOS on input 7 (address C4h)	N/A	R
6	0: Reserved (address C3h), No LOS on input 6 (address C4h) 1: Reserved (address C3h), LOS on input 6 (address C4h)	N/A	R
5	0: Reserved (address C3h), No LOS on input 5 (address C4h) 1: Reserved (address C3h), LOS on input 5 (address C4h)	N/A	R
4	0: Reserved (address C3h), No LOS on input 4 (address C4h) 1: Reserved (address C3h), LOS on input 4 (address C4h)	N/A	R
3	0: No LOS on input 11 (address C3h), input 3 (address C4h) 1: LOS on input 11 (address C3h), input 3 (address C4h)	N/A	R
2	0: No LOS on input 10 (address C3h), input 2 (address C4h) 1: LOS on input 10 (address C3h), input 2 (address C4h)	N/A	R
1	0: No LOS on input 9 (address C3h), input 1 (address C4h) 1: LOS on input 9 (address C3h), input 1 (address C4h)	N/A	R
0	0: No LOS on input 8 (address C3h), input 0 (address C4h) 1: LOS on input 8 (address C3h), input 0 (address C4h)	N/A	R

Register Address: FCh
Register Name: MIC Checksum
Description: After an EEPROM download, this register contains the checksum calculated value. If this value is not equal to 2Eh after an MIC download, there was either an issue with the download or the checksum seed value in register 01h is not correct.

Bit	Bit Description	Default	R/W
7:0	MIC Checksum Calculated Value	00h	R

Register Address: FDh
Register Name: Chip Code
Description: Contains the Chip ID code.

Bit	Bit Description	Default	R/W
7:0	Device Identification Register	20h	R

Register Address: FEh
Register Name: Chip Revision
Description: Contains the Chip revision number.

Bit	Bit Description	Default	R/W
7:0	Device Revision Register M21353G-13 = 02h	---	R

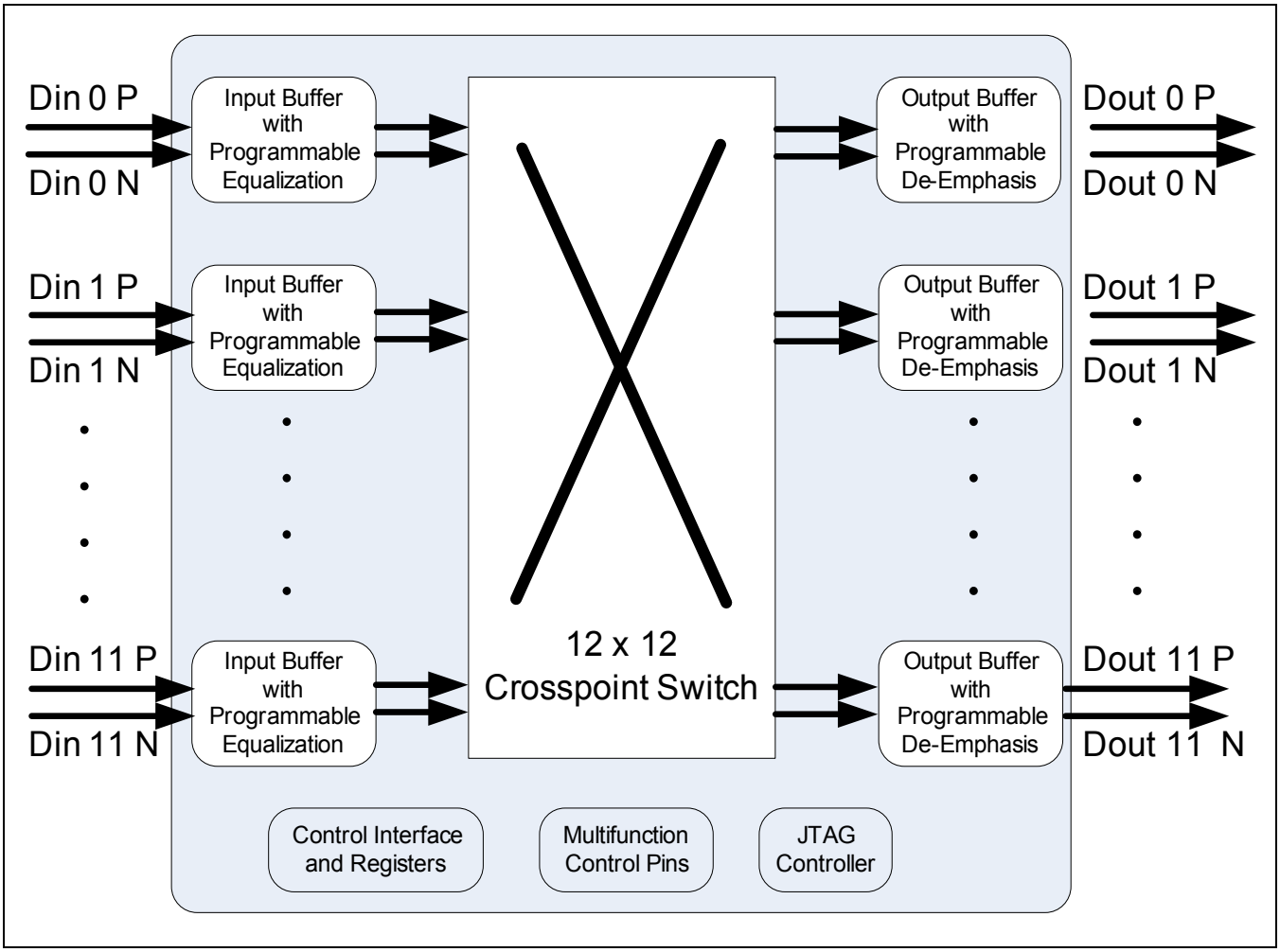
Register Address: FFh
Register Name: Master Reset
Description: Used to perform master reset of device. Write "AAh" to this register, followed by a second write of "00h" to perform a master reset.

Bit	Bit Description	Default	R/W
7:0	00h: Normal Operation AAh: Reset	00h	R/W

5.0 Functional Description

The M21353 is a twelve channel device with programmable input equalization, programmable output de-emphasis, and an embedded 12x12 crosspoint switch matrix. Details on various functionality and features are described in the following sections.

Figure 5-1. Functional Block Diagram



5.1 Power Supply

The M21353 includes four distinct power supply domains: AVDDCORE, DVDDCORE, AVDDIO, and DVDDIO.

AVDDCORE powers the analog core circuitry in the device, and must be set to 1.2V.

DVDDCORE powers the digital core circuitry in the device, and must be set to 1.2V.

AVDDIO powers the input/output circuits in the device, and can be set to either 1.2V or 1.8V. Note that to achieve output swing levels higher than 800 mVppd, AVDDIO must be set to 1.8V.

DVDDIO powers the digital circuitry within the device, and can be set to 1.2V, 1.8V, 2.5V, or 3.3V to allow for interface with various external digital devices. It is recommended that DVDDIO is connected to the same voltage level as any digital devices that are used to control the M21353.

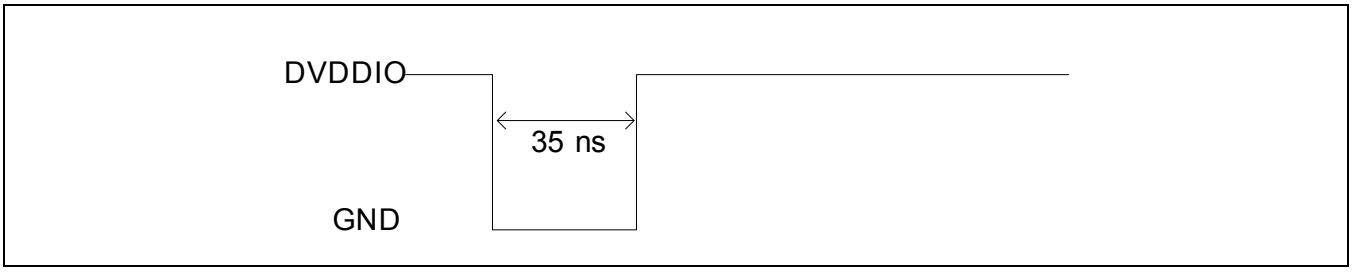
5.2 Input and Output Buffers

The input buffers in the M21353 are designed to work with AC coupled input signals, and support operation with a wide range of AC coupling capacitor values. Applications that use PRBS and/or 8b/10b encoded data will typically use AC coupling capacitors with a value of 0.1 uF. SDI video applications will typically use AC coupling capacitors with a value of 4.7 uF or larger. The output buffers are designed with PCML logic, and can operate with either AC coupled or DC coupled systems. To enable support for the PCIe receiver detect function, the input buffer can be configured in a high-impedance state where the single ended input impedance is greater than 100 kΩ. The input buffer should not be configured in a high-impedance state when data needs to be passed through the M21353. For typical operation, the input buffer should be enabled with a 50Ω single ended (100Ω differential) termination. The high-speed outputs are powered-down by default, and should be set to the desired output swing level using registers 41h-4Ch.

5.3 LOS Alarm

There is signal detect circuit that will assert an alarm if the signal level at the input of the device is lower than the assert threshold level of the LOS circuit of the squelch is forced on for an input. Once asserted, the alarm will remain asserted until the signal is above the de-assert threshold level of the LOS circuit or the force squelch on an input channel has been removed. There is hysteresis between the assert and de-assert levels to prevent chattering of the LOS alarm. Please refer to Figure 2-11 for an illustration of the typical LOS assert/de-assert behavior. The LOS circuit should be disabled when used with strings of 1010 data that last for more than approximately 3 μs to avoid false LOS alarms. The LOS alarm status register (address C3h, C4h), will latch when the LOS alarm for a channel is asserted, and will remain latched until them is cleared by setting bit 4 of address 03h to '1', and then back to '0'. When the LOS alarm is asserted and register 00h[3]=0b, the xALARM pin will send one interrupt pulse with a pulse width of approximately 35 ns as shown in Figure 5-2 below.

Figure 5-2. Timing of xAlarm Interrupt Signal



5.4 Input Equalization

Each input channel of the M21353 includes an input equalizer, design to compensate for bandwidth limitations of PCB traces. The equalizer operates in a programmable mode, where a fixed equalization setting is selected. There are 16 equalization settings available, which are programmed through register addresses 1Dh–28h when the device is used in lane switching mode. When the device is used in group switching mode (default mode), the input equalization setting is configured for the entire group using registers addresses 26h, 27h, and 28h. Addresses 1Dh-25h are not used when the device is in group switching mode. See the register description table for details on how to select each equalization level. It is recommended that each channel of the system is characterized once to optimize the equalization for each system channel.

5.5 Output De-emphasis

Each output buffer of the M21353 includes a de-emphasis circuit that is configured by the user. There is approximately 6 dB of de-emphasis available, and the de-emphasis levels are selectable through registers 41h-4Ch. Note that when the device is used in group switching (default) mode, the output de-emphasis is set for each group using registers 4Ah, 4Bh, and 4Ch.

5.6 Electrical Bus Idle Pass-through

Some protocols, such as SATA/SAS and PCIe, define a third logic state at the common mode for transmission of an electrical bus idle (EBI) level. In SAS/SATA systems, OOB signals such as COMRESET, COMWAKE, and COMSAS utilize burst and idle levels for communication. The M21353 is designed to pass the electrical bus idle through the device to support SATA/SAS and PCIe protocol requirements. When the EBI feature of the M21353 is enabled, the device will detect and pass EBI signals with minimal distortion of the signal. The EBI circuit is controlled through registers 35h-40h.

5.7 Squelch

To avoid random chattering of the output due to noise when there is no signal present at the inputs, the M21353 includes a squelch feature to automatically inhibit the output when there is a LOS alarm. There is an option to inhibit to either logic H, logic L, or the EBI common mode level on squelch. In addition to the automatic squelch feature, a manual squelch can be forced through a register setting. When an input channel is squelched, any output configured to be connected to the squelched input will be H, L, or F depending on the selected squelch level. LOS should either be disabled or set to "never squelch" when the EBI circuit is enabled to allow the device to detect data bursts quickly after electrical idle periods that last longer than approximately 5 us. The squelch circuit is controlled through register 03h, and also through registers 35h-40h.

5.8 Operation in SDI Video Applications

The M21353 can pass pathological video data error-free for SD-SDI, HD-SDI, and 3G-SDI data rates. for optimal performance, AC coupling capacitors with a minimum value of 4.7 uF should be used on the high-speed inputs and outputs of the M21353. Also, the amplitude used to drive a signal across a system backplane should be increased in systems that pass SDI video as noted in the input launch amplitude specification in Table 1-4.

5.9 Crosspoint Switch Core

The 12x12 crosspoint switch core is configured through the Active Switch Configuration, Intermediate Switch Configuration #1, and Intermediate Switch Configuration #2 registers. The switch supports multicast and broadcast modes.

The current switch configuration is stored in the “Active Switch Configuration” (ASC) registers, addresses 08h-0Dh. The switch configuration is updated immediately when a write operation to these registers takes place. One ASC register controls two output channels, so two crosspoint switch paths can be updated at a time by writing directly to the ASC registers. To configure a crosspoint switch path, the input channel is used as the register data value, and the output channel is the register address that is used. For example, to configure the crosspoint core so that input channel 2 is routed to output channel 0, write data = '0010' into register 0Dh[3:0]. Register 0Dh contains the active switch configuration for outputs 0 and 1, so the data for the desired input channel for output channel 1 would also need to be written into register 0Dh[7:4].

To allow for immediate reconfiguration of one to all crosspoint switch paths, there are two “Intermediate Switch Configuration” (ISC#1 and ISC#2) registers located in addresses 0Eh-19h. These registers allow for a new crosspoint switch configuration to be loaded into the registers in advance. When a “strobe” event occurs, the ASC registers will be updated with the contents from the appropriate “ISC” register, and the entire switch core configuration is updated. The switch core can be updated through either a software “strobe” in register 05h, or a hardware strobe by toggling the xSEL hardware pin. When a software strobe is being used, bit 7 of register address 05h is used to select which ISC register is used when the ASC is updated. When the M21353 is configured for hardware strobe mode by setting bit 3 of register address 03h to "1", the xSEL hardware pin is used to update the ASC contents. The device can be configured in two different hardware strobe modes with bit 6 of register address 05h. With this bit set to "0", ISC #1 is the active switch configuration when xSEL is H, and ISC #2 is the active switch configuration when xSEL is L. With this bit set to "1", a H to L transition on the xSel pin will update the active switch configuration register with ISC #1 or ISC #2 as determined by bit 7 of register address 05h.

The switch core can be programmed in two modes, group switch mode or lane switch mode. In group switch mode, four high-speed channels are treated as one group and switched together. Group 0 includes Input/Output channels 0,1, 2, and 3; Group 1 includes Input/Output channels 4, 5, 6, and 7; Group 2 includes Input/Output channels 8, 9, 10, and 11.

In lane switch mode, each high speed channel is independent and switched individually. By default, the device is in group switch mode with the following switch core configuration:

Input group 0 ---> Output group 1
Input group 1 ---> Output group 0
Input group 2 ---> Output group 2

The group switch configuration can be updated by writing to the group switch ASC, ISC #1, and ISC #2 registers, addresses 08h-19h.

If the M21353 is being used in a protection switching application, two alternate switch states can be stored in each ISC register, and the HW strobe can be used to select between the two switch settings. This mode is enabled by default. Figures 5-3 and 5-4 show how the M21353 can be used in a protection switching application using the default group switch mode settings.

Figure 5-3. M21353 Default ASC/ISC # 1 in group switch mode

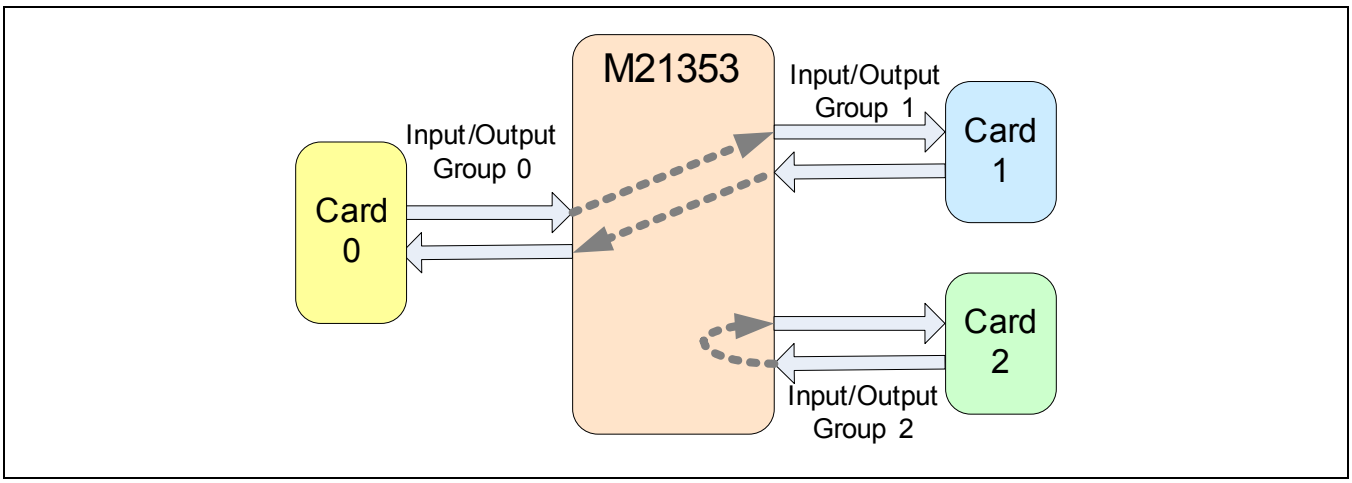
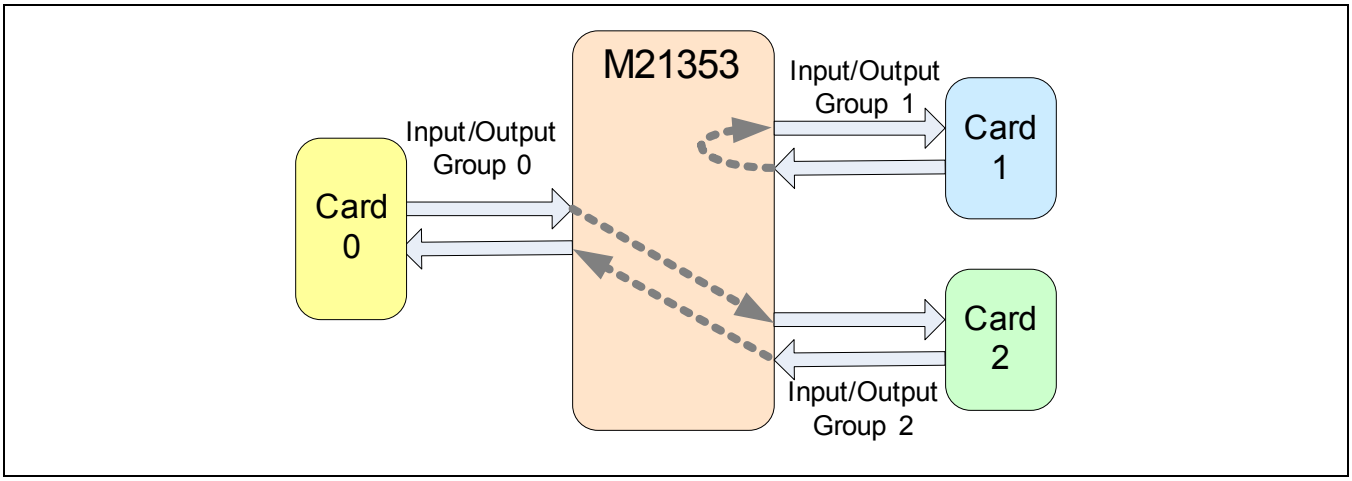


Figure 5-4. M21353 Default ISC # 2 in group switch mode



5.10 Control Options

There are two control modes available for the M21353. To control using a two wire, I²C compatible programming interface, the device can be configured for Software Interface Control (SIC). The M21353 can also self configure from an external EEPROM when the Memory Interface Control (MIC) mode is selected. In addition to the two control modes, the M21353 also supports boundary scan through a JTAG port. The boundary scan mode is enabled by setting the ADDR2 and ADDR1 pins to the logic floating level.

To configure the device for Boundary Scan or Memory Interface Control Mode, configure the ADDR2, ADDR1, and ADDR0 pins as shown:

Table 5-1. Control Mode

Operating Mode	ADDR2	ADDR1	ADDR0
Memory Interface Control (EEPROM)	X	F	H
Boundary Scan	F	F	X

5.11 Boundary Scan Operation

In order to test external connections to and from the M21353, the device includes support for boundary scan through a JTAG port when configured for boundary scan mode. Boundary scan is supported on control pins and high-speed input pins. Boundary scan is not supported on high-speed output pins.

When the M21353 is in boundary scan test mode, the following pins are used for JTAG signals:

Table 5-2. Boundary Scan Mode Functionality

Pin Name	Pin Number	Functionality in Boundary Scan Mode
SDA	24	TMS
SCL	22	TCLK
ADDR0	88	TDI
xSEL	21	TDO

5.12 Software Interface Control Mode Operation

The functionality of the M21353 is controlled through register settings. Refer to Sections 4.1 and 4.2 for a full description of the registers available within the M21353. To access the registers, an I²C compatible, two-wire programming interface is available in the device. The two-wire device address is determined by the status of the pins ADDR [2:0]. The table below shows the address for each combination of settings for ADDR [2:0].

Table 5-3. Two Wire Serial Device Address (1 of 2)

ADDR2	ADDR1	ADDR0	M21353 Device Address	Mode
F	x	x	None	Reserved
H or L	F	H	0100000	MIC mode
H or L	F	L	0100000	SIC mode

Table 5-3. Two Wire Serial Device Address (2 of 2)

ADDR2	ADDR1	ADDR0	M21353 Device Address	Mode
L	L	L	0100001	SIC mode
L	L	H	0100010	SIC mode
L	H	L	0100011	SIC mode
L	H	H	0100100	SIC mode
H	L	L	0100101	SIC mode
H	L	H	0100110	SIC mode
H	H	L	0100111	SIC mode
H	H	H	0101000	SIC mode
L	L	F	0101001	SIC mode
L	H	F	0101010	SIC mode
H	L	F	0101011	SIC mode
H	H	F	0101100	SIC mode

The two wire programming interface is designed to drive 500 pF at 100 and 400 kHz, and 100 pF at 3.4 MHz operation. During a write operation, data is latched into the M21353 registers on the rising edge of SCL during the acknowledge phase (ACK) of communication. Refer to the I^2C buss specification standard for timing information that is applicable to the two-wire programming interface.

5.13 Memory Interface Control Mode Operation

With the M21353 configured for Memory Interface Control (MIC) operation, a single M21353 device or an array of M21353 devices can self configure from a single EEPROM with a two wire serial programming interface upon device power up.

If the M21353 is configured for MIC operation at power up, the M21353 interface operates as a temporary two wire quasi-master operating at 100 kHz when downloading from external memory and 400 kHz when configuring other M21353 devices. In an array of M21353 devices, only one device should be configured for MIC operation, and subsequent devices in the array should be configured for SIC operation. All devices in an array will receive the same configuration. When the M21353 device begins to self configure, it will read the contents of an external EEPROM and configure its registers accordingly. The expected EEPROM device address is 1010000b, and the M21353 quasi master device address should be set to 0100000b.

Register 01h is used to load the checksum seed value. The checksum seed value should be selected such that the 8 LSB of the sum of the register values from address 00h through 4Ch is equal to 2Eh. After the download from the EEPROM, the checksum value is computed and written into register address FCh. If the checksum value is equal to 2Eh, then this is recognized as a valid checksum and the quasi-master device will continue to program other device on the interface buss. If the checksum value is not equal to 2Eh, the quasi master device will repeat the download process and look for the correct checksum value up to 512 times before timing out. If the correct checksum value is not detected, the quasi-master device will not configure any additional devices on the interface buss.

Register address 02h is used to identify the number of M21353 devices that will be self configured by the quasi master in MIC mode. When multiple M21353 devices are self configured in an array, the quasi master M21353 device will copy its register contents into other devices in the array sequentially using a 400 kHz interface buss. The devices in the array must have sequential programming addresses, starting with 0100000b for the quasi master

device. After the last device in the M21353 array has been configured, the device will revert to normal two-wire serial programmed operation.

If the MIC mode is used in conjunction with an external host controller, the two wire interface on the host controller must not interrupt the programming buss while self configuration is taking place. This can be ensured by timing out the host controller for N x 0.8 seconds (N= number of M21353 devices in the self configure array), or by monitoring the SDA/SCL buss for activity.

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