ZARLINK SEMICONDUCTOR

ISO^2-CMOS MT9196
Integrated Digital Phone Circuit (IDPC)

Data Sheet

January 2006

Features

- Programmable m-Law/A-Law CODEC and Filters
- Programmable CCITT (G.711)/sign-magnitude coding
- Programmable transmit, receive and side-tone gains
- Digital DTMF and single tone generation
- Fully differential interface to handset transducers
- Auxiliary analog interface
- Interface to ST-BUS/SSI (compatible with GCI)
- Serial microport control
- Single 5 volt supply, low power operation
- Anti-howl circuit for group listening speakerphone applications

Applications

- Digital telephone sets
- Wireless telephones
- Local area communications stations

Ordering Information

MT9196AP	28 Pin PLCC	Tubes
MT9196AE	28 Pin PDIP	Tubes
MT9196AS	28 Pin SOIC	Tubes
MT9196ASR	28 Pin SOIC	Tape & Reel
MT9196APR	28 Pin PLCC	Tape & Reel
MT9196AE1	28 Pin PDIP*	Tubes
MT9196APR1	28 Pin PLCC*	Tape & Reel
MT9196AP1	28 Pin PLCC*	Tubes
MT9196AS1	28 Pin SOIC*	Tubes
MT9196ASR1	28 Pin SOIC*	Tape & Reel

*Pb Free Matte Tin

-40°C to +85°C

Description

The MT9196 Integrated Digital Phone Circuit (IDPC) is designed for use in digital phone products. The device incorporates a built-in Filter/Codec, digital gain pads, DTMF generator and tone ringer. Complete telephony interfaces are provided for connecting to handset and speakerphone transducers. Internal register access is provided through a serial microport compatible with various industry standard micro-controllers.

The device is fabricated in Zarlink's ISO^2-CMOS technology ensuring low power consumption and high reliability.

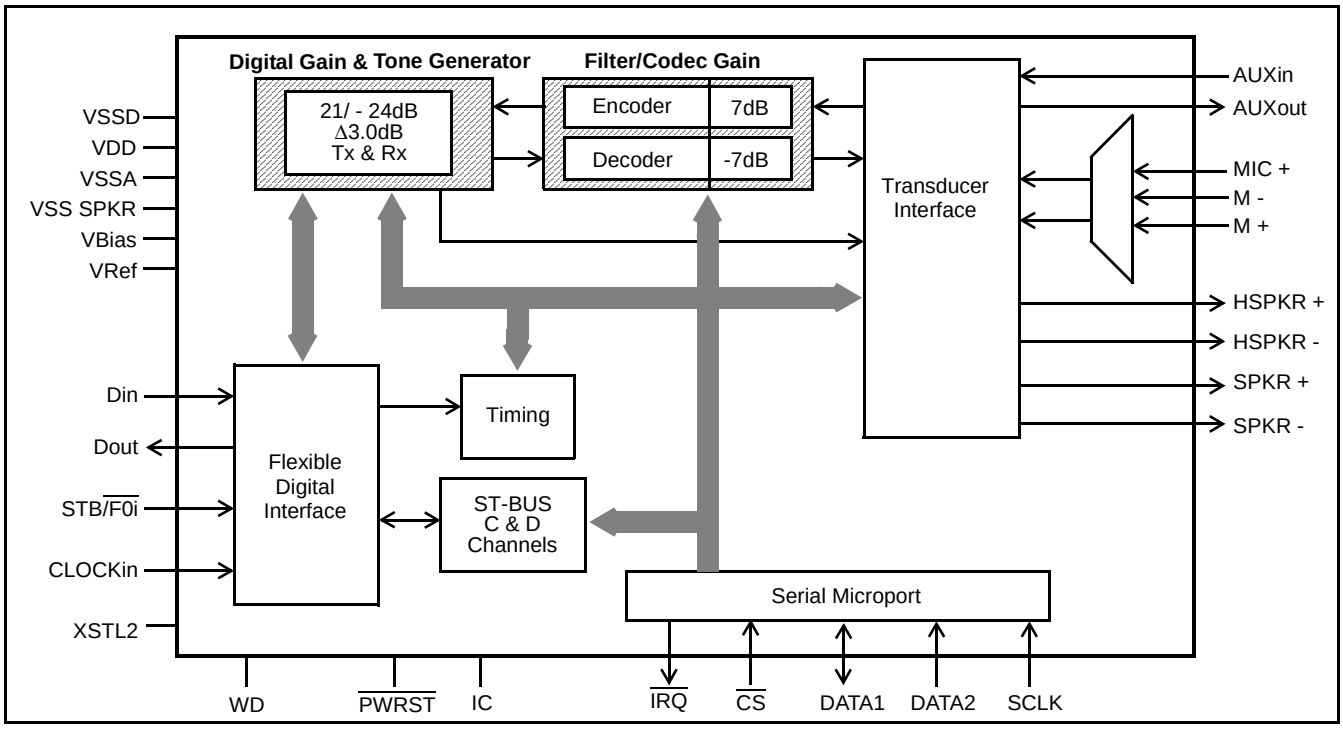


Figure 1 - Functional Block Diagram

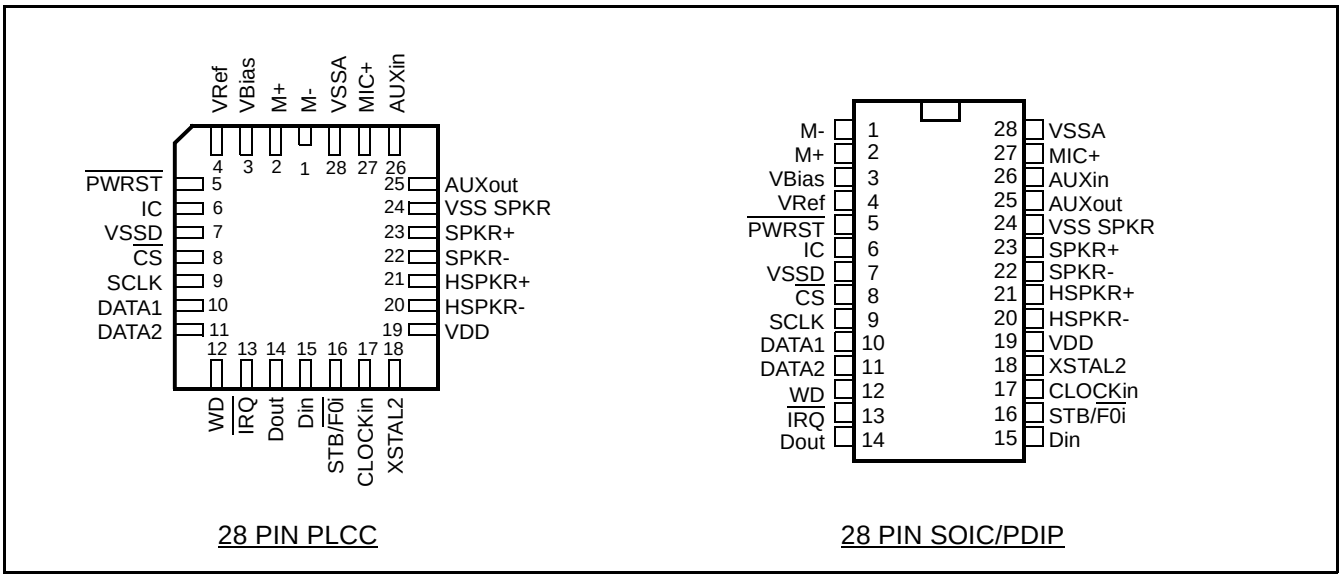


Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	M-	**Inverting Microphone (Input).** Inverting input to microphone amplifier from the handset microphone.
2	M+	**Non-Inverting Microphone (Input).** Non-inverting input to microphone amplifier from the handset microphone.
3	V_{Bias}	**Bias Voltage (Output).** (V_{DD}/2) volts is available at this pin for biasing external amplifiers. Connect 0.1 µF capacitor to V_{SSA}.
4	V_{Ref}	**Reference voltage for codec (Output).** Nominally [(V_{DD}/2)-1.5] volts. Used internally. Connect 0.1 µF capacitor to V_{SSA}.
5	$\overline{PWRST}$	**Power-up Reset (Input).** CMOS compatible input with Schmitt Trigger (active low).
6	IC	**Internal Connection.** Tie externally to V_{SS} for normal operation.
7	V_{SSD}	**Digital Ground.** Nominally 0 volts.
8	$\overline{CS}$	**Chip Select (Input).** This input signal is used to select the device for microport data transfers. Active low. TTL level compatible.
9	SCLK	**Serial Port Synchronous Clock (Input).** Data clock for microport. TTL level compatible.
10	DATA1	**Bidirectional Serial Data.** Port for microprocessor serial data transfer. In Motorola/National mode of operation, this pin becomes the data transmit pin only and data receive is performed on the DATA2 pin. TTL level compatible input levels.
11	DATA2	**Serial Data Receive.** In Motorola/National mode of operation, this pin is used for data receive to the IDPC. In Intel mode, serial data transmit and receive are performed on the DATA1 pin and DATA2 is disconnected. Input level TTL compatible.
12	WD	**Watchdog (Output).** Watchdog timer output. Active high.
13	IRQ	**Interrupt Request (Open Drain Output).** Low true interrupt output to microcontroller.

Pin Description (continued)

Pin #	Name	Description
14	D_{out}	**Data Output.** A tri-state digital output for 8 bit wide channel data being sent to the Layer 1 device. Data is shifted out via this pin concurrent with the rising edge of BCL during the timeslot defined by STB, or according to standard ST-BUS timing.
15	D_{in}	**Data Input.** A digital input for 8 bit wide channel data received from the Layer 1 device. Data is sampled on the falling edge of BCL during the timeslot defined by STB, or according to standard ST-BUS timing. Input level is CMOS compatible.
16	STB/$\overline{F0i}$	**Data Strobe/Frame Pulse (Input).** For SSI mode this input determines the 8 bit timeslot used by the device for both transmit and receive data. This active high signal has a repetition rate of 8 kHz. Standard frame pulse definitions apply in ST-BUS mode. CMOS level compatible input.
17	CLOCKin	**Clock Input.** The clock provided to this input is used by the internal phone functions. In ST-BUS mode this is the $\overline{C4i}$ input. In SSI synchronous mode, this is the Bit Clock input. In SSI-asynchronous mode this is an asynchronous 4 MHz Master Clock input.
18	XSTL2	**Crystal Input (4.096 MHz).** Used in conjunction with the CLOCKin pin to provide the master clock signal via external crystal.
19	V_{DD}	**Positive Power Supply (Input).** Nominally 5 volts.
20	HSPKR-	**Inverting Handset Speaker (Output).** Output to the handset speaker (balanced).
21	HSPKR+	**Non-Inverting Handset Speaker (Output).** Output to the handset speaker (balanced).
22	SPKR-	**Inverting Speaker (Output).** Output to the speakerphone speaker (balanced).
23	SPKR+	**Non-Inverting Speaker (Output).** Output to the speakerphone speaker (balanced).
24	V_{SS}SPKR	**Power Supply Rail for Speaker Driver.** Nominally 0 Volts.
25	AUX_{out}	**Auxiliary Port (Output).** Access point to the D/A (analog) signals of the receive path as well as to the various analog inputs.
26	AUX_{in}	**Auxiliary Port (Input).** An analog signal may be fed to the filter/codec transmit section and various loopback paths via this pin. No external anti-aliasing is required.
27	MIC+	**Non-inverting on-hook answer back Microphone (Input).** Microphone amplifier non-inverting input pin.
28	V_{SSA}	**Analog Ground (Input).** Nominally 0 V.

Overview

The functional block diagram of Figure 1 depicts the main operations performed by the MT9196 IDPC. Each of these functional blocks will be described individually in the sections to follow. This overview will describe some of the end-user features which may be implemented as a direct result of the level of integration found within the IDPC.

The main feature required of a digital telephone is to convert the digital Pulse Code Modulated (PCM) information, being received by the telephone set, into an analog electrical signal. This signal is then applied to an appropriate audio transducer such that the information is finally converted into intelligible acoustic energy. The same is true of the reverse direction where acoustic energy is converted first into an electrical analog and then digitized (into PCM) before being transmitted from the set. Along the way if the signals can be manipulated, either in the analog or the digital domains, other features such as gain control and signal generation may be added. Finally, most electro-acoustic transducers (loudspeakers) require a large amount of power if they are to develop an acoustic signal. The inclusion of audio amplifiers to provide this power is required.

The IDPC features complete Analog/Digital and Digital/Analog conversion of audio signals (Filter/CODEC) and an analog interface to electro-acoustic devices (Transducer Interface). Full programmability of the receive path and side-tone gains is available to set comfortable listening levels for the user. Transmit path gain control is available for setting nominal transmit levels into the network. A digital, anti-feedback circuit permits both the handset microphone and the speaker-phone speaker to be enabled at the same time for group listening applications. This anti-feedback circuit limits the total loop gain there by preventing a singing condition from developing.

Signalling in digital telephone systems, behind the PBX or standard ISDN applications, is handled on the D-channel and generally does not require DTMF tones. Locally generated tones, in the set, however, can be used to provided “comfort tones” or “key confirmation” to the user, similar to the familiar DTMF tones generated by conventional phones during initial call set-up. Also, as the network slowly evolves from the dial pulse/DTMF methods to the D-Channel protocols it is essential that the older methods be available for backward compatibility. As an example, once a call has been established (i.e., from your office to your home) using the D-Channel signalling protocol it may be necessary to use in-band DTMF signalling to manipulate your personal answering machine in order to retrieve messages. Thus the locally generated tones must be of network quality. The IDPC can generate the required tone pairs as well as single tones to accommodate any in-band signalling requirement.

Each of the programmable parameters within the functional blocks is accessed through a serial microcontroller port compatible with Intel MCS-51®, Motorola SPI® and National Semiconductor Microwire® specifications.

Functional Description

In this section each of the functional blocks within IDPC is described along with all of the associated control/status bits. Each time a control/status bit(s) is described it is followed by the address register where it will be found. The reader is referred to the section titled 'Register Summary' for a complete listing of all address registers, the control/status bits associated with each register and a definition of the function of each control/status bit. The Register Summary is useful for future reference of control/status bits without the need to locate them in the text of the functional descriptions.

Filter/CODEC

The Filter/CODEC block implements conversion of the analog 3.3 kHz speech signals to/from the digital domain compatible with 64 kb/s PCM B-Channels. Selection of companding curves and digital code assignment are register programmable. These are CCITT G.711 A-law or μ-Law, with true-sign/ Alternate Digit Inversion or true-sign/Inverted Magnitude coding, respectively. Optionally, sign- magnitude coding may also be selected for proprietary applications.

The Filter/CODEC block also implements transmit and receive audio path gains in the analog domain. These gains are in addition to the digital gain pad section and provide an overall path gain resolution of 1.0 dB. A programmable gain, voice side-tone path is also included to provide proportional transmit speech feedback to the handset receiver. Figure 3 depicts the nominal half-channel and side-tone gains for the IDPC.

On $\overline{\text{PWRST}}$ (pin 5) the Filter/CODEC defaults such that the side-tone path, dial tone filter and 400 Hz transmit filter are off, all programmable gains are set to 0 dB and CCITT μ-Law is selected. Further, the Filter/CODEC is powered down due to the control bits of the Path Control Registers (addresses 12h and 13h) being reset.

The internal architecture is fully differential to provide the best possible noise rejection as well as to allow a wide dynamic range from a single 5 volt supply design. This fully differential architecture is continued into the Transducer Interface section to provide full chip realization of these capabilities for the handset and loudspeaker functions.

A reference voltage (V_{Ref}), for the conversion requirements of the CODEC section, and a bias voltage (V_{Bias}), for biasing the internal analog sections, are both generated on-chip. V_{Bias} is also brought to an external pin so that it may be used for biasing external gain plan setting amplifiers. A 0.1 μF capacitor must be connected from V_{Bias} to analog ground at all times. Likewise, although V_{Ref} may only be used internally, a 0.1 μF capacitor from the V_{Ref} pin to ground is required at all times. The analog ground reference point for these two capacitors must be physically the same point. To facilitate this the V_{Ref} and V_{Bias} pins are situated on adjacent pins.

The transmit filter is designed to meet CCITT G.714 specifications. The nominal gain for this filter path is 0 dB (gain control = 0 dB). Gain control allows the output signal to be increased up to 7 dB. An anti-aliasing filter is included. This is a second order lowpass implementation with a corner frequency at 25 kHz. Attenuation is better than 32 dB at 256 kHz and less than 0.01 dB within the passband.

An optional 400 Hz high-pass function may be included into the transmit path by enabling the Tfhp bit in the Control Register 1 (address 0Eh). This option allows the reduction of transmitted background noise such as motor and fan noise.

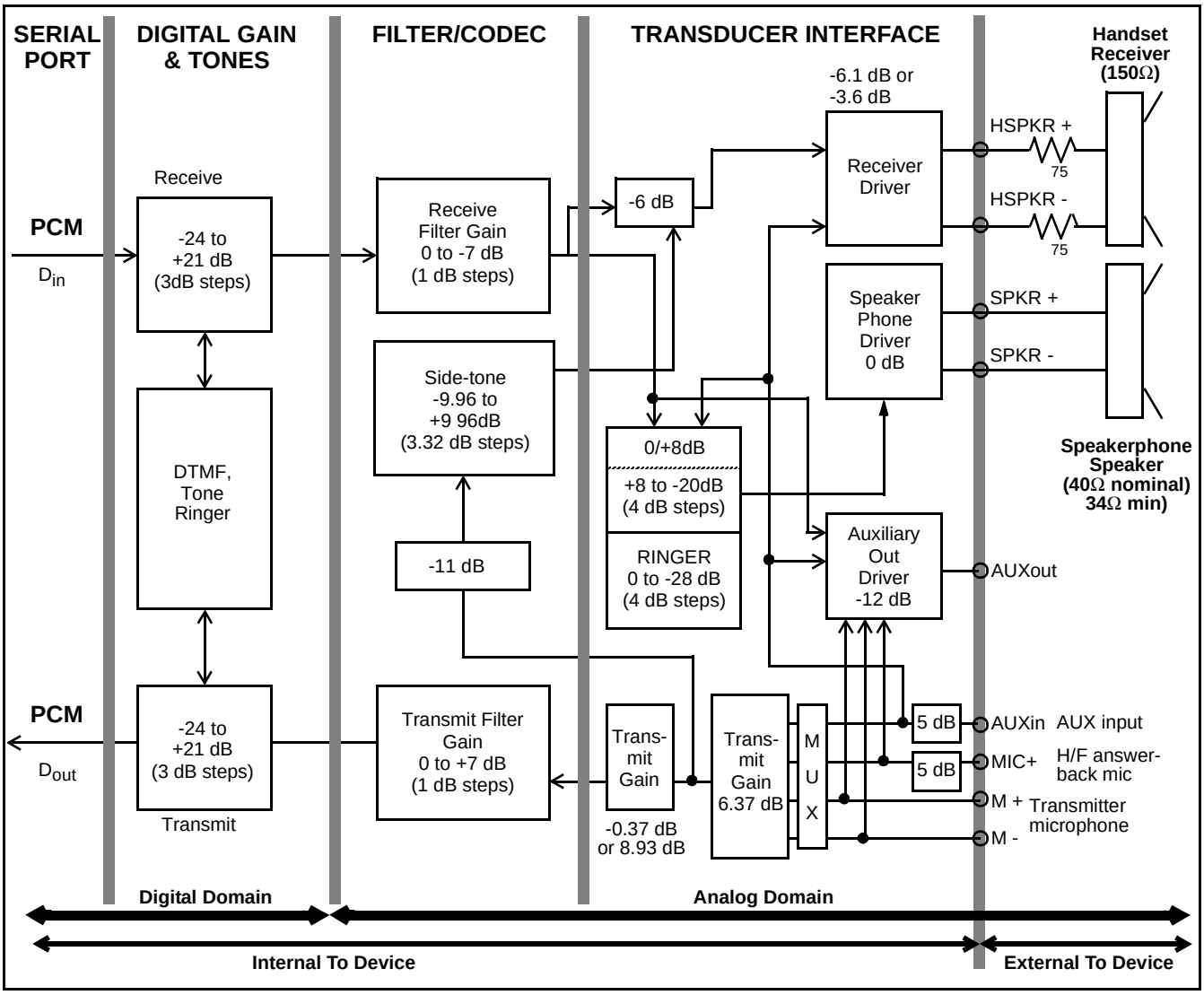


Figure 3 - Audio Gain Partitioning

The receive filter is designed to meet CCITT G.714 specifications. The nominal gain for this filter path is 0 dB (gain control = 0dB). Gain control allows the output signal to be attenuated up to 7 dB. Filter response is peaked to compensate for the sinx/x attenuation caused by the 8 kHz sampling rate.

The Rx filter function can be altered by enabling the Dial EN control bit in Control Register 1 (address 0Eh). This causes another low-pass function to be added with a 3 dB point at 1200 Hz. This function is intended to improve the sound quality of digitally generated dial tone received as PCM.

Side-tone is derived from the Tx filter before the LP/HP filter section and is not subject to the gain control of the Tx filter section. Side-tone is summed into the receive handset transducer driver path after the Rx filter gain control

section so that Rx gain adjustment will not affect side-tone levels. The side-tone path may be enabled/disabled with the Voice sidetone bit located in the Receive Path Control Register (address 13h).

Transmit and receive filter gains are controlled by the $TxFG_0$-$TxFG_2$ and $RxFG_0$-$RxFG_2$ control bits, respectively. These are located in the FCODEC Control Register 1 (address 0Ah). Transmit filter gain is adjustable from 0 dB to +7 dB and receive filter gain from 0 dB to -7 dB, both in 1 dB increments.

Side-tone filter gain is controlled by the STG_0-STG_2 control bits located in the FCODEC Control Register 2 (address 0Bh). Side-tone gain is adjustable from
-9.96 dB to +9.96 dB in 3.32 dB increments.

Companding law selection for the Filter/CODEC is provided by the A/μ companding control bit while the coding scheme is controlled by the sign-mag/$\overline{\text{CCITT}}$ control bit. Both of these reside in Control Register 2 (address 0Fh). Table 1 illustrates these choices.

Code	Sign/ Magnitude	CCITT (G.711)	
		μ-Law	A-Law
+ Full Scale	1111 1111	1000 0000	1010 1010
+ Zero	1000 0000	1111 1111	1101 0101
-Zero (quiet code)	0000 0000	0111 1111	0101 0101
- Full Scale	0111 1111	0000 0000	0010 1010

Table 1

The Filter/CODEC autonull circuit ensures that transmit PCM will contain no more than ±1 bit of offset due to internal circuitry.

Digital Gain and Tone Generation

The Digital gain and Tone generator block is located, functionally, between the serial FDI port and the Filter/CODEC block. Its main function is to provide digital gain control of the transmit and receive audio signals and to generate digital patterns for DTMF and tone ringer signals.

Gain Control

Gain control is performed on linear code for both the receive and the transmit PCM. Gain control is set via the Digital Gain Control Register at address 19h. Gain, in 3.0 dB increments, is available within a range of +21.0 dB to -24 dB.

DTMF Generator

The digital DTMF circuit generates a dual sine-wave pattern which may be routed into the receive path as comfort tones or into the transmit path as network signalling. In both cases the digitally generated signal will undergo gain adjustment as programmed into the transmit and receive gain control registers. Gain control is assigned automatically as functions are selected via the transmit and receive path control registers.

The composite signal output level in the transmit direction is -4 dBm0 (μ-Law) and -10 dBm0 (A-law) with programmable gains at zero dB. Pre-twist of 2.0 dB is incorporated into the composite signal resulting in a low tone output level of -8.12 dBm0 and a high group level of -6.12 dBm0 (for μ-Law, 6 dB lower for A-Law). Note that these levels will be influenced by the Anti-Howling circuit when it is enabled (see Anti-Howling section for more details). DTMF side-tone levels are set to -28 dBm0 from the generator circuit. Other receive path gains must be included when calculating the analog output signal levels. Adjustments to these levels may be made by altering the settings of the Gain Control register (address 19h).

The frequency of the low group tone is programmed by writing an 8-bit coefficient into the Low Tone Coefficient Register (address 1Ah) while the high group tone frequency uses the 8-bit coefficient programmed into the High Tone Coefficient Register (address 1Bh). Both coefficients are determined by the following equation:

Frequency (in Hz) = 7.8125 x COEFF

Where COEFF is an integer between 0 and 255. Frequency resolution is 7.8125 Hz in the range 0 to 1992 Hz.

Low and high tones are enabled individually via the LoEn and HiEN control bits (DTMF/Ringer Control Register, address 18h). This not only provides control over dual tone generation but also allows single tone generation using either of the enable bits and its associated coefficient register.

After programming and enabling the tone generators as described, selection of transmit and/or receive path destinations are carried out via the Path Control Registers (see Path Control section). In addition receive sidetone DTMF must be selected via the DTMF StEN bit (DTMF/Tone ringer Register, address 18h) so that it replaces the received PCM in the Rx Filter path.

Frequency (Hz)	COEFF	Actual Frequency	% Deviation
697	59h	695.3	-.20%
770	63h	773.4	+.40%
852	6Dh	851.6	-.05%
941	79h	945.3	+.46%
1209	9Bh	1210.9	+.20%
1336	ABh	1335.9	.00%
1477	BDh	1476.6	-.03%
1633	D1h	1632.8	-.01%

Table 2 - DTMF Frequencies

DTMF Signal to distortion:

The sum of harmonic and noise power in the frequency band from 50 Hz to 3500 Hz is typically more than 30 dB below the power in the tone pair. All individual harmonics are typically more than 40 dB below the level of the low group tone.

Table 2 gives the standard DTMF frequencies, the coefficient required to generate the closest frequency, the actual frequency generated and the percent deviation of the generated tone from the nominal.

Tone Ringer

A dual frequency squarewave ringing signal may be applied to the handsfree speaker driver to generate a call alerting signal. To enable this mode the Ring En bit (address 18h) must be set as well as the ringer function to the loudspeaker via the Receive Path Control Register (address 13h). Ring En is independent of the DTMF enable control bits (see Lo EN and Hi EN). Since both functions use the same coefficient registers they are not usually enabled simultaneously.

The digital tone generator uses the values programmed into the low and high Tone Coefficient Registers (addresses 1Ah and 1Bh) to generate two different squarewave frequencies.

Both coefficients are determined by the following equation:

COEFF = [32000/Frequency (Hz)] - 1

where COEFF is an integer between 1 and 255. This produces frequencies between 125 - 16000 Hz with a non-linear resolution.

The ringer program switches between these two frequencies at a 5 Hz or 10 Hz rate as selected by the WR bit in the DTMF/Tone ringer register (address 18h).

Anti-Howl

IDPC includes an Anti-Howling circuit plus speaker gain control circuit to allow for group listening operation. Although this is the main function of the circuit there are additional modes in which it may be used as defined by the MS1 and MS0 control bits (address 1Ch).

MS1	MS0	Operational Mode
0	0	Tx noise reduction (squelch)
0	1	Rx noise reduction (squelch)
1	0	switched loss group listening (anti-howling)
1	1	Tx/Rx switched loss

The circuit is enabled by setting the Anti-howl Enable bit (address 1Ch) and selecting the required operational mode (MS0 & MS1) as described.

For all modes of operation the switching levels and inserted loss are programmed as follows.

Switching decisions are made by comparing either the transmit or the receive signal level to threshold levels stored in the High Threshold Register (address 1Dh) and the Low Threshold Register (address 1Eh). Threshold data is encoded in PCM sign-magnitude format excluding the sign bit. For example; THh0 - THh3 encode the PCM step number while THh4 - THh6 encode the PCM chord number for the high threshold. Similarly for the THl0 - THl6 bits of the low threshold. The difference between the high and low threshold levels provides the circuit with hysteresis to prevent uncontrolled operation. The low level threshold must never be programmed to a value higher than the one stored in the high level threshold. If this occurs the circuit will become unstable.

Loss is implemented, in the chosen path, by subtracting the value set by the Pad0 - Pad3 control bits from the appropriate gain value set by the RxG0 - RxG3 or TxG0 - TxG3 control bits (see Digital Gain Register, address 19h). The minimum digital gain is limited to -24 dB regardless of the mathematical result of this operation. The path without loss reverts to the gain value programmed into the Digital Gain Register.

The magnitude of the switched loss defaults to 12 dB on power up but can be programmed to between 0 and 21 dB using the Pad0 - Pad2 control bits (address 1Ch).

Pad2	Pad1	Pad0	Attenuation (dB)
0	0	0	0
0	0	1	3
0	1	0	6
0	1	1	9
1	0	0	12
1	0	1	15
1	1	0	18
1	1	1	21

Switched Loss for Group Listening (anti-howling)

Group listening is defined as a normal handset conversation with received speech also directed to the loudspeaker for third party observation. In this mode, if the handset microphone is moved into close proximity of the loudspeaker a feedback path will occur resulting in a singing connection. To prevent this the anti-howling circuit introduces a switched loss into either the transmit or receive paths dependent upon the transmit path speech activity.

Loss switching is determined by comparing the signal level in the transmit path with the high level threshold stored at address 1Dh. When the transmit signal level exceeds this threshold the programmed loss is switched from the transmit path to the receive path. Once switching has occurred the transmit signal level is then compared to a low level threshold stored at address 1Eh. When the transmit signal level falls below this threshold the programmed loss is switched from the received path back to the transmit path and comparison reverts back to the high threshold level.

Since the received digital gain control is used to set the listening level of the received speech, for both handset receiver and loudspeaker, it is necessary to provide additional gain in the loudspeaker path so that its receive level can be controlled independently from the receiver output. The Gain0 to Gain3 control bits (address 0Bh) are used to boost the loudspeaker output to a comfortable listening level for the third parties in group listening. Generally the Gain3 bit should be set to logic 1 in this mode. This increases the gain programmed via the Gain0 - Gain2 bits by a factor of 8 dB. In group listening a speaker gain setting of 4 to 16 dB will be required to set a comfortable group listening level after the handset user has adjusted their listening level as required.

Since the anti-howling circuit has dynamic control over the transmit and receive gain control registers, it is recommended that this function be turned off momentarily when DTMF tone generation is required. This will ensure that the proper transmit levels are attained.

Transmit Noise Reduction (squelch)

The transmit signal may be muted to eliminate transmission of excessive background noise.

In this mode the signal level in the transmit path is compared with the high level threshold stored at address 1Dh. When the transmit signal level exceeds this threshold no loss is inserted into the transmit path. After exceeding the high level threshold the transmit signal level is then compared to a low level threshold stored at address 1Eh. When the transmit signal level falls below this threshold the transmit digital gain is reduced by the programmed amount (Pad0-2) and comparison reverts back to the high threshold level. The receive path gain is not altered by transmit noise reduction.

Receive Noise Reduction (squelch)

The receive signal may be muted to eliminate background noise resulting from a poor trunk connection.

In this mode the signal level in the receive path is compared with the high level threshold stored at address 1Dh. When the receive signal level exceeds this threshold no loss is inserted into the receive path. After exceeding the high level threshold the receive signal level is then compared to a low level threshold stored at address 1Eh. When the receive signal level falls below this threshold the receive digital gain is reduced by the programmed amount (Pad2-0) and comparison reverts back to the high threshold level. The transmit path gain is not altered by receive noise reduction.

Tx/Rx Switched Loss

In this mode the programmed switched loss is inserted into either the transmit or receive path dependent only upon activity in the receive path. If receive path activity is above the programmed high level threshold then the switched loss is inserted into the transmit path. If receive path activity is below the programmed low level threshold then the switched loss is inserted into the receive path.

This mode can be used to implement a loudspeaking function where the receive audio is routed to the SPKR± pins and transmit audio is sourced from the MIC+ pin. In this mode there is no algorithmic cancellation of echo so it is recommended that this switched loss program be used only in 4-wire systems (i.e., digital set to digital set).

Transducer Interfaces

Four standard telephony transducer interfaces plus an auxiliary I/O are provided by the IDPC. These are:

- The handset microphone inputs (transmitter), pins M+/M- and the answerback microphone input MIC+. The nominal transmit path gain may be adjusted to either 6.0 dB or 15.3 dB. Control of this gain is provided by the TxINC control bit (Control register 2, address 0Fh). This gain adjustment is in addition to the programmable gain provided by the transmit filter and Digital Gain circuit.
- The handset speaker outputs (receiver), pins HSPKR+/HSPKR-. This internally compensated, fully differential output driver is capable of driving the load shown in Figure 4. The nominal handset receive path gain may be adjusted to either -12.1 dB or -9.6 dB. Control of this gain is provided by the RxINC control bit (Control

register 2, address 0Fh). This gain adjustment is in addition to the programmable gain provided by the receive filter and Digital Gain circuit.

- The loudspeaker outputs, pins SPKR+/SPKR-. This internally compensated, fully differential output driver is capable of directly driving 6.5v p-p into a 40 ohm load.
- The Auxiliary Port provides an analog I/O, pins AUXin and AUXout, for connection of external equipment to the CODEC path as well as allowing access to the speaker driver circuits.
  - AUXin is a single ended high impedance input (>10 Kohm). This is a self-biased input with a maximum input range of 2.5vp-p. Signals should be capacitor-coupled to this input.
  - AUXout is a buffered output capable of driving 40 Kohms//150 pF. Signals for this output are derived from the receive path or from the AUXin and transmit microphones.
  - Auxiliary port path gains are:

AUXin to Dout	11 dB	TxINC=0
	20.3 dB	TxINC=1
Din to AUXout	-12 dB	
AUXin to AUXout	-7.0 dB	
AUXin to HSPKR±	-1.1 dB	RxINC=0
	1.4 dB	RxINC=1
AUXin to SPKR±	5.0 dB	

Refer to the application diagrams of Figures 10 and 11 for typical connections to this analog I/O section.

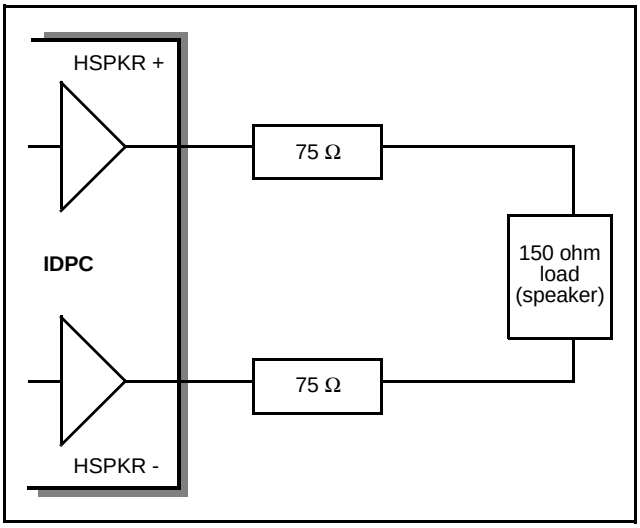


Figure 4 - Handset Speaker Driver

Microport

The serial microport, compatible with Intel MCS-51 (mode 0), Motorola SPI (CPOL=0,CPHA=0) and National Semiconductor Microwire specifications provides access to all IDPC internal read and write registers. This microport consists of a transmit/receive data pin (DATA1), a receive data pin (DATA2), a chip select pin ($\overline{CS}$) and a synchronous data clock pin (SCLK).

The microport dynamically senses the state of the serial clock each time chip select becomes active. The device then automatically adjusts its internal timing and pin configuration to conform to Intel or Motorola/National requirements. If SCLK is high during chip select activation then Intel mode 0 timing is assumed. The DATA1 pin is defined as a bi-directional (transmit/receive) serial port and DATA2 is internally disconnected. If SCLK is low during chip select activation then Motorola/National timing is assumed. Motorola processor mode CPOL=0, CPHA=0 must be used. DATA1 is defined as the data transmit pin while DATA2 becomes the data receive pin. Although the dual

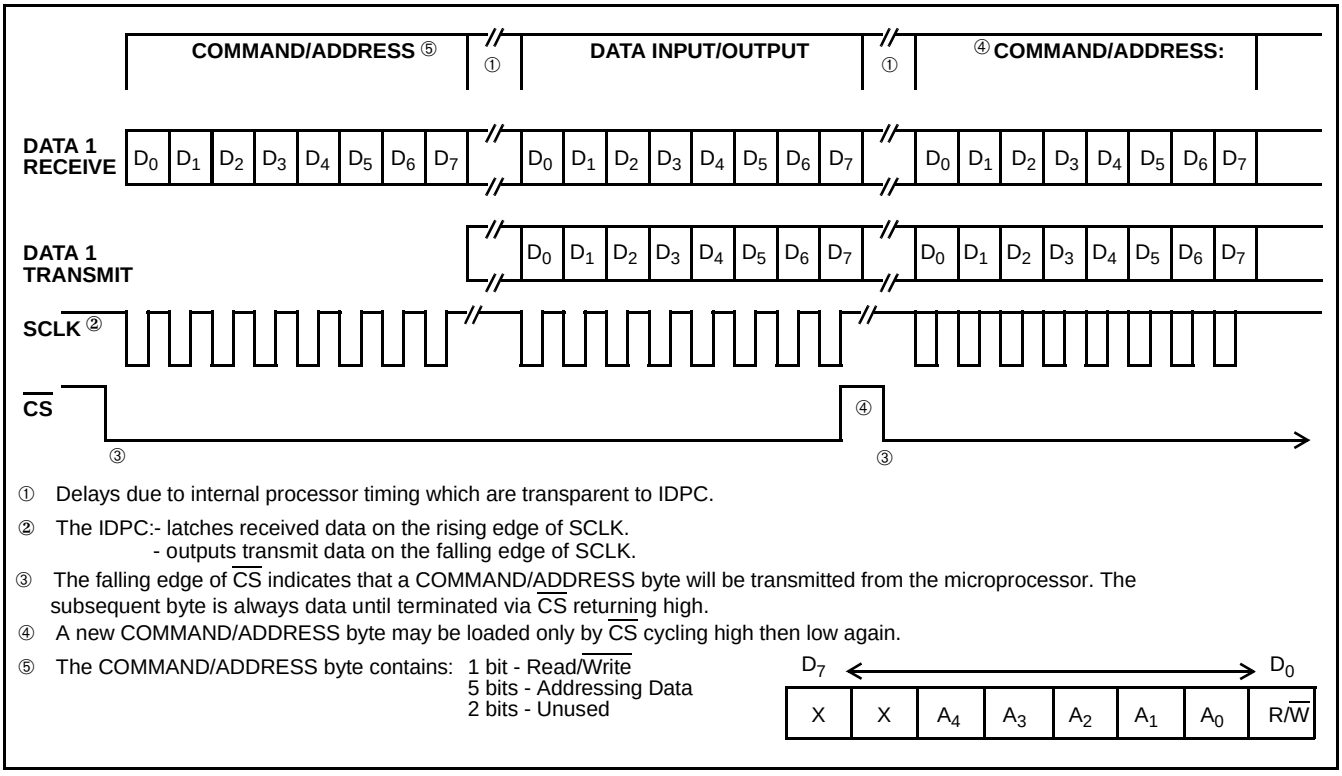
port Motorola controller configuration usually supports full-duplex communication, only half-duplex communication is possible in IDPC. The micro must discard non-valid data which it clocks in during a valid write transfer to IDPC. During a valid read transfer from IDPC data simultaneously clocked out by the micro is ignored by IDPC.

All data transfers through the microport are two-byte transfers requiring the transmission of a Command/Address byte followed by the data byte written or read from the addressed register. $\overline{CS}$ must remain asserted for the duration of this two-byte transfer. As shown in Figures 5 and 6 the falling edge of $\overline{CS}$ indicates to the IDPC that a microport transfer is about to begin. The first 8 clock cycles of SCLK after the falling edge of $\overline{CS}$ are always used to receive the Command/Address byte from the microcontroller. The Command/Address byte contains information detailing whether the second byte transfer will be a read or a write operation and at what address. The next 8 clock cycles are used to transfer the data byte between the IDPC and the microcontroller. At the end of the two-byte transfer $\overline{CS}$ is brought high again to terminate the session. The rising edge of $\overline{CS}$ will tri-state the output driver of DATA1 which will remain tri-stated as long as $\overline{CS}$ is high.

Intel processors utilize least significant bit first transmission while Motorola/National processors employ most significant bit first transmission. The IDPC microport automatically accommodates these two schemes for normal data bytes. However, to ensure timely decoding of the R/W and address information, the Command/Address byte is defined differently for Intel operation than it is for Motorola/National operation. Refer to the relative timing diagrams of Figures 5 and 6.

Receive data is sampled on the rising edge of SCLK while transmit data is made available concurrent with the falling edge of SCLK.

Detailed microport timing is shown in Figure 15.



① Delays due to internal processor timing which are transparent to IDPC.

② The IDPC:- latches received data on the rising edge of SCLK.
- outputs transmit data on the falling edge of SCLK.

③ The falling edge of $\overline{CS}$ indicates that a COMMAND/ADDRESS byte will be transmitted from the microprocessor. The subsequent byte is always data until terminated via $\overline{CS}$ returning high.

④ A new COMMAND/ADDRESS byte may be loaded only by $\overline{CS}$ cycling high then low again.

⑤ The COMMAND/ADDRESS byte contains: 1 bit - Read/$\overline{Write}$
5 bits - Addressing Data
2 bits - Unused

D_7							D_0
X	X	A_4	A_3	A_2	A_1	A_0	R/$\overline{W}$

Figure 5 - Serial Port Relative Timing for Intel Mode 0

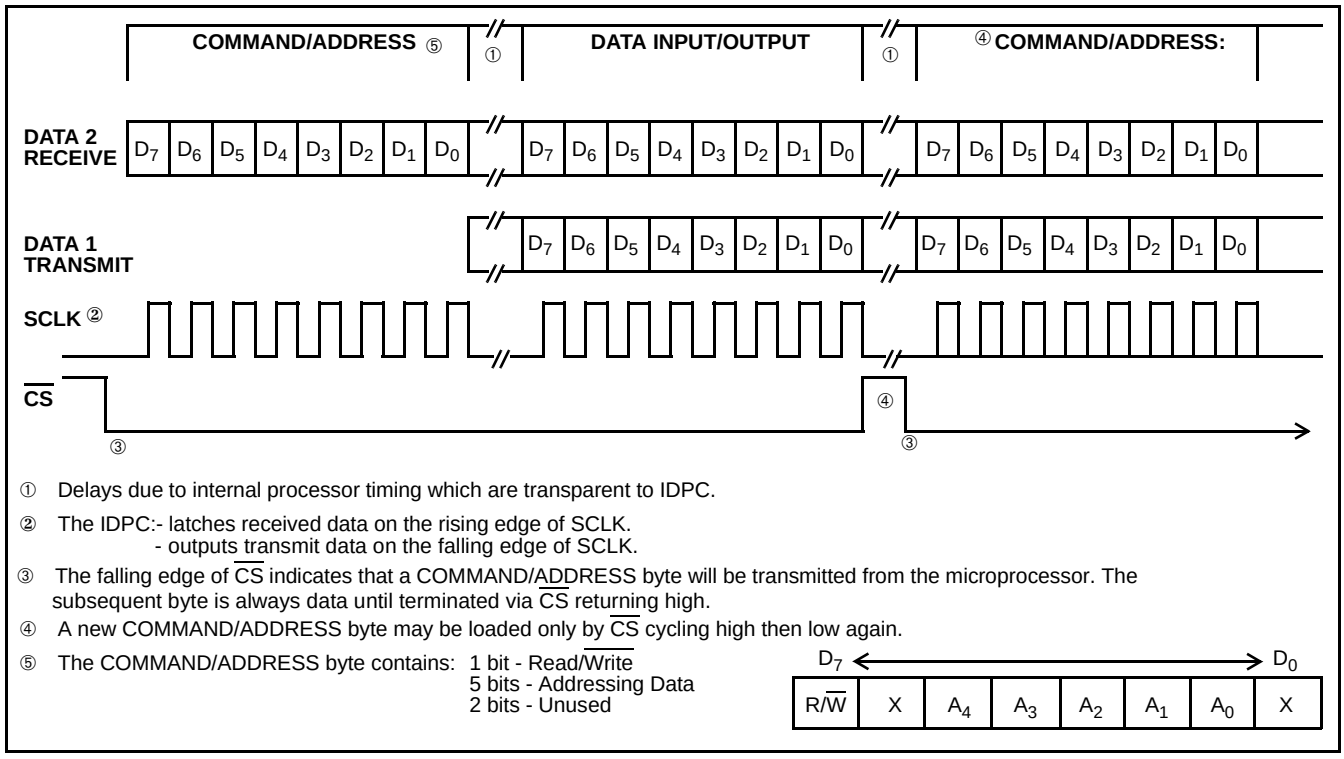


Figure 6 - Serial Port Relative Timing for Motorola Mode 00/National Microwire

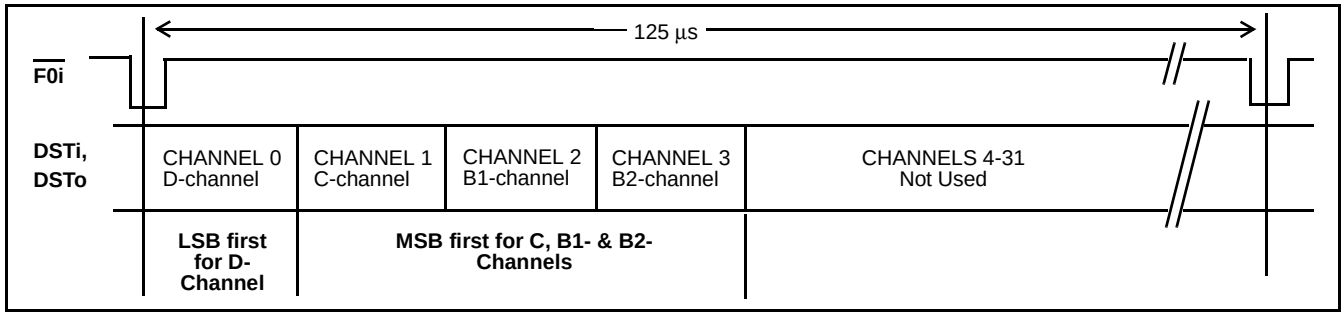


Figure 7 - ST-BUS Channel Assignment

Flexible Digital Interface

A serial link is required to transport data between the IDPC and an external digital transmission device. IDPC utilizes the ST-BUS architecture defined by Zarlink Semiconductor but also supports a strobed data interface found on many standard CODEC devices. This interface is commonly referred to as Synchronous Serial Interface (SSI). The combination of ST-BUS and SSI provides a Flexible Digital Interface (FDI) capable of supporting all Zarlink basic rate transmission devices as well as many other 2B + D transceivers.

The required mode of operation is selected via the ST-BUS/$\overline{\text{SSI}}$ control bit (FDI Control Register, address 10h). Pin definitions alter dependent upon the operational mode selected, as described in the following subsections as well as in the Pin Description tables.

Quiet Code

The FDI can be made to send quiet code to the decoder and receive filter path by setting the RxMUTE bit high. Likewise, the FDI will send quiet code in the transmit (DSTo) path when the TxMUTE bit is high. Both of these

control bits reside in Control Register 1 at address 0Eh. When either of these bits are low their respective paths function normally. The -Zero entry of Table 1 is used for the quiet code definition.

ST-BUS Mode

The ST-BUS consists of output (DSTo) and input (DSTi) serial data streams, in FDI these are named Dout and Din respectively, a synchronous clock input signal CLOCKin (C4i), and a framing pulse input (F0i). These signals are direct connections to the corresponding pins of Zarlink basic rate devices. Note that in ST-BUS mode the XSTL2 pin is not used. The CSL1 and CSL0 bits, as described in the SSI Mode section, are also ignored since the data rate is fixed for ST-BUS operation. However, the Asynch/Synch bit must be set to logic “0” for ST-BUS operation.

The data streams operate at 2048 kb/s and are Time Division Multiplexed into 32 identical channels of 64 kb/s bandwidth. A frame pulse (a 244 nSec low going pulse) is used to parse the continuous serial data streams into the 32 channel TDM frames. Each frame has a 125 µSecond period translating into an 8 kHz frame rate. A valid frame begins when F0i is logic low coincident with a falling edge of C4i. Refer to Figure 12 for detailed ST-BUS timing. C4i has a frequency (4096 kHz) which is twice the data rate. This clock is used to sample the data at the 3/4 bit-cell position on DSTi and to make data available on DSTo at the start of the bit-cell. C4i is also used to clock the IDPC internal functions (i.e., Filter/CODEC, Digital gain and tone generation) and to provide the channel timing requirements.

The IDPC uses only the first four channels of the 32 channel frame. These channels are always defined, beginning with Channel 0 after the frame pulse, as shown in Figure 7 (ST-BUS channel assignments).

The first two (D & C) Channels are enabled for use by the DEN and CEN bits respectively, (FDI Control Register, address 10h). ISDN basic rate service (2B+D) defines a 16kb/s signalling (D) Channel. IDPC supports transparent access to this signalling channel. ST-BUS basic rate transmission devices, which may not employ a microport, provide access to their internal control/status registers through the ST-BUS Control (C) Channel. IDPC supports microport access to this C-Channel.

DEN - D-Channel

In ST-BUS mode access to the D-Channel (transmit and receive) data is provided through an 8-bit read/write register (address 15h) D-Channel data is accumulated in, or transmitted from this register at the rate of 2 bits/frame for 16 kb/s operation (1 bit/frame for 8 kb/s operation). Since the ST-BUS is asynchronous, with respect to the microport, valid access to this register is controlled through the use of an interrupt (IRQ) output. D-Channel access is enabled via the (DEn) bit.

DEn:

When 1, ST-BUS D-channel data (1 or 2 bits/frame depending on the state of the D8 bit) is shifted into/out of the D-channel (READ/WRITE) register.

When 0, the receive D-channel data (READ) is still shifted into the proper register while the DSTo D-channel timeslot and IRQ outputs are tri-stated (default).

D8:

When 1, D-Channel data is shifted at the rate of 1 bit/frame (8 kb/s).

When 0, D-Channel data is shifted at the rate of 2 bits/frame (16 kb/s default).

16 kb/s D-Channel operation is the default mode which allows the microprocessor access to a full byte of D-Channel information every fourth ST-BUS frame. By arbitrarily assigning ST-BUS frame n as the reference frame, during which the microprocessor D-Channel read and write operations are performed, then:

a. A microport read of address 15 hex will result in a byte of data being extracted which is composed of four di-bits (designated by roman numerals I,II,III,IV). These di-bits are composed of the two D-Channel bits received during each of frames n, n-1, n-2 and n-3. Referring to Fig. 8a: di-bit I is mapped from frame n-3, di-bit II is mapped from frame n-2, di-bit III is mapped from frame n-1 and di-bit IV is mapped from frame n.

The D-Channel read register is not preset to any particular value on power-up ($\overline{PWRST}$) or software reset (RST).

b. A microport write to Address 15hex will result in a byte of data being loaded which is composed of four di-bits (designated by roman numerals I, II, III, IV). These di-bits are destined for the two D-Channel bits transmitted during each of frames n+1, n+2, n+3, n+4. Referring to Fig.8a: di-bit I is mapped to frame n+1, di-bit II is mapped to frame n+2, di bit III is mapped to frame n+3 and di bit IV is mapped to frame n+4.

If no new data is written to address 15hex, the current D-channel register contents will be continuously re-transmitted. The D-Channel write register is preset to all ones on power-up ($\overline{PWRST}$) or software reset (RST).

An interrupt output is provided ($\overline{IRQ}$) to synchronize microprocessor access to the D-Channel register during valid ST-BUS periods only. $\overline{IRQ}$ will occur every fourth (eighth in 8 kb/s mode) ST-BUS frame at the beginning of the third (second in 8 kb/s mode) ST-BUS bit cell period. The interrupt will be removed following a microprocessor Read or Write of Address 15 hex or upon encountering the following frames's $\overline{FP}$ input, whichever occurs first. To ensure D-Channel data integrity, microport read/write access to Address 15 hex must occur before the following frame pulse. See Figure 8b for timing.

8 kb/s operation expands the interrupt to every eight frames and processes data one-bit-per-frame. D-Channel register data is mapped according to Figure 8c.

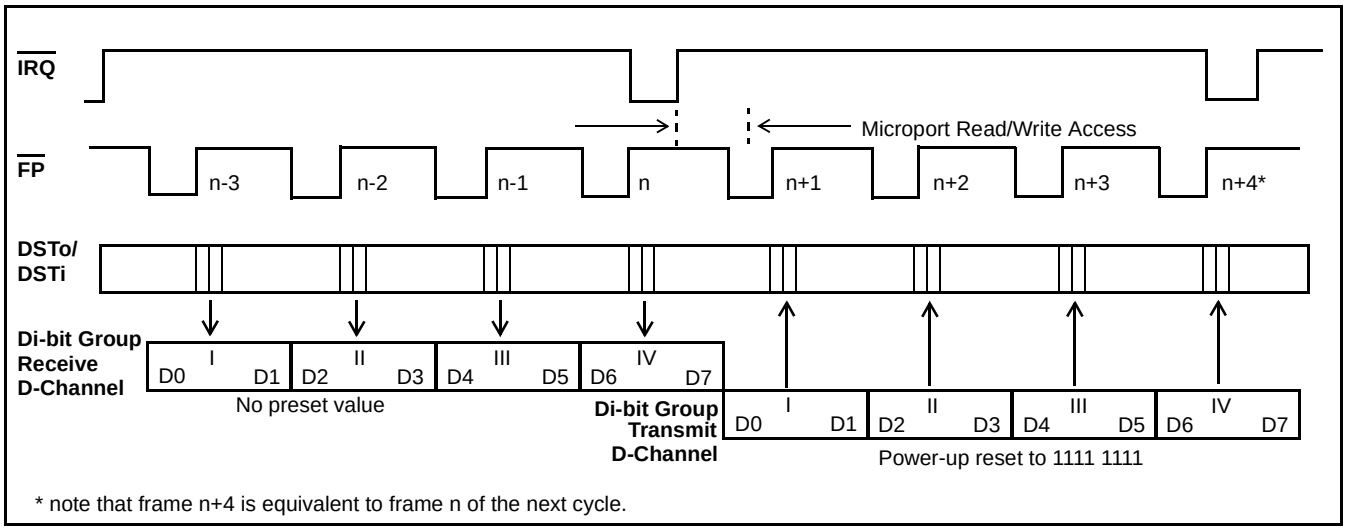


Figure 8a - D-Channel 16 kb/s Operation

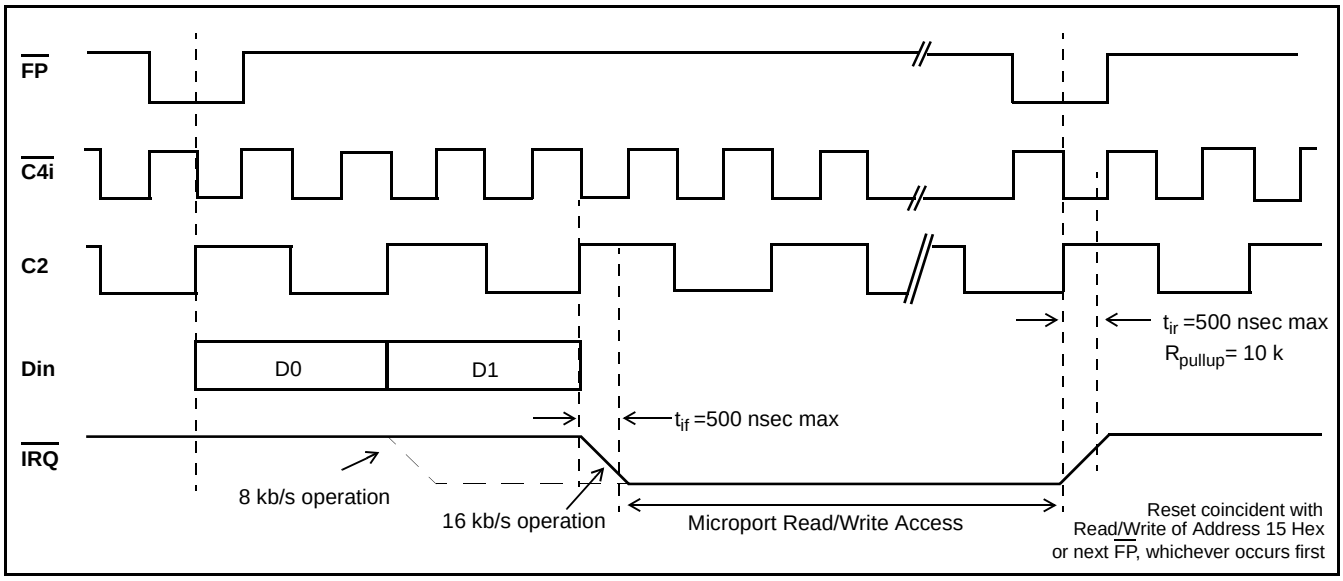


Figure 8b - IRQ Timing Diagram

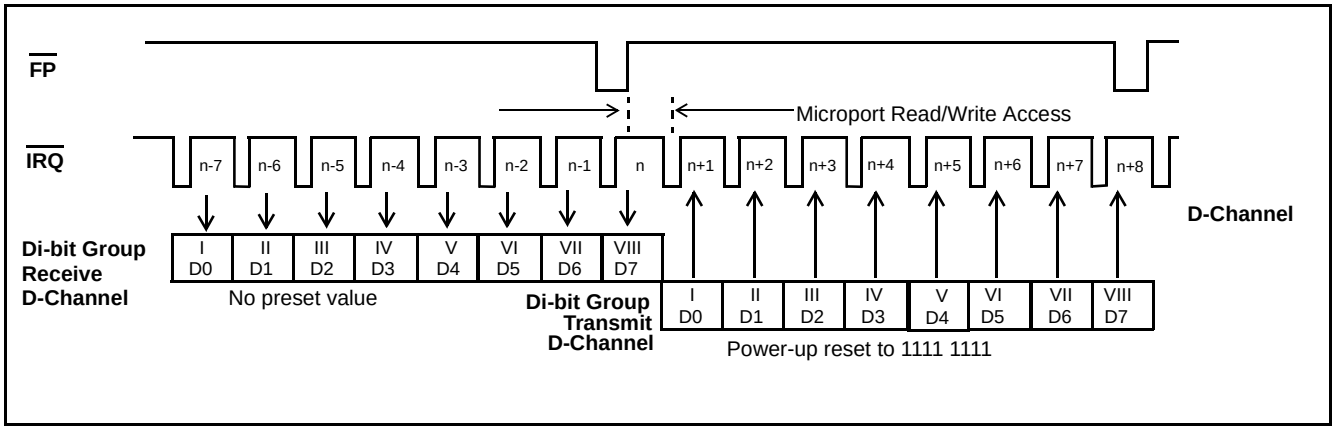


Figure 8c - D-Channel 8 kb/s Operation

CEn - C-Channel

Channel 1 conveys the control/status information for the layer 1 transceiver. C-Channel data is transferred MSB first on the ST-BUS by IDPC. The full 64 kb/s bandwidth is available and is assigned according to which transceiver is being used. Consult the data sheet for the selected transceiver for its C-Channel bit definitions and order of bit transfer.

When CEN is high, data written to the C-Channel register (address 14h) is transmitted, most significant bit first, on DSTo. On power-up reset (PWRST) or software reset (RST, address 0Fh) all C-Channel bits default to logic high. Receive C-Channel data (DSTi) is always routed to the read register regardless of this control bit's logic state.

When low, data transmission is halted and this timeslot is tri-stated on DSTo.

B1-Channel and B2-Channel

Channels 2 and 3 are the B1 and B2 channels, respectively. B-channel PCM associated with the Digital Gain, Filter/CODEC and transducer audio paths is selected on an independent basis for the transmit and receive paths. For example, the transmit path may use the B1 channel while the receive path uses the B2 channel. Although not normally required, this flexibility is allowed.

For ST-BUS mode the configuration of bits 0 to 3, at address 12h, defines both the source of transmit audio and the B-Channel destination. The configuration of this register permits selection of only one transmit B-Channel at a time. If no valid transmit path has been selected, via the Transmit Path Selection Register, for a particular B-Channel then that timeslot output on DSTo is tri-stated.

When a valid receive path has been selected, via the Receive Path Selection Register (address 13h), the active receive B-Channel is governed by the state of the B2/B1 control bit in Control register 1 (address 0Eh).

Refer to the Path Selection section for detailed information.

SSI Mode

The SSI BUS consists of input and output serial data streams named Din and Dout respectively, a Clock input signal (CLOCKin), and a framing strobe input (STB). A 4.096 MHz master clock, at CLOCKin, is required for SSI operation if the bit clock is less than 512 kHz. The timing requirements for SSI are shown in Figures 13 and 14.

In SSI mode the IDPC supports only B-Channel operation. The internal C and D Channel registers used in ST-BUS mode are not functional for SSI operation. The control bit B2/B1, as described in the ST-BUS section, is ignored since the B-Channel timeslot is defined by the input STB strobe. Hence, in SSI mode transmit and receive B-Channel data are always in the channel defined by the STB input.

The data strobe input STB determines the 8-bit timeslot used by the device for both transmit and receive data. This is an active high signal with an 8 kHz repetition rate.

SSI operation is separated into two categories based upon the serial data rate. If the bit clock is 512 kHz or greater then the bit clock is used directly by the internal IDPC functions allowing synchronous operation. In this case, the bit clock is connected directly to the CLOCKin pin while XSTAL2 is left unconnected. If the available bit clock rate is 128 kHz or 256 kHz then a 4096 kHz master clock is required to derive clocks for the internal IDPC functions. If this clock is available externally then it may be applied directly to the CLOCKin pin. If a 4096 kHz clock is not available then provision is made to connect a 4096 kHz crystal across the CLOCKin and XSTAL2 pins as shown in Figure 9. The oscillator circuit has been designed to require an external feedback resistor and load capacitors. This configuration allows normal ST-BUS operation and synchronous SSI operation with clocks which are not loaded by these extra components.

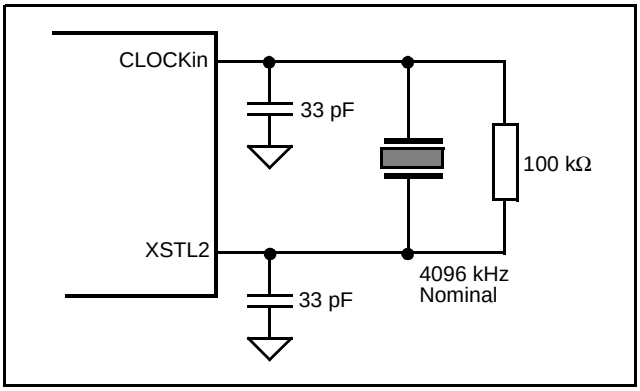


Figure 9 - External Crystal Circuit (for asynchronous operation)

Applications where the bit clock rate is below 512 kHz are designated as asynchronous. The IDPC will generate and re-align its internal clocks to allow operation when the external master and bit clocks are asynchronous. In this case, the external bit clock is not connected to the IDPC. Control bits Asynch/Synch, CSL1 and CSL0 in FDI Control Register (address 10h) are used to program the bit rates as shown in Table 3.

Asynch/ Synch	CSL1	CSL0	Bit Clock Rate (kHz)	CLOCKin (kHz)
1	0	0	128	4096 mandatory
1	0	1	256	4096 mandatory
0	0	0	512	512
0	0	1	1536	1536
0	1	0	2048	2048
0	1	1	4096	4096

Table 3

For synchronous operation data is sampled, from Din, on the falling edge of the bit clock during the time slot defined by the STB input. Data is made available, on Dout, on the rising edge of the bit clock during the time slot defined by the STB input. Dout is tri-stated at all times when STB is not true. If STB is valid but no transmit path has been selected (via the Transmit Path Control Register) then quiet code will be transmitted on Dout during the valid strobe period. There is no frame delay through the FDI circuit for synchronous operation.

For asynchronous operation Dout and Din are as defined for synchronous operation except that data is transferred according to the internally generated bit clock. Due to resynchronization circuitry activity, the output jitter on Dout is nominally larger but will not affect operation since the bit cell period at 128 kb/s and 256 kb/s is relatively large. There is a one frame delay through the FDI circuit for asynchronous operation. Refer to the specifications of Figures 13 and 14 for both synchronous and asynchronous SSI timing.

Path Selection

Transmit and receive audio paths are independently programmed through their respective Path Control Registers at addresses 12h and 13h. Individual audio path circuit blocks are powered up only as they are required to satisfy the programmed values in the path control registers. More detail is provided in the Power-up/down Reset section.

Transmit

Transmit audio path configuration (Path Control Register, address 12h) is simply a matter of assigning one of the three analog signal inputs, or the digital tone generator, to the required transmit B- Channel. Intermediate functions such as the transmit filter, encoder and transmit gain are automatically powered up and assigned as required. If transmit tones is selected then the digital tone generator must be programmed and enabled properly as described in the Digital Tone Generator section. Note that transmit tones may be enabled independently of the receive path.

For ST-BUS mode the configuration of bits 0 to 3, at address 12h, defines both the source of transmit audio and the B-Channel destination. The configuration of this register permits selection of only one transmit B-Channel at a time. For SSI mode only the selections where bit 3 = 0 are allowed. This is because the B-Channel timeslot is defined by the input strobe at STB. If a selection where bit 3 = 1 is made it will be treated the same as the condition where B3 - B0 = all zero's.

All reserved configurations should not be used.

Receive

The receive path assignment (Receive Path Control Register, address 13h) is different from the transmit path assignment. In this case a particular analog output port is assigned a source for its audio signal. The receive filter audio path and the Auxiliary In analog port are the available choices. This configuration allows flexibility in assignment. Two examples; the receive filter path can be assigned to the handset receiver, for a standard handset conversation, while permitting the loudspeaker to announce a message originating from the Auxiliary In port. Or

perhaps the receive filter is assigned to both the loudspeaker and the Auxiliary Out port. This would allow a voice recorder or Facsimile machine, connected to the AUXout port to be monitored over the loudspeaker.

The receive filter path itself has two possible signal sources, PCM from the Din port or synthesized tones, from the digital tone generator. In both cases receive digital gain is assigned automatically. The Receive Path Control Register combines all of these choices into simple output port assignments.

In ST-BUS mode receive PCM from the Din port must be selected from either the B1 or the B2 channel. Control Bit B2/$\overline{B1}$ in Control Register 1 (address 0Eh) is used to define the active receive B-Channel. In SSI mode the active PCM channel is automatically defined by the STB input signal.

Sidetone

A voice sidetone path provides proportional transmit signal summing into the receive handset transducer driver. Details are provided in the Filter/CODEC section.

Watchdog

To maintain program integrity an on-chip watchdog timer is provided for connection to the microcontroller reset pin. The watchdog output WD goes high while the IDPC is held in reset via $\overline{PWRST}$. Release of $\overline{PWRST}$ will cause WD to return low immediately and will also start the watchdog timer. The watchdog timer is clocked on the falling edge of STB/F0i and requires only this input, along with V_{DD}, for operation. Note that in SSI mode, if STB disappears the watchdog will stop clocking. This will not harm processor operation but there is no longer any protection provided.

If the watchdog reset word is written to the watchdog register (address 11h) after $\overline{PWRST}$ is released, but before the timeout period (T=512 mSec) expires, a reset of the timer results and WD will remain low. Thereafter, if the reset word is loaded correctly at intervals less than 'T' then WD will continue low. The first break from this routine, in which the watchdog register is not written to within the correct interval or it is written to with incorrect data, will result in a high going WD output after the current interval 'T' expires. WD will then toggle at this rate until the watchdog register is again written to correctly.

5-Bit Watchdog Reset Word

B7	B6	B5	B4	B3	B2	B1	B0
X	X	X	0	1	0	1	0

x=don’t care

Power-up/down & $\overline{\text{PWRST}}$/Software Reset

While the IDPC is held in $\overline{\text{PWRST}}$ no device control or functionality is possible. While in software reset (RST=1, address 0Fh) only the microport and watchdog are functional. Software reset can only be removed by writing RST logic low or by the $\overline{\text{PWRST}}$ pin.

After Power-up reset ($\overline{\text{PWRST}}$) or software reset (RST) all control bits assume their default states; µ-Law functionality, usually 0 dB programmable gains and all sections of IDPC, except the microport and watchdog, into powered down states. This is the low power, stand-by condition. This includes:

- The receive output drive transducers. All transducer output drivers are powered down forcing the output signals into tri-state. Output drivers (handset, handsfree-speaker, AUXout) are powered up/down individually as required by the state of the programmed bits in the Receive Path Control Register (address 13h)
- The transmit and receive filters and CODEC. All clocks for this circuit block are disabled. The complete section is automatically powered up as required by the programmed bits in the Transmit and Receive Path Control registers (addresses 12h and 13h). Whenever all path control selections are off this section is powered down. The CODEC and transmit/ receive filters cannot be powered up individually.
- The VRef and VBias circuits. Reference and Bias voltage drivers are tri-stated during power down causing the voltage at the pins to float. This circuit block is automatically powered up/down as it is required by either the Filter/CODEC or the transducer driver circuits. Whenever all path control selections are off this section is powered down. If the AUXin path to (any combination of the) output transducer drivers is selected then the VRef/VBias circuit is powered up but the Filter/CODEC circuit is not.
- The FDI and oscillator circuits. After $\overline{\text{PWRST}}$, the device assumes SSI operation with Dout tri-stated while there is no strobe active on STB. If a valid strobe is supplied to STB, then Dout will be active, during the defined channel, supplying quiet code as defined in Table 1. If the device is switched to ST-BUS operation following $\overline{\text{PWRST}}$, the entire Dout stream will be tri-stated until an active transmit channel is programmed. As well, following $\overline{\text{PWRST}}$, the oscillator circuit is disabled and all timing for the IDPC functional blocks is halted. A clock signal applied to the MCL pin is prevented from entering further into the IDPC when the Asynch/Synch bit is logic “1”.

To power up the FDI and oscillator circuits the PD bit of Control Register 1 (address 0Eh) must be cleared.

To attain complete power-down from a normal operating condition, write all “0s” to the Transmit and Receive Path Control Registers (address 12h and 13h), set PD to logic 1 at address 0Eh, and Asynch/Synch to logic 1 at address 10h.

IDPC Register Map

00 • • • 09	RESERVED								
0A	-	$RxFG_2$	$RxFG_1$	$RxFG_0$	-	$TxFG_2$	$TxFG_1$	$TxFG_0$	FCodec Control 1
0B	Gain3	Gain2	Gain1	Gain0	-	STG_2	STG_1	STG_0	FCodec Control 2
0C	----------RESERVED----------								
0D	----------RESERVED----------								
0E	PD	Tfhp	DialEn	-	-	B2/$\overline{B1}$	RxMute	TxMute	Control Register 1
0F	RST	-	A/$\overline{\mu}$	Smag/ $\overline{CCITT}$	RxINC	TxINC	-	-	Control Register 2
10	-	ST-BUS/ $\overline{SSI}$	CEN	DEN	D_8	Asynch/ $\overline{Synch}$	CSL_1	CSL_0	FDI Control
11	-	-	-	W_4	W_3	W_2	W_1	W_0	Watchdog
12	-	-	-	-	b_3	b_2	b_1	b_0	Tx Path Control
13	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	Rx Path Control
14	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	C-Channel Register
15	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D-Channel Register
16	----------RESERVED----------								
17	-	-	$Loop_2$	$Loop_1$	-	-	-	-	Loopback Register
18	HiEN	LoEn	DTMF StEn	Ring En	-	-	-	WR	DTMF/Tone Ringer
19	TxG_3	TxG_2	TxG_1	TxG_0	RxG_3	RxG_2	RxG_1	RxG_0	Digital Gain
1A	L_7	L_6	L_5	L_4	L_3	L_2	L_1	L_0	Low Tone Coeff
1B	H_7	H_6	H_5	H_4	H_3	H_2	H_1	H_0	High Tone Coeff
1C	Enable	-	MS_1	MS_0	-	Pad_2	Pad_1	Pad_0	Anti-Howl Control
1D	-	TH_{h6}	TH_{h5}	TH_{h4}	TH_{h3}	TH_{h2}	TH_{h1}	TH_{h0}	High Threshold
1E	-	TH_{l6}	TH_{l5}	TH_{l4}	TH_{l3}	TH_{l2}	TH_{l1}	TH_{l0}	Low Threshold
1F • • • 3F	RESERVED								

Register Summary

ADDRESSES = 00h to 09h ARE RESERVED

Filter Codec Control Register 1

ADDRESS = 0Ah WRITE/READ VERIFY

Power Reset Value
X000 X000

-	$RxFG_2$	$RxFG_1$	$RxFG_0$	-	$TxFG_2$	$TxFG_1$	$TxFG_0$
7	6	5	4	3	2	1	0

Receive Gain Setting (dB)	$RxFG_2$	$RxFG_1$	$RxFG_0$
(default) 0	0	0	0
-1	0	0	1
-2	0	1	0
-3	0	1	1
-4	1	0	0
-5	1	0	1
-6	1	1	0
-7	1	1	1

Transmit Gain Setting (dB)	$TxFG_2$	$TxFG_1$	$TxFG_0$
(default) 0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

$RxFG_n$ = Receive Filter Gain n

$TxFG_n$ = Transmit Filter Gain n

Filter Codec Control Register 2

ADDRESS = 0Bh WRITE/READ VERIFY

Power Reset Value
0010 X000

Gain3	Gain2	Gain1	Gain0	-	STG_2	STG_1	STG_0
7	6	5	4	3	2	1	0

Speaker Gain (dB)		Gain2	Gain1	Gain0
Gain3 = 1	Gain3 = 0			
16	8	0	0	0
12	4	0	0	1
8	0	0	1	0
4	-4	0	1	1
0	-8	1	0	0
-4	-12	1	0	1
-8	-16	1	1	0
-12	-20	1	1	1

Side-tone Gain Setting (dB)	STG_2	STG_1	STG_0
(default) OFF	0	0	0
-9.96	0	0	1
-6.64	0	1	0
-3.32	0	1	1
0	1	0	0
3.32	1	0	1
6.64	1	1	0
9.96	1	1	1

STG_n = Side-tone Gain n

ADDRESS = 0Ch RESERVED

Note: Bits marked "-" are reserved bits and should be written with logic "0".

ADDRESS = 0Dh RESERVED

Control Register 1 ADDRESS = 0Eh WRITE/READ VERIFY

Power Reset Value
100X X000

PD	Tfhp	DialEN	-	-	B2/$\overline{B1}$	RxMute	TxMute
7	6	5	4	3	2	1	0

PD	When high, the crystal oscillator and FDI blocks are powered down. When low, the oscillator and FDI circuits are active.
Tfhp	When High, an additional highpass function (passband beginning at 400 Hz) is inserted into the transmit path. When low, this highpass filter is disabled.
DialEN	When high, a first order lowpass filter is inserted into the receive path (3 dB = 1.2 kHz). When low, this lowpass filter is disabled.
B2/$\overline{B1}$	When high, the receive Filter/CODEC operates on the B2-Channel. When low, the receive Filter/CODEC operates on the B1-Channel. This control bit has significance only for ST-BUS operation and is ignored for SSI operation.
RxMUTE	When high the received PCM stream is interrupted and replaced with quiet code; thus forcing the receive path into a mute state. When low the full receive path functions normally.
TxMUTE	When high the transmit PCM stream is interrupted and replaced with quiet code; thus forcing the output code into a mute state (only the output code is muted, the transmit microphone and transmit Filter/CODEC are still functional). When low the full transmit path functions normally.

Control Register 2 ADDRESS = 0Fh WRITE/READ VERIFY

Power Reset Value
0X00 00XX

RST	-	A/$\overline{\mu}$	Smag/$\overline{\text{CCITT}}$	RxINC	TxINC	-	-
7	6	5	4	3	2	1	0

RST	When high, a software reset occurs performing the same function as the hardware reset ($\overline{\text{PWRST}}$) except that the microport and watchdog circuitry are not affected. A software reset can be removed only by writing this bit low or by a $\overline{\text{PWRST}}$. When low, the reset condition is removed.
A/$\overline{\mu}$	When high, A-Law (de)coding is selected for the Filter/CODEC and DTMF generator circuits. When low, μ-Law (de)coding is selected for these circuits.
Smag/$\overline{\text{CCITT}}$	When high, sign-magnitude code assignment is selected for the CODEC input/output. When low, CCITT code assignment is selected for the CODEC input/output; true sign, inverted magnitude (μ-Law) or true sign, alternate digit inversion (A-Law).
RxINC	When high, the receiver driver nominal gain is set at -9.6 dB. When low, this driver nominal gain is set at -12.1 dB.
TxINC	When high, the transmit amplifier nominal gain is set at 15.3 dB. When low, this amplifier nominal gain is set at 6.0 dB.

Note: Bits marked "-" are reserved bits and should be written with logic "0".

FDI Control Register ADDRESS = 10h WRITE/READ VERIFY

-	ST-BUS/$\overline{SSI}$	CEN	DEN	D8	Asynch/$\overline{Synch}$	CSL_1	CSL_0
7	6	5	4	3	2	1	0

Power Reset Value
X000 0000

ST-BUS/$\overline{SSI}$ — When high, the FDI port operates in ST-BUS mode. When low, the FDI operates in $\overline{SSI}$ mode.

CEN — When high, data written into the C-Channel register (address 14h) are transmitted during channel 1 on DSTo. When low, the channel 1 timeslot is tri-stated on DSTo. Channel 1 data received on DSTi is read via the C-Channel register (address 14h) regardless of the state of CEN. This control bit has significance only for ST-BUS operation and is ignored for SSI operation.

DEN — When high, data written into the D-Channel Register (address 15h) are transmitted during channel 0 on DSTo. When low, the channel 0 timeslot is tri-stated on DSTo. Channel 0 data received on DSTi is read via the D-Channel register regardless of the state of DEN. This control bit has significance only for ST-BUS mode and is ignored for SSI operation.

D8 — When high, the D-Channel operates at 8 kb/s.

When low, the D-Channel operates at 16 kb/s default.

Asynch/$\overline{Synch}$, CSL_1,CSL_0 — Control bits Asynch/$\overline{Synch}$, CSL_1 and CSL_0 are used to program the data clock (BCL) bit rates as shown in the following table (CSL_1 and CSL_0 are ignored in ST-BUS mode):

Asynch/$\overline{Synch}$	CSL_1	CSL_0	Bit Clock Rate (kHz)	CLOCKin (kHz)
1	0	0	128	4096 mandatory
1	0	1	256	4096 mandatory
0	0	0	512	512
0	0	1	1536	1536
0	1	0	2048	2048
0	1	1	4096	4096

Note: Asynch/$\overline{Synch}$ must be set low for ST-BUS operation

Watchdog Register ADDRESS = 11h WRITE

-	-	-	0	1	0	1	0
7	6	5	4	3	2	1	0

Power Reset Value
XXXX XXXX

Note: Bits marked "-" are reserved bits and should be written with logic "0".

Transmit Path Control Register

ADDRESS = 12h WRITE/READ VERIFY

Power Reset Value
XXXX 0000

7	6	5	4	3	2	1	0
-	-	-	-	b3	b2	b1	b0

Control bits b0 to b3 are used to configure the transmit path and select the transmit source. Note that for SSI mode all selections where b3 = 1 are not used and are interpreted as b0 - b3 = 0 (i.e., transmit path off).

Destination	Source Programming b_3	b_2	b_1	b_0	
B1	0	0	0	0	B_1 & B_2 Off
	0	0	0	1	Handset mic (M + /M -)
	0	0	1	0	Handsfree mic (MIC +)
	0	0	1	1	AUXin
	0	1	0	0	Tx tones
	0	1	0	1	Reserved
	0	1	1	0	Reserved
	0	1	1	1	Reserved
B2	1	0	0	0	Reserved
	1	0	0	1	Handset mic (M + /M -)
	1	0	1	0	Handsfree ic (MIC +)
	1	0	1	1	AUXin
	1	1	0	0	Tx Tones
	1	1	0	1	Reserved
	1	1	1	0	Reserved
	1	1	1	1	Reserved

Receive Path Control Register

ADDRESS = 13h WRITE/READ VERIFY

Power Reset Value
0000 0000

7	6	5	4	3	2	1	0
b7	b6	b5	b4	b3	b2	b1	b0

Control bits b0 to b7 are used to assign a signal source individually to each receive path output. In addition transmit to receive voice sidetone path control is included.

Destination	Source Programming			
Handset Speaker	b_1	b_0		
	0	0		Off
	0	1		Rx Filter
	1	0		AUXin
	1	1		Reserved
Handsfree Speaker	b_3	b_2		
	0	0		Off
	0	1		Rx Filter
	1	0		AUXin
	1	1		Ringer
Aux out	b_6	b_5	b_4	
	0	0	0	Off
	0	0	1	Rx Filter
	0	1	0	Reserved
	0	1	1	AUXin
	1	0	0	Handset mic (M+ /M -)
	1	0	1	Handsfree mic (MIC +)
	1	1	0	Reserved
	1	1	1	Reserved
Voice Sidetone	b_7			
	0	Voice sidetone path disabled		
	1	Voice sidetone path enabled		

Note: Bits marked "-" are reserved bits and should be written with logic "0".

C-Channel Register ADDRESS = 14h WRITE/READ

Power Reset Value
1111 1111

B7	B6	B5	B4	B3	B2	B1	B0
7	6	5	4	3	2	1	0

Micro-port access to the ST-BUS C-Channel information

D-Channel Register ADDRESS = 15h WRITE/READ

Power Reset Value
1111 1111

D7	D6	D5	D4	D3	D2	D1	D0
7	6	5	4	3	2	1	0

ADDRESS = 16h RESERVED

Loopback Register ADDRESS = 17h WRITE/READ VERIFY

Power Reset Value
XX00 XXXX

-	-	Loop2	Loop1	-	-	-	-
7	6	5	4	3	2	1	0

Loop1 When high, the selected B-channel in ST-BUS mode (i.e., B2/$\overline{B1}$ and Transmit and Receive Path selections) or the strobed B-channel in SSI mode is looped back from Din to Dout through the FDI block. The C & D channels (ST-BUS mode) are not looped back. When low, the device operates normally.

Loop2 When high, Loop1 is invoked with the transmit and receive digital gain adjustment being included. This loopback should only be used if PCM resides in the B-channel. If a data pattern is being looped back then use Loop1 or use Loop2 after ensuring that the transmit and receive digital gain registers are set to 0dB (address 19h). When low, the device operates normally.

Notes:
1) do not enable Loop1 and Loop2 simultaneously.
2) both loopback modes add an extra frame delay to the data transmission.
3) ensure that all other bits of address 17h are written logic low when accessing this register.

Note: Bits marked "-" are reserved bits and should be written with logic "0".

DTMF/Tone Ringer Control Register ADDRESS = 18h WRITE/READ VERIFY

Power Reset Value
0000 XXX0

7	6	5	4	3	2	1	0
HiEN	LoEN	DTMF St EN	Ring En	-	-	-	WR

HiEN, LoEN — When high, the programmed tone, for the respective high or low group, is generated. When low, tone generation is disabled for the respective low or high group.

DTMF St EN — When high, programmed DTMF is muxed into the receive path replacing the receive PCM signal. When low, the receive path functions normally.

Ring EN — When high, the tone ringer generator is enabled using the coefficients at addresses 1Ah and 1Bh as well as the WR control bit. For the ringer tone to be applied to the loudspeaker the proper path must be selected via the Receive Path Control Register (address 13h). When low, the ring generator circuit is disabled.

WR — When high, the tone ringer circuit will toggle between the two programmed frequencies at a 5 Hz rate. When low, the tone ringer warble rate is 10Hz.

Digital Gain Register ADDRESS = 19h WRITE/READ VERIFY

Power Reset Value
1000 1000

7	6	5	4	3	2	1	0
TxG_3	TxG_2	TxG_1	TxG_0	RxG_3	RxG_2	RxG_1	RxG_0

Transmit (TxG_{3-0}) and receive (RxG_{3-0}) control bits for programming gain in 3 dB increments.

RxG_3	RxG_2	RxG_1	RxG_0	Gain Adjustment (dB)	TxG_3	TxG_2	TxG_1	TxG_0
0	0	0	0	-24	0	0	0	0
0	0	0	1	-21	0	0	0	1
0	0	1	0	-18	0	0	1	0
0	0	1	1	-15	0	0	1	1
0	1	0	0	-12	0	1	0	0
0	1	0	1	-9	0	1	0	1
0	1	1	0	-6	0	1	1	0
0	1	1	1	-3	0	1	1	1
1	0	0	0	0	1	0	0	0
1	0	0	1	+3	1	0	0	1
1	0	1	0	+6	1	0	1	0
1	0	1	1	+9	1	0	1	1
1	1	0	0	+12	1	1	0	0
1	1	0	1	+15	1	1	0	1
1	1	1	0	+18	1	1	1	0
1	1	1	1	+21	1	1	1	1

Low Tone Coefficient Register ADDRESS = 1Ah WRITE/READ VERIFY

Power Reset Value
0000 0000

7	6	5	4	3	2	1	0
L7	L6	L5	L4	L3	L2	L1	L0

The frequency of the low group tone is programmed by writing an 8-bit hexadecimal coefficient at this address according to the following equation:

Frequency (in Hz) = 7.8125 x COEFF

Where the hexadecimal COEFF is converted into a decimal integer between 0 and 255. Frequency resolution is 7.8125Hz in the range 0 to 1992 Hz.

Note: Bits marked "-" are reserved bits and should be written with logic "0".

High Tone Coefficient Register ADDRESS = 1Bh WRITE/READ VERIFY

H7	H6	H5	H4	H3	H2	H1	H0
7	6	5	4	3	2	1	0

Power Reset Value
0000 0000

The frequency of the high group tone is programmed by writing an 8-bit hexadecimal coefficient at this address according to the following equation:

Frequency (in Hz) = 7.8125 x COEFF

Where the hexadecimal COEFF is converted into a decimal integer between 0 and 255. Frequency resolution is 7.8125Hz in the range 0 to 1992 Hz.

Anti-Howl Control Register ADDRESS = 1Ch WRITE/READ VERIFY

Enable	-	MS1	MS0	-	Pad2	Pad1	Pad0
7	6	5	4	3	2	1	0

Power Reset Value
0X10 X100

Enable — When high, the anti-howling circuit is enabled. When low, the anti-howling circuit is disabled.

MS1, MS0 — Encode the operational mode of the anti-howling circuit as follows. Details of each mode are found in the functional description of the anti-howling circuit.

MS1	MS0	Operational Mode
0	0	Transmit Noise Squelch
0	1	Receive Noise Squelch
1	0	Anti-howling for group listening
1	1	Tx/Rx Switched Loss

Pad2-0 — Three bits encoding the attenuation depth which will be switched into the transmit or receive paths by the anti-howling circuit. Note that 12 dB is the default value.

Pad2	Pad1	Pad0	Attenuation (dB)
0	0	0	0
0	0	1	3
0	1	0	6
0	1	1	9
1	0	0	12
1	0	1	15
1	1	0	18
1	1	1	21

High Threshold Register ADDRESS = 1Dh WRITE/READ VERIFY

-	THh6	THh5	THh4	THh3	THh2	THh1	THh0
7	6	5	4	3	2	1	0

Power Reset Value
X011 0000

THh6-0 — Seven bits encoding the magnitude of the high threshold level. Encoding is in PCM sign-magnitude excluding the sign bit. THh0 - THh3 encode the step number while THh4 - THh6 encode the chord number. The default setting of 'X011 0000' encodes chord 3 step 0. The difference between the high and low thresholds defines the hysteresis for anti-howling.

Low Threshold Register ADDRESS = 1Eh WRITE/READ VERIFY

-	THl6	THl5	THl4	THl3	THl2	THl1	THl0
7	6	5	4	3	2	1	0

Power Reset Value
X001 0100

THl6-0 — Seven bits encoding the magnitude of the low threshold level. Encoding is in PCM sign-magnitude excluding the sign bit. THl0 - THl3 encode the step number while THl4 - THl6 encode the chord number. The default setting of 'X001 0100' encodes chord 1 step 4. The difference between the high and low thresholds defines the hysteresis for anti-howling.

ADDRESSES 1Fh to 3Fh are RESERVED

Note: Bits marked "-" are reserved bits and should be written with logic "0".

Applications

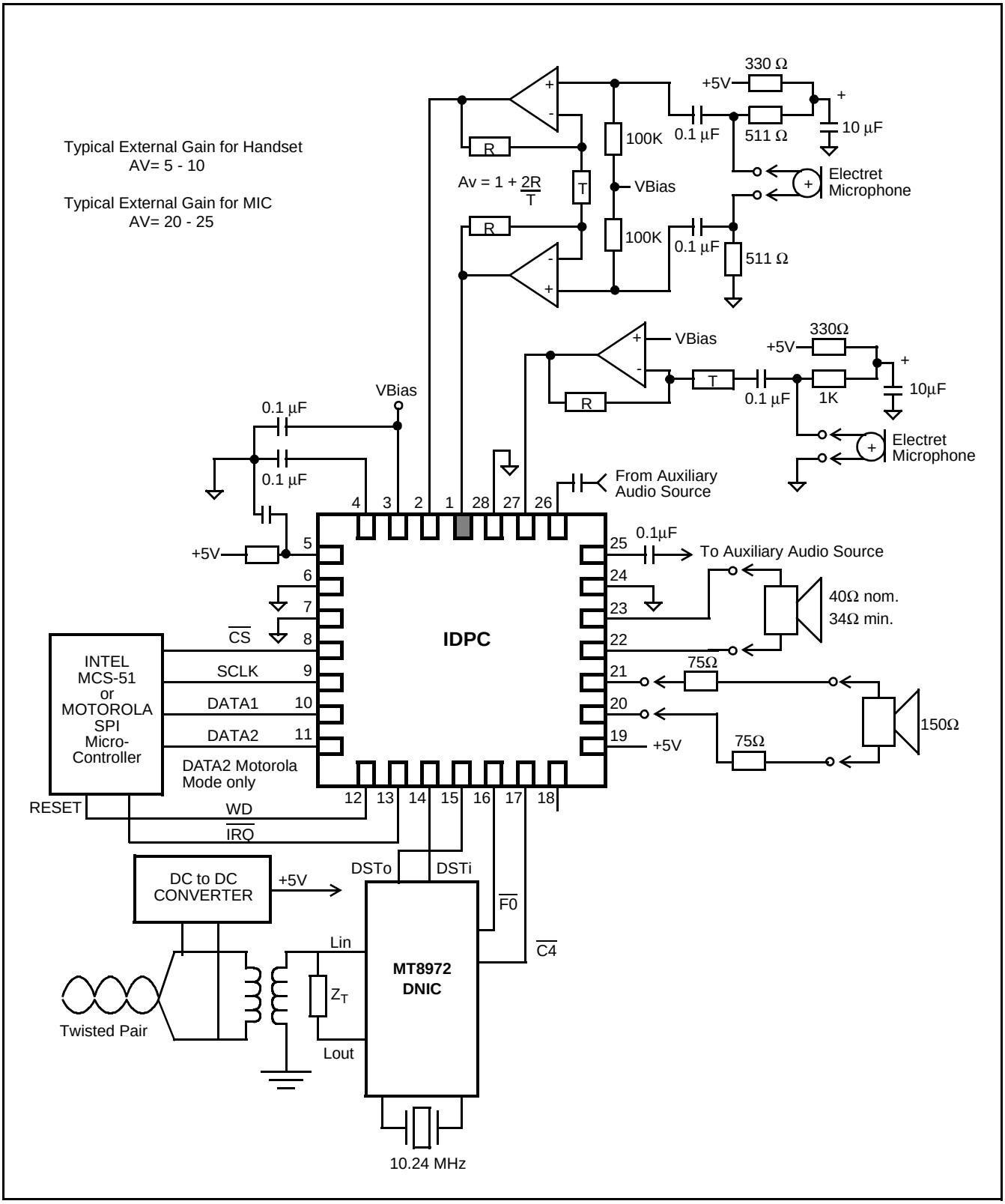


Figure 10 - ST-BUS Application Circuit with MT8972 (DNIC)

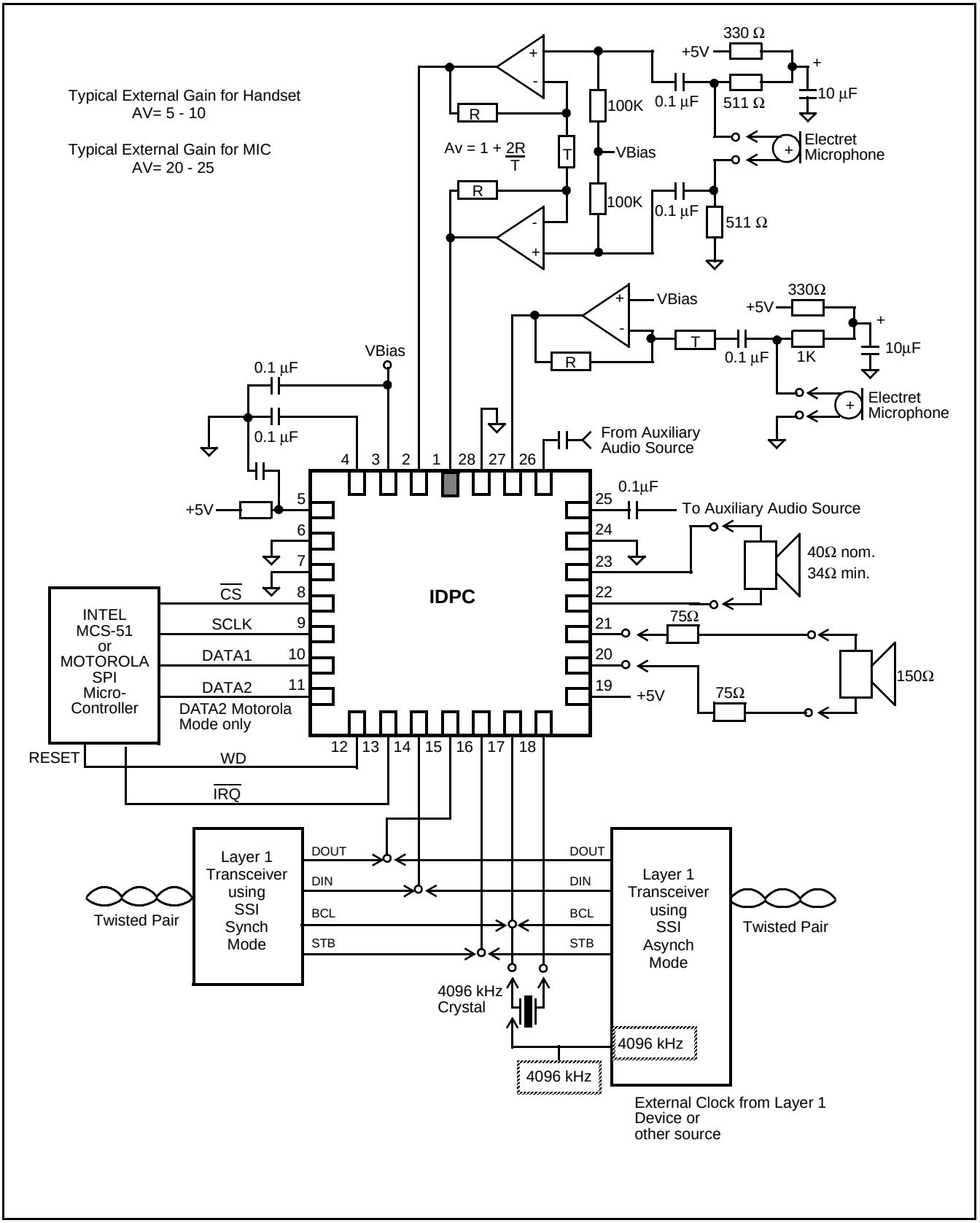


Figure 11 - SSI Application Circuit showing Synchronous or Asynchronous Operation

Programming Examples

Some examples of the programming steps required to set-up various telephony functions are given. Note that these steps are from the power-up reset default definition. If some other state is currently true then some programming steps may be omitted while new ones may be required.

Initialization

Description	Address	DATA
choose ST-BUS vs SSI		
(ie ST-BUS with C&D channels enabled)	10h	70h
or (ie SSI at 256kHz BCL)	10h	05h
power up oscillator and FDI	0Eh	00h (other bits as required)
same as above with B2 channel for ST-BUS	0Eh	04h (other bits as required)
A-Law vs μ-Law as required		
(ie CCITT μ-Law and gains low)	0Fh	00h (default value so no write required)
or (ie CCITT A-Law and gains increased)	0Fh	2Ch

Standard Full-duplex handset call

Description	Address	DATA
program Initialization steps above		
set sidetone gain (ie 0 dB)	0Bh	04h (leave speaker gain defaulted to 0dB)
set gain (ie Rx = +3 dB, Tx = 0 dB)	19h	89h (or as required, defaults = 0dB)
select transmit path		
(ie handset mic to B2 for ST-BUS)	12h	09h
or (ie handset mic for SSI)	12h	01h
select receive path		
(ie handset speaker to Rx filter plus sidetone)	13h	81h (for standard headset only)
	13h	91h
or (as above plus receive to AUXout also)		
optional:		
set Filter/CODEC Rx and Tx gain	0Ah	as required (0dB default)

Group Listening

Description	Address	DATA
program Initialization steps above		
set gain (ie Rx = +3 dB, Tx = 0 dB)	19h	89h (or as required, defaults = 0dB)
set sidetone gain (ie 0 dB) and also set handsfree speaker gain independent of the rest of the receive path (ie 12dB)	0Bh	94h
set high threshold level	1Dh	as required or leave default value
set low threshold level	1Eh	as required or leave default value
enable group listening with 12dB of atten.	1Ch	A4h
select transmit path		
(ie handset mic to B2 for ST-BUS)	12h	09h
or (ie handset mic for SSI)	12h	01h
select receive path (ie Rx filter to both handset and handsfree speakers with sidetone)	13h	85h

Generate tone ringer

Description	Address	DATA
Program Initialization steps above except A-Law vs μ-Law choices are not required.		
set speaker gain (ie -12dB)	0Bh	50h (or as required)
write low tone coefficient	1Ah	as required
write high tone coefficient	1Bh	as required
select ringer as source for loudspeaker	13h	0Ch
start tone ringer (warble = 5Hz)	18h	11h
or (warble = 10Hz)	18h	10h (default)
control ringer cadence by toggling Ring EN (ie warble = 10Hz)	18h	10h (on) 00h (off) 10h (on) 00h (off) etc...

Generate DTMF tones transmit only

Description	Address	DATA
Program Initialization steps above		
set Tx digital gain (ie 0 dB) (-4dBm0/μ-Law,-10dBm0/A-Law)	19h	80h (or as required)
write low tone coefficient	1Ah	as required
write high tone coefficient	1Bh	as required
select transmit path		
(ie Tx tones to B2 for ST-BUS)	12h	0Ch
or (ie Tx tones for SSI)	12h	04h
start DTMF	18h	C0h (both Hi EN and Lo EN)
or for single tones	18h	80h or 40h as required

DTMF sidetones only

Description	Address	DATA
Program Initialization steps above		
set Rx digital gain (ie 0 dB) (-28dBm0)	19h	08h (or as required)
write low tone coefficient	1Ah	as required
write high tone coefficient	1Bh	as required
select receive path		
(ie Rx Filter to handset)	13h	01h
or (ie Rx Filter to handsfree speaker)	13h	04h
or (ie Rx Filter to AUX out)	13h	10h
start DTMF program with sidetone	18h	E0h (both Hi EN and Lo EN)
or for single tones	18h	A0h or 60h as required

DTMF transmit and sidetone

Description	Address	DATA
Program Initialization steps above		
set Tx digital gain (ie 0 dB) (-4dBm0/μ-Law,-10dBm0/A-Law) set Rx digital gain (ie 0 dB) (-28dBm0)	19h	88h (or as required)
write low tone coefficient	1Ah	as required
write high tone coefficient	1Bh	as required
select transmit path		
(ie Tx tones to B2 for ST-BUS)	12h	0Ch
or (ie Tx tones for SSI)	12h	04h
select receive path		
(ie Rx Filter to handset)	13h	01h
or (ie Rx Filter to handsfree speaker)	13h	04h
or (ie Rx Filter to AUX out)	13h	10h
start DTMF program with sidetone	18h	E0h (both Hi EN and LO EN)
or for single tones	18h	A0h or 60h as required

Absolute Maximum Ratings

	Parameter	Symbol	Min.	Max.	Units
1	Supply Voltage	V_{DD} - V_{SS}	- 0.3	7	V
2	Voltage on any I/O pin	V_I/V_O	V_{SS} - 0.3	V_{DD} + 0.3	V
3	Current on any I/O pin (transducers excluded)	I_I/I_O		± 20	mA
4	Storage Temperature	T_S	- 65	+ 150	°C
5	Power Dissipation (package) Plastic	P_D		750	mW

Recommended Operating Conditions - Voltages are with respect to V_{SS} unless otherwise stated

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	Supply Voltage	V_{DD}	4.75	5	5.25	V	
2	TTL Input Voltage (high)*	V_{IHT}	2.4		V_{DD}	V	Includes Noise margin = 400 mV
3	TTL Input Voltage (low)*	V_{ILT}	V_{SS}		0.4	V	Includes Noise margin = 400 mV
4	CMOS Input Voltage (high)	V_{IHC}	4.5		V_{DD}	V	
5	CMOS Input Voltage (low)	V_{ILC}	V_{SS}		0.5	V	
6	Operating Temperature	T_A	- 40		+ 85	°C	

* Excluding $\overline{\text{PWRST}}$ which is a Schmitt Trigger Input.

Power Characteristics

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	Supply Current (clock disabled, all functions off, P_D=1)	I_{DDC1}		400		µA	Outputs unloaded, Input signals static, not loaded
2	Supply Current by function:						
	Filter/Codec	I_{DDF1}		1.5		mA	
	Digital Gain/Tone	I_{DDF2}		1.5		mA	
	Handset Driver (bias only, no signal)	I_{DDF3}		1.25		mA	See Note 1.
	Speaker Driver (bias only, no signal)	I_{DDF4}		1.25		mA	See Note 1.
	Timing Control, C-channel, ST-BUS, etc.	I_{DDF5}		1.0		mA	
	Total all functions enabled	I_{DDFT}		14.0	19.0	mA	See Notes 1 & 2.

Note 1: Power delivered to the load is in addition to the bias current requirements.
Note 2: I_{DDFT} is not additive to I_{DDC1}.

DC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Input HIGH Voltage TTL inputs	V_{IHT}	2.0			V	
2	Input LOW Voltage TTL inputs	V_{ILT}			0.8	V	
3	Input HIGH Voltage CMOS inputs	V_{IHC}	3.5			V	
4	Input LOW Voltage CMOS inputs	V_{ILC}			1.5	V	
5	VBias Voltage Output	V_{Bias}		$V_{DD}/2$		V	Max. Load = 10kΩ
6	Input Leakage Current	I_{IZ}		0.1	10	µA	$V_{IN}=V_{DD}$ to V_{SS}
7	Positive Going Threshold Voltage ($\overline{PWRST}$ only) Negative Going Threshold Voltage ($\overline{PWRST}$ only)	V_{T+} V_{T-}	3.7		 1.3	V V	
8	Output HIGH Current	I_{OH}	- 5	- 16		mA	V_{OH} = 2.4V
9	Output LOW Current	I_{OL}	5	10		mA	V_{OL} = 0.4V
10	Output Reference Voltage	V_{Ref}		$V_{DD}/2$-1.5		V	No load
11	Output Leakage Current	I_{OZ}		0.01	10	µA	$V_{OUT} = V_{DD}$ and V_{SS}
12	Output Capacitance	C_o		15		pF	
13	Input Capacitance	C_i		10		pF	

† DC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

CLOCKin Tolerance Characteristics

	Characteristics	Min.	Typ.‡	Max.	Units	Test Conditions
1	CLOCKin ($\overline{C4i}$) Frequency	4095.6	4096	4096.4	kHz	

† AC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

Preferred Crystal Characteristics

Nominal Frequency	4096 kHz
Frequency Tolerance	±100 ppm @25°C
Operating Temperature	-40°C to +85°C
Shunt Capacitance	7pF Maximum
Drive Level	5 mW
Series Resistance	130 Ω maximum
Load Capacitance	20 pF
Frequency Stability	±0.003%/°C from 25°C

AC Characteristics† for A/D (Transmit) Path - 0dBm0 = 1.421V_{rms} for µ-Law and 1.477V_{rms} for A-Law, at the CODEC. (V_{Ref}=1.0 volts and V_{Bias}=2.5 volts.)

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Analog input equivalent to overload decision	$A_{Li3.17}$ $A_{Li3.14}$		5.79 6.0		Vp-p Vp-p	µ-Law A-Law Both at CODEC
2	Absolute half-channel gain						Transmit filter gain=0dB setting. Digital gain=0dB setting.
	M ± to PCM	G_{AX1} G_{AX2}	5.0 14.3	6.0 15.3	7.0 16.3	dB dB	TxINC = 0* TxINC = 1*
	MIC + to PCM	G_{AX3} G_{AX4}	9.5 18.8	11 20.3	12.5 21.8	dB dB	TxINC = 0* TxINC = 1*
	AUXin to PCM	G_{AX5} G_{AX6}	9.5 18.8	11 20.3	12.5 21.8	dB dB	TxINC = 0* TxINC = 1* @1020 Hz
	Tolerance at all other transmit filter settings (1 to 7dB)		-0.2		+0.2	dB	
3	Gain tracking vs. input level CCITT G.714 Method 2	G_{TX}	-0.3 -0.6 -1.6		0.3 0.6 1.6	dB dB dB	3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0
4	Signal to total Distortion vs. input level CCITT G.714 Method 2	D_{QX}	35 29 24			dB dB dB	0 to -30 dBm0 -40 dBm0 -45 dBm0
5	Transmit Idle Channel Noise	N_{CX} N_{PX}		15 -71	16.5 -69	dBrnC0 dBm0p	µ-Law A-Law
6	Gain relative to gain at 1020Hz <50Hz 60Hz 200Hz 300 - 3000 Hz 3000 - 3400 Hz 4000 Hz >4600 Hz	G_{RX}	 -0.25 -0.9 		 -25 -30 0.0 0.25 0.25 -12.5 -25	 dB dB dB dB dB dB dB	
7	Absolute Delay	D_{AX}		360		µs	at frequency of minimum delay
8	Group Delay relative to D_{AX}	D_{DX}		750 380 130 750		µs µs µs µs	500-600 Hz 600 - 1000 Hz 1000 - 2600 Hz 2600 - 2800 Hz
9	Power Supply Rejection f=1020 Hz f=0.3 to 3 kHz f=3 to 4 kHz f=4 to 50 kHz	 PSSR PSSR1 PSSR2 PSSR3	 37 40 35 40			 dB dB dB dB	100mVRMS V_{DD} µ-law PSSR1-3 not production tested

† AC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* Note: TxINC, refer to Control Register 2, address 0Fh.

AC Characteristics† for D/A (Receive) Path - 0dBm0 = 1.421V_{rms} for µ-Law and 1.477V_{rms} for A-Law, at the CODEC. (V_{Ref}=1.0 volts and V_{Bias}=2.5 volts.)

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Analog output at the CODEC full scale	$A_{Lo3.17}$ $A_{Lo3.14}$		5.704 5.906		Vp-p Vp-p	µ-Law A-Law
2	Absolute half-channel gain PCM to HSPKR± PCM to SPKR± PCM to AUXout	 G_{AR1} G_{AR2} G_{AR3} G_{AR4}	 -13.1 -10.6 -1.0 -14	 -12.1 -9.6 0 -12	 -11.1 -8.6 1.0 -10	 dB dB dB dB	Receive filter gain = 0dB setting. Digital gain = 0dB setting. RxINC = 0* RxINC = 1* @1020 Hz
	Tolerance at all other receive filter settings (-1 to -7dB)		-0.2		+0.2	dB	
3	Gain tracking vs. input level CCITT G.714 Method 2	G_{TR}	-0.3 -0.6 -1.6		0.3 0.6 1.6	dB dB dB	3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0
4	Signal to total distortion vs. input level CCITT G.714 Method 2	G_{QR}	35 29 24			dB dB dB	0 to -30 dBm0 -40 dBm0 -45 dBm0
5	Receive Idle Channel Noise	N_{CR} N_{PR}		13 -78.5	15.5 -77	dBrnC0 dBm0p	µ-Law A-Law
6	Gain relative to gain at 1020Hz 200Hz 300 - 3000 Hz 3000 - 3400 Hz 4000 Hz >4600 Hz	G_{RR}	 -0.25 -0.90		 0.25 0.25 0.25 -12.5 -25	 dB dB dB dB dB	
7	Absolute Delay	D_{AR}		240		µs	at frequency of min. delay
8	Group Delay relative to D_{AR}	D_{DR}		750 380 130 750		µs µs µs µs	500-600 Hz 600 - 1000 Hz 1000 - 2600 Hz 2600 - 2800 Hz
9	Crosstalk D/A to A/D A/D to D/A	CT_{RT} CT_{TR}			-74 -80	dB dB	G.714.16

† AC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.
* Note: RxINC, refer to Control Register 2, address 0Fh.

AC Electrical Characteristics† for Side-tone Path

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Absolute path gain Gain adjust = 0dB	G_{AS1} G_{AS2}	-17.2 -14.7	-16.7 -14.2	-16.2 -13.7	dB dB	TxINC, RxINC both 0* TxINC, RxINC both 1* M± inputs to HSPKR± outputs 1000 Hz
	All other settings (-9.96 to +9.96dB)	G_{AS} G_{AS}	-0.3 -0.3		+0.3 +0.3	dB dB	SIDEA/$\overline{u}$=0 SIDEA/$\overline{u}$=1 from nominal relative measurements w.r.t. G_{AS1} & G_{AS2}

† AC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.
* Note: RxINC and TxINC, refer to Control Register 2, address 0Fh.

AC Characteristics† for Auxiliary Analog LoopbackPath

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Absolute gain for analog loopback from Auxiliary port.						
	AUXin to HSPKR±	G_{AA1} G_{AA2}	-3.1 -0.6	-1.1 1.4	0.9 3.4	dB dB	RxINC = 0* RxINC = 1*
	AUXin to SPKR±	G_{AA3}	3.0	5.0	7.0	dB	
	AUXin to AUXout	G_{AA4}	-9	-7	-5	dB	@1020 Hz

† AC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.
* Note: RxINC, refer to Control Register 2, address 0Fh.

AC Electrical Characteristics† for Ringer Tone

	Characteristics	Sym.	Typ.‡	Units	Test Conditions		
1	Ringer Tone Output voltage (SPKR+ to SPKR-)				Gain2	Gain1	Gain0
		V_{R0}	6.0	Vp-p	0	0	0
		V_{R-4}	3.79	Vp-p	0	0	1
		V_{R-8}	2.39	Vp-p	0	1	0
		V_{R-12}	1.51	Vp-p	0	1	1
		V_{R-16}	951	mVp-p	1	0	0
		V_{R-20}	600	mVp-p	1	0	1
		V_{R-24}	379	mVp-p	1	1	0
		V_{R-28}	239	mVp-p	1	1	1
					Gain3 = 0 load>34 ohms across SPKR±		

† AC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

Electrical Characteristics† for Analog Outputs

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Earpiece load impedance	E_{ZL}	260	300		ohms	across HSPKR±
2	Allowable Earpiece capacitive load	E_{CL}		300		pF	each pin: HSPKR+, HSPKR-
3	Earpiece harmonic distortion	E_D			0.5	%	300 ohms load across HSPKR± (tol-15%), VO ≤ 693mV_{RMS}, RxINC=1*, Rx gain=0dB
4	Speaker load impedance	S_{ZL}	34	40		ohms	across SPKR±
5	Allowable Speaker capacitive load	S_{CL}		300		pF	each pin SPKR+, SPKR-
6	Speaker harmonic distortion	S_D			0.5	%	40 ohms load across SPKR± (tol-15%), VO ≤ 6.2Vp-p, Rx gain=0dB

† Electrical Characteristics are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.
* Note: RxINC, refer to Control Register 2, address 0Fh.

Electrical Characteristics† for Analog Inputs

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Input voltage without overloading CODEC						
	at MIC+	V_{IOLM}		1.63 0.580		Vp-p Vp-p	TxINC = 0, A/$\overline{\mu}$ = 0* TxINC = 1, A/$\overline{\mu}$ = 1*
	at AUXin	V_{IOLA}		1.63 0.580		Vp-p Vp-p	TxINC = 1, A/$\overline{\mu}$ = 0* TxINC = 1, A/$\overline{\mu}$ = 1*
	across M+/M-	V_{IOLH}		2.90 1.03		Vp-p Vp-p	TxINC = 0, A/$\overline{\mu}$ = 0* TxINC = 1, A/$\overline{\mu}$ = 1* Tx filter gain=0dB setting
2	Input impedance	Z_I Z_{IA}	50 10			kΩ kΩ	M+/M-, MIC+ AUXin to V_{SS}

† Electrical Characteristics are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.
* Note: TxINC and A/$\overline{\mu}$ and refer to Control Register 2, address 0Fh.

AC Electrical Characteristics† - ST-BUS Timing (See Figure 12)

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	$\overline{C4i}$ Clock Period	t_{C4P}		244		ns	
2	$\overline{C4i}$ Clock High period	t_{C4H}		122		ns	
3	$\overline{C4i}$ Clock Low period	t_{C4L}		122		ns	
4	$\overline{C4i}$ Clock Transition Time	t_T		20		ns	
5	$\overline{F0i}$ Frame Pulse Setup Time	t_{F0iS}	50			ns	
6	$\overline{F0i}$ Frame Pulse Hold Time	t_{F0iH}	50			ns	
7	DSTo Delay	t_{DSToD}		100	125	ns	C_L = 50pF, 1kΩ load.*
8	DSTi Setup Time	t_{DSTiS}	30			ns	
9	DSTi Hold Time	t_{DSTiH}	30			ns	

† Timing is over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.
* Note: All conditions → data-data, data-HiZ, HiZ-data.

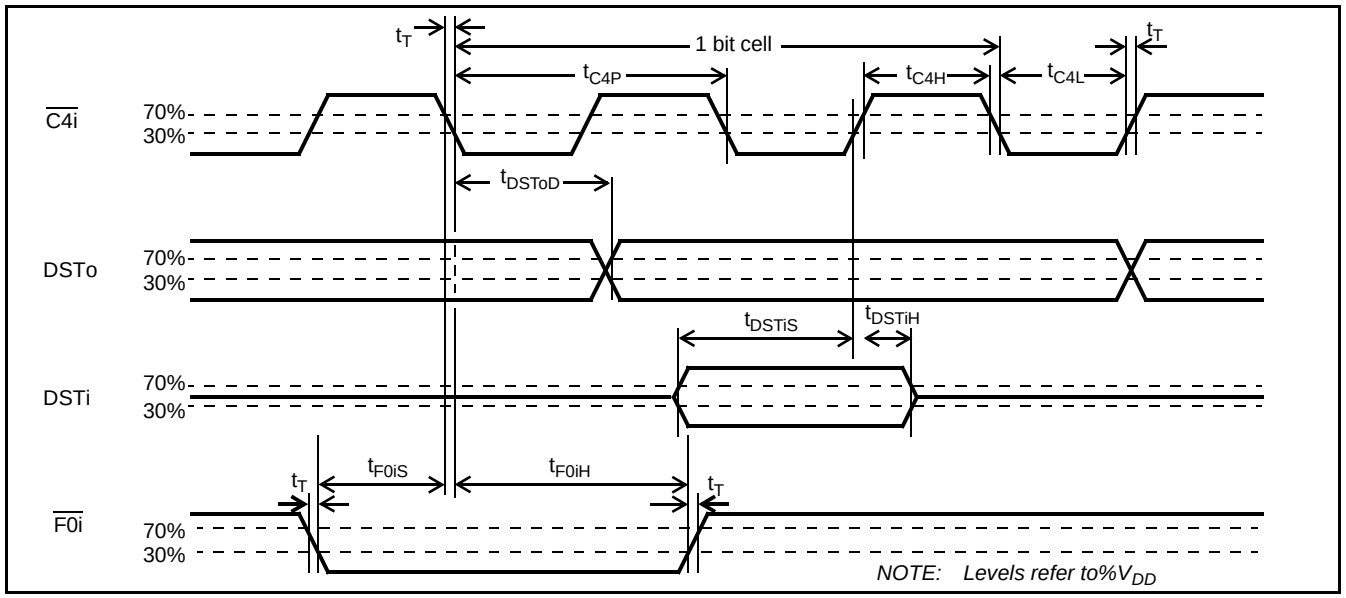


Figure 12 - ST-BUS Timing Diagram

AC Electrical Characteristics† - SSI BUS Synchronous Timing (see Figure 13)

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	BCL Clock Period	t_{BCL}	244		1953	ns	BCL=4096 kHz to 512 kHz
2	BCL Pulse Width High	t_{BCLH}		122		ns	BCL=4096 kHz
3	BCL Pulse Width Low	t_{BCLL}		122		ns	BCL=4096 kHz
4	BCL Rise/Fall Time	t_R/t_F		20		ns	Note 1
5	Strobe Pulse Width	t_{ENW}		8 x t_{BCL}		ns	Note 1
6	Strobe setup time before BCL falling	t_{SSS}	80		t_{BCL}-80	ns	
7	Strobe hold time after BCL falling	t_{SSH}	80		t_{BCL}-80	ns	
8	Dout High Impedance to Active Low from Strobe rising	t_{DOZL}			90	ns	C_L=150 pF, R_L=1K
9	Dout High Impedance to Active High from Strobe rising	t_{DOZH}			90	ns	C_L=150 pF, R_L=1K
10	Dout Active Low to High Impedance from Strobe falling	t_{DOLZ}			90	ns	C_L=150 pF, R_L=1K
11	Dout Active High to High Impedance from Strobe falling	t_{DOHZ}			90	ns	C_L=150 pF, R_L=1K
12	Dout Delay (high and low) from BCL rising	t_{DD}			90	ns	C_L=150 pF
13	Din Setup time before BCL falling	t_{DIS}	50			ns	
14	Din Hold Time from BCL falling	t_{DIH}	50			ns	

† Timing is over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
NOTE 1: Not production tested, guaranteed by design.

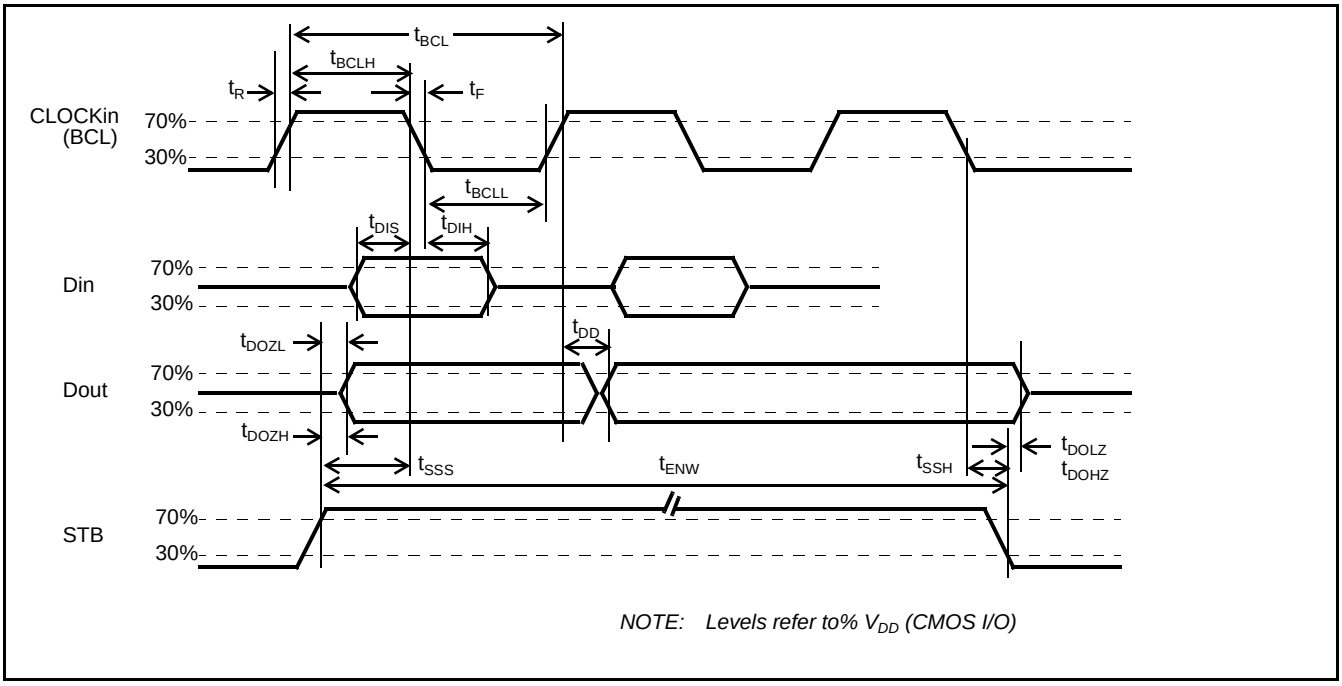


Figure 13 - SSI Synchronous Timing Diagram

AC Electrical Characteristics† - SSI BUS Asynchronous Timing (note 1) (see Figure 14)

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Bit Cell Period	T_{DATA}		7812 3906		ns ns	BCL=128 kHz BCL=256 kHz
2	Frame Jitter	T_j			600	ns	
3	Bit 1 Dout Delay from STB going high	t_{dda1}			T_j+600	ns	C_L=150 pF, R_L=1K
4	Bit 2 Dout Delay from STB going high	t_{dda2}	600+ T_{DATA}-T_j	600+ T_{DATA}	600 + T_{DATA}+T_j	ns	C_L=150 pF, R_L=1K
5	Bit n Dout Delay from STB going high	t_{ddan}	600 + (n-1) x T_{DATA}-T_j	600 + (n-1) x T_{DATA}	600 + (n-1) x T_{DATA}+T_j	ns	C_L=150 pF, R_L=1K n=3 to 8
6	Bit 1 Data Boundary	T_{DATA1}	T_{DATA}-T_j		T_{DATA}+T_j	ns	
7	Din Bit n Data Setup time from STB rising	t_{SU}	T_{DATA}\2 +500ns-T_j +(n-1) x T_{DATA}			ns	n=1-8
8	Din Data Hold time from STB rising	t_{ho}	T_{DATA}\2 +500ns+T_j +(n-1) x T_{DATA}			ns	

† Timing is over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
NOTE 1: Not production tested, guaranteed by design.

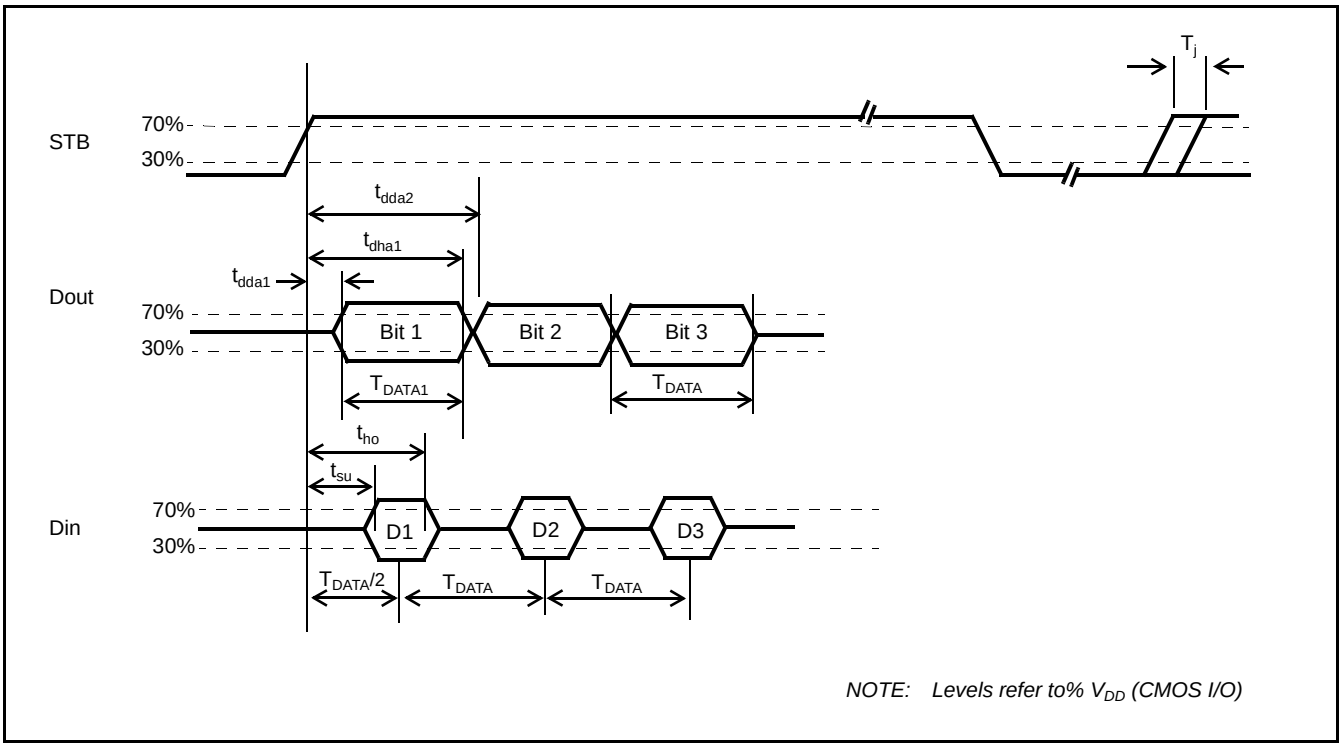


Figure 14 - SSI Asynchronous Timing Diagram

AC Electrical Characteristics† - Microport Timing (see Figure 15)

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Input data setup	t_{IDS}	100			ns	
2	Input data hold	t_{IDH}	30			ns	
3	Output data delay	t_{ODD}			100	ns	C_L = 150pF, R_L = 1K *
4	Serial clock period	t_{CYC}	500	1000		ns	
5	SCLK pulse width high	t_{CH}	250	500		ns	
6	SCLK pulse width low	t_{CL}	250	500		ns	
7	$\overline{CS}$ setup-Intel	t_{CSSI}	200			ns	
8	$\overline{CS}$ setup-Motorola	t_{CSSM}	100			ns	
9	$\overline{CS}$ hold	t_{CSH}	100			ns	
10	$\overline{CS}$ to output high impedance	t_{OHZ}			100	ns	C_L = 150pF, R_L = 1K

† Timing is over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* Note: All conditions → data-data, data-HiZ, HiZ-data.

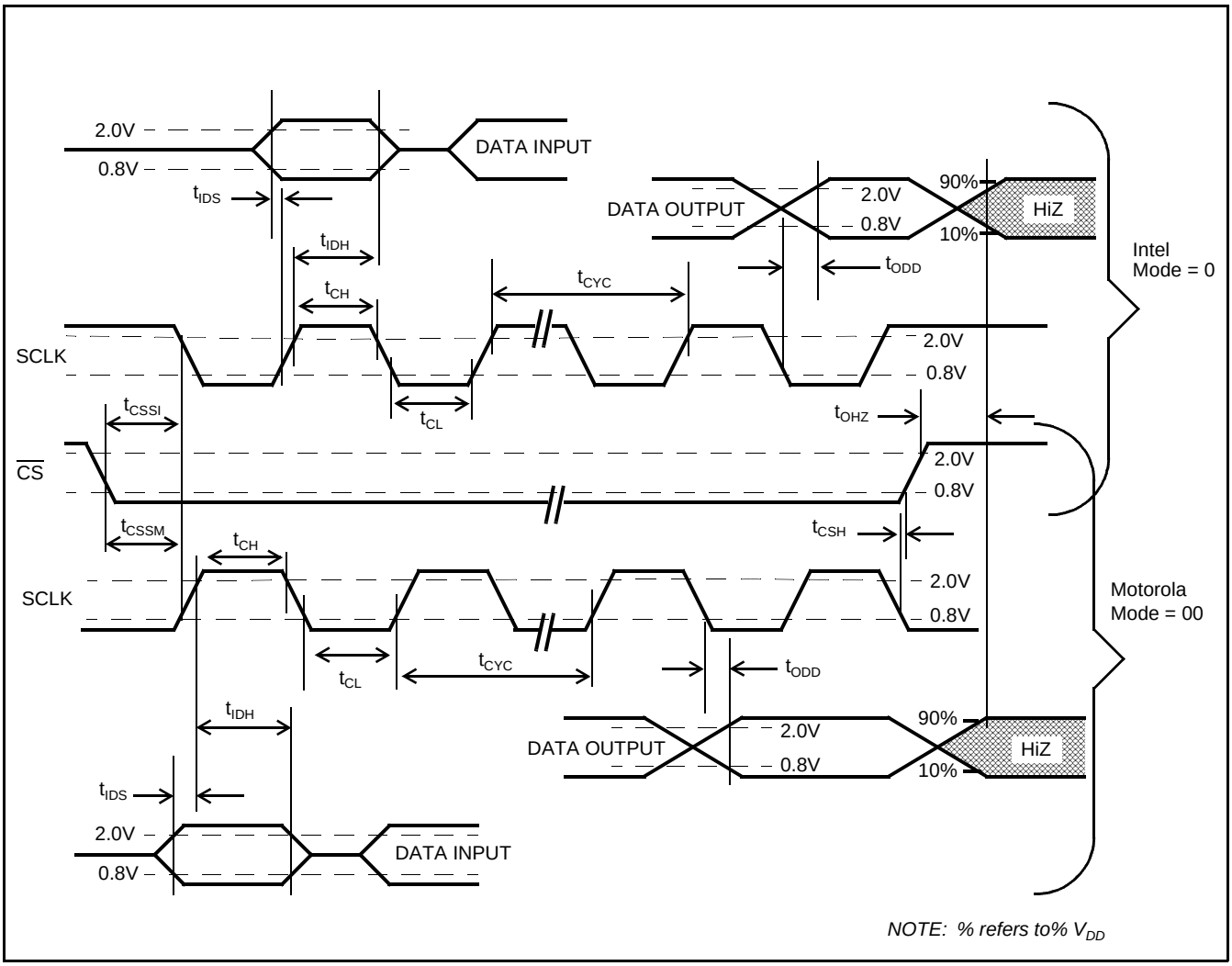
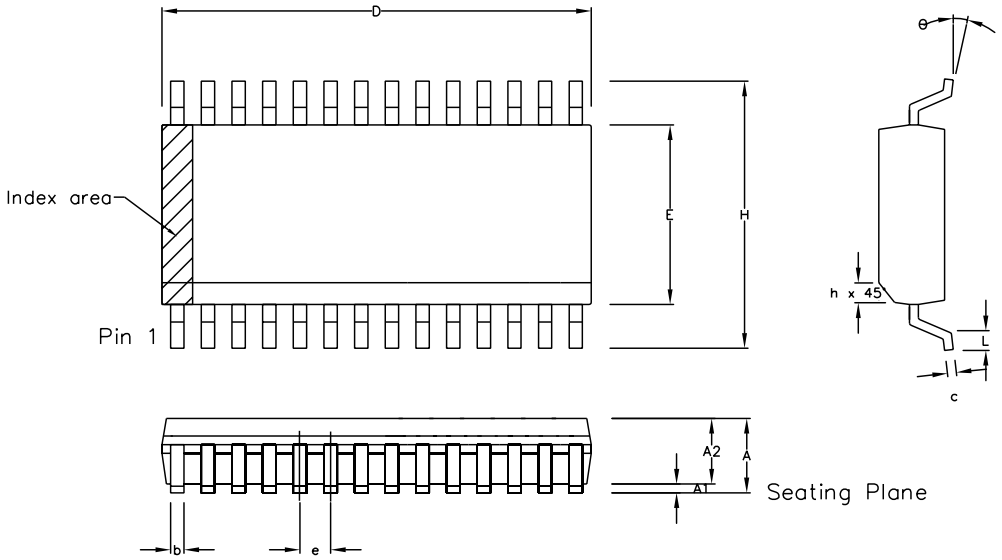


Figure 15 - Serial Microport Timing Diagram



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	2.35		2.65		0.093		0.104
A1	0.10		0.30		0.004		0.012
A2	2.25		2.35		0.089		0.092
D	17.70		18.10		0.697		0.713
H	10.00		10.65		0.394		0.419
E	7.40		7.60		0.291		0.299
L	0.40		1.27		0.016		0.050
e	1.27 BSC.				0.050 BSC.		
b	0.33		0.51		0.013		0.020
c	0.23		0.32		0.009		0.013
θ	0°		8°		0°		8°
h	0.25		0.75		0.010		0.029
	Pin features						
N	28						
Conforms to JEDEC MS-013AE Iss. C							

Notes:
1. The chamfer on the body is optional. If it not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimension D do not include mould flash, protrusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protrusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.004" total in excess of b dimension.

ISSUE	1	2	3	
ACN	6746	201943	213100	
DATE	7Apr95	27Feb97	15Jul02	
APPRD.				

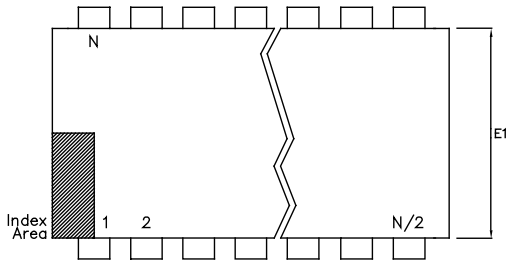
ZARLINK SEMICONDUCTOR

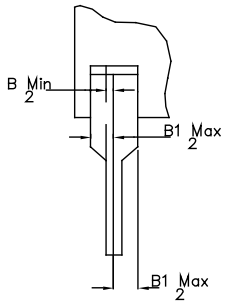
Previous package codes
MP / S

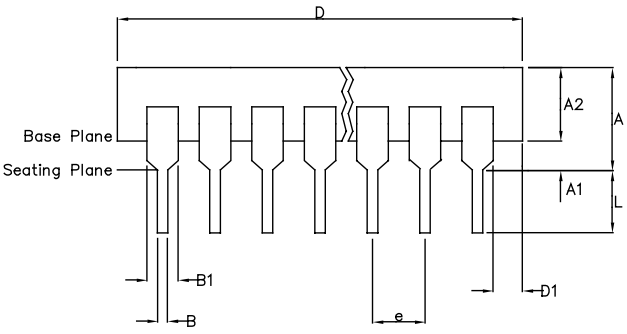
Package Code DC

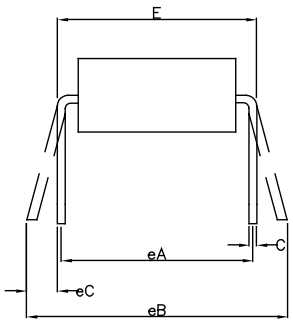
Package Outline for
28 lead SOIC
(0.300" Body Width)

GPD00017









	Min mm	Max mm	Min Inches	Max Inches
A		6.35		0.250
A1	0.38		0.015	
A2	3.18	4.95	0.125	0.195
B	0.36	0.56	0.014	0.022
B1	0.76	1.78	0.030	0.070
C	0.20	0.38	0.008	0.015
D	35.05	39.75	1.380	1.565
D1	0.13		0.005	
E	15.24	15.88	0.600	0.625
E1	12.32	14.73	0.485	0.580
e	2.54 BSC		0.100 BSC	
eA	15.24 BSC		0.600 BSC	
eB		17.78		0.700
L	2.92	5.08	0.115	0.200
N	28		28	
Conforms to Jedec MS-011AB ISS.B				

Notes:
1. Controlling Dimensions are in inches
2. Dimension A, A1 and L are measured with the package seated in the Seating Plane
3. Dimensions D & E1 do not include mould flash or protrusions. Mould flash or protrusion shall not exceed 0.010 inch.
4. Dimensions E & eA are measured with leads constrained to be perpendicular to plane T.
5. Dimensions eB & eC are measured at the lead tips with the leads unconstrained; eC must be zero or greater.

ISSUE	1	2	3	4
ACN	7010	203532	213102	CDCA
DATE	20Apr95	25Nov97	15Jul02	02Dec05
APPRD.				

ZARLINK SEMICONDUCTOR

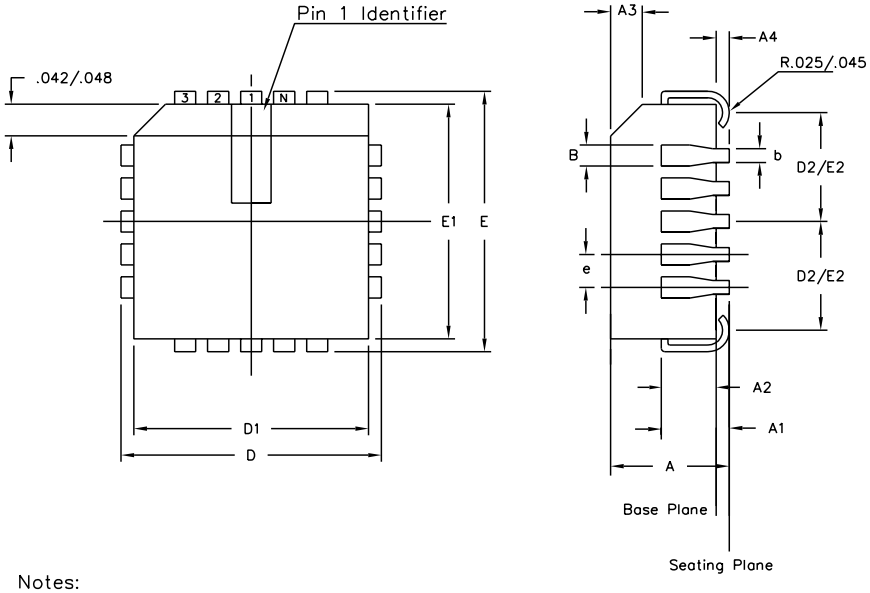
Previous package codes

DP / E

Package Code DA

Package Outline for 28 lead 600mils PDIP

GPD00072



Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.062	0.083	1.57	2.11
A3	0.042	0.056	1.07	1.42
A4	0.020	–	0.51	–
D	0.485	0.495	12.32	12.57
D1	0.450	0.456	11.43	11.58
D2	0.191	0.219	4.85	5.56
E	0.485	0.495	12.32	12.57
E1	0.450	0.456	11.43	11.58
E2	0.191	0.219	4.85	5.56
B	0.026	0.032	0.66	0.81
b	0.013	0.021	0.33	0.53
e	0.050 BSC		1.27 BSC	
	Pin features			
ND	7			
NE	7			
N	28			
Note	Square			
Conforms to JEDEC MS-018AB Iss. A				

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M–1982
2. Dimensions D1 and E1 do not include mould protrusions. Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
3. Controlling dimensions in Inches.
4. "N" is the number of terminals.
5. Not To Scale
6. Dimension R required for 120° minimum bend.

ISSUE	1	2	3	
ACN	5958	207469	212422	
DATE	15Aug94	10Sep99	22Mar02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes
HP / P

Package Code QA

Package Outline for 28 lead PLCC

GPD00002

For more information about all Zarlink products visit our Web Site at

www.zarlink.com

TECHNICAL DOCUMENTATION - NOT FOR RESALE