

APPLICATIONS

- Enables a cost effective voice solution for long or short loop applications providing POTS and integrated test capabilities
 - CO
 - DLC
 - PBX/KTS
 - Pair gain

FEATURES

- **Monitor of two-wire interface voltages and currents supports**
 - Voice transmission
 - Internal chip ring generation
 - Programmable DC feed characteristics
 - Independent of battery
 - Current limited
 - Selectable off-hook and ground-key thresholds
 - Subscriber line diagnostics
 - Leakage resistance
 - Loop resistance
 - Line capacitance
 - Bell capacitance
 - Foreign voltage sensing
 - Power cross and fault detection
- **Supports internal short loop or external ringing**
- **+5 V and battery supplies**
- **Dual battery operation for system power saving**
 - Automatic battery switching
 - Intelligent thermal management
- **Compatible with inexpensive protection networks**
 - Accommodates low tolerance fuse resistors or PTC thermistors
- **Metering capable**
 - 12 kHz and 16 kHz
 - Smooth polarity reversal
- **Tip-open state supports ground start signaling**
- **Integrated test load switches/relay drivers**
- **5 REN with DC offset trapezoid.**
 - For US standard:
 - drives ring up to 4.4 kft of 26 gauge wire.
 - drives ring up to 7 kft of 24 gauge wire.
 - For European (British) standard:
 - drives ring up to 1.7 km of 0.5 mm copper cable.
- **Space Saving Package Options (8x8 QFN)**

ORDERING INFORMATION

A VE790 series ISLAC™ device must be used with this part.

Device	Package Type ^{1, 2}	Packing ³
Le79R241JC	32-pin PLCC	Tube
Le79R241DJC	32-pin PLCC (Green)	
Le79R241QC	32-pin QFN	Tray
Le79R241FQC	32-pin QFN (Green)	

1. Due to size constraints, QFN devices are marked by omitting the "Le" prefix and the performance grade dash character. For example, Le79R241QC is marked 79R241QC.
2. The green package meets RoHS Directive 2002/95/EC of the European Council to minimize the environmental impact of electrical equipment.
3. For delivery using a tape and reel packing system, add a "T" suffix to the OPN (Ordering Part Number) when placing an order.

DESCRIPTION

The Le79R241 Intelligent Subscriber Line Interface Circuit (ISLIC™) device, in combination with a VE790 series ISLAC™ device, implements the telephone line interface function. This enables the design of a low cost, high performance, fully software programmable line interface for multiple country applications worldwide. All AC, DC, and signaling parameters are fully programmable via microprocessor or GCI interfaces on the VE790 series ISLAC device. Additionally, the Le79R241 ISLIC device has integrated self-test and line-test capabilities to resolve faults to the line or line circuit. The integrated test capability is crucial for remote applications where dedicated test hardware is not cost effective.

RELATED LITERATURE

- 080248 Le79231 ISLIC™ Device Data Sheet
- 080253 Le79R251 ISLIC™ Device Data Sheet
- 080250 Le79Q224x Quad ISLAC™ Device Data Sheet
- 081065 Le79228 Quad ISLAC™ Device Data Sheet
- 080262 VE790 Series Evaluation Board User's Guide
- 080804 Le79R2xx/Le79Q224x Chip Set User's Guide
- 080923 Le79R2xx/Le79228 Chip Set User's Guide
- 081103 Le79610 PacketSLAC™ Device Data Sheet

NOTE: On August 3, 2007, Zarlink Semiconductor acquired the products and technology of Legerity Holdings.

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PRODUCT DESCRIPTION

Legerity's VE790 series voice chip sets integrate all functions of the subscriber line. Two chip types are used to implement the line card — the Le79R241 ISLIC device and a VE790 series ISLAC device. These provide the following basic functions:

1. The Le79R241 ISLIC device: A high voltage, bipolar device that drives the subscriber line, maintains longitudinal balance and senses line conditions.
2. The VE790 series ISLAC devices: Low voltage CMOS ICs that provide conversion, control and DSP functions for the Le79R241 ISLIC device.

A complete schematic of the line card using a VoiceEdge chip set for internal and external ringing is shown in [Application Circuits, on page 19](#).

The Le79R241 ISLIC device uses reliable, bipolar technology to provide the power necessary to drive a wide variety of subscriber lines. It can be programmed by the VE790 series ISLAC device to operate in eight different modes that control power consumption and signaling. This enables it to have full control over the subscriber loop. The Le79R241 ISLIC device is designed to be used exclusively with the VE790 series ISLAC devices. The Le79R241 ISLIC device requires only +5 V power and the battery supplies for its operation.

The Le79R241 ISLIC device implements a linear loop-current feeding method with the enhancement of intelligent thermal management. This limits the amount of power dissipated on the Le79R241 ISLIC device by dissipating power in external resistors in a controlled manner.

Each codec contains high-performance circuits that provide A/D and D/A conversion for the voice (codec), DC-feed and supervision signals. The VE790 series ISLAC devices contain a DSP core that handles signaling, DC-feed, supervision and line diagnostics for all channels.

The DSP core selectively interfaces with three types of backplanes:

- Standard PCM/MPI
- Standard GCI
- Modified GCI with a single analog line per GCI channel

The 790 series voice chip set provides a complete software configurable solution to the BORSCHT functions as well as complete programmable control over subscriber line DC-feed characteristics, such as current limit and feed resistance. In addition, these chip sets provide system level solutions for the loop supervisory functions and metering. In total, they provide a programmable solution that can satisfy worldwide line card requirements by software configuration.

Software programmed filter coefficients, DC-feed data and supervision data are easily calculated with WinSLAC™ software. This PC software is provided free of charge. It allows the designer to enter a description of system requirements. WinSLAC then computes the necessary coefficients and plots the predicted system results.

The Le79R241 ISLIC device interface unit inside the VE790 series ISLAC device processes information regarding the line voltages, loop currents and battery voltage levels. These inputs allow the VE790 series ISLAC device to place several key Le79R241 ISLIC device performance parameters under software control.

The main functions that can be observed and/or controlled through the VE790 series ISLAC device backplane interface are:

- DC-feed characteristics
- Ground-key detection
- Off-hook detection
- Metering signal
- Longitudinal operating point
- Subscriber line voltage and currents
- Ring-trip detection
- Abrupt and smooth battery reversal
- Subscriber line matching
- Ringing generation
- Sophisticated line and circuit tests

To accomplish these functions, the Le79R241 ISLIC device collects the following information and feeds it, in analog form, to the VE790 series ISLAC device:

- The metallic (IMT) and longitudinal (ILG) loop currents
- The AC (VTX) and DC (VSAB) loop voltage

The outputs supplied by the VE790 series ISLAC devices to the Le79R241 ISLIC device are then:

- A voltage (VHL_i*) that provides control for the following high-level Le79R241 ISLIC device outputs:

- DC loop current
- Internal ringing signal
- 12 or 16 kHz metering signal
- A low-level voltage proportional to the voice signal ($VOUT_i$)
- A voltage that controls longitudinal offset for test purposes (VLB_i)

The VE790 series ISLAC devices perform the codec and filter functions associated with the four-wire section of the subscriber line circuitry in a digital switch. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. During conversion, digital filters are used to band-limit the voice signals.

The user-programmable filters set the receive and transmit gain, perform the transhybrid balancing function, permit adjustment of the two-wire termination impedance and provide frequency attenuation adjustment (equalization) of the receive and transmit paths. Adaptive transhybrid balancing is also included. All programmable digital filter coefficients can be calculated using WinSLAC software. The PCM codes can be either 16-bit linear two's-complement or 8-bit companded A-law or μ -law.

Besides the codec functions, the 790 series voice chip set provides all the sensing, feedback, and clocking necessary to completely control Le79R241 ISLIC device functions with programmable parameters. System-level parameters under programmable control include active loop current limits, feed resistance, and feed mode voltages.

The VE790 series ISLAC devices supply complete mode control to the Le79R241 ISLIC device using the control bus (P1-P3) and tri-level load signal (LD).

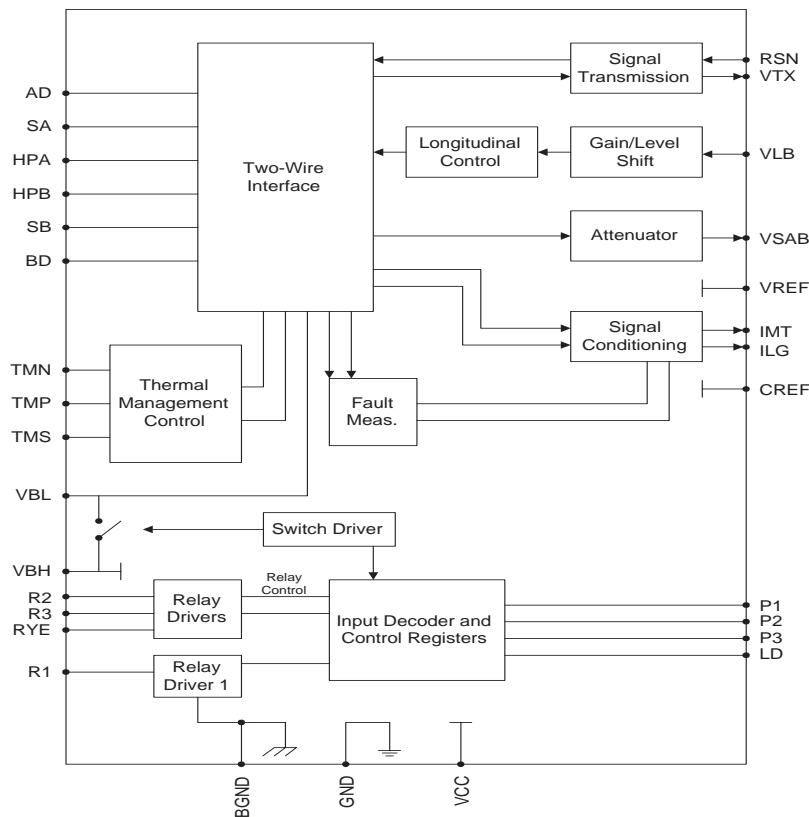
The 790 series voice chip set provides extensive loop supervision capability including off-hook, ring-trip and ground-key detection. Detection thresholds for these functions are programmable. A programmable debounce timer is available that eliminates false detection due to contact bounce.

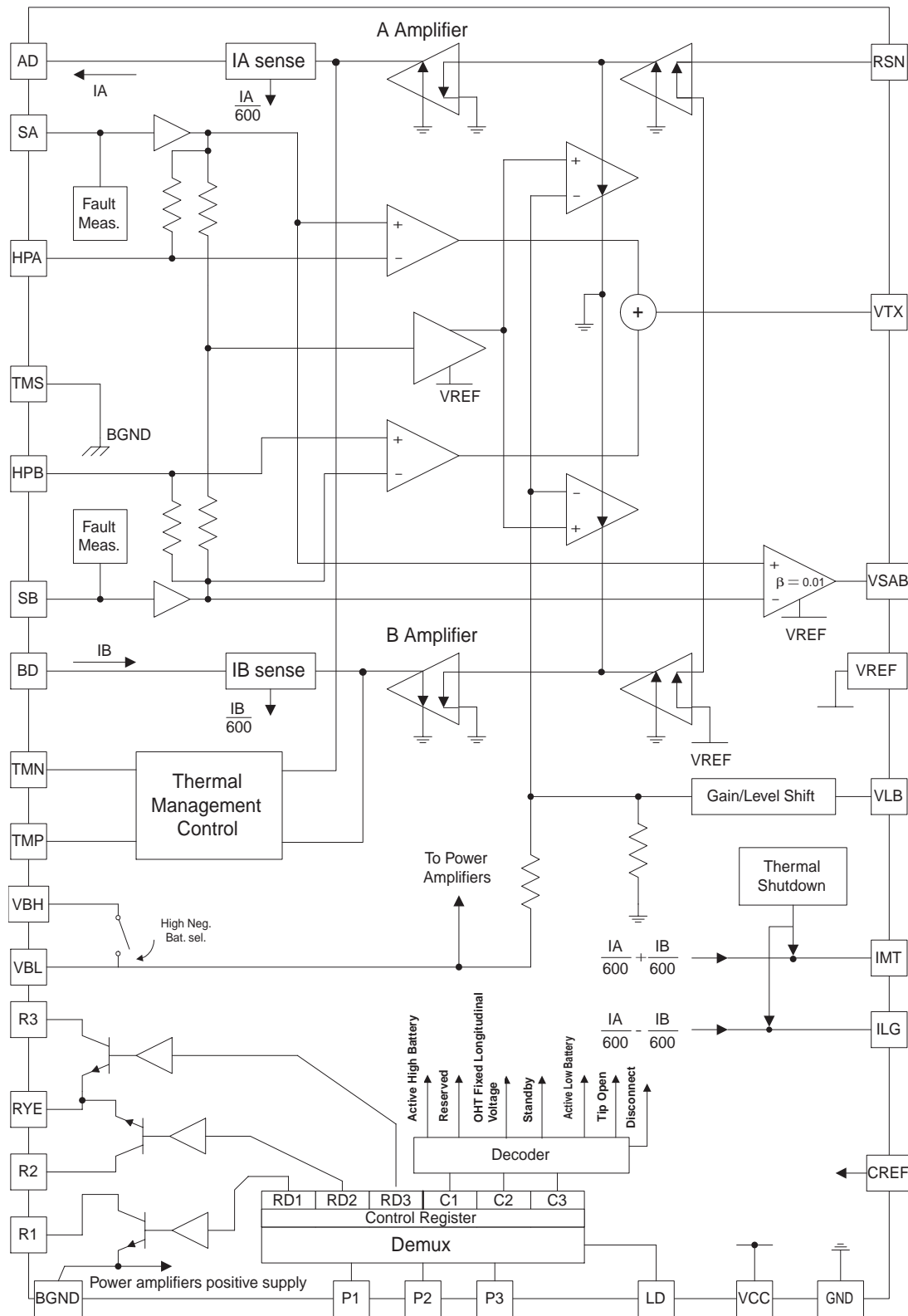
For subscriber line diagnostics, AC and DC line conditions can be monitored using built-in test tools. Measured parameters can be compared to programmed threshold levels to set a pass/fail bit. The user can choose to send the actual measurement data directly to a higher level processor by way of the PCM voice channel. Both longitudinal and metallic resistance and capacitance can be measured, which allows leakage resistance, line capacitance, and telephones to be identified.

***Note:**

i = channel number

Figure 1. Block Diagram

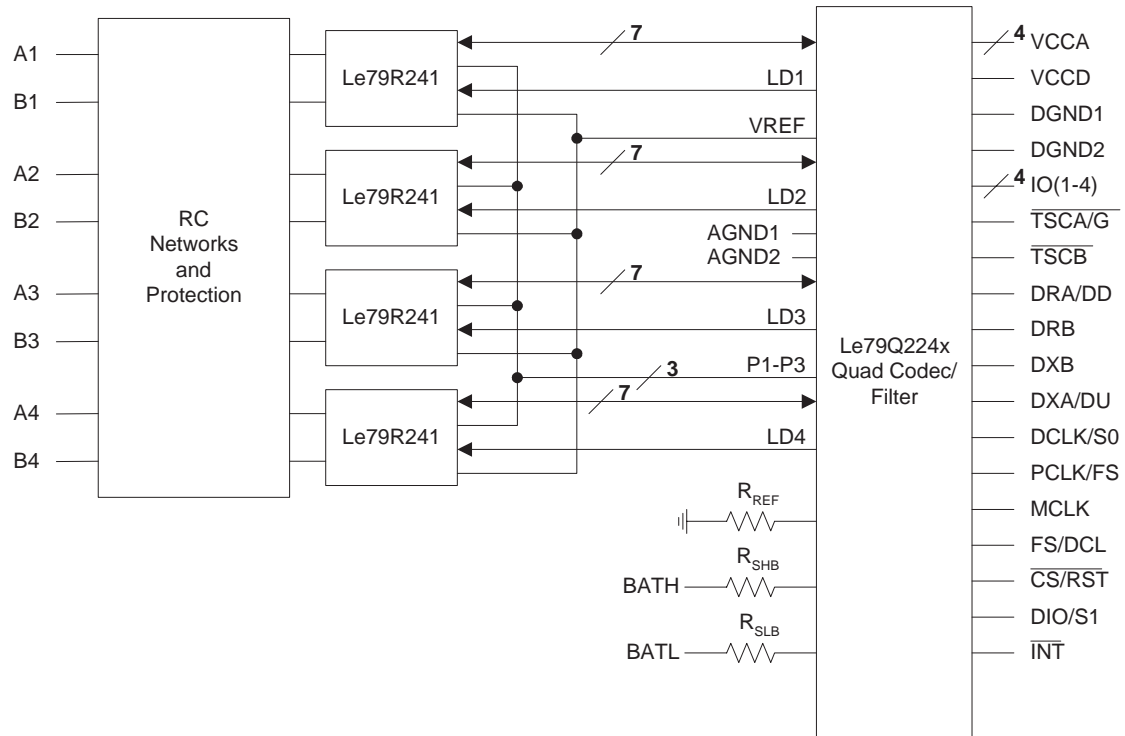


LE79R241 ISLIC™ DEVICE INTERNAL BLOCK DIAGRAM

FEATURES OF THE VE790 SERIES CHIP SET

- Performs all battery feed, ringing, signaling, hybrid and test (BORSCHT) functions
- Two chip solution supports high density, multi-channel architecture
- Single hardware design meets multiple country requirements through software programming of:
 - Ringing waveform and frequency
 - DC loop-feed characteristics and current-limit
 - Loop-supervision detection thresholds
 - Off-hook debounce circuit
 - Ground-key and ring-trip filters
 - Off-hook detect de-bounce interval
 - Two-wire AC impedance
 - Transhybrid balance
 - Transmit and receive gains
 - Equalization
 - Digital I/O pins
 - A-law/ μ -law and linear selection
- Supports internal and external battery-backed ringing
 - Self-contained ringing generation and control
 - Supports external ringing generator and ring relay
 - Ring relay operation synchronized to zero crossings of ringing voltage and current
 - Integrated ring-trip filter and software enabled manual or automatic ring-trip mode
- Supports metering generation with envelope shaping
- Smooth or abrupt polarity reversal
- Adaptive transhybrid balance
 - Continuous or adapt and freeze
- Supports both loop-start and ground-start signaling
- Exceeds LSSGR and CCITT central office requirements
- Selectable PCM or GCI interface
 - Supports most available master clock frequencies from 512 kHz to 8.192 MHz
- On-hook transmission
- Power/service denial mode
- Line-feed characteristics independent of battery voltage
- Only 5 V, 3.3 V and battery supplies needed
- Low idle-power per line
- Linear power-feed with intelligent power-management feature
- Compatible with inexpensive protection networks; Accommodates low-tolerance fuse resistors while maintaining longitudinal balance
- Monitors two-wire interface voltages and currents for subscriber line diagnostics
- Built-in voice-path test modes
- Power-cross, fault, and foreign voltage detection
- Integrated line-test features
 - Leakage
 - Line and ringer capacitance
 - Loop resistance
- Integrated self-test features
 - Echo gain, distortion, and noise
- Guaranteed performance over commercial and industrial temperature ranges.
- Up to three relay drivers per Le79R241 ISLIC device
 - Configurable as test load switches

CHIP SET BLOCK DIAGRAM - FOUR CHANNEL LINE CARD



CONNECTION DIAGRAMS

Figure 2. Le79R241DJC

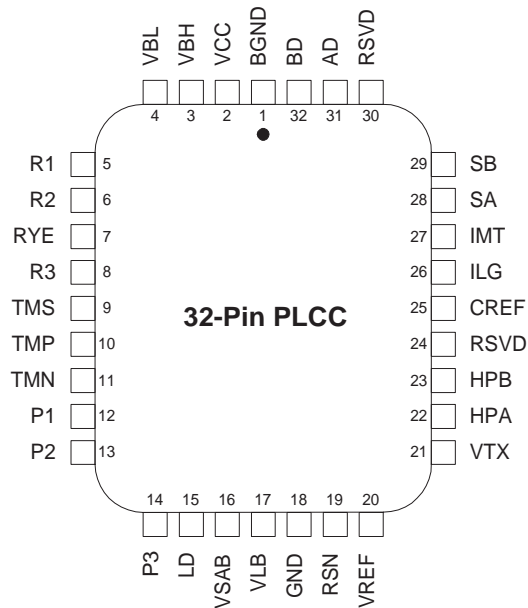
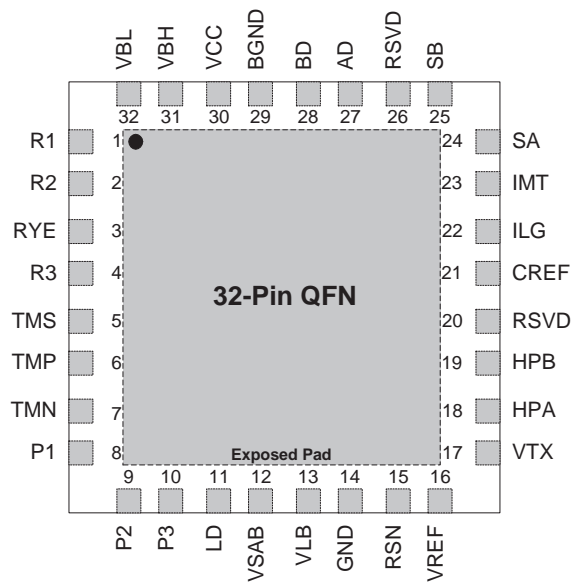


Figure 3. Le79R241FQC



1. Pin 1 is marked for orientation.
2. RSVD = Reserved. Do not connect to this pin.
3. The thermally enhanced QFN package features an exposed pad on the underside which must be electrically tied to VBH.

PIN DESCRIPTIONS

Pin Name	Type	Description
AD, BD	Output	Provide the currents to the A and B leads of the subscriber loop.
BGND	Ground	Ground return for high and low battery supplies.
CREF	+3.3 VDC	VCCD reference. It is the digital high logic supply rail, used by the Le79R241 ISLIC device to codec interface.
GND	Ground	Analog and digital ground return for VCC.
HPA, HPB	Output	These pins connect to CHP, the external high-pass filter capacitor that separates the DC loop-voltage from the voice transmission path.
ILG	Output	ILG is proportional to the common-mode line current (IAD–IBD), except in disconnect mode, where ILG is proportional to the current into grounded SB.
IMT	Output	IMT is proportional to the differential line current (IAD + IBD), except in disconnect mode, where IMT is proportional to the current into grounded SA. The Le79R241 ISLIC device indicates thermal overload by pulling IMT to CREF.
LD	Input	The LD pin controls the input latch and responds to a 3-level input. When the LD pin is a logic 1 ($C_{REF} - 1$), the logic levels on P1–P3 latch into the Le79R241 control register bits that operate the mode-decoder. When the LD pin is a logic 0 (< 0.6), the logic levels on P1–P3 latch into the Am79R241 control register bits that control the relay drivers (RD1–RD3). When the LD pin level is at $\sim V_{REF} \pm 0.3$ V, the control register contents are locked.
P1–P3	Input	Inputs to the latch for the operating-mode decoder and the relay-drivers.
R1	Output	Collector connection for relay 1 driver. Emitter internally connected to BGND.
R2	Output	Collector connection for relay 2 driver. Emitter internally connected to RYE
R3	Output	Collector connection for relay 3 driver. Emitter internally connected to RYE.
RSN	Input	The metallic current between AD and BD is equal to 500 times the current into this pin. Networks that program receive gain and two-wire impedance connect to this node. This input is at a virtual potential of VREF.
RSVD	Reserved	These pins are used during Legerity testing. In the application, they must be left floating.
RYE	Output	Emitter connection for R2 and R3. Normally connected to relay ground.
SA, SB	Input	Sense the voltages on the line side of the fuse resistors at the A and B leads. External sense resistors, RSA and RSB, protect these pins from lightning or power-cross.
TMP, TMN, TMS	Output	External resistors connected from TMP to TMS and TMN to VBL to offload excess power from the Le79R241 ISLIC device.
VBH	Battery (Power)	Connection to high-battery supply used for ringing and long loops. Connects to the substrate. When only a single battery is available, it connects to both VBH and VBL.
VBL	Battery (Power)	Connection to low-battery supply used for short loops. When only a single battery is available, this pin can be connected to VBH.
VCC	+5 V Power Supply	Positive supply for low voltage analog and digital circuits in the Le79R241 ISLIC device.
VLB	Input	Sets the DC longitudinal voltage of the Le79R241 ISLIC device. It is the reference for the longitudinal control loop. When the VLB pin is greater than VREF, the Le79R241 ISLIC device sets the longitudinal voltage to a voltage approximately half-way between the positive and negative power supply battery rails. When the VLB pin is driven to levels between 0V and VREF, the longitudinal voltage decreases linearly with the voltage on the VLB pin.
VREF	Input	The VE790 series SLAC device provides this voltage which is used by the Le79R241 ISLIC device for internal reference purposes. All analog input and output signals interfacing to the VE790 series SLAC device are referenced to this pin.
VSAB	Output	Scaled-down version of the voltage between the sense points SA and SB on this pin.
VTX	Output	The voltage between this pin and VREF is a scaled down version of the AC component of the voltage sensed between the SA and SB pins. One end of the two-wire input impedance programming network connects to VTX. The voltage at VTX swings positive and negative with respect to VREF.
Exposed Pad	Battery	This must be electrically tied to VBH.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability

Storage temperature	–55 to +150°C
Ambient temperature, under bias	–40 to +85°C
Humidity	5% to 95%
VCC with respect to GND	–0.4 to +7 V
VBH, VBL with respect to GND (See note 2)	+0.4 to –104 V
BGND with respect to GND	–3 to +3 V
Voltage on relay outputs	+7 V
AD or BD to BGND: Continuous 10 ms (F = 0.1 Hz) 1 µs (F = 0.1 Hz) 250 ns (F = 0.1 Hz)	VBH – 1 to BGND + 1 VBH – 5 to BGND + 5 VBH – 10 to BGND + 10 VBH – 15 to BGND + 15
Current into SA or SB: 10 µs rise to I _{peak} 1000 µs fall to 0.5 I _{peak} ; 2000 µs fall to I = 0	I _{peak} = ±5 mA
Current into SA or SB: 2 µs rise to I _{peak} 10 µs fall to 0.5 I _{peak} ; 20 µs fall to I = 0	I _{peak} = ±12.5 mA
SA SB continuous	5 mA
Current through AD or BD	± 150 mA
P1, P2, P3, LD to GND	–0.4 to VCC + 0.4 V
Maximum power dissipation (see note 1) T _A = 70° C In 32-pin PLCC package In 32-pin QFN package T _A = 85° C In 32-pin PLCC package In 32-pin QFN package	1.67 W 3.00 W 1.33 W 2.40 W
ESD Immunity (Human Body Model)	JESD22 Class 1C compliant

Note:

1. Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. Operation above 145°C junction temperature may degrade device reliability.

The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad be soldered to an equally sized exposed copper surface, which, in turn, conducts heat through multiple vias to a large internal copper plane.

2. Rise time of VBH (dv/dt) must be limited to less than 27 v/ms.

Thermal Resistance

The junction to air thermal resistance of the Le79R241 ISLIC device in a 32-pin PLCC package is 45° C/W and in a 32-pin QFN package is 25° C/W (measured under free air convection conditions and without external heat sinking).

Package Assembly

The standard (non-green) package devices are assembled with industry-standard mold compounds, and the leads possess a tin/lead (Sn/Pb) plating. These packages are compatible with conventional SnPb eutectic solder board assembly processes. The peak soldering temperature should not exceed 225°C during printed circuit board assembly.

Green package devices are assembled with enhanced, environmental compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes. The peak soldering temperature should not exceed 245°C during printed circuit board assembly.

Refer to IPC/JEDEC J-Std-020B Table 5-2 for the recommended solder reflow temperature profile.

Operating Ranges

Legerity guarantees the performance of this device over commercial (0°C to 70°C) and industrial (-40°C to 85°C) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore GR-357-CORE Component Reliability Assurance Requirements for Telecommunications Equipment.

Environmental Ranges

Ambient Temperature	0 to 70°C Commercial -40 to +85 °C extended temperature
Ambient Relative Humidity	15 to 85%

Electrical Ranges

VCC	5 V \pm 5%
VBL	-15 V to VBH
VBH	-42.5 to -99 V
BGND with respect to GND	-100 to +100 mV
Load resistance on VTX to Vref	20 k Ω minimum
Load resistance on VSAB to Vref	20 k Ω minimum

SPECIFICATIONS

Power Dissipation

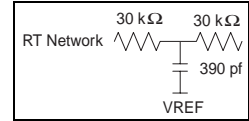
Loop resistance = 0 to ∞ unless otherwise noted (not including fuse resistors), 2 x 50 Ω fuse resistors, BATL = -36 V, BATH = -90 V, VCC = +5 V. For power dissipation measurements, DC-feed conditions are as follows:

- ILA (Active mode current limit) = 25 mA (IRSN = 50 μ A)
- RFD (Feed resistance) = 500 Ω
- VAS (Anti-sat activate voltage) = 10 V
- VAPP (Apparent Battery Voltage) = 48 V
- RMGLi = RMGPi (Thermal management resistors) = 1 k Ω

Description	Test Conditions	Min	Typ	Max	Unit
Power Dissipation Normal Polarity	On-Hook Disconnect		55	70	mW
	On-Hook Standby		80	100	
	On-Hook Transmission Le79R241 ISLIC device Fixed Longitudinal Voltage		175	215	
	On-Hook Active High Battery Le79R241 ISLIC device		340	400	
	Off-Hook Active Low Battery Le79R241 ISLIC device RL = 294 Ω TMG		700 200	800	
Power Supply Currents	On-Hook Disconnect	VBH	0.4	0.7	mA
		VBL	0.1		
		VCC	3.0	3.5	
	On-Hook Standby	VBH	0.75	1.1	
		VBL	0		
		VCC	3.1	3.5	
	On-Hook Transmission Fixed Longitudinal Voltage	VBH	1.85	2.5	
		VBL	0		
		VCC	5	6	
	On-Hook Active High Battery	VBH	3.6	4.5	
		VBL	0		
		VCC	7.3	8.0	
	Off-Hook Active Low Battery RL = 294 Ω	VBH	0.9	2.0	
		VBL	26.9		
		VCC	7.5	10	

DC Specifications

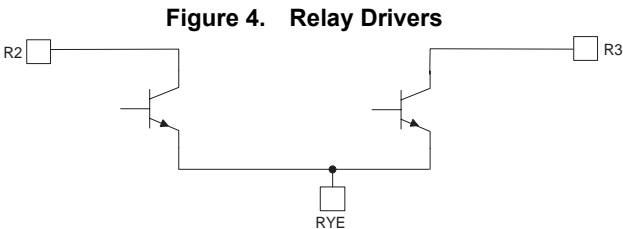
Unless otherwise specified, test conditions are: VCC = 5 V, RMGPI = RMGLI = 1 kΩ, BATH = -90 V, BATL = -36 V, RRX = 150 kΩ, RL = 600 Ω, RSA = RSB = 200 kΩ, RFA = RFB = 50 Ω, CHP = 22 nF, CAD = CBD = 22 nF, IRSN = 50 μA, Active low battery. DC-feed conditions are normally set by the 790 series codec. When the Le79R241 ISLIC device is tested by itself, its operating conditions must be simulated as if it were connected to an ideal 790 series codec.



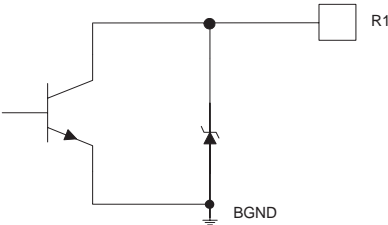
No.	Item	Condition	Min	Typ	Max	Unit	Note
1	Two-wire loop voltage (including offset)	Standby mode, open circuit, VBH < 55 V VBH > 55 V GND – VB Any Active mode (does not include OHT), RL = 600 Ω, I _{RSN} = 50 μA OHT mode, RL = 2200 Ω I _{RSN} = 20 μA	VBH – 8 48 13.88 19.8	VBH–7 51 15 22	VBH–6 55.5 55.5 16.13	V	2.
2	Feed resistance per leg at pins AD & BD	Standby mode	130	250	375	ohms	2.
3	Feed current limit	Feed current Standby mode, RL = 600 Ω	18	34	45	mA	
	IMT current	Standby mode, RL = 2200 Ω	44.6	56			
	ILG current	Standby mode A to VBH B to Ground	28 28			μA	
4	Ternary input voltage boundaries for LD pin. Mid-level input source must be Vref.	Low boundary Mid boundary High boundary Input high current Input low current Mid-level current	VREF–0.3 CREF – 1	V _{REF} 108 47 51	0.6 VREF+0.3	V V V μA μA μA	2. 2. 2.
5	Logic Inputs P1, P2, P3	Input high voltage Input low voltage Input high current Input low current	2.0 -20 -20	 0 0	 0.8 20 20	V V μA μA	
6	VTX output offset		-50	0	+50	mV	
7	VREF input current	VREF = 1.4 V		50		μA	2.
8	CREF input current	CREF = 3.3 V	-3	0	3	μA	2.
9	β, DC Ratio of VSAB to loop voltage: $\beta = \frac{V_{SAB}}{V_{SA} - V_{SB}}$	T _j < 145°C, VSA – VSB = 22 V	0.0088	0.0097	0.0106	V/V	
10	Fault Indicator Threshold	Voltage Output on IMT	2.8	CREF – 0.3 V	CREF	V	2.
11	Gain from VLB pin to A or B pin, KLG			30		V/V	
12	VLB pin input current	VLB = VREF ± 1 V		0	100	μA	2.
13	ILOOP/IMT	ILOOP = 10 mA	283	308	333	A/A	
14	ILONG/ILG	ILONG = 10 mA	575	615	655	A/A	
15	Input current, SA and SB pins	Active modes		1.0	3.0	μA	2.
16	K1	Incremental DC current gain	462.5	500	537.5		2.
17	ISA/IMT	Disconnect ISA = 2 mA	4	6	8.75	A/A	
18	ISB/ILG	Disconnect ISB = 2 mA	10	12	16		
19	VSAB output offset	-40°C +25°C +85°C		7.0 3.6 1.4		mV	
20	IMT output offset		-3	0	3	μA	
21	ILG output offset		-1	0	1	μA	

Relay Driver Specifications

Item	Condition	Min	Typ	Max	Unit	Note
On Voltage	25 mA/relay sink		0.4	0.5	V	2
	40 mA/relay sink		0.8	1.0		
R2,R3 Off Leakage	R2,R3 = BGND RYE = VBH		0	100	μA	
Zener Break Over	Iz = 100 μA	6.6	7.9	10	V	
Zener On Voltage	Iz = 30 mA	6	11	17		



A. Relay Driver Configuration



B. Ring Relay

Transmission Specifications

No.	Item	Condition	Min	Typ	Max	Unit	Note
1	RSN input impedance	$f = 300$ to 3400 Hz		1		Ω	2.
2	VTX output impedance			3			
3	Max, AC + DC loop current	Active High Battery or Active Low Battery	70			mA	2.
4	Longitudinal impedance, A or B to GND	Active mode		70	135	Ω	
5	2-4 wire gain	-10 dBm, 1 kHz, 0 to 70°C $T_A = -40^{\circ}\text{C}$ to 85°C	-14.13 -14.18	-13.98 -13.98	-13.83 -13.78	dB	2.
6	2-4 wire gain variation with frequency	300 to 3400 Hz, relative to 1 kHz $T_A = -40^{\circ}\text{C}$ to 85°C	-0.1 -0.15		$+0.1$ $+0.15$		2.
7	2-4 wire gain tracking	$+3$ dBm to -55 dBm Reference: -10 dBm $T_A = -40$ to 85°C	-0.1 -0.15		$+0.1$ $+0.15$		2. , 5.
8	4-2 wire gain	-10 dBm, 1 kHz $T_A = -40^{\circ}\text{C}$ to 85°C	-0.15 -0.2		$+0.15$ $+0.2$		2.
9	4-2 wire gain variation with frequency	300 to 3400 Hz, relative to 1 kHz	-0.1		$+0.1$		
10	4-2 wire gain tracking	$+3$ dBm to -55 dBm Reference: -10 dBm -40°C to 85°C	-0.1 -0.15		$+0.1$ $+0.15$		2. , 5.
11	Total harmonic distortion level	300 Hz to 3400 Hz				dB	
	2-wire	0 dBm			-50		
	4-wire	11.2 dBm			-40		
	4-wire overload level at VTX OHT	-12 dBm -0.8 dBm RLOAD = $600\ \Omega$ VAB - $50\ \text{V}$ 0 dBm		± 1 -50	-48 -38		2. 2.
12	Idle channel noise	Active modes, $R_L = 600\ \Omega$				dBmC	
	C-message	2-wire		$+9$	$+11$		
	Weighted	4-wire		-5			
	Psophometric	2-wire		-81	-79		
13	Longitudinal balance (IEEE method)	$L - T$ 200 to 1000 Hz $T_A = -40^{\circ}\text{C}$ to 85°C	58 53			dB	2.
	Normal Polarity	1000 to 3400 Hz $T_A = -40^{\circ}\text{C}$ to 85°C	53 48				2.
		$T - L$ 200 to 3400 Hz	40				
		$L - T$, IL = 0 50 to 3400 Hz		63			3.
	Reverse Polarity	$L - T$ 200 to 1000 Hz $T_A = -40^{\circ}\text{C}$ to 85°C	50 48				2.
14	PSRR (VBH, VBL)	50 to 3400 Hz 3.4 to 50 kHz	25	45 40			3. , 4. 1. , 2. , 4.
15	PSRR (VCC)	50 to 3400 Hz 3.4 to 50 kHz	25	45 35			3. , 4. 1. , 2. , 4.
16	Longitudinal AC current per wire	$F = 15$ to 60 Hz Active mode	20	30		mArms	2.
17	Metering distortion	Freq = 12 kHz $2.8\ \text{Vrms}$ Freq = 16 kHz metering load = $200\ \Omega$	40			dB	2.

Ringing Specifications

Item	Condition	Min	Typ	Max	Unit	Note
Peak Ringing Voltage	Active Internal Ringing		VBH+6		V	7.

Current-Limit Behavior

SLIC Mode	Condition	Min	Typ	Max	Unit	Note
Disconnect	Applied fault between ground and T/R VBH applied to Tip or Ring		1 VBH/200K	100	μA A	6.
Tip Open	Ring Short to GND	20	35	46	mA	
Standby	Short Tip-to-VBH Short Ring-to-GND	24 26	38 35	47 44		
Active Ringing	790 series codec generating internal ringing		100			2.

Thermal Shutdown Fault Indications

Fault	Indication
No Fault	IMT operates normally ($V_{\text{REF}} \pm 1 \text{ V}$)
Thermal Shutdown	KG, IMT above 2.8 V; ILG operates normally

Note:

- These tests are performed with the following load impedances:
Frequency < 12 kHz – Longitudinal impedance = 500 Ω ; metallic impedance = 300 Ω
Frequency > 12 kHz – Longitudinal impedance = 90 Ω ; metallic impedance = 135 Ω
- Not tested or partially tested in production. This parameter is guaranteed by characterization or correlation to other tests.
- This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.
- When the Le79R241 ISLIC device and 790 series codec is in the anti-sat operating region, this parameter is degraded. The exact degradation depends on system design.
- 55 dBm gain tracking level not tested in production. This parameter is guaranteed by characterization and correlation to other tests.
- This spec is valid from 0 V to VBL or –50 V, whichever is lower in magnitude.
- Other ringing-voltage characteristics are set by the 790 series codec.

OPERATING MODES

The Le79R241 ISLIC device receives multiplexed control data on the P1, P2 and P3 pins. The LD pin then controls the loading of P1, P2, and P3 values into the proper bits in the Le79R241 ISLIC device control register. When the LD pin is less than 0.3 V below VREF (< ($V_{\text{REF}} - 0.3 \text{ V}$)), P1–P3 must contain data for relay control bits RD1, RD2 and RD3. These are latched into the first three bits in the Le79R241 ISLIC device control register. When the LD pin is more than 0.3 V above VREF, P1–P3 must contain Le79R241 ISLIC device control data C1, C2, and C3, which are latched into the last three bits of the Le79R241 ISLIC device control register. Connecting the LD pin to VREF locks the contents of the Le79R241 ISLIC device control register.

The operating mode of the Le79R241 ISLIC device is determined by the C1, C2, and C3 bits in the control register of the Le79R241 ISLIC device. Table 1 defines the Le79R241 ISLIC device operating modes set by these signals.

Under normal operating conditions, the Le79R241 ISLIC device does not have active relays. The Le79R241 ISLIC device to VE790 series ISLAC device interface is designed to allow continuous real-time control of the relay drivers to avoid incorrect data loads to the relay bit latches of the Le79R241 devices.

To perform external ringing, the VE790 series ISLAC device is set to external ringing mode (RMODE = 1), enables the ring relay, and puts the Le79R241 ISLIC device in the Standby mode.

Table 1. Operating Modes

C3	C2	C1	Operating Mode	Battery Voltage Selection	Operating Mode	Connection to RMGPI & RMGLI Resistors
0	0	0	Standby (See note 1)	High Battery (BATH) and BGND	(High ohmic feed): Loop supervision active, A and B amplifiers shut down	Open
0	0	1	Tip Open (See note 1)	High Battery (BATH) and BGND	Tip Open: AD at High-Impedance, Channel A power amplifier shut down	Open
0	1	0	On-Hook Transmission, Fixed Longitudinal Voltage	High Battery (BATH) and BGND	Fixed longitudinal voltage of –28 V	A and B Amplifier Output
0	1	1	Disconnect	Low Battery selection at VBL	AD and BD at High-Impedance, Channel A and B power amplifiers shut down	
1	0	0	RSVD		Active feed, normal or reverse polarity	
1	0	1	Active High Battery	High Battery (BATH) and BGND		
1	1	0	Active Low Battery	Low Battery (BATL) and BGND		
1	1	1	Active Internal Ringing	High Battery (BATH) and BGND	Active internal ringing	

Note:

1. In these modes, the ring lead (B-lead) output has a –50 V internal clamp to battery ground (BGND).

Operating Mode Descriptions

Operating Mode	Description
Disconnect	This mode disconnects both A and B output amplifiers from the AD and BD outputs. The A and B amplifiers are shut down and the Le79R241 ISLIC device selects the low battery voltage at the VBL pin. In the Disconnect state, the currents on IMT and ILG represent the voltages on the SA and SB pins, respectively. These currents are scaled to produce voltages across RMTi and RLGi of $\frac{V_{SA}}{400}$ and $\frac{V_{SB}}{400}$, respectively.
Standby	The power amplifiers are turned off. The AD output is driven by an internal 250 Ω (typical) resistor, which connects to ground. The BD output is driven by an internal 250 Ω (typical) resistor, which connects to the high battery (BATH) at the VBH pin, through a clamp circuit, which clamps to approximately –50 V with respect to BGND. For VBH values above –55 V, the open-circuit voltage, which appears at this output is $\sim VBH + 7$ V. If VBH is below –55 V, the voltage at this output is –50 V. The battery selection for the balance of the circuitry on the chip is VBL. Line supervision remains active. Current limiting is provided on each line to limit power dissipation under short-loop conditions as specified in Current-Limit Behavior, on page 15 . In external ringing, the Standby Le79R241 ISLIC device state is selected.
Tip Open	In this mode, the AD (Tip) lead is opened and the BD (Ring) lead is connected to a clamp, which operates from the high battery on VBH pin and clamps to approximately –50 V with respect to BGND through a resistor of approximately 250 Ω (typical). The battery selection for the balance of the circuitry on the chip is VBL.
Active High Battery	In the Active High Battery mode, battery connections are connected as shown in Table 1. Both output amplifiers deliver the full power level determined by the programmed DC-feed conditions. Active High Battery mode is enabled during a call in applications when a long loop can be encountered.
Active Low Battery	Both output amplifiers deliver the full power level determined by the programmed DC-feed conditions. VBL, the low negative battery, is selected in the Active Low Battery mode. This is typically used during the voice part of a call.
Active Internal Ringing	In the Internal Ringing mode, the Le79R241 ISLIC device selects the battery connections as shown in Table 1. When using internal ringing, both the AD and BD output amplifiers deliver the ringing signal determined by the programmed ringing level.
On-Hook Transmission (OHT), Fixed Longitudinal Voltage	In the On-Hook Transmission, Fixed Longitudinal Voltage mode, battery connections are as shown in Table 1 . The longitudinal voltage is fixed at the voltage shown in Table 1 to allow compliance with safety specifications for some classes of products.

Driver Descriptions

Driver	Description
R1	A logic 1 on RD1 turns the R1 driver on and operates a relay connected between the R1 pin and VCCD. R1 drives the ring relay when external ringing is selected.
R2	A logic 1 on the RD2 signal turns the R2 driver on and routes current from the R2 pin to the RYE pin. In the option where the RYE pin is connected to ground, the R2 pin can sink current from a relay connected to VCCD. Another option is to connect the RYE pin to the BD (Ring) lead and connect a test load between R2 and the AD (Tip) lead. This technique avoids the use of a relay to connect a test load. However, it does not isolate the subscriber line from the line card. The test load must be connected to the Le79R241 ISLIC device side of the protection resistor to avoid damage to the R2 driver.
R3	A logic 1 on the RD3 signal turns the R3 driver on and routes current from the R3 pin to the RYE pin. In the option where the RYE pin is connected to ground, the R3 pin can sink current from a relay connected to VCCD. Another option is to connect the RYE pin to the B (Ring) lead and connect a test load between R3 and the A (Tip) lead. This technique avoids the use of a relay to connect a test load. However, it does not isolate the subscriber line from the line card. The test load must be connected to the Le79R241 ISLIC device side of the protection resistor to avoid damage to the R3 driver.

Control bits RD1, RD2, and RD3 do not affect the operating mode of the Le79R241 ISLIC device. These signals usually perform the following functions.

Thermal-Management Equations

Applies to all modes except Standby and Ringing, which have no thermal management.

Equation	Description
$I_L < 5 \text{ mA}$ $P_{SLIC} = (S_{BAT} - I_L(R_L + 2R_{FUSE})) \cdot I_L + 0.3 \text{ W}$ $P_{RTMG} = 0$	TMG resistor-current is limited to be $5 \text{ mA} < I_L$. If $I_L < 5 \text{ mA}$, no current flows in the TMG resistor and it all flows in the Am79241.
$I_L > 5 \text{ mA}$ $RMGP_i = RMGL_i = R_{TMG}$ P_{RTMG} : total power dissipation of $RMGP_i$ and $RMGL_i$ $R_{TMG} = (S_{BAT} - I_L(R_L + 2R_{FUSE})) / (2(I_L - 5 \text{ mA}))$ $P_{SLIC} = I_L(S_{BAT} - I_L(R_L + 2R_{FUSE})) + 0.3 \text{ W} - P_{RTMG}$ $P_{RTMG} = (I_L - 5 \text{ mA})^2(2R_{TMG})$	These equations are valid when $R_{TMG} \cdot (I_L - 5 \text{ mA}) < (S_{BAT} - (R_F + R_L)I_L) / 2 - 2$ because the longitudinal voltage is one-half the battery voltage and the TMG switches require approximately 2 V. To choose a power rating for $RTMG$: $P_{RATING} > P_{RTMG} / 2$

TIMING SPECIFICATIONS

Symbol	Signal	Parameter	Min	Typ	Max	Unit
trSLD	LD	Rise time Le79R241 ISLIC device LD pin			2	US
tfSLD	LD	Fall time Le79R241 ISLIC device LD pin			2	
tSLDPW	LD	LD minimum pulse width	3			
tSDXSU	P1,P2,P3	P1–3 data Setup time	4.5			
tSDXHD	P1,P2,P3	P1–3 data hold time	4.5			
tSDXD	P1,P2,P3	Max P1–3 data delay			5	

Notes:

- The P1–3 pins are updated continuously during operation by the LD signal.
- After a power-on reset or hardware reset, the relay outputs from the Le79R241 ISLIC device turn all relays off. An unassuming state is to place the relay control pins, which are level triggered, to a reset state for all relays. Any noise encountered only raises the levels toward the register lock state.
- When writing to the Le79R241 ISLIC device registers, the sequence is:
 - Set LD pin to mid-state.
 - Place appropriate data on the P1–3 pins.
 - Assert the LD pin to High or Low to write the proper data.
 - Return LD pin to mid-state.
- Le79R241 ISLIC device registers are refreshed at 5.33 kHz when used with an 790 series codec.
- If the clock or MPI becomes disabled, the LD pins and P1–3 returns to 0 V state, protecting the Le79R241 ISLIC device and the line connection.

6. Not tested in production. Guaranteed by characterization.

WAVEFORMS

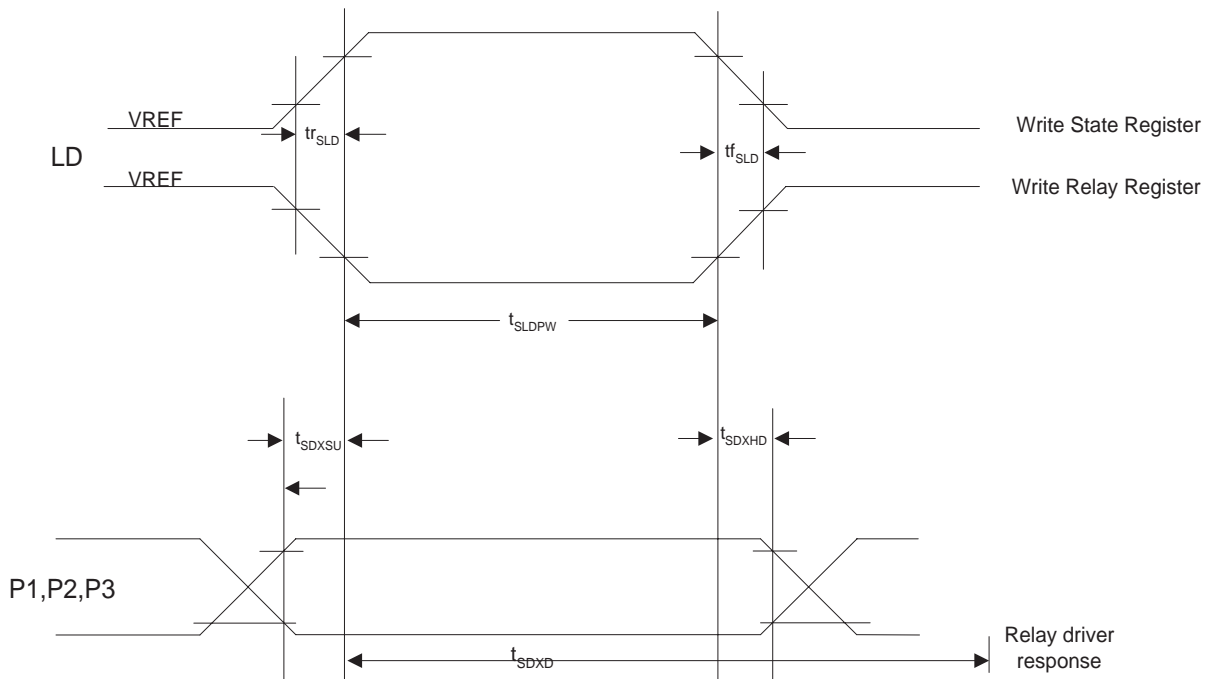
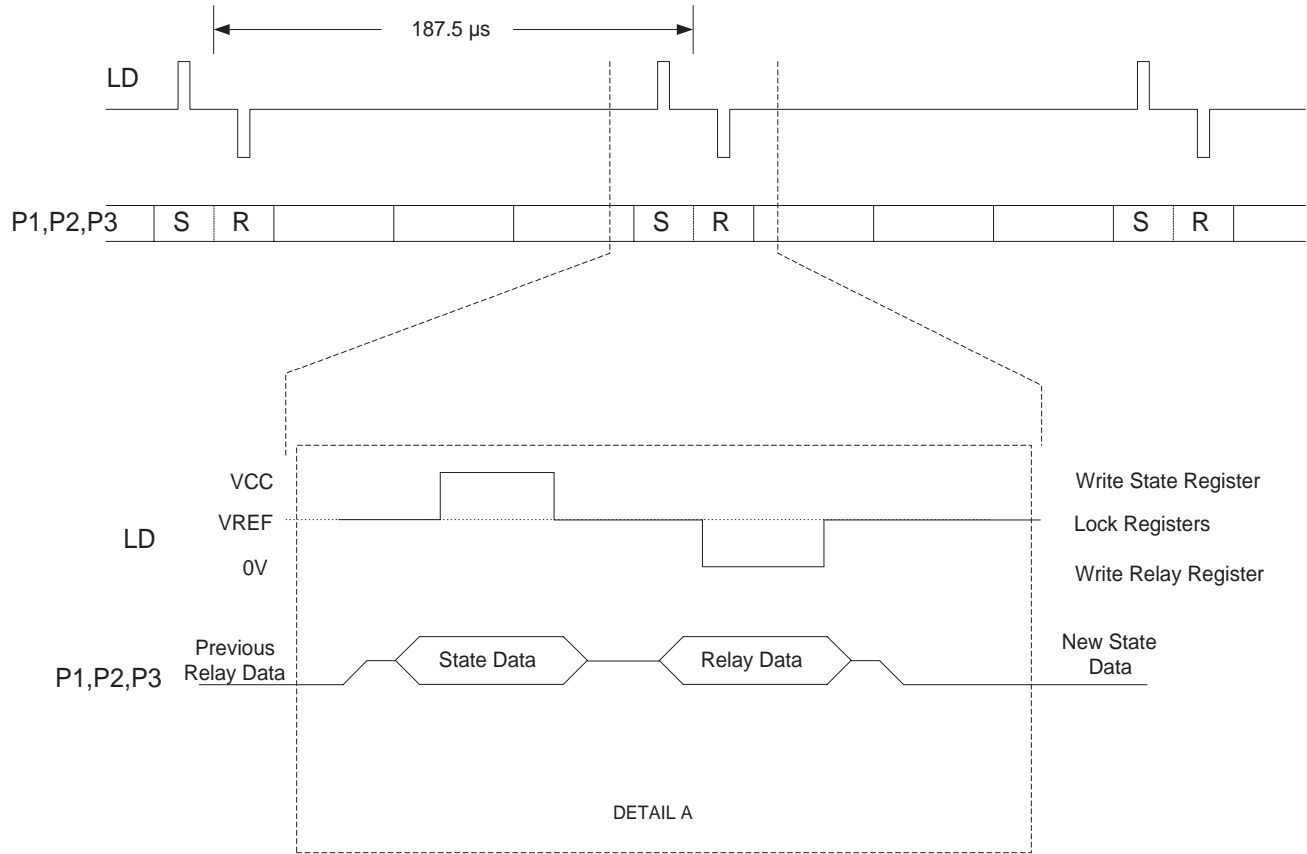


Figure 5. Internal Ringing Line Schematic



LINE CARD PARTS LIST- INTERNAL RINGING

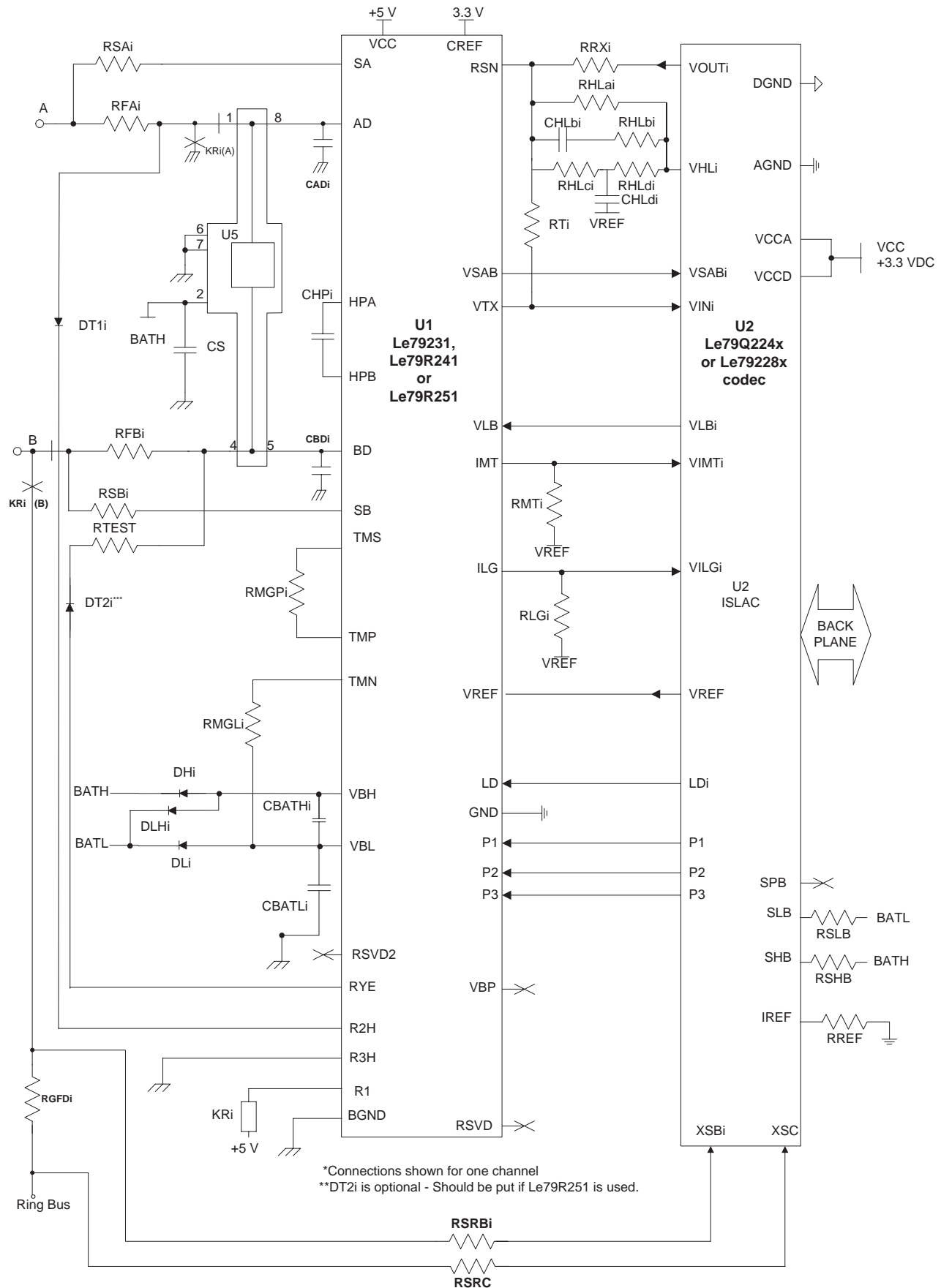
The following list defines the parts and part values required to meet target specification limits for channel i of the line card (i = 1,2,3,4).

Item	Type	Value	Tol.	Rating	Comments
U1	Le79R241 ISLIC device		-		
U2	VE790 series ISLAC device		-		codec
U3, U4, U5, U6	B1100CC		-	100 V	TECCOR Battrax protector
DT1 _i , DT2 _i	Diode	1 A	-	100 V	
DH _i ¹ , DL _i , DT1 _i , DT2 _i , DLH _i	Diode	100 mA	-	100 V	50 ns response time
RFA _i , RFB _i	Resistor	50 Ω	2%	2 W	Fusible or PTC protection resistors
RSA _i , RSB _i	Resistor	200 k Ω	2%	1/4 W	Sense resistors
RT _i	Resistor	80.6 k Ω	1%	1/8 W	Impedance control resistor
RRX _i	Resistor	90.9 k Ω	1%	1/8 W	Receive path gain resistor
RREF	Resistor	69.8 k Ω	1%	1/8 W	Current reference setting resistor
RSHB, RSLB, RSPB	Resistor	750 k Ω	1%	1/8 W	Battery sense resistors
RHLA _i	Resistor	40.2 k Ω	1%	1/10 W	Feed/metering resistor
RHLB _i	Resistor	4.32 k Ω	1%	1/10 W	Feed/metering resistor
RHLC _i	Resistor	2.87 k Ω	1%	1/10 W	Feed/metering resistor
RHLD _i	Resistor	2.87 k Ω	1%	1/10 W	Feed/metering resistor
CHLB _i	Capacitor	3.3 nF	10%	10 V	Feed/metering capacitor - Not Polarized
CHLD _i	Capacitor	0.82 μ F	10%	10 V	Feed/metering capacitor -Ceramic
RMT _i	Resistor	3.01 k Ω	1%	1/8 W	Metallic loop current gain resistor
RLG _i	Resistor	6.04 k Ω	1%	1/8 W	Longitudinal loop current gain resistor
RTEST	Resistor	2 k Ω	1%	1 W	Test board
CAD _i , CBD _i ²	Capacitor	22 nF	10%	100 V	Ceramic
CBATH _i , CBATL _i , CBATP _i	Capacitor	100 nF	20%	100 V	Ceramic
CHP _i	Capacitor	22 nF	20%	100 V	High pass filter capacitor - Ceramic
CS1 _i , CS2 _i ²	Capacitor	100 nF	20%	100 V	Protector speed up capacitor
RMGL _i	Resistor	1 k Ω	5%	2 W	Thermal management resistor
RMGP _i	Resistor	1 k Ω	5%	2 W	Thermal management resistor

Notes:

1. Required to insure $VBH < VBL$ during startup. May not be needed for some supplies.
2. DT2_i is optional - Should be put if Le79R251 is used.
3. Value can be adjusted to suit application.

Figure 6. External Ringing Line Schematic



LINE CARD PARTS LIST - EXTERNAL RINGING

The following list defines the parts and part values required to meet target specification limits for channel i of the line card (i = 1, 2, 3, 4).

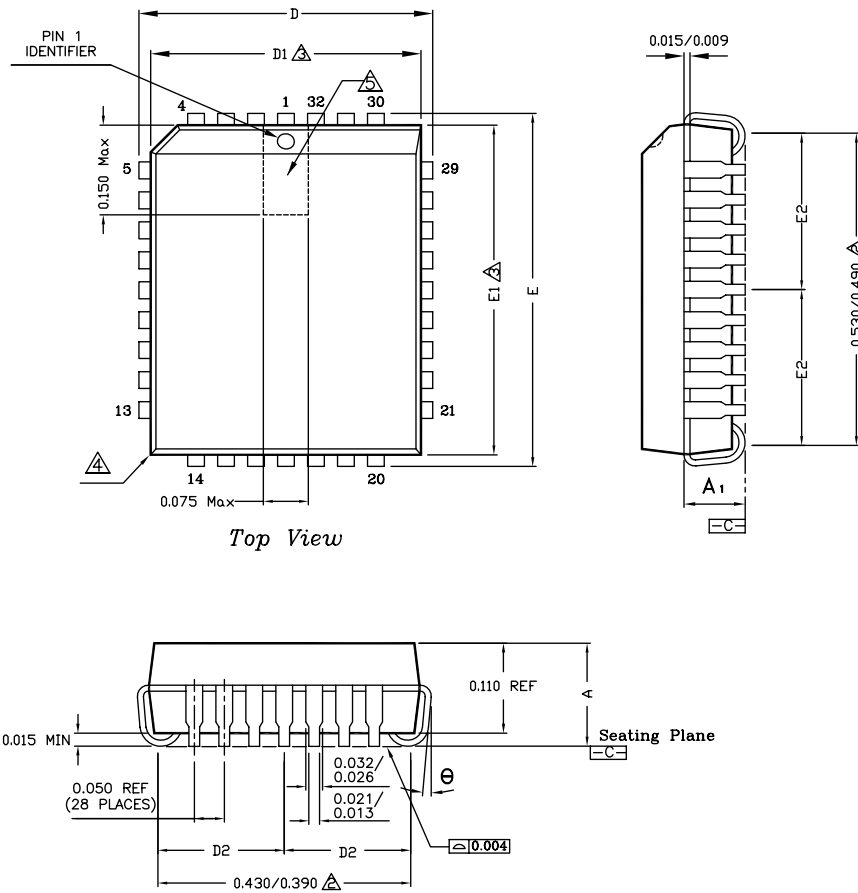
Item	Type	Value	Tol.	Rating	Comments
U1	Le79R241 ISLIC device				
U2	VE790 series ISLAC device				codec
U5	TISP61089			80 V	Transient Voltage Suppressor, Power Innovations
DLH_i^1 , DH_i , DL_i , $DT1_i$ $DT2_i^2$	Diode	100 mA		100 V	50 ns response time
RFA_i , RFB_i	Resistor	50 Ω	2%	2 W	Fusible or PTC protection resistors
RSA_i , RSB_i	Resistor	200 k Ω	2%	1/4 W	Sense resistors
RT_i	Resistor	80.6 k Ω	1%	1/8 W	Impedance control resistor
RRX_i	Resistor	90.9 k Ω	1%	1/8 W	Receive path gain resistor
RREF	Resistor	69.8 k Ω	1%	1/8 W	Current reference setting resistor
$RMGL_i$, $RMGP_i$	Resistor	1 k Ω	5%	1 W	Thermal management resistors
RSHB, RSLB	Resistor	750 k Ω	1%	1/8 W	Battery Sense Resistors
$RHLa_i$	Resistor	40.2 k Ω	1%	1/10 W	Feed/Metering resistor
$RHLb_i$	Resistor	4.32 k Ω	1%	1/10 W	Feed/Metering resistor
$RHLc_i$	Resistor	2.49 k Ω	1%	1/10 W	Use 2.87k Ω in metering Feed/Metering resistor
$RHLd_i$	Resistor	2.49 k Ω	1%	1/10 W	Use 2.87k Ω in metering Feed/Metering resistor
$CHLb_i$	Capacitor	3.3 nF	10%	10 V	Feed/Metering capacitor - Not Polarized
$CHLd_i$	Capacitor	0.82 μ F	10%	10 V	Feed/Metering capacitor - Ceramic
RMT_i	Resistor	3.01 k Ω	1%	1/8 W	Metallic Current Sense Resistors
RLG_i	Resistor	6.04 k Ω	1%	1/8 W	Longitudinal Current Sense Resistors
RTEST	Resistor	2 k Ω	1%	1 W	Test board
CAD_i , CBD_i^3	Capacitor	22 nF	10%	100 V	Ceramic
$CBATH_i$, $CBATL_i$	Capacitor	100 nF	20%	100 V	Ceramic
CHP_i	Capacitor	22 nF	20%	100 V	Ceramic
CS_i^3	Capacitor	100 nF	20%	100 V	Protector speed up capacitor
$RGFD_i$	Resistor	510 Ω	2%	2 W	1.2 W typ
$RSRB_i$, RSRC	Resistor	750 k Ω	1%	1/4 W	External Ringing sense resistors
KR_i	Relay	5 V Coil			DPDT

Notes:

1. Required to insure $VBH < VBL$ during startup. May not be needed for some supplies.
2. $DT2i$ is optional - Should be put if Le79R251 is used.
3. Value can be adjusted to suit application.

PHYSICAL DIMENSIONS

32-Pin PLCC



NOTES:

32-Pin PLCC			
JEDEC # MS-016			
Symbol	Min	Nom	Max
A	0.125	--	0.140
A1	0.075	0.090	0.095
D	0.485	0.490	0.495
D1	0.447	0.450	0.453
D2	0.205 REF		
E	0.585	0.590	0.595
E1	0.547	0.550	0.553
E2	0.255 REF		
Θ	0 deg	--	10 deg

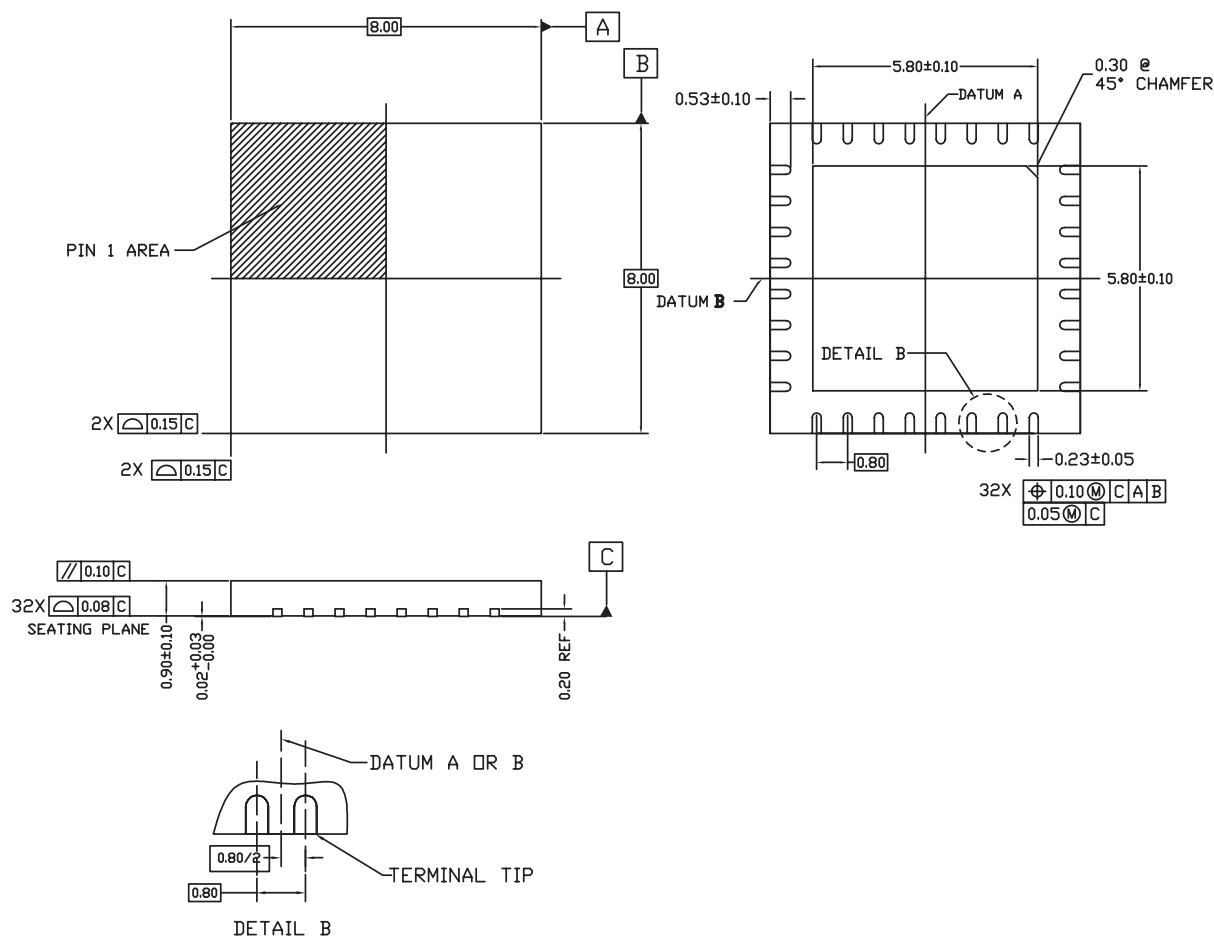
- 1 Dimensioning and tolerancing conform to ASME Y14.5M-1994.
- 2 To be measured at seating plan \perp C - contact point.
- 3 Dimensions "D1" and "E1" do not include mold protrusion. Allowable mold protrusion is 0.010 inch per side. Dimensions "D" and "E" include mold mismatch and determined at the parting line; that is "D1" and "E1" are measured at the extreme material condition at the upper or lower parting line.
- 4 Exact shape of this feature is optional.
- 5 Details of pin 1 identifier are optional but must be located within the zone indicated.
- 6 Sum of DAM bar protrusions to be 0.007 max per lead.
- 7 Controlling dimension : Inch.
- 8 Reference document : JEDEC MS-016

32-Pin PLCC

Note:

Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.

32-Pin QFN



Symbol	32 LEAD QFN		
	Min	Nom	Max
A	0.80	0.90	1.00
A2	0.57 REF		
b	0.18	0.23	0.28
D	8.00 BSC		
D2	5.70	5.80	5.90
E	8.00 BSC		
E2	5.70	5.80	5.90
e	0.80 BSC		
L	0.43	0.53	0.63
N	32		
A1	0.00	0.02	0.05
A3	0.20 REF		
aaa	0.20		
bbb	0.10		
ccc	0.10		

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Φ is in degrees.
3. N is the total number of terminals.
4. The Terminal #1 identifier and terminal numbering convention shall conform to JEP 95-1 and SSP-012. Details of the Terminal #1 identifier are optional, but must be located within the zone indicated. The Terminal #1 identifier may be either a mold or marked feature.
5. Coplanarity applies to the exposed pad as well as the terminals.
6. Reference Document: JEDEC MO-220.
7. Lead width deviates from the JEDEC MO-220 standard.

32-Pin QFN

Note:

Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.

REVISION HISTORY

Revision H to Revision I

- Page 11, Figure 3, DT1i was added and the last note was modified.
- Page 12, Figure 4, DT1i was added and the last note was modified.
- Page 15, Electrical Characteristics, Numbers changed in the Max column.
- Page 16, Absolute Maximum Ratings, The "Humidity" row was deleted.
- Page 17, Specifications, There were changes to rows one, four, six, 12, and 17–21, and to the Note column.
- Page 18, Relay Driver Specifications, There were changes in the last two rows.
- Page 19, Transmission Specifications, There were changes to rows, six, eight, 10, and 13, and to the Note column.
- Page 20, Fault Indications, "ILG operates normally" was deleted from the Indication column on the second row.

Revision I to Revision J

- Applied new format.
- Global change: RTMG1 to RMGLi, and RTMG2 to RMGPi.
- Updated "Target Specifications" for rows 10, and 19.
- Updated "Transmission Specifications" for row 12.
- "Thermal Management Equations" modified.
- Added "Applications" section.

Revision J to K

- Added 5 REN bullet to Features.
- Updated Device Internal Block Diagram.
- Modified description of LD pin.
- In "Thermal Resistance" section, updated temperature to 43° C.
- New Temperature statement added to "Chipset Features".
- New Temperature statement added to "Environmental Ranges".
- Removed reference to $V_{LOOPMAX}$ in the "Electrical Ranges" section.
- "Waveforms," new image.
- In "DC Specificaitons" section, the following changes were made:
 - Added test conditions for two-wire loop voltage.
 - Added a typical value for Ternary input voltage, Mid boundary.
 - Removed references to T_A under test conditions for idle channel noise.
- "DC Specifications," "Transmission Specifications," and "Line Card Parts List," corrected W's to omega's.
- Added typical value for Ringing Specifications.
- Renamed "Fault Indications" table to "Thermal Shutdown Fault Indications"; modified text.
- Modified text in "Operating Modes" section.
- "Thermal-Management Equations," corrected " P_{TMG} " to " PT_{RTMG} " and corrected " $(R_L I_L)$ " to " $(R_F + R_L) I_L$."
- "Application Circuits," added line to arrow head at DT1i, and deleted "H" from R2 and R3.
- Modified note for External Ringing Line card schematic.

Revision K to L

- Added QFN package data to "Connection Diagram," "Absolute Maximum Ratings," and "Physical Dimensions."
- Updated "Am" OPNs (Ordering Part Numbers) to "Le" throughout document
- In "Ordering Information" the following changes were made:
 - Added entries for Le79R241JC and Le79R241QC
 - Removed the chip graphic
 - Added notes
- In "Features," added bullet for space savings feature
- Removed references to DISLAC documents in "Related Literature"
- In "Pin Descriptions," added row describing exposed pad
- Standardized notes in "Absolute Maximum Ratings" section

- In "Thermal Management Equations", $I_L > 5$ mA, deleted the last sentence in the Description section
- Updated 32-Pin PLCC physical dimensions graphic

Revision L to M1

- Modified internal and external ringing schematics and BOMs (removed CSS capacitor)
- Updated QFN *Physical Dimensions* drawing

Revision M1 to N1

- Added 5.1-k VHL network in to both application circuits in [Application Circuits, on page 19](#)

Revision N1 to O1

- Added Packing column and related note to [Ordering Information, on page 1](#).
- Added green package OPNs to [Ordering Information, on page 1](#).
- Added [Package Assembly, on page 10](#)
- Revised DC Specifications, page 12, No. 12, 13 for I_{LOOP}/I_{MT} and I_{LONG}/I_{LG} for min. typ and max.
- Added note to [Physical Dimensions, on page 23](#)

Revision O1 to O2

- Enhanced format of package drawings in [Physical Dimensions, on page 23](#)
- Added new headers/footers due to Zarlink purchase of Legerity on August 3, 2007



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