ZARLINK SEMICONDUCTOR

VoiceEdge

Le75183

Line Card Access Switch
VE750 Series

A Legerity Voice Solution

APPLICATIONS

- **Central office**
- **DLC**
- **PBX**
- **DAML**
- **HFC/FITL**

FEATURES

- **Small size/surface-mount packaging**
- **Monolithic IC reliability**
- **Low impulse noise**
- **Make-before-break, break-before-make operation**
- **Clean, bounce-free switching**
- **Low, matched ON-resistance**
- **Built-in current limiting, thermal shutdown, and SLIC protection**
- **5-V only operation, very low power consumption**
- **Battery monitor, all OFF state upon loss of battery**
- **No EMI**
- **Latched logic level inputs, no drive circuitry**
- **Only one external protector required**
- **TTL logic control compatible**
- **Default power up state**

RELATED LITERATURE

- **081123 Le75282 Dual Intelligent Line Card Access Switch Data Sheet**
- **081105 Le75181 Ringing Access Switch Data Sheet**
- **080754 Le58QL061/063 QLSLAC Data Sheet**
- **080676 Le5711 Dual SLIC Data Sheet**
- **081047 Le5712 Dual SLIC Data Sheet**

DESCRIPTION

The VoiceEdge™ family VE750 series of Line Card Access Switches (LCAS), which includes the Le75181, Le75282 and Le75183 devices, is a family of monolithic solid-state switches that is designed to provide both power ringing access and test access on the analog line card. These devices, while not a pin-for-pin replacement for the traditional electromechanical relay (EMR) solution, provide the equivalent switching functionality. The VE750 series of LCAS is meant as a solid-state alternative to the EMRs.

The Le75183A/B/C/D devices are pin-for-pin compatible with Legerity's L7583A/B/C/D devices.

Legerity also offers a range of compatible SLIC devices and codec/filters that can be used with the VE750 series LCAS for complete line card solutions that can be used worldwide in analog line card applications.

ORDERING INFORMATION

Device	Package Type[1]	Packing[2]
Le75183ADSC	20-Pin SOIC (GULL)	Tube
Le75183BDSC		
Le75183CDSC		
Le75183DDSC		
LE75183AFQC	32-Pin QFN	Tray
Le75183BFQC		
Le75183CFQC		
Le75183DFQC		
Le75183AFSC	28-pin SOIC (GULL)	Tube
Le75183BFSC		
Le75183CFSC		
Le75183CZFSC		
Le75183DFSC		

1. *The green package meets RoHS Directive 2002/95/EC of the European Council to minimize the environmental impact of electrical equipment.*
2. *For delivery using a tape and reel packing system, add a "T" suffix to the OPN (Ordering Part Number) when placing an order.*

NOTE: On August 3, 2007, Zarlink Semiconductor acquired the products and technology of Legerity Holdings.

Document ID#	**081105**	Date:	**Sep 18, 2007**
Rev:	**C**	Version:	**2**
Distribution:	**Public Document**		

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PRODUCT DESCRIPTION

The Le75183A/B/C/D Line Card Access Switch is a monolithic solid-state device providing the equivalent switching functionality of three 2 form C switches. The Le75183 is designed to provide power ringing access, line test access (test out), and SLIC test access (test in) to tip and ring in central office, digital loop carrier, private branch exchange, digitally added main line, and hybrid fiber coax/fiber-in-the-loop analog line card applications. An additional pair of solid-state contacts are also available to provide access for testing of the ringing generator.

The Le75183A/B has seven states: the idle talk state (line break switches closed, all other switches open), the power ringing state (ringing access switches closed, all other switches open), loop access (test out) state (loop access (test out) switches closed, all other switches open), SLIC test state (test in switches closed, all other switches open), simultaneous loop and SLIC access state (loop and test in switches closed, all others open), ringing generator test state (ring test switches closed, all others open), and an all OFF state. The seven states in the Le75183A/B are also in the Le75183C/D, with an additional simultaneous test-out and ring-test state, making the Le75183C/D appropriate for digital loop carrier and other Telcordia TR-57 applications.

The Le75183 offers break-before-make or make-before-break switching, with simple logic level input control. Because of the solid-state construction, voltage transients generated when switching into an inductive ringing lead during ring cadence or ring trip are minimized, possibly eliminating the need for external zero cross switching circuitry. State control is via logic level inputs, so no additional driver circuitry is required.

The line break switch is a linear switch that has exceptionally low ON-resistance and an excellent ON-resistance matching characteristic. The ringing access switch has a breakdown voltage rating >480 V which is sufficiently high, with proper protection, to prevent breakdown in the presence of a transient fault condition (i.e., passing the transient on to the ringing generator).

Incorporated into the Le75183A and Le75183C is a diode bridge/SCR clamping circuit, current-limiting circuitry, and a thermal shutdown mechanism to provide protection to the SLIC device and subsequent circuitry during fault conditions. This is shown in block diagram as version A/C. Positive and negative lightning is reduced by the current-limiting circuitry and steered to ground via diodes and the integrated SCR. Power cross is also reduced by the current-limiting and thermal shutdown circuits.

The Le75183B and Le75183D versions provide only an integrated diode bridge along with current limiting and thermal shutdown (see block diagram for version B/D). This will cause positive faults to be directed to ground and negative faults to battery. In either polarity, faults are reduced by the current-limit and/or thermal shutdown mechanisms.

To protect the Le75183 from an overvoltage fault condition, use of a secondary protector is required. The secondary protector must limit the voltage seen at the tip/ring terminals to prevent the breakdown voltage of the switches from being exceeded. To minimize stress on the solid-state contacts, use of a foldback- or crowbar- type secondary protector is recommended. With proper choice of secondary protection, a line card using the Le75183 will meet all relevant ITU-T, LSSGR, FCC, or UL* protection requirements.

The Le75183 operates off of a 5-V supply only. This gives the device extremely low idle and active power dissipation and allows use with virtually any range of battery voltage. This makes the Le75183 especially appropriate for remote power applications such as DAML or FOC/FITL or other Telcordia TA 909 applications where power dissipation is particularly critical.

A battery voltage is also used by the Le75183, only as a reference for the integrated protection circuit. The Le75183 will enter an all OFF state upon loss of battery.

During power ringing, to turn on and maintain the ON state, the ring access switch and ring test switch will draw a nominal 2 mA from the ring generator.

The default power up state of Le75183 is in all OFF state, unless otherwise being overwritten by external controls.

The Le75183 device is packaged in a 20-pin, plastic SOIC (GULL) (Le75183ASC/BSC/CSC/DSC), a 32-pin QFN (Le75183AQC/BQC/CQC/DQC), and a 28-pin, plastic SOIC (GULL) (Le75183AESC/BESC/CESC/CZESC/DESC). The 28-pin package is available to support existing designs. For new designs, it may be advantageous to use the other two packages for smaller in size.

BLOCK DIAGRAMS

Figure 1. Le75183A/C

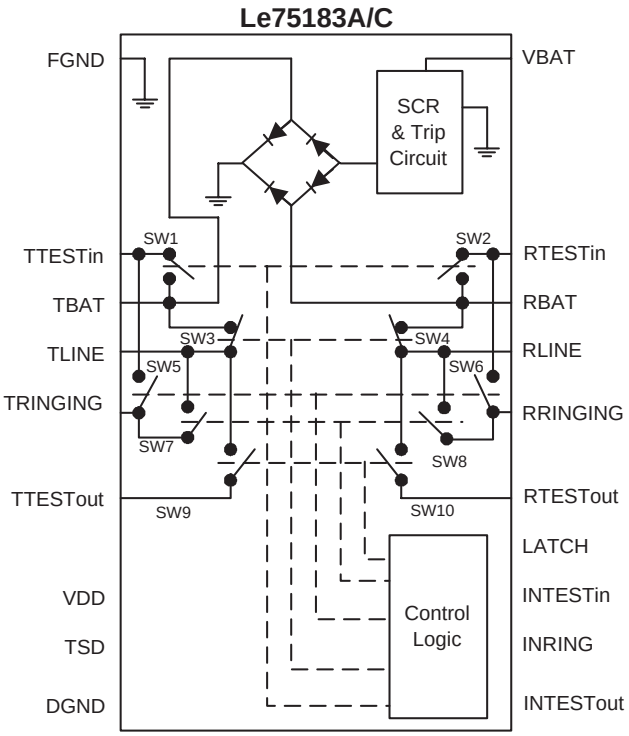
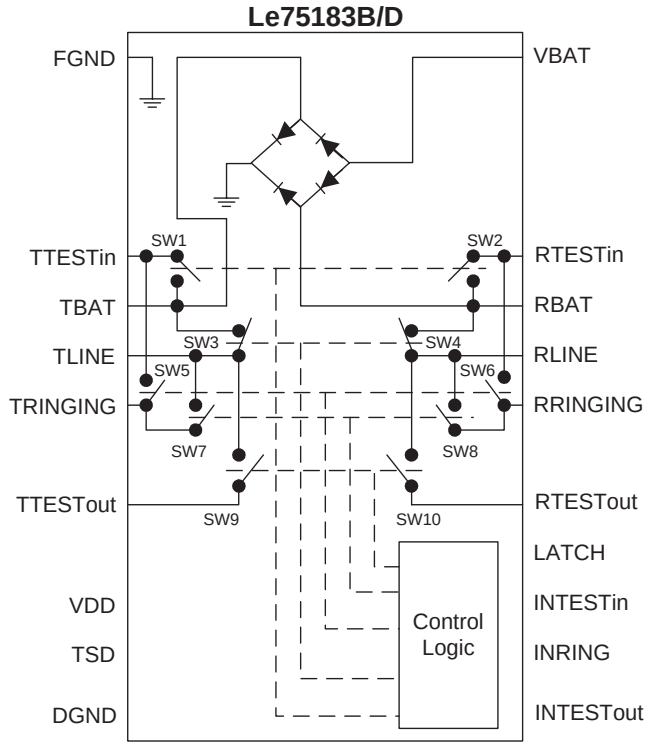
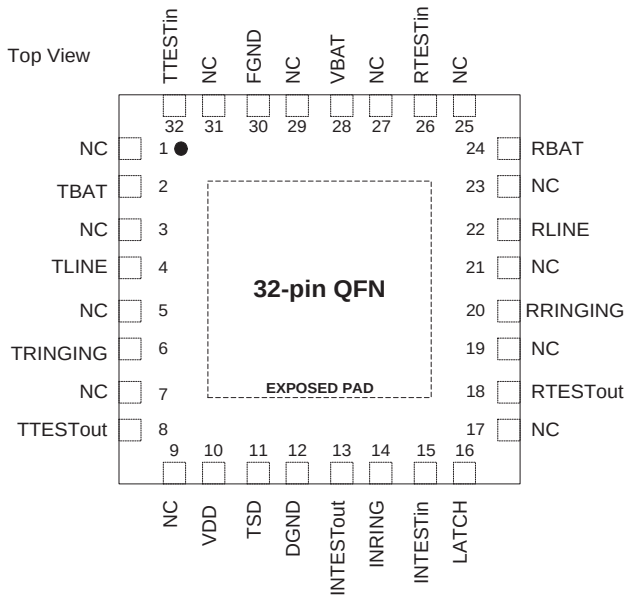
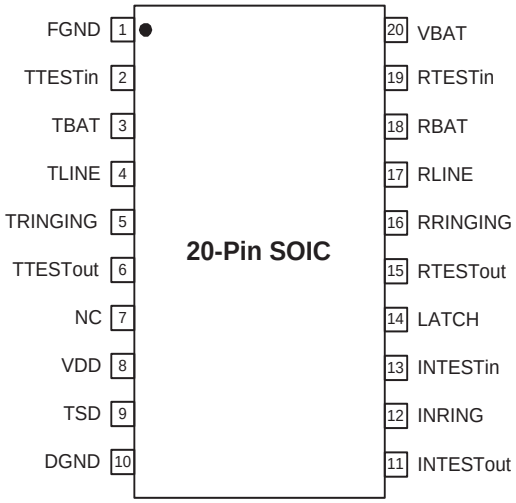


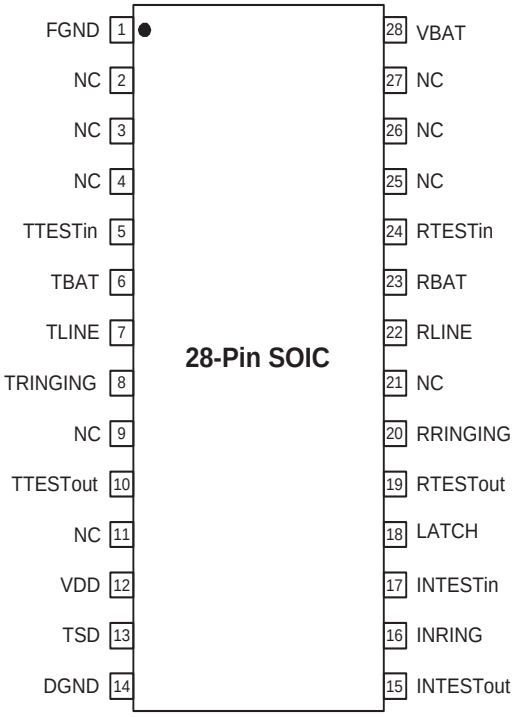
Figure 2. Le75183B/D



CONNECTION DIAGRAMS







Pin Descriptions .

Pin Name	Type	Description
DGND	Ground	Digital ground.
FGND	Ground	Fault ground.
INRING	Input	Logic level switch input control. Internally 75 kΩ typical pull up.
INTESTIN	Input	Logic level switch input control. Internally 75 kΩ typical pull down.
INTESTOUT	Input	Logic level switch input control. Internally 75 kΩ typical pull up.
LATCH	Input	Data input control, active-high, transparent low. Internally 75 kΩ typical pull down.
NC	—	No connection.
RBAT	Input/Output	Connect to RING on SLIC side.
RLINE	Input/Output	Connect to RING on line side.
RRINGING	Input/Output	Connect to ringing generator.
RTESTin	Input/Output	Test (in) access on RING.
RTESTout	Input/Output	Test (out) access on RING.
TBAT	Input/Output	Connect to TIP on SLIC side.
TLINE	Input/Output	Connect to TIP on line side.
TRINGING	Input/Output	Connect to return ground for ringing generator.
TTESTin	Input/Output	Test (in) access on TIP.
TTESTout	Input/Output	Test (out) access on TIP.
TSD	Input/Output	Temperature shutdown pin. Can be used as a logic level input or an output. See Tables 12 and 13, Truth Tables, and the Switching Behavior section of this data sheet for input pin description. As an output flag, will read HIGH when the device is in its operational mode and LOW in the thermal shutdown mode. To disable the thermal shutdown mechanism, tie this pin to HIGH (**not** recommended)
VBAT	Battery	Battery voltage. Used as a reference for protection circuit.
VDD	Power	5 V supply.
EPAD	—	Exposed pad in QFN package. No internal electrical connection. Not recommended to make any external electrical connection (such as VBAT or ground) to the EPAD.

D: Internally 75 kΩ typical pull down.
U: Internally 75 kΩ typical pull up.

ABSOLUTE MAXIMUM RATINGS

Stresses above those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Parameter	Min	Max	Unit
Operating Temperature Range	–40	110	°C
Storage Temperature Range	–40	150	°C
Relative Humidity Range	5	95	%
Pin Soldering Temperature (t=10s max)	—	260	°C
5 V Power Supply	-0.3	7	V
Battery Supply	—	–85	V
Logic Input Voltage	-0.3	V_{DD}+0.3	V
Input-to-output Isolation	—	330	V
Pole-to-pole Isolation (All except SW6, SW8)	—	330	V
Pole-to-pole Isolation (Ringing Access Switch, SW8)	—	480	V
Pole-to-pole Isolation (Ringing Test Swtich, SW6)	—	260	V
ESD Immunity (Human Body Model)	JESD22 Class 1C compliant		

Note:

For LCAS in the QFN package, it is desirable that the exposed pad be soldered to an equally sized exposed copper surface (with no further electrical connection such as VBAT or ground) for mechanical stability.

OPERATING RANGES

Package Assembly

Green package devices are assembled with enhanced, environmental compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes. The peak soldering temperature should not exceed 245°C during printed circuit board assembly.

Refer to IPC/JEDEC J-Std-020B Table 5-2 for the recommended solder reflow temperature profile.

Environmental Ranges

Legerity guarantees the performance of this device over commercial (0 to 70º C) and industrial (-40 to 85ºC) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore GR-357-CORE Component Reliability Assurance Requirements for Telecommunications Equipment.

Ambient Temperature	–40° to 85°C

Electrical Ranges

Supply	Min	Typ	Max	Unit
V_{DD}	4.5	5	5.5	V
V_{BAT}*	–19	—	–72	V

**V_{BAT} is used only as a reference for internal protection circuitry. If V_{BAT} rises above typically –10 V, the device will enter an all OFF state and remain in this state until the battery voltage drops below typically –15 V.*

**Applied voltage is 100 Vp-p square wave at 100 Hz.*

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Legerity employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for CDM. However, a standard HBM (resistance = 1500Ω , capacitance = 100 pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters.

ELECTRICAL CHARACTERISTICS

Summary of Assumptions

Unless otherwise noted, the test conditions are defined by the Le75183 device application circuit shown in Figure 8, on page 19 with:

V_{BAT} = –48 V, V_{DD} = 5.0 V.

Supply Currents and Power Dissipation

Operational State	Condition	I_{DD} mA			I_{BAT} µA			LCAS Device Power mW		
		Min.	Typ	Max	Min.	Typ	Max	Min.	Typ	Max
All OFF	VDD=5V, VBAT=-48V	—	0.760	1.1	—	4	10	—	3.8	6
Power Ringing or Access	VDD=5V, VBAT=-48V	—	0.850	2.1	—	4	10	—	4.4	11
Idle/Talk	VDD=5V, VBAT=-48V	—	0.860	1.3	—	4	10	—	4.5	7

SPECIFICATIONS

Device Specifications

Table 1. Test-In Switches, 1 and 2

Parameter	Test Condition	Measure	Min	Typ	Max	Unit
OFF-state Leakage Current:						µA
+25°C	Vswitch (differential) = –320 V to Gnd Vswitch (differential) = –60 V to +260 V	I_{SWITCH}	—	—	1	
+85°C	Vswitch (differential) = –330 V to Gnd Vswitch (differential) = –60 V to +270 V	I_{SWITCH}	—	—	1	
–40°C	Vswitch (differential) = –310 V to Gnd Vswitch (differential) = –60 V to +250 V	I_{SWITCH}	—	—	1	
ON-resistance (SW1, SW2):						Ω
+25 °C	I_{SWITCH} (on) = ±5 mA, ±10 mA	Δ VON	—	49	—	
+85 °C	I_{SWITCH} (on) = ±5 mA, ±10 mA	Δ VON	—	—	77	
–40 °C	I_{SWITCH} (on) = ±5 mA, ±10 mA	Δ VON	—	37	—	
Isolation:						µA
+25 °C	Vswitch (both poles) = ±320 V, Logic inputs = Gnd	Iswitch	—	—	1	
+85 °C	Vswitch (both poles) = ±330 V, Logic inputs = Gnd	Iswitch	—	—	1	
–40 °C	Vswitch (both poles) = ±310 V, Logic inputs = Gnd	Iswitch	—	—	1	
dV/dt Sensitivity*	—	—	—	200	—	V/µs

**Applied voltage is 100 Vp-p square wave at 100 Hz. Not tested in production.*

Table 2. Break Switches, 3 and 4

Parameter	Test Condition	Measure	Min	Typ	Max	Unit
OFF-state Leakage Current:						
+25°C	Vswitch (differential) = –320 V to Gnd Vswitch (differential) = –60 V to +260 V	I_{SWITCH}	—	—	1	
+85°C	Vswitch (differential) = –330 V to Gnd Vswitch (differential) = –60 V to +270 V	I_{SWITCH}	—	—	1	µA
–40°C	Vswitch (differential) = –310 V to Gnd Vswitch (differential) = –60 V to +250 V	I_{SWITCH}	—	—	1	
ON-resistance (SW3, SW4):						
+25 °C	TLINE = ±10 mA, ±40 mA, TBAT = –2 V	Δ VON	—	21.5	—	
+85 °C	TLINE = ±10 mA, ±40 mA, TBAT = –2 V	Δ VON	—	—	31	Ω
–40 °C	TLINE = ±10 mA, ±40 mA, TBAT = –2 V	Δ VON	—	16	—	
ON-resistance Match All except Le75183CZESC	Per ON-resistance test condition of SW3, SW4	Magnitude $R_{ON\_SW3} – R_{ON\_SW4}$	—	0.2	1.0	Ω
ON-resistance Match Le75183CZESC	Per ON-resistance test condition of SW3, SW4	Magnitude $R_{ON\_SW3} – R_{ON\_SW4}$	—	0.2	0.55	Ω
ON-state Voltage* (Figure 2, Switch 3)	Iswitch = I_{LIMIT} @ 50 Hz/60 Hz	VON	—	—	220	V
ON-state Voltage* (Figure 3, Switch 4)	Maximum Differential Voltage (Vmax) Foldback Voltage Breakpoint 1 (V1) Foldback Voltage Breakpoint 2 (V2)	VON VON VON	— 100 V1+0.5	— — —	320 — —	V
DC Current Limit (Figure 2, Switch 3):						
+85 °C	Vswitch (on) = ±10 V	Iswitch	80	—	—	mA
–40 °C	Vswitch (on) = ±10 V	Iswitch	—	—	250	
DC Current Limit (Figure 3, Switch 4):	I_{LIMIT1} I_{LIMIT2}	Iswitch Iswitch	80 2	— —	250 —	mA
Dynamic Current Limit (t = <0.5 µs)	Break switches in ON state; ringing access switches off; apply ±1000 V at 10/1000 µs pulse; appropriate secondary protection in place	Iswitch	—	2.5	—	A
Isolation:						
+25 °C	Vswitch (both poles) = ±320 V, Logic inputs = Gnd	Iswitch	—	—	1	
+85 °C	Vswitch (both poles) = ±330 V, Logic inputs = Gnd	Iswitch	—	—	1	µA
–40 °C	Vswitch (both poles) = ±310 V, Logic inputs = Gnd	Iswitch	—	—	1	
dV/dt Sensitivity†	—	—	—	200	—	V/µs

**This parameter is not tested in production. Choice of secondary protector should ensure this rating is not exceeded.*

†Applied voltage is 100 Vp-p square wave at 100 Hz. Not tested in production.

Table 3. Ring Test Return Switch, 5

Parameter	Test Condition	Measure	Min	Typ	Max	Unit
OFF-state Leakage Current:						
+25°C	Vswitch (differential) = –320 V to Gnd Vswitch (differential) = –60 V to +260 V	I_{SWITCH}	—	—	1	µA
+85°C	Vswitch (differential) = –330 V to Gnd Vswitch (differential) = –60 V to +270 V	I_{SWITCH}	—	—	1	
–40°C	Vswitch (differential) = –310 V to Gnd Vswitch (differential) = –60 V to +250 V	I_{SWITCH}	—	—	1	
ON-resistance	Iswitch (on) = ±0 mA, ±10 mA	Δ VON	—	50	100	Ω
Isolation:						
+25 °C	Vswitch (both poles) = ±320 V, Logic inputs = Gnd		—	—	1	
+85 °C	Vswitch (both poles) = ±330 V, Logic inputs = Gnd	Iswitch	—	—	1	µA
–40 °C	Vswitch (both poles) = ±310 V, Logic inputs = Gnd		—	—	1	
dV/dt Sensitivity*	—	—	—	200	—	V/µs

**Applied voltage is 100 Vp-p square wave at 100 Hz. Not tested in production.*

Table 4. Ringing Test Switch, 6

Parameter	Test Condition	Measure	Min	Typ	Max	Unit
OFF-state Leakage Current:						
+25°C	Vswitch (differential) = –60 to +190 V Vswitch (differential) = +60 to –190 V	I_{SWITCH}	—	—	1	
+85°C	Vswitch (differential) = –60 to +200 V Vswitch (differential) = +60 to –200 V	I_{SWITCH}	—	—	1	µA
–40°C	Vswitch (differential) = –60 to +180 V Vswitch (differential) = +60 to –180 V	I_{SWITCH}	—	—	1	
ON-resistance	Iswitch (on) = ±70 mA, ±80 mA	Δ VON	—	—	20	Ω
ON Voltage	Iswitch (on) = ±1 mA	—	—	—	1.5	V
Steady-state Current*	—	—	—	—	100	mA
Release Current	—	—	—	500	—	µA
Isolation:						
+25 °C	Vswitch (both poles) = ±320 V, Logic inputs = Gnd	Iswitch	—	—	1	
+85 °C	Vswitch (both poles) = ±330 V, Logic inputs = Gnd	Iswitch	—	—	1	µA
–40 °C	Vswitch (both poles) = ±310 V, Logic inputs = Gnd	Iswitch	—	—	1	
dV/dt Sensitivity†	—	—	—	200	—	V/µs

**Choice of secondary protector and series current-limit resistor should ensure these ratings are not exceeded.*

†Applied voltage is 100 Vp-p square wave at 100 Hz. Not tested in production.

Table 5. Ring Return Switch, 7

Parameter	Test Condition	Measure	Min	Typ	Max	Unit
OFF-state Leakage Current:						
+25°C	Vswitch (differential) = –320 V to Gnd Vswitch (differential) = –60 to +260 V	I_{SWITCH}	—	—	1	
+85°C	Vswitch (differential) = –330 V to Gnd Vswitch (differential) = –60 to +270 V	I_{SWITCH}	—	—	1	µA
–40°C	Vswitch (differential) = –310 V to Gnd Vswitch (differential) = –60 to +250 V	I_{SWITCH}	—	—	1	
DC Current Limit	Vswitch (on) = ±20 V	Iswitch	—	200	—	mA
ON-resistance	Iswitch (on) = ±0 mA, ±10 mA	Δ VON	—	—	100	Ω
ON-state Voltage*	Iswitch = I_{LIMIT} @ 50 Hz/60 Hz	VON	—	—	130	V
Isolation:						
+25 °C	Vswitch (both poles) = ±320 V, Logic inputs = Gnd	Iswitch	—	—	1	
+85 °C	Vswitch (both poles) = ±330 V, Logic inputs = Gnd	Iswitch	—	—	1	µA
–40 °C	Vswitch (both poles) = ±310 V, Logic inputs = Gnd	Iswitch	—	—	1	
dV/dt Sensitivity†	—	—	—	200	—	V/µs

**This parameter is not tested in production. Choice of secondary protector should ensure this rating is not exceeded.*

†Applied voltage is 100 Vp-p square wave at 100 Hz. Not tested in production.

Table 6. Ringing Access Switch, 8

Parameter	Test Condition	Measure	Min	Typ	Max	Unit
OFF-state Leakage Current:						
+25°C	Vswitch (differential) = –255 to +210 V Vswitch (differential) =+255 to –210 V	I_{SWITCH}	—	—	1	
+85°C	Vswitch (differential) = –270 to +210 V Vswitch (differential) = +270 to –210 V	I_{SWITCH}	—	—	1	µA
–40°C	Vswitch (differential) = –245 to +210 V Vswitch (differential) = +245 to –210 V	I_{SWITCH}	—	—	1	
ON Voltage	Iswitch (on) = ±1 mA	—	—	—	3	V
Ring Generator Current During Ring	VCC = 5 V INRING = 1 INTESTin = 0 INTESTout = 0	IRINGSOURCE	—	2	—	mA
Steady-state Current*	—	—	—	—	150	mA
Surge Current*	—	—	—	—	2	A
Release Current	—	—	—	500	—	µA
ON-resistance	Iswitch (on) = ±70 mA, ±80 mA	Δ VON	—	—	12	Ω
Isolation:						
+25 °C	Vswitch (both poles) = ±320 V, Logic inputs = Gnd	Iswitch	—	—	1	
+85 °C	Vswitch (both poles) = ±330 V, Logic inputs = Gnd	Iswitch	—	—	1	µA
–40 °C	Vswitch (both poles) = ±310 V, Logic inputs = Gnd	Iswitch	—	—	1	
dV/dt Sensitivity†	—	—	—	200	—	V/µs

**Choice of secondary protector and series current-limit resistor should ensure these ratings are not exceeded.*

†Applied voltage is 100 Vp-p square wave at 100 Hz. Not tested in production.

Table 7. Loop Access (Test Out) Switches, 9 and 10

Parameter	Test Condition	Measure	Min	Typ	Max	Unit
OFF-state Leakage Current:						
+25°C	Vswitch (differential) = –320 V to Gnd Vswitch (differential) = –60 to +260 V	I_{SWITCH}	—	—	1	
+85°C	Vswitch (differential) = –330 V to Gnd Vswitch (differential) = –60 to +270 V	I_{SWITCH}	—	—	1	µA
–40°C	Vswitch (differential) = –310 V to Gnd Vswitch (differential) = –60 V to +250 V	I_{SWITCH}	—	—	1	
ON-resistance:						
+25 °C	Iswitch (on) = ±5 mA, ±10 mA	Δ Von	—	49	—	
+85 °C	Iswitch (on) = ±5 mA, ±10 mA	Δ Von	—	—	77	Ω
–40 °C	Iswitch (on) = ±5 mA, ±10 mA	Δ Von	—	37	—	
ON-state Voltage*	Iswitch = ILIMIT @ 50 Hz/60 Hz	VON	—	—	130	V
DC Current Limit:						
+85 °C	Vswitch (on) = ±10 V	Iswitch	80	—	—	mA
–40 °C	Vswitch (on) = ±10 V	Iswitch	—	—	250	
Dynamic Current Limit (t = <0.5 µs)	Break switches in ON state; ringing access switches OFF; apply ±1000 V at 10/1000 µs pulse; appropriate secondary protection in place	Iswitch	—	2.5	—	A
Isolation:						
+25 °C	Vswitch (both poles) = ±320 V, Logic inputs = Gnd	Iswitch	—	—	1	
+85 °C	Vswitch (both poles) = ±330 V, Logic inputs = Gnd	Iswitch	—	—	1	µA
–40 °C	Vswitch (both poles) = ±310 V, Logic inputs = Gnd	Iswitch	—	—	1	
dV/dt Sensitivity†	—	—	—	200	—	V/µs

**This parameter is not tested in production. Choice of secondary protector should ensure this rating is not exceeded.*

†Applied voltage is 100 Vp-p square wave at 100 Hz. Not tested in production.

Table 8. Additional Electrical Characteristics

Parameter	Test Condition	Measure	Min	Typ	Max	Unit
Digital Input Characteristics:						
Input Low Voltage	—	—	—	—	0.8	V
Input High Voltage	—	—	2.2	—	—	V
Input Leakage Current (high)	V_{DD} = 5.5 V, V_{BAT} = –75 V, Vlogicin = 5 V	Ilogicin	—	—	500	µA
Input Leakage Current (low)	V_{DD} = 5.5 V, V_{BAT} = –75 V, Vlogicin = 0 V	Ilogicin	—	—	500	
Input Leakage Current (high) INTESTOUT, INRING	V_{DD} = 5.5 V, V_{BAT} = –58 V, Vlogicin = 5 V	Ilogicin	—	0.5	—	
Input Leakage Current (low) INTESTOUT, INRING	V_{DD} = 5.5 V, V_{BAT} = –58 V, Vlogicin = 0 V	Ilogicin	—	100	—	
Input Leakage Current (high) INTESTIN, LATCH	V_{DD} = 5.5 V, V_{BAT} = –58 V, Vlogicin = 5 V	Ilogicin	—	100	—	
Input Leakage Current (low) INTESTIN, LATCH	V_{DD} = 5.5 V, V_{BAT} = –58 V, Vlogicin = 0 V	Ilogicin	—	0.5	—	
Temperature Shutdown Requirements*:						
Shutdown Activation Temperature	—	—	110	125	150	°C
Shutdown Circuit Hysteresis	—	—	10	—	25	°C

**Temperature shutdown flag (TSD) will be HIGH during normal operation and LOW during temperature shutdown state.*

ZERO CROSS CURRENT TURN OFF

The ring access switch (SW8) is designed to turn off on the next zero current crossing after application of the appropriate logic input control. This switch requires a current zero cross to turn off. Switch 8, once on, will remain in the ON state (regardless of logic input) until a current zero cross. Therefore, to ensure proper operation of switch 8, this switch should be connected, via proper impedance, to the ringing generator or some other ac source. Do not attempt to switch pure DC with switch 8. The ringing test access switch, SW6, also has similar characteristics to switch 8 and should also only be used to switch signals with zero current crossings.

For a detailed explanation of the operation of switches 6 and 8, please refer to the *An Introduction to Le758X Series of Line Card Access Switches* application note.

SWITCHING BEHAVIOR

When switching from the power ringing state to the idle/talk state via simple logic level input control, the Le75183 is able to provide control with respect to the timing when the ringing access contacts are released relative to the state of the line break contacts.

Make-before-break operation occurs when the line break switch contacts are closed (or made) before the ringing access switch contact is opened (or broken). Break-before-make operation occurs when the ringing access contact is opened (broke) before the line break switch contacts are closed (made).

Using the logic level input pins INRING, INTESTin, and INTESTout, either make-before-break or break-before-make operation of the Le75183 is easily achieved. The logic sequences for either mode of operation are given in Table 13 and Table 14. See the Truth Tables (Table 16 and Table 17) for an explanation of logic states.

When using an Le75183 in the make-before-break mode, during the ring-to-idle transition, for a period of up to one-half the ringing frequency, the ring break switch and the pnpn-type ring access switch can both be in the ON state. This is the maximum time after the logic signal at INRING has transitioned that the ring access switch is waiting for the next zero current cross, so it can close. During this interval, current that is limited to the dc break switch current-limit value will be source from the ring node of the SLIC.

This current is presented to the internal protection circuit. If the SCR-type protector is used (A or C codes), if by random probability the ring-to-idle transition occurs during a portion of the ring cycle when the ringing voltage exceeds the protection circuit SCR turn-on voltage, and if current in excess of the SCR's turn-on current is also available, the SCR may turn on. Once the SCR is triggered on, if the SLIC is capable of supplying current in excess of the holding current, the SCR may be latched on by the SLIC.

The probability of this event depends on the characteristics of the given SLIC and of the holding current of the Le75183 A or C device. The SCR hold current distribution is designed to be safely away from the test limit of 80 mA. The higher the distribution, the lower the probability of the latch.

If this situation is of concern for a given board design, either use the A or C series device in the break-before-make mode (eliminates the original 25 ms current pulse) or use a B or D series device (eliminates the SCR).

Table 9. Make-Before-Break Operation

INRING	INTESTin	INTESTout	TSD	State	Timing	Break Switches 3 & 4	Ring Return Switch 7	Ring Access Switch 8	All Other Access Switches
1	0	0	1/Float	Power Ringing	—	Open	Closed	Closed	Open
0	0	0	1/Float	Make-before-break	SW8 waiting for next zero current crossing to turn off maximum time—one-half of ringing. In this transition state, current that is limited to the dc break switch current-limit value will be sourced from the ring node of the SLIC.	Closed	Open	Closed	Open
0	0	0	1/Float	Idle/Talk	Zero cross current has occurred.	Closed	Open	Open	Open

Table 10. Break-Before-Make Operation

INRING	INTESTin	INTESTout	TSD	State	Timing	Break Switches 3 & 4	Ring Return Switch 7	Ring Access Switch 8	All Other Switches
1	0	0	1/Float	Power Ringing	—	Open	Closed	Closed	Open
1	0	1	1/Float	All Off	Hold this state for ≤25 ms. SW8 waiting for zero current to turn off.	Open	Open	Closed	Open
1	0	1	1/Float	All Off	Zero current has occurred and SW8 has opened.	Open	Open	Open	Open
0	0	0	1/Float	Idle/Talk	Release break switches.	Closed	Open	Open	Open

Notes:

Break-before-make operation can be achieved using TSD as an input. In lines two and three of Table 10, instead of using the logic input pins to force the all OFF state, force TSD to logic 0. This will override the logic inputs and also force the all OFF state. Hold this state for 25 ms. During this 25 ms all OFF state, toggle the inputs from 10 (ringing state) to 00 (idle/talk state). After 25 ms, release TSD to return switch control to the input pins which will set the idle talk state.

When using the Le75183A/B/C/D in this mode, forcing TSD to logic 0 will override the INPUT pins and force an all OFF state. Setting TSD to logic 1 will allow switch control via the logic INPUT pins. However, setting TSD to logic 1 will also disable the thermal shutdown mechanism. This is not recommended. Therefore, to allow switch control via the logic INPUT pins, allow TSD to float.

Thus, when using TSD as an input, the two recommended states are 0 (overrides logic input pins and forces all OFF state) and float (allows switch control via logic input pins and thermal shutdown mechanism is active). This may require use of an open-collector buffer.

Also note that TSD operation in Le75183 is different than TSD operation of the L75181, where application of logic 1 does not disable the thermal shutdown mechanism.

POWER SUPPLIES

Though both the 5-V and battery supplies are brought onto the Le75183 device, only the 5-V supply is required for switch operation; that is, state control is powered exclusively off of the 5-V supply. Because of this, the Le75183 device offers extremely low power dissipation, both in the Idle and Active states.

The battery voltage is not used for switch state control, but rather as a reference voltage by the integrated secondary protection circuit. When the voltage at TBAT or RBAT drops 2 V to 4 V below the battery, the integrated SCR will trigger, thus preventing fault-induced overvoltage situations at the TBAT/RBAT nodes.

LOSS OF BATTERY VOLTAGE

As an additional protection feature, the Le75183 device monitors the battery voltage. Upon loss of battery voltage, the Le75183 will automatically enter an all OFF state and remain in that state until the battery voltage is restored. The Le75183 is designed so that the device will enter the all OFF state if the battery rises above typically –10 V and will remain off until the battery drops below typically –15 V.

Monitoring the battery for the automatic shutdown feature will draw a small current from the battery, typically 4 µA. This will add slightly to the overall power dissipation of the device.

IMPULSE NOISE

Using the Le75183 will minimize and possibly eliminate the contribution to the overall system impulse noise that is associated with ringing access switches. Because of this characteristic of the Le75183 device, it may not be necessary to incorporate a zero cross switching scheme. This ultimately depends upon the characteristics of the individual system and is best evaluated at the board level.

PROTECTION

Integrated SLIC Device Protection

Diode Bridge/SCR

In the Le75183A and the Le75183C versions, protection to the SLIC device or other subsequent circuitry is provided by a combination of current-limited break switches, a diode bridge/SCR clamping circuit, and a thermal shutdown mechanism. In the Le75183B and the Le75183D versions, protection to the SLIC device or other subsequent circuitry is provided by a combination of current-limited break switches, a diode bridge, and a thermal shutdown mechanism.

In both protection versions, during a positive lightning event, fault current is directed to ground via steering diodes in the diode bridge. Voltage is clamped to a diode drop above ground. In the A version, negative lightning causes the SCR to conduct when the voltage goes 2 V to 4 V more negative than the battery. Fault currents are then directed to ground via the SCR and steering diodes in the diode bridge.

Note that for the SCR to foldback or crowbar, the ON voltage (see Table 14) of the SCR must be less negative than the battery reference voltage. If the battery voltage is less negative than the SCR ON voltage, the SCR will conduct fault currents to ground; however, it will not crowbar.

In the B/D version, negative lightning is directed to battery via steering diodes in the diode bridge.

For power cross and power induction faults, in both protection versions, the positive cycle of the fault is clamped a diode drop above ground and fault currents steered to ground. In the A/C version, the negative cycle will cause the SCR to trigger when the voltage exceeds the battery reference voltage by 2 V to 4 V. When the SCR triggers, fault current is steered to ground. In the B/D version, the negative cycle of the power cross is steered to battery.

Current Limiting

During a lightning event, the current that is passed through the break switches and presented to the integrated protection circuit and subsequent circuitry is limited by the dynamic current-limit response of the break switches (assuming idle/talk state). When the voltage seen at the TLINE/RLINE nodes is properly clamped by an external secondary protector, upon application of a 1000 V, 10 x 1000 pulse (LSSGR lightning), the current seen at the TBAT/RBAT nodes will typically be a pulse of magnitude 2.5 A and duration less than 0.5 µs.

During a power cross event, the current that is passed through the break switches and presented to the integrated protection circuit and subsequent circuitry is limited by the dc current-limit response of the break switches (assuming idle/talk state). The dc current limit is specified over temperature between 100 mA and

250 mA. Note that the current-limit circuitry has a negative temperature coefficient. Thus, if the device is subjected to an extended power cross, the value of current seen at TBAT/RBAT will decrease as the device heats due to the fault current. If sufficient heating occurs, the temperature shutdown mechanism will activate and the device will enter an all off mode.

Temperature Shutdown Mechanism

When the device temperature reaches a minimum of 110 °C, the thermal shutdown mechanism will activate and force the device into an all OFF state, regardless of the logic input pins. Pin TSD, when used as an output, will read LOW when

the device is in the thermal shutdown mode and HIGH during normal operation.

During a lightning event, due to the relatively short duration, the thermal shutdown will not typically activate.

During an extended power cross, the device temperature will rise and cause the device to enter the thermal shutdown mode. This forces an all off mode, and the current seen at TBAT/RBAT drops to zero. Once in the thermal shutdown mode, the device will cool and exit the thermal shutdown mode, thus reentering the state it was in prior to thermal shutdown. Current, limited to the dc current-limit value, will again begin to flow and device heating will begin again. This cycle of entering and exiting thermal shutdown will last as long as the power cross fault is present. The frequency of entering and exiting thermal shutdown will depend on the magnitude of the power cross. If the magnitude of the power cross is great enough, the external secondary protector may trigger shunting all current to ground.

In the Le75183, the thermal shutdown mechanism can be disabled by forcing the TSD pin to HIGH. This functionality is different from the Le75181, whose thermal shutdown mechanism cannot be disabled.

Electrical specifications relating to the integrated overvoltage clamping circuit are outlined in Table 15.

External Secondary Protector

With the above integrated protection features, only one overvoltage secondary protection device on the loop side of the Le75183 is required. The purpose of this device is to limit fault voltages seen by the Le75183 so as not to exceed the breakdown voltage or input-output isolation rating of the device. To minimize stress on the Le75183, use of a foldback- or crowbar-type device is recommended. A detailed explanation and design equations on the choice of the external secondary protection device are given in the *An Introduction to Le758X Series of Line Card Access Switches* application note. Basic design equations governing the choice of external secondary protector are given below.

- $|V_{BATmax}| + |V_{breakovermax}| < |V_{breakdownmin(break)}|$
- $|V_{ringingpeakmax}| + |V_{BATmax}| + |V_{breakovermax}| < |V_{breakdownmin(ring)}|$
- $|V_{ringingpeakmax}| + |V_{BATmax}| < |V_{breakovermin}|$

where:

V_{BATmax}—Maximum magnitude of battery voltage.

$V_{breakovermax}$—Maximum magnitude breakover voltage of external secondary protector.

$V_{breakovermin}$—Minimum magnitude breakover voltage of external secondary protector.

$V_{breakdownmin(break)}$—Minimum magnitude breakdown voltage of Le75183 break switch.

$V_{breakdownmin(ring)}$—Minimum magnitude breakdown voltage of Le75183 ring access switch.

$V_{ringingpeakmax}$—Maximum magnitude peak voltage of ringing signal.

Series current-limiting fused resistors or PTC resistors should be chosen so as not to exceed the current rating of the external secondary protector. Refer to the manufacturer’s data sheet for specifications.

Table 11. Electrical Specifications, Protection Circuitry

Parameters Related to Diodes (in Diode Bridge)						
Parameter	**Test Condition**	**Measure**	**Min**	**Typ**	**Max**	**Unit**
Voltage Drop at Continuous Current (50 Hz/60 Hz)	Apply ±dc current limit of break switches	Forward Voltage	—	—	3.5	V
Voltage Drop at Surge Current	Apply ±dynamic current limit of break switches	Forward Voltage	—	5	—	
Parameters Related to Protection SCR						
Surge Current	—	—	—	—	‡	A
Gate Trigger Current*†	—	—	—	25	50	mA
Gate Trigger Current† Temperature Coefficient	—	—	—	–0.5	—	%/°C
Hold Current	—	—	70	—	—	mA
Gate Trigger Voltage	Trigger current	—	V_{BAT} – 4	—	V_{BAT} – 2	V
Reverse Leakage Current	V_{BAT}	—	—	—	1.0	µA
ON-State Voltage§	0.5 A, t = 0.5 µs 2.0 A, t = 0.5 µs	V_{ON} —	— —	–3 –5	— —	V

** Trigger Current is defined as the minimum current drawn from tip and ring to turn on the SCR. The specification in this data sheet is Gate Trigger Current, which is defined as the maximum current that can flow into the battery before the SCR turns on.*

† Typical at 25 °C

‡ Twice ± dynamic current limit of break switches.

§ In some instances, the typical ON-state voltage can range as low as –25 V.

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 3. Protection Circuits

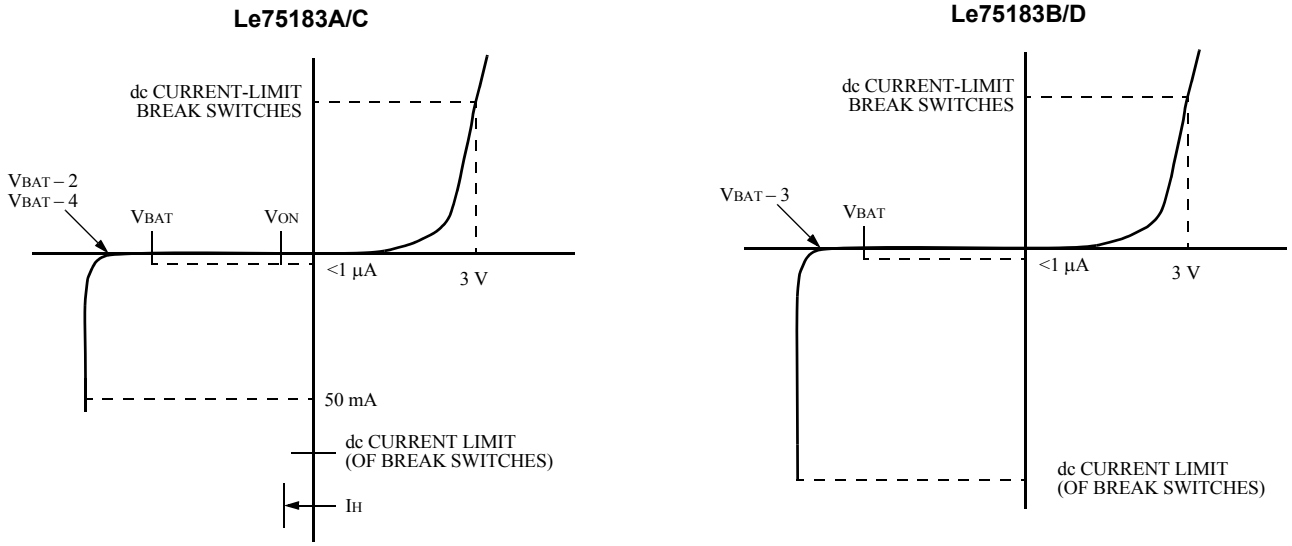


Figure 4. Switches 3, 7, 9, and 10

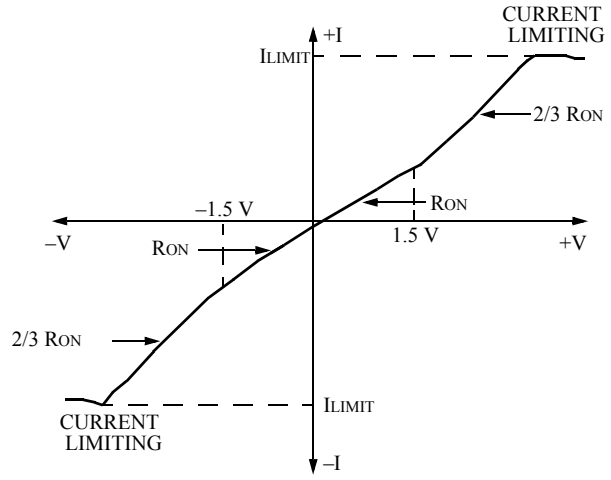


Figure 5. Switch 4

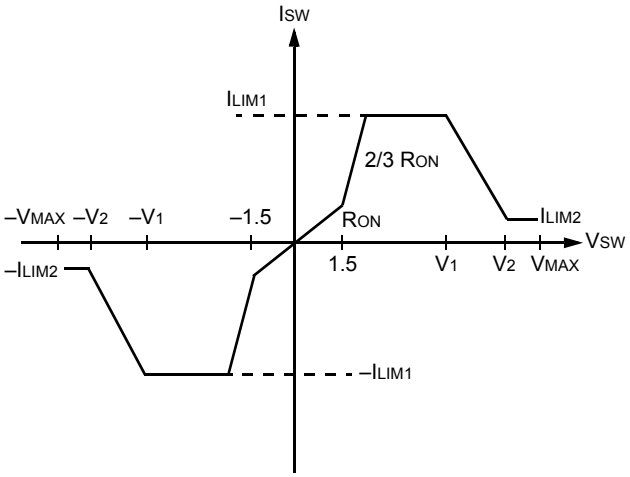


Figure 6. Switches 1, 2, and 5

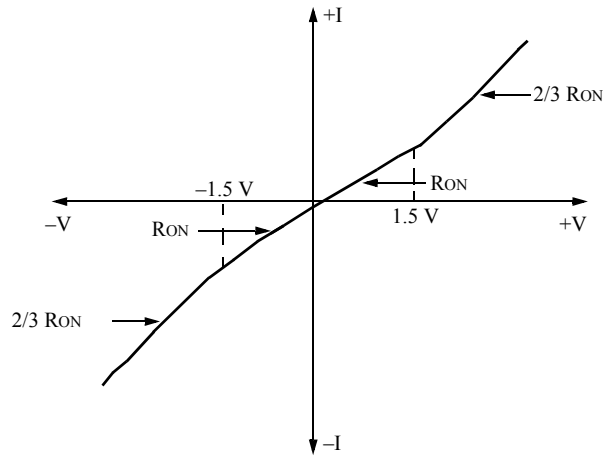
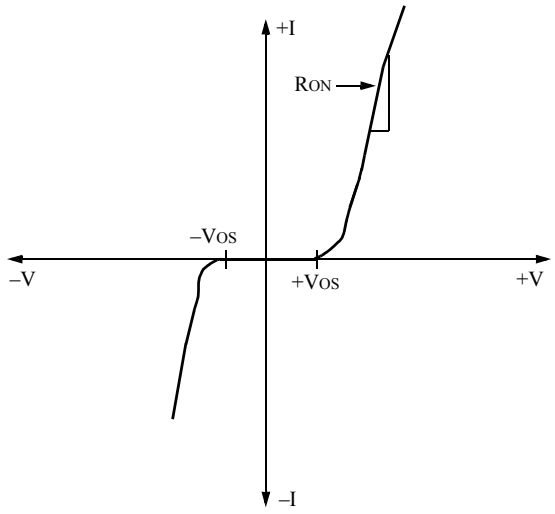
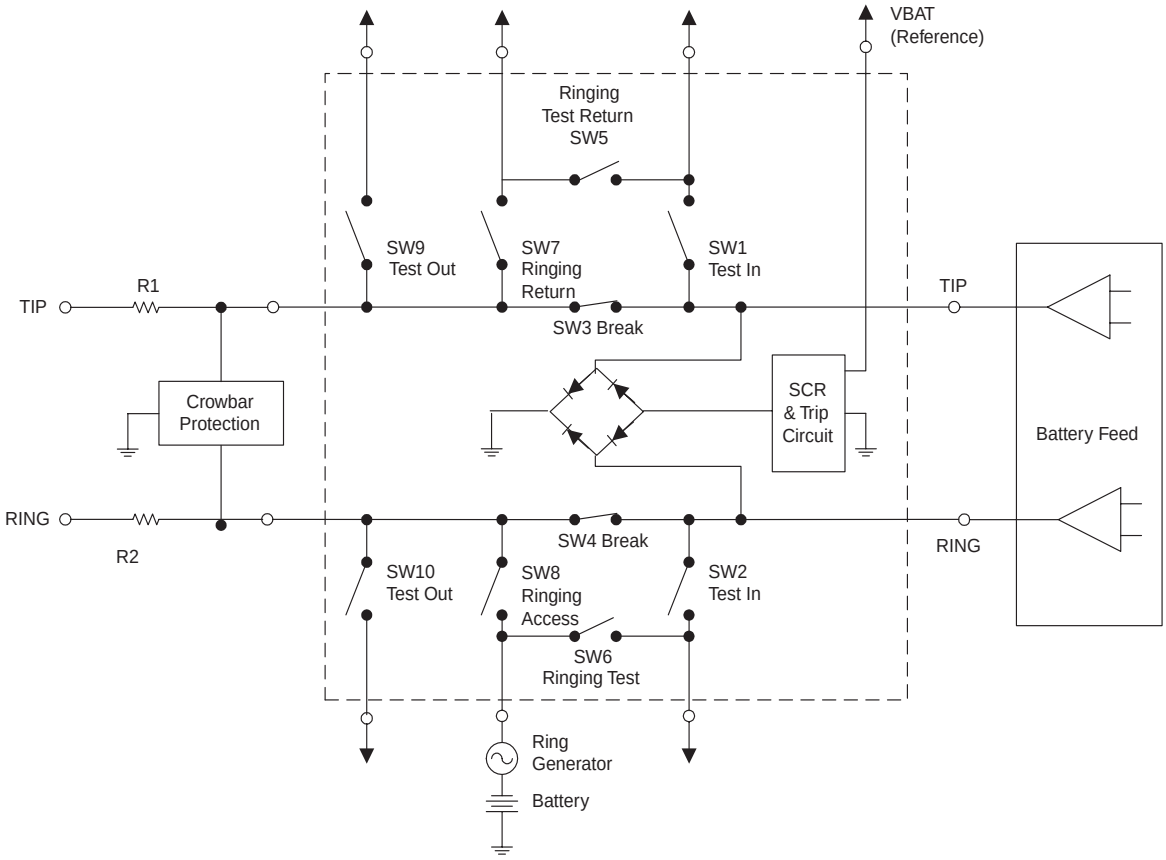


Figure 7. Switches 6, 8



APPLICATION

Figure 8. Typical LCAS Application, A/C Versions, Idle or Talk State Shown



**Contact a Legerity Sales/Application representative for recommendations.*

Table 12. Truth Table for the Le75183A/B Devices

INRING	INTESTin	INTESTout	TSD	TESTin Switches	Break Switches	Ring Test Switches	Ring Switches	TESTout Switches
0	0	0	1/Float[1]	Off	On	Off	Off	Off[3]
0	0	1	1/Float[1]	Off	Off	Off	Off	On[4]
0	1	0	1/Float[1]	On	Off	Off	Off	Off[5]
1	0	0	1/Float[1]	Off	Off	Off	On	Off[6]
1	1	0	1/Float[1]	Off	Off	On	Off	Off[7]
0	1	1	1/Float[1]	On	Off	Off	Off	On[8]
1	0	1	1/Float[1]	Off	Off	Off	Off	Off[9, 10]
1	1	1	1Float[1]	Off	Off	Off	Off	Off[9]
Don't Care	Don't Care	Don't Care	0[2]	Off	Off	Off	Off	Off[9]

1. *If TSD is logic 1, the thermal shutdown mechanism is disabled. If TSD is floating, the thermal shutdown mechanism is active.*
2. *Forcing TSD to logic 0 overrides the logic input pins and forces an all OFF state.*
3. *Idle/Talk state.*
4. *TESTout state.*
5. *TESTin state*
6. *Power ringing state.*
7. *Ringing generator test state.*
8. *Simultaneous TESTout and TESTin state.*
9. *All OFF state.*
10. *Default power up state.*

A parallel in/parallel out data latch is integrated into the Le75183A/B. Operation of the data latch is controlled by the logic level input pin LATCH. The data input to the latch is the INPUT pin of the Le75183A/B, and the output of the data latch is an internal node used for state control.

When the LATCH control pin is at logic 0, the data latch is transparent and data control signals flow directly from INPUT, through the data latch to state control. Any changes in INPUT will be reflected in the state of the switches.

When the LATCH control pin is at logic 1, the data latch is active—the Le75183A/B will no longer react to changes at the INPUT control pin. The state of the switches is now latched; that is, the state of the switches will remain as they were when the LATCH input transitioned from logic 0 to logic 1. The switches will not respond to changes in INPUT as long as LATCH is held high.

Note that the TSD input is not tied to the data latch. TSD is not affected by the LATCH input. TSD input will override state control via INPUT and LATCH.

Table 13. Truth Table for the Le75183C/D Devices

INRING	INTESTin	INTESTout	TSD	TESTin Switches	Break Switches	Ring Test Switches	Ring Switches	TESTout Switches
0	0	0	1/Float[1]	Off	On	Off	Off	Off[3]
0	0	1	1/Float[1]	Off	Off	Off	Off	On[4]
0	1	0	1/Float[1]	On	Off	Off	Off	Off[5]
1	0	0	1/Float[1]	Off	Off	Off	On	Off[6]
1	1	0	1/Float[1]	Off	Off	On	Off	Off[7]
0	1	1	1/Float[1]	On	Off	Off	Off	On[8]
1	0	1	1/Float[1]	Off	Off	Off	Off	Off[9, 11]
1	1	1	1/Float[1]	Off	Off	On	Off	On[10]
Don't Care	Don't Care	Don't Care	0[2]	Off	Off	Off	Off	Off[9]

1. *If TSD is logic 1, the thermal shutdown mechanism is disabled. If TSD is floating, the thermal shutdown mechanism is active.*
2. *Forcing TSD to logic 0 overrides the logic input pins and forces an all OFF state.*
3. *Idle/Talk state.*
4. *TESTout state.*
5. *TESTin state*
6. *Power ringing state.*
7. *Ringing generator test state.*
8. *Simultaneous TESTout and TESTin state.*
9. *All OFF state.*
10. *Simultaneous TESTout—Ring Test state.*
11. *Default power up state.*

A parallel in/parallel out data latch is integrated into the Le75183C/D. Operation of the data latch is controlled by the logic level input pin LATCH. The data input to the latch is the INPUT pin of the Le75183C/D and the output of the data latch is an internal node used for state control.

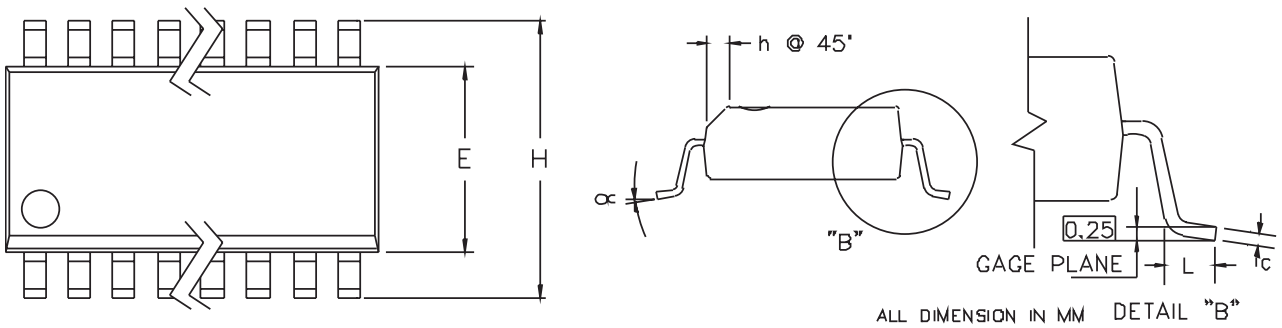
When the LATCH control pin is at logic 0, the data latch is transparent and data control signals flow directly from INPUT, through the data latch to state control. Any changes in INPUT will be reflected in the state of the switches.

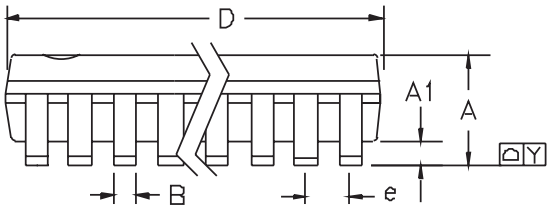
When the LATCH control pin is at logic 1, the data latch is active; the Le75183C/D will no longer react to changes at the INPUT control pin. The state of the switches is now latched; that is, the state of the switches will remain as they were when the LATCH input transitioned from logic 0 to logic 1. The switches will not respond to changes in INPUT as long as LATCH is held high.

Note that the TSD input is not tied to the data latch. TSD is not affected by the LATCH input. TSD input will override state control via INPUT and LATCH.

PHYSICAL DIMENSIONS

28-Pin, Plastic SOIC (GULL) (Le75183AESC/BESC/CESC/CZESC/DESC)





Small Outline Package (28 SOIC)						
Symbol	Millimeter			Inch		
	Min	Nom	Max	Min	Nom	Max
A	2.35	2.54	2.65	0.092	0.100	0.104
A1	0.10	0.17	0.30	0.004	0.006	0.012
B	0.33	0.42	0.51	0.013	0.016	0.020
C	0.23	0.25	0.32	0.009	0.010	0.012
E	7.40	7.50	7.60	0.291	0.295	0.299
e	1.27 BSC			0.050 BSC		
H	10.00	10.30	10.65	0.394	0.406	0.419
h	0.25	0.50	0.75	0.009	0.020	0.029
L	0.40	0.70	1.27	0.015	0.028	0.050
	0 deg	-	8 deg	0 deg	-	8 deg
Y	0.00		0.01	0.000	-	0.004
D	17.70	17.90	18.10	0.697	0.705	0.712

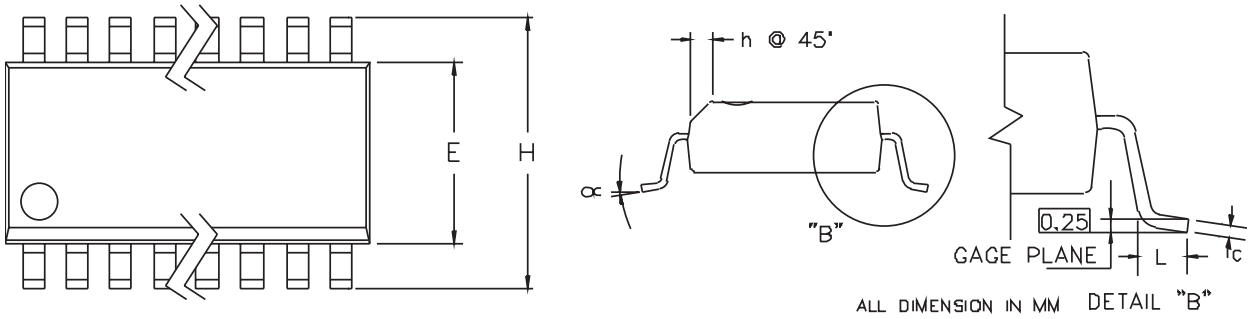
NOTE:
Option: Square dotted line is E-Pad outline
Size dependent on die attach pad

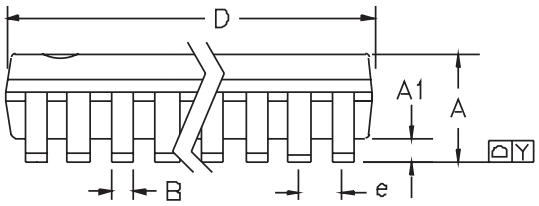
28-Pin SOIC

Note:

Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.

20-Pin, Plastic SOIC (GULL) (Le75183ASC/BSC/CSC/DSC)





Small Outline Package (20 SOIC)						
Symbol	Millimeter			Inch		
	Min	Nom	Max	Min	Nom	Max
A	2.35	2.54	2.65	0.092	0.100	0.104
A1	0.10	0.17	0.30	0.004	0.006	0.012
B	0.33	0.42	0.51	0.013	0.016	0.020
C	0.23	0.25	0.32	0.009	0.010	0.012
E	7.40	7.50	7.60	0.291	0.295	0.299
e	1.27 BSC			0.050 BSC		
H	10.00	10.30	10.65	0.394	0.406	0.419
h	0.25	0.50	0.75	0.009	0.020	0.029
L	0.40	0.70	1.27	0.015	0.028	0.050
	0 deg	-	8 deg	0 deg	-	8 deg
Y	0.00		0.01	0.000	-	0.004
D	12.60	12.80	13.00	0.496	0.504	0.512

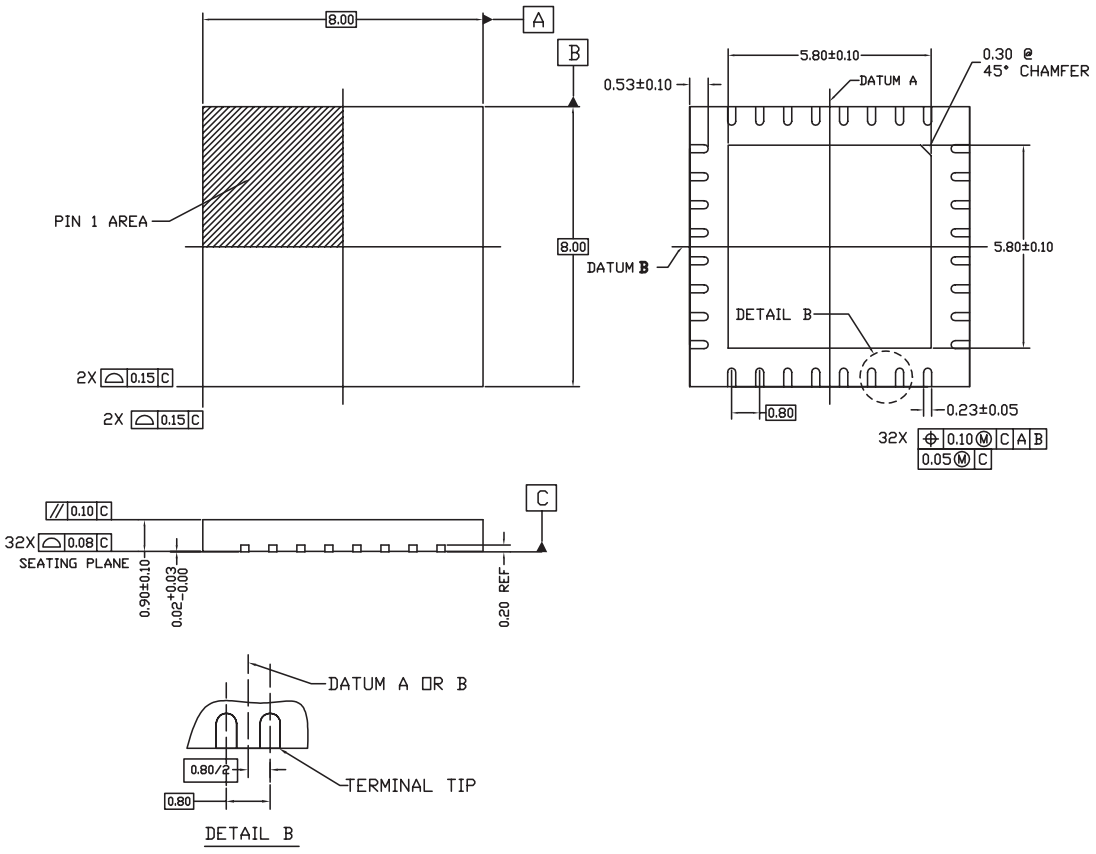
NOTE:
Option: Square dotted line is E-Pad outline
Size dependent on die attach pad

20-Pin SOIC

Note:

Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.

32-Pin QFN (Le75183QC/BEQC/CQC/DQC)



Symbol	32 LEAD QFN		
	Min	Nom	Max
A	0.80	0.90	1.00
A2		0.57 REF	
b	0.18	0.23	0.28
D		8.00 BSC	
D2	5.70	5.80	5.90
E		8.00 BSC	
E2	5.70	5.80	5.90
e		0.80 BSC	
L	0.43	0.53	0.63
N		32	
A1	0.00	0.02	0.05
A3		0.20 REF	
aaa		0.20	
bbb		0.10	
ccc		0.10	

NOTES:
1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. ⌖ is in degrees.
3. N is the total number of terminals.
4. The Terminal #1 identifier and terminal numbering convention shall conform to JEP 95-1 and SSP-012. Details of the Terminal #1 identifier are optional, but must be located within the zone indicated. The Terminal #1 identifier may be either a mold or marked feature.
5. Coplanarity applies to the exposed pad as well as the terminals.
6. Reference Document: JEDEC MO-220.
7. Lead width deviates from the JEDEC MO-220 standard.

32-Pin QFN

Note:

Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.

REVISION HISTORY

Revision A1 to B1

- Added new product offering, Le75183CZESC.
- Page 10, Table 5 Ring Return Switch DC Current Limit test condition from Vswitch(on)=+/-10V to +/-20V.
- Page 5, Pin Descriptions about EPAD, from "internally connected to digital ground" to "no internal electrical connection".

Revision B1 to C1

- Added green package OPNs in *Ordering Information*, on page 1; removed non-green OPNs.
- Added notes to table in *Ordering Information*, on page 1.
- Added *Package Assembly*, on page 7

Revision C1 to C2

- Enhanced format of package drawings in *Physical Dimensions*, on page 22
- Added new headers/footers due to Zarlink purchase of Legerity on August 3, 2007

For more information about all Zarlink products visit our Web Site at:

www.zarlink.com