MT88E45

4-Wire Calling Number Identification Circuit 2 (4-Wire CNIC2)

Data Sheet

August 2005

Features

- Compatible with:
  - Bellcore GR-30-CORE, SR-TSV-002476, ANSI/TIA/EIA-716, TIA/EIA-777;
  - ETSI ETS 300 778-1 (FSK only variant) & -2;
  - BT (British Telecom) SIN227 & SIN242
- Bellcore 'CPE Alerting Signal' (CAS), ETSI 'Dual Tone Alerting Signal' (DT-AS), BT Idle State and Loop State 'Tone Alert Signal' detection
- 1200 baud Bell 202 and CCITT V.23 FSK demodulation
- Separate differential input amplifiers with adjustable gain for Tip/Ring and telephone hybrid or speech IC connections
- Selectable 3-wire FSK data interface (bit stream or 1 byte buffer)
- Facility to monitor the stop bit for framing error check
- FSK Carrier detect status output
- 3 to 5V +/- 10% supply voltage
- Uses 3.579545 MHz crystal or ceramic resonator
- Low power CMOS with power down

Ordering Information

MT88E45BN	20 Pin SSOP	Tubes
MT88E45BS	20 Pin SOIC	Tubes
MT88E45BSR	20 Pin SOIC	Tape & Reel
MT88EBNR	20 Pin SSOP	Tape & Reel
MT88E45BN1	20 Pin SSOP*	Tubes
MT88E45BNR1	20 Pin SSOP*	Tape & Reel

*Pb Free Matte Tin

-40°C to +85°C

Applications

- Bellcore CID (Calling Identity Delivery) and CIDCW (Calling Identity Delivery on Call Waiting) telephones and adjuncts
- ETSI, BT CLIP (Calling Line Identity Presentation) and CLIP with Call Waiting telephones and adjuncts
- Fax and answering machines
- Computer Telephony Integration (CTI) systems

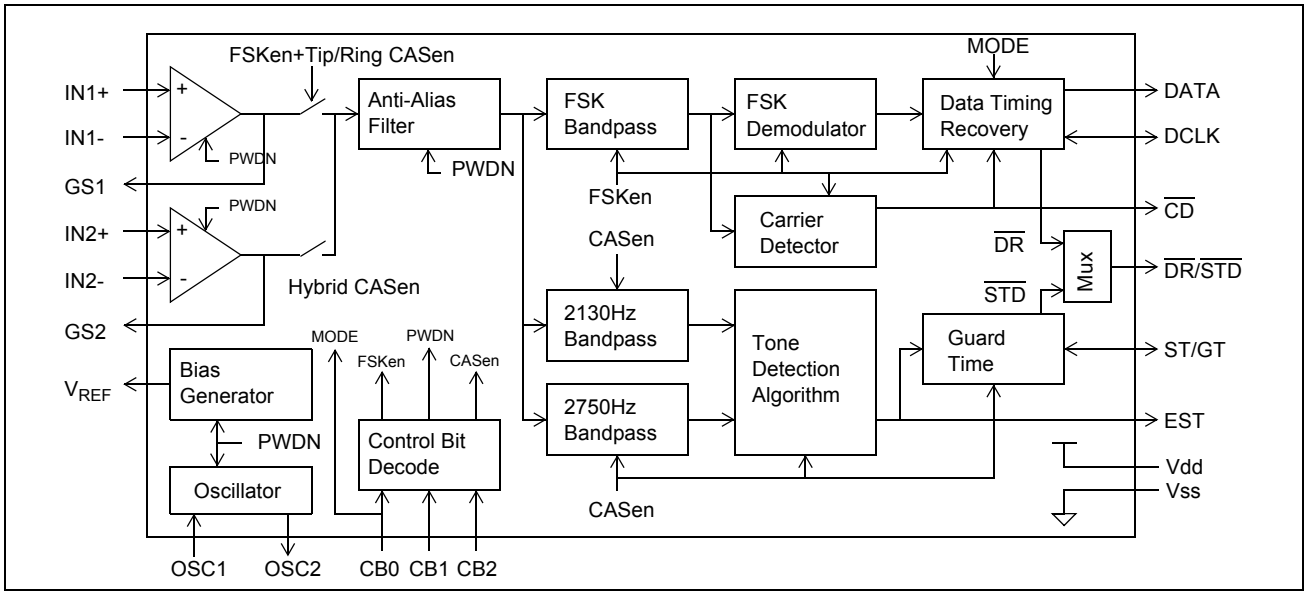


Figure 1 - Functional Block Diagram

Description

The MT88E45B is a low power CMOS integrated circuit suitable for receiving the physical layer signals used in North American (Bellcore) Calling Identity Delivery on Call Waiting (CIDCW) and Calling Identity Delivery (CID) services. It is also suitable for ETSI and BT Calling Line Identity Presentation (CLIP) and CLIP with Call Waiting services.

The MT88E45B contains a 1200 baud Bell 202/CCITT V.23 FSK demodulator and a CAS/DT-AS detector. Two input op-amps allow the MT88E45B to be connected to both Tip/Ring and the telephone hybrid or speech IC receive pair for optimal CIDCW telephone architectural implementation. FSK demodulation is always on Tip/Ring, while CAS detection can be on Tip/Ring or Hybrid Receive. Tip/Ring CAS detection is required for the Bellcore/TIA Multiple Extension Interworking (MEI) and BT's on-hook CLIP. A selectable FSK data interface allows the data to be processed as a bit stream or extracted from a 1 byte on chip buffer. Power management has been incorporated to power down the FSK or CAS section when not required. Full chip power down is also available. The MT88E45B is suitable for applications using a fixed power source (with a +/-10% variation) between 3 and 5 V.

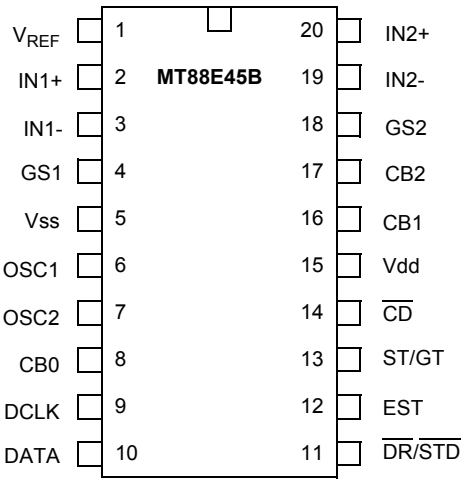


Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	V_{REF}	**Voltage Reference (Output).** Nominally Vdd/2. It is used to bias the Tip/Ring and Hybrid input op-amps.
2	IN1+	**Tip/Ring Op-amp Non-inverting (Input).**
3	IN1-	**Tip/Ring Op-amp Inverting (Input).**
4	GS1	**Tip/Ring Gain Select (Output).** This is the output of the Tip/Ring connection op-amp. The op-amp should be used to connect the MT88E45B to Tip and Ring. The Tip/Ring signal can be amplified or attenuated at GS1 via selection of the feedback resistor between GS1 and IN1-. FSK demodulation (which is always on Tip/Ring) or CAS detection (for MEI or BT on-hook CLIP) of the GS1 signal is enabled via the CB1 and CB2 pins. See Tables 1 and 2.
5	Vss	Power supply ground.
6	OSC1	**Oscillator (Input).** Crystal connection. This pin can also be driven directly from an external clock source.
7	OSC2	**Oscillator (Output).** Crystal connection. When OSC1 is driven by an external clock, this pin should be left open.
8	CB0	**Control Bit 0 (CMOS Input)**. This pin is used primarily to select the 3-wire FSK data interface mode. When it is low, interface mode 0 is selected where the FSK bit stream is output directly. When it is high, interface mode 1 is selected where the FSK byte is stored in a 1 byte buffer which can be read serially by the application's microcontroller. The FSK interface is consisted of the DATA, DCLK and $\overline{DR}/\overline{STD}$ pins. See the 3 pin descriptions to understand how CB0 affects the FSK interface. When CB0 is high and CB1, CB2 are both low the MT88E45B is put into a power down state consuming minimal power supply current. See Tables 1 and 2.
9	DCLK	**3-wire FSK Interface Data Clock (Schmitt Input/CMOS Output).** In mode 0 (when the CB0 pin is logic low) this is a CMOS output which denotes the nominal mid-point of a FSK data bit. In mode 1 (when the CB0 pin is logic high) this is a Schmitt trigger input used to shift the FSK data byte out to the DATA pin.

Pin Description

Pin #	Name	Description
10	DATA	**3-wire FSK Interface Data (CMOS Output).** Mark frequency corresponds to logical 1. Space frequency corresponds to logical 0. In mode 0 (when the CB0 pin is logic low) the FSK serial bit stream is output to the DATA pin directly. In mode 1 (when the CB0 pin is logic high) the start bit is stripped off, the data byte and the trailing stop bit are stored in a 9 bit buffer. At the end of each word signalled by the $\overline{DR}/\overline{STD}$ pin, the microcontroller should shift the byte out onto the DATA pin by applying 8 read pulses to the DCLK pin. A 9th DCLK pulse will shift out the stop bit for framing error checking.
11	$\overline{DR}/\overline{STD}$	**3-wire FSK Interface Data Ready/CAS Detection Delayed Steering (CMOS Output).** Active low. When FSK demodulation is enabled via the CB1 and CB2 pins this pin is the Data Ready output. It denotes the end of a word. In both FSK interface modes 0 and 1, it is normally hi and goes low for half a bit time at the end of a word. But in mode 1 if DCLK starts during $\overline{DR}$ low, the first rising edge of the DCLK input will return $\overline{DR}$ to high. This feature allows an interrupt requested by a low going $\overline{DR}$ to be cleared upon reading the first DATA bit. When CAS detection is enabled via the CB1 and CB2 pins this pin is the Delayed Steering output. It goes low to indicate that a time qualified CAS has been detected.
12	EST	**CAS Detection Early Steering (CMOS Output).** Active high. This pin is the raw CAS detection output. It goes high to indicate the presence of a signal meeting the CAS accept frequencies and signal level. It is used in conjunction with the ST/GT pin and external components to time qualify the detection to determine whether the signal is a real CAS.
13	ST/GT	**CAS Detection Steering/Guard Time (CMOS Output/Analog Input).** It is used in conjunction with the EST pin and external components to time qualify the detection to determine whether the signal is a real CAS. A voltage greater than V_{TGt} at this pin causes the MT88E45B to indicate that a CAS has been detected by asserting the $\overline{DR}/\overline{STD}$ pin low. A voltage less than V_{TGt} frees up the MT88E45B to accept a new CAS and returns $\overline{DR}/\overline{STD}$ to high.
14	$\overline{CD}$	**Carrier Detect (CMOS Output).** Active low. A logic low indicates that an FSK signal is present. A time hysteresis is provided to allow for momentary signal discontinuity. The demodulated FSK data is ignored by the MT88E45B until carrier detect has been activated.
15	Vdd	Positive power supply.
16	CB1	**Control Bit 1 (CMOS Input).** Together with CB2 this pin selects the MT88E45B's functionality between FSK demodulation, Tip/Ring CAS detection and Hybrid CAS detection. When CB0 is high and CB1, CB2 are both low the MT88E45B is put into a power down state consuming minimal power supply current. See Tables 1 and 2.
17	CB2	**Control Bit 2 (CMOS Input).** Together with CB1 this pin selects the MT88E45B's functionality between FSK demodulation, Tip/Ring CAS detection and Hybrid CAS detection. When CB0 is high and CB1, CB2 are both low the MT88E45B is put into a power down state consuming minimal power supply current. See Tables 1 and 2.
18	GS2	**Hybrid Gain Select (Output).** This is the output of the hybrid receive connection op-amp. The op-amp should be used to connect the MT88E45B to the telephone hybrid or speech IC receive pair. The hybrid receive signal can be amplified or attenuated at GS2 via selection of the feedback resistor between GS2 and IN2-. When the CPE is off-hook CAS detection of the GS2 signal should be enabled via the CB1 and CB2 pins. See Tables 1 and 2.
19	IN2-	**Hybrid Op-amp Inverting (Input).**
20	IN2+	**Hybrid Op-amp Non-Inverting (Input).**

CB0	CB1	CB2	FSK Interface	Function
0/1	1	1	Set by CB0	FSK Demodulation. Tip/Ring input (GS1) selected. $\overline{DR}/\overline{STD}$ is $\overline{DR}$.
0/1	1	0	Set by CB0	Hybrid CAS Detection. Hybrid Receive input (GS2) selected. $\overline{DR}/\overline{STD}$ is $\overline{STD}$.
0/1	0	1	Set by CB0	Tip/Ring CAS Detection. Tip/Ring input (GS1) selected. $\overline{DR}/\overline{STD}$ is $\overline{STD}$. When the line is off-hook, a Bellcore/TIA Multiple Extension Interworking (MEI) compatible Type 2 CPE should be able to detect CAS from Tip/Ring while the CPE is on-hook because it may be the ACK sender. Tip/Ring CAS detection is also required for BT's on-hook CLIP.
1	0	0	Mode 1	Power Down. The MT88E45B is disabled and draws virtually no power supply current.
0	0	0	Mode 0	Reserved for factory testing.

Table 1 - CB0/1/2 Functionality

The number of control bits (CB) required to interface the MT88E45B with the microcontroller depends on the functionality of the application, as shown in Table 2.

Functionality Group	Controls	Description
FSK (mode 0 or 1) and Hybrid CAS only (Non MEI compatible)	CB2	CB0 is hardwired to Vdd or Vss to select the FSK interface. CB1 hardwired to Vdd. The microcontroller uses CB2 to select between the 2 functions.
FSK (mode 0 or 1), Hybrid CAS, Tip/Ring CAS (MEI compatible or BT on-hook CLIP)	CB1 CB2	CB0 is hardwired to Vdd or Vss to select the FSK interface. The microcontroller uses CB1 and CB2 to select between the 3 functions.
FSK (mode 1), Hybrid CAS, Tip/Ring CAS, Power Down (MEI compatible or BT on-hook CLIP)	CB1 CB2	CB0 is hardwired to Vdd to select FSK interface mode 1. The microcontroller uses CB1 and CB2 to select between the 4 functions.
FSK (mode 0), Hybrid CAS, Tip/Ring CAS, Power Down (MEI compatible or BT on-hook CLIP)	CB0 CB1 CB2	All 3 pins are required.

Table 2 - Control Bit Functionality Groups

Functional Overview

The MT88E45B is compatible with FSK and FSK plus CAS (CPE Alerting Signal) based Caller ID services around the world. Caller ID is the generic name for a group of services offered by telephone operating companies whereby information about the calling party is delivered to the subscriber. In Europe and some other countries Caller ID is known as Calling Line Identity Presentation (CLIP). ETSI calls CAS 'Dual Tone Alerting Signal' (DT-AS), BT calls it 'Tone Alert Signal'.

Depending on the service, data delivery can occur when the line is in the on-hook or off-hook state. In most countries the data is modulated in either Bell 202 or CCITT V.23 FSK format and transmitted at 1200 baud from the serving end office to the subscriber's terminal. Additionally in off-hook signalling, the special dual tone CAS is used

to alert the terminal before FSK data transmission. BT uses CAS to alert the terminal prior to FSK in both on-hook (Idle State) and off-hook (Loop State) signalling.

In North America, Caller ID uses the voiceband data transmission interface defined in the Bellcore document GR-30-CORE. The terminal or CPE (Customer Premises Equipment) requirements are defined in Bellcore document SR-TSV-002476. Typical services are CND (Calling Number Delivery), CNAM (Calling Name Delivery), VMWI (Visual Message Waiting Indicator) and CIDCW (Calling Identity Delivery on Call Waiting).

In Europe, Caller ID requirements are defined by ETSI. The CPE documents are ETS 300 778-1 for on-hook, ETS 300 778-2 for off-hook. The end office requirements are ETS 300 659-1 (on-hook) and ETS 300 659-2 (off-hook). ETSI has defined services such as CLIP and CLIP with Call Waiting which are similar to those of Bellcore. Some European countries produce their own national specifications. For example, in the UK BT's standards are SIN227 and SIN242, the UK CCA (Cable Communications Association) standard is TW/P&E/312.

In on-hook Caller ID, such as CND, CNAM and CLIP, the information is typically transmitted (in FSK) from the end office before the subscriber picks up the phone. There are various methods such as between the first and second rings (North America), between an abbreviated ring and the first true ring (Japan, France and Germany). On-hook Caller ID can also occur without ringing for services such as VMWI. In BT's on-hook CLIP, the signalling begins with a line polarity reversal, followed by CAS and then FSK. Bellcore calls an on-hook capable Caller ID CPE a 'Type 1 CPE'.

In off-hook Caller ID, such as CIDCW and CLIP with Call Waiting, information about a new calling party is sent to the subscriber who is already engaged in a call. Bellcore's method uses CAS to alert the CPE. When the CPE detects CAS and there are no off-hook extensions, the CPE should mute its transmission path and send an acknowledgment to the end office via a DTMF digit called ACK. Upon receiving ACK, the end office will send the FSK data. Bellcore calls an off-hook capable CPE a 'Type 2 CPE'. A Type 2 CPE is capable of off-hook and Type 1 functionalities and should ACK with a DTMF 'D'. The ETSI and BT off-hook signalling protocols are similar to Bellcore's but with timing and signal parametric differences. ETSI has no requirement for off-hook extension checking before ACK.

One factor affecting the quality of the CIDCW service is the CPE's CAS speech immunity. Although the end office has muted the far end party before and after it sends CAS, the near end (the end which is to receive the information) user may be still talking. Therefore the CPE must be able to detect CAS successfully in the presence of near end speech. This is called the talkdown immunity. The CPE must also be immune to imitation of CAS by speech from both ends of the connection because the CAS detector is continuously exposed to speech throughout the call. This is called the talkoff immunity.

If the CPE is a telephone, one way to achieve good CAS speech immunity is to put CAS detection on the telephone hybrid or speech IC receive pair instead of on Tip and Ring. Talkdown immunity improves because the near end speech has been attenuated while the CAS level is the same as on Tip/Ring, resulting in improved signal to speech ratio. Talkoff immunity is also improved because the near end speech has been attenuated.

In the Bellcore SR-TSV-002476 Issue 1 off-hook protocol, the CPE should not ACK if it detected an off-hook extension. The FSK will not be sent and the customer will not receive the Call Waiting ID. Bellcore, together with the TIA (Telecommunications Industry Association) TR41.3.1 working group, has defined a CPE capability called Multiple Extension Interworking (MEI) which overcomes this problem.

In the MEI scheme, all MEI compatible CPEs must be capable of detecting CAS when the line is off-hook, even though the CPE itself may be on-hook. This is because under some conditions an on-hook CPE may become the ACK sender. Another reason for the on-hook CPE to detect CAS is to maintain synchronous call logs between on and off-hook CPEs. When CAS is received and all off-hook CPEs are MEI compatible, one of the CPEs will ACK and all compatible CPEs will receive FSK.

A problem arises in a CPE where the CAS detector is connected only to the hybrid or speech IC receive pair: it cannot detect CAS when it is on-hook. The reason is that when the CPE is on-hook either the hybrid/speech IC is non functional or the signal level is severely attenuated. Therefore an on-hook Type 2 CPE must be capable of

detecting CAS from Tip/Ring, in addition to detecting CAS from the hybrid/speech IC receive signal when it is off-hook.

The MT88E45B offers an optimal solution which combines good speech immunity and MEI compatibility. Two input op-amps allow the MT88E45B to be connected both to Tip/Ring and to the hybrid/speech IC receive pair. Both connections can be differential or single ended. FSK demodulation is always on the Tip/Ring signal. CAS detection can be from the Tip/Ring or hybrid/speech IC receive signal. Being able to detect CAS on Tip/Ring also makes the MT88E45B suitable for BT on-hook CLIP applications.

For applications such as those in most European countries where Tip/Ring CAS detection is not needed, then the Tip/Ring and Hybrid op-amp gains can be tailored independently to meet country specific FSK and CAS signal level requirements respectively. Note that since the Hybrid op-amp is for CAS detection only, its gain can always be tailored specifically for the CAS signal level.

The FSK demodulator is compatible with Bellcore, ETSI and BT standards. The demodulated FSK data is either output directly (bit stream mode) or stored in a one byte buffer (buffer mode). In the buffer mode, the stop bit immediately following a byte is also stored and can be shifted out after the data byte. This facility allows for framing error checking required in Type 2 CPEs. In the bit stream mode, two timing signals are provided. One indicates the bit sampling instants of the data byte, the other the end of byte. A carrier detector indicates presence of signal and shuts off the data stream when there is no signal.

The entire chip can be put into a virtually zero current power down mode. The input op-amps, FSK demodulator, CAS detector and the oscillator are all shut off. Furthermore, power management has been incorporated to minimize operating current. When FSK is selected the CAS detector is powered down. When CAS is selected the FSK demodulator is powered down.

Functional Description

3 to 5 V Operation

The MT88E45B's FSK and CAS reject levels are proportional to Vdd. When operated at Vdd equal 3 V +/- 10%, to keep the FSK and CAS reject levels as at 5 V (nominal) the Tip/Ring and Hybrid op-amp gains should be reduced from those of 5 V. Gains for nominal Vdd (with a +/- 10% variation) other than 3 or 5 V can be chosen as interpolation between the 3 and 5 V settings.

Input Configuration

The MT88E45B provides an input arrangement comprised of two op-amps and a bias source (V_{REF}). V_{REF} is a low impedance voltage source which is used to bias the op-amp inputs at Vdd/2. The Tip/Ring op-amp (IN1+, IN1-, GS1 pins) is for connecting to Tip and Ring. The Hybrid op-amp (IN2+, IN2-, GS2 pins) is for connecting to the telephone hybrid or speech IC receive pair.

Either FSK or CAS detection can be selected for the Tip/Ring connection, while the hybrid connection is for CAS detection only. Phrased in another way, FSK demodulation is always on Tip/Ring, while CAS detection can be on Tip/Ring or Hybrid Receive. Tip/Ring CAS detection is required for MEI and BT on-hook CLIP, while Hybrid CAS detection is needed for optimal CAS speech immunity.

The feedback resistor connected between GS1 and IN1- can be used to adjust the Tip/Ring signal gain. The feedback resistor connected between GS2 and IN2- can be used to adjust the hybrid receive signal gain. When the Tip/Ring op-amp is selected, the GS2 signal is ignored. When the Hybrid op-amp is selected, the GS1 signal is ignored.

Either or both op-amps can be configured in the single ended input configuration shown in Figure 33, or in the differential input configuration shown in Figure 44.

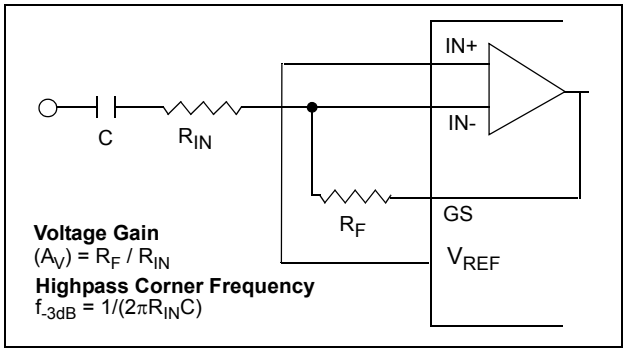


Figure 3 - Single Ended Input Configuration

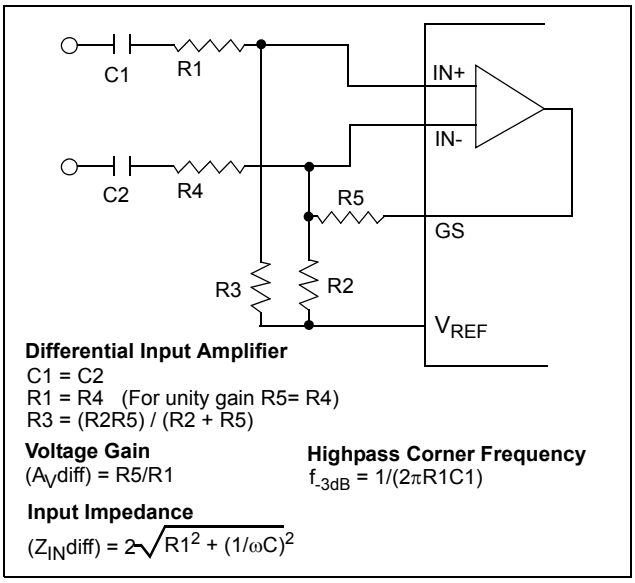


Figure 4 - Differential Input Configuration

CAS Detection

In North America, CAS is used in off-hook signalling only. In Europe (ETSI) it is used in off-hook signalling, and by BT in both on and off-hook signalling. ETSI calls it the Dual Tone Alerting Signal (DT-AS). Although the ETSI on-hook standard contains a DT-AS specification, BT is the only administration known to employ CAS in on-hook signalling. (BT calls it Tone Alert Signal.) The CAS/DT-AS characteristics are summarized in Table 3.

2130 Hz and 2750 Hz CAS/DT-AS Characteristics	Bellcore[a] (Off-hook only)	ETSI[b] (Off-hook)	BT[c] (Off-hook = 'Loop State') (On-hook = 'Idle State')
Frequency Tolerance	+/-0.5%	+/-0.5%	Off-hook: +/-0.6% On-hook: +/-1.1%
Signal Level (per tone)	-14 to -32 dBm[d]	-9.78 to -32.78 dBm (-12 to -35 dBV[e])	+0.22 to -37.78 dBm (-2 to -40 dBV)
Reject Level (per tone)	-45 dBm		On-hook: -43.78 dBm (-46 dBV)
Maximum Twist (V_{2130Hz}/V_{2750Hz})	+/-6 dB	+/-6 dB	+/-7 dB

2130 Hz and 2750 Hz CAS/DT-AS Characteristics	Bellcore[a] (Off-hook only)	ETSI[b] (Off-hook)	BT[c] (Off-hook = 'Loop State') (On-hook = 'Idle State')
Duration	75 to 85 ms	75 to 85 ms	Off-hook: 80 to 85 ms On-hook: 88 to 110 ms
Reject Duration			Off-hook: <=70 ms On-hook: <=20 ms
Signal to Noise Ratio	Speech	Speech	Off-hook: Speech On-hook: >= 20 dB (300-3400 Hz)
Hybrid Op-amp (GS2) Gain Vdd = 5V +/- 10%	0 to -5 dB	0 to -5 dB	0 dB
Hybrid Op-amp (GS2) Gain Vdd = 3V +/- 10%	-3.5 to -8.5 dB	-3.5 to -8.5 dB	-3.5 dB

a. SR-TSV-002476, Issue 1 Dec 1992
b. ETS 300 778-2 Jan 98. The DT-AS plus FSK variant of ETSI on-hook signalling described in ETS 300 778-1 is not supported because on-hook DT-AS uses the GS1 op-amp. With the GS1 gain in Table 4, the DT-AS minimum level will be below the MT88E45B's minimum accept level.
c. SIN227 Issue 3 Nov 97, SIN242 Issue 2 Nov 96
d. dBm - Decibels above or below a reference power of 1 mW into 600 ohms. 0 dBm = 0.7746 Vrms.
e. dBV - Decibels above or below a reference voltage of 1 Vrms. 0 dBV = 1 Vrms

Table 3 - CAS/DT-AS Characteristics

Table 3 shows the Hybrid op-amp (GS2) gain for operation at 3 V and 5 V nominal Vdd, with a ± 10% Vdd variation. For 3 V operation, the Hybrid op-amp gain should be reduced from the 5 V setting to maintain the CAS reject level and to maintain the talkoff immunity: the CAS threshold is directly proportional to Vdd, when Vdd is reduced the threshold becomes lower, hence lower level CAS are accepted. If the gain is not reduced, the MT88E45B will be more talkoff prone. In Table 3, the GS2 gain is shown as a range. By adopting the lower gain, talkoff immunity can be improved.

When CAS detection is selected, the dual purpose output pin $\overline{DR}/\overline{STD}$ is $\overline{STD}$. $\overline{STD}$ goes low when CAS has been detected, and returns high after CAS has ended.

CAS Guard Time

The guard time circuit shown in Figure 55 implements a timing algorithm which determines whether the signal is a CAS. Proper selection of the guard time(s) is key to good speech immunity. The first indication that there might be a CAS is when EST goes high. EST high indicates that both tones are present. EST low indicates that one or both tones is not present. $\overline{STD}$ low indicates that CAS has been detected. When $\overline{STD}$ returns high it indicates that CAS has ended.

The timing algorithm consists of 2 components: a tone present guard time (t_{GP}) and a tone absent guard time (t_{GA}). t_{GP} sets the minimum accept duration for CAS. That is, both tones must be detected continuously for t_{GP} for $\overline{STD}$ to go low to indicate that CAS has been detected. For $\overline{STD}$ to return high to indicate that CAS has ended, one or both tones must have disappeared for t_{GA}. The purpose of t_{GA} is to bridge over momentary EST dropouts once EST has met the minimum tone duration so as to decrease the likelihood of a long talkoff being broken up into several talkoffs. Usually t_{GA} is set very short or removed altogether because there is another way to deal with the problem (by ignoring further detections for 2 seconds after every detection).

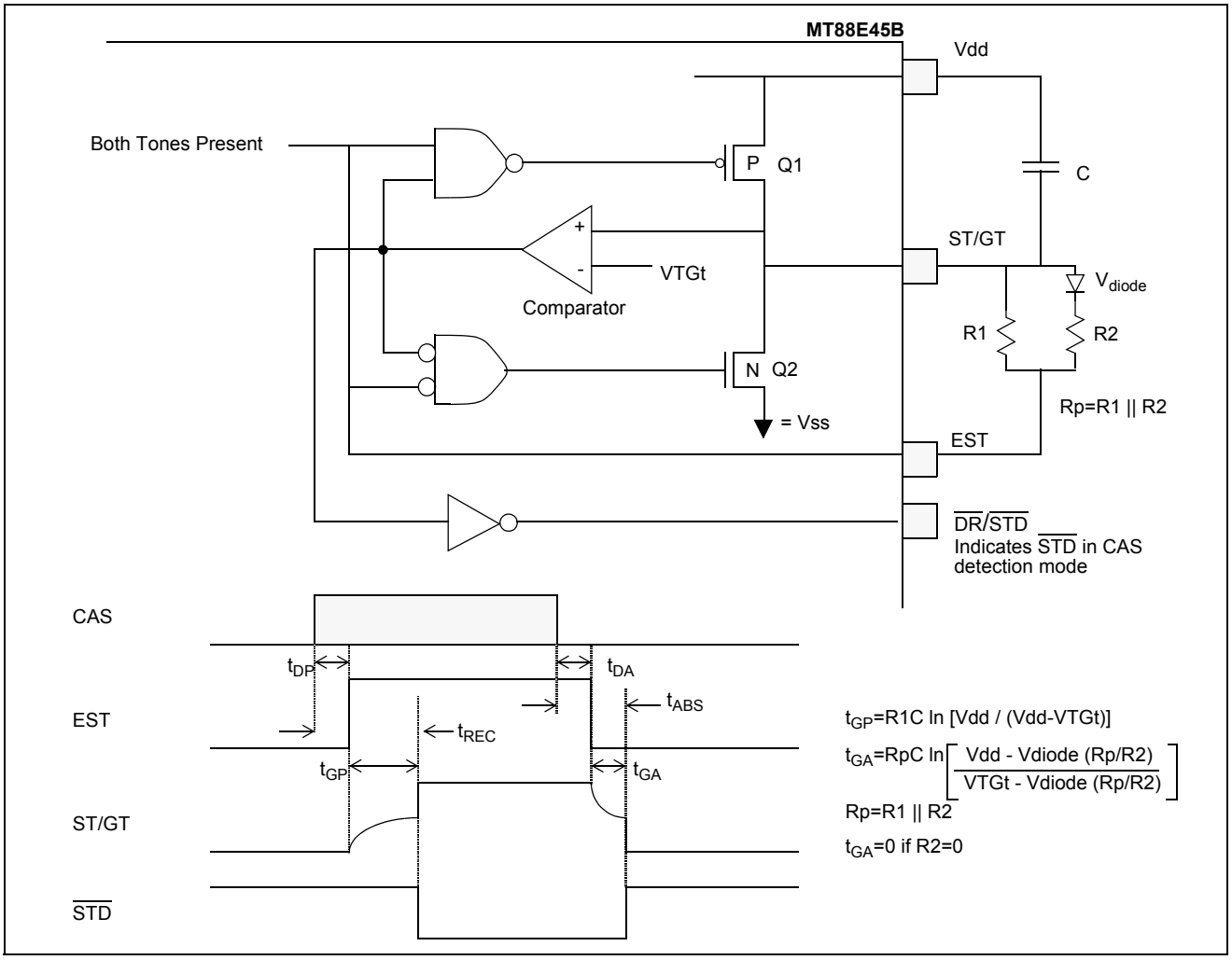


Figure 5 - CAS Guard Time Circuit Operation

Tone present guard time (t_{GP}) operation: In Figure 5 5 initially there is no CAS, EST is low so Q1 is off. C has been fully charged applying 0 V to ST/GT so Q2 is on. When both tones are detected EST goes high and turns off Q2. Because C has been fully charged (ST/GT=0V), the comparator output is low and Q1 stays off. With both Q1 and Q2 off the high at EST discharges C through R1 and the ST/GT voltage increases from 0 V. When the voltage exceeds the comparator threshold VTGt, which is typically 0.5 Vdd, the comparator output goes high; Q1 turns on and accelerates the discharge of C (ST/GT goes quickly to Vdd); $\overline{STD}$ goes low to indicate that a valid CAS has been received. If one or both tones disappeared before t_{GP} has been reached (i.e. when ST/GT voltage is still below VTGt), Q2 turns back on and charges C quickly to bring the ST/GT voltage back to 0 V. Then if EST goes high again the t_{GP} duration must start over.

Tone absent guard time (t_{GA}) operation: In Figure 5 5 initially both tones have been detected for t_{GP} so C is fully discharged and ST/GT is at Vdd. While both tones continue to be detected EST stays high; ST/GT is at Vdd (the comparator output is high); so Q1 is on and Q2 is off. When one or both tones stop EST goes low and turns off Q1. Because C is fully discharged (ST/GT=Vdd), the comparator output is high and Q2 stays off. With both Q1 and Q2 off the low at EST charges C through Rp=(R1 || R2) and the ST/GT voltage falls towards 0V. When the voltage has fallen below VTGt, the comparator output goes low. Since EST is also low Q2 turns on and accelerates the charging of C so that ST/GT goes quickly to 0V. $\overline{STD}$ goes high to indicate that the CAS has ended. If EST goes back to high before t_{GA} has been reached (i.e. when ST/GT voltage is still above V_{TGt}), Q1 turns back on and discharges C quickly to bring the ST/GT voltage back to Vdd. Then if EST goes low again the t_{GA} duration must start over. To set t_{GA}=0, set R2 to 0.

In Figure 55, t_{DP} is the delay from the start of CAS to EST responding, t_{DA} is the delay from the end of CAS to EST responding. The total delay from the start of CAS to STD responding is $t_{REC}=t_{DP}+t_{GP.}$ The total delay from the end of CAS to STD responding is $t_{ABS}=t_{DA}+t_{GA}$.

Parameter	North America: Bellcore[a]	Europe: ETSI[b]	UK: BT[c]
Mark (Logical 1) Frequency	1200 Hz +/- 1%	1300 Hz +/- 1.5%	
Space (Logical 0) Frequency	2200 Hz +/- 1%	2100 Hz +/- 1.5%	
Received Signal Level	-4.23 to -36.20 dBm (476 to 12 mVrms)[d]	-5.78 to -33.78 dBm[e] (-8 to -36 dBV)[f,g]	-5.78 to -37.78 dBm (-8 to -40 dBV)
Signal Reject Level	-48.24 dBm (3mVrms) for On-hook No Ring Signalling such as VMWI	On-hook only: -47.78 dBm (-50dBV)	
Transmission Rate	1200 baud +/- 1%	1200 baud +/- 1%	
Twist (V_{MARK}/V_{SPACE})	-6 to +10 dB	-6 to +6 dB	
Signal to Noise Ratio	Single Tone (f): -18 dB (f<=60Hz) -12 dB (60<f<=120Hz) -6 dB (120<f<=200Hz) +25 dB (200<f<3200Hz) +6 dB (f>=3200Hz)	>= 25 dB (300 to 3400 Hz)	>= 20 dB (300 to 3400 Hz)
Tip/Ring Op-Amp (GS1) Gain Vdd = 5V +/- 10%	0 dB	-2 dB[h]	0 dB
Tip/Ring Op-Amp (GS1) Gain Vdd = 3V +/- 10%	-3.5 dB	-5.5 dB[i]	-3.5 dB

a. ANSI/TIA/EIA-716 and TIA/EIA-777. Bellcore has agreed to the values and will synchronize its requirements.
b. ETS 300 778-1 (On-hook) Sep 97, ETS 300 778-2 (Off-hook) Jan 98.
c. SIN 227 Issue 3 Nov 97, SIN242 Issue 2 Nov 96.
d. North American on-hook signalling range. The off-hook range is inside the on-hook range: 190mVrms to 12mVrms.
e. dBm - Decibels above or below a reference power of 1 mW into 600 ohms. 0 dBm = 0.7746 Vrms
f. dBV - Decibels above or below a reference voltage of 1 Vrms. 0 dBV = 1 Vrms.
g. ETSI on-hook signalling range. The off-Hook signalling levels are inside this range: -8.78 to -30.78 dBm (-11 to -33 dBV).
h. The 5V ETSI Tip/Ring op-amp gain can be 0 dB if there is no FSK reject level requirement.
i. The 3V ETSI Tip/Ring op-amp gain can be -3.5dB if there is no FSK reject level requirement.

Table 4 - FSK Signal Characteristics

FSK Demodulation

The FSK characteristics are shown in Table 4. In North America, TIA (Telecommunications Industry Association) also sets standards. The Type 1 Caller ID CPE standard is ANSI/TIA/EIA-716. The Type 2 standard is TIA/EIA-777. The North American FSK characteristics in Table 4 are from ANSI/TIA/EIA-716. They differ from those Bellcore published in SR-TSV-002476 and SR-3004. Bellcore is represented in TR41.3.1 and will synchronize to the TIA requirements in its future documents.

The TIA Type 1 standard includes an FSK reject level:

- if data is not preceded by ringing (e.g., VMWI), FSK signals below 3mVrms (-48.24 dBm) shall be rejected
- if data is preceded by ringing, FSK detection may be extended below 3mVrms

The MT88E45B is compliant with the Bellcore/TIA, ETSI and BT requirements with the Tip/Ring op-amp gains in Table 4. In Europe if the country specific FSK requirements do not incorporate ETSI's FSK reject level then the Tip/Ring op-amp gain can also be 0 dB at 5 V and -3.5 dB at 3 V to meet the ETSI minimum CAS level for on-hook signalling (-40 dBV).

For 3 V operation, the FSK receiver becomes more sensitive and lower level signals will be accepted than at 5 V. To maintain the FSK reject level, the Tip/Ring input op-amp gain should be reduced. Note that since the Tip/Ring op-amp is also used for Tip/Ring CAS detection, the CAS level will also be reduced for on-hook detection.

FSK Data Interface

The MT88E45B provides a powerful dual mode 3-wire interface so that the data bytes in the demodulated FSK bit stream can be extracted without the need either for an external UART or for the CPE's microcontroller to perform the function in software. The interface is specifically designed for the 1200 baud rate and is consisted of 3 pins: DATA, DCLK (Data Clock) and DR (Data Ready). DR/STD is a dual purpose output pin. When FSK is selected it is DR.

Two modes (modes 0 and 1) are selectable via the CB0 pin. In mode 0, the FSK bit stream is output directly. In mode 1, the data byte and the trailing stop bit are stored in a 9 bit buffer. If mode 1 is desired, the CB0 pin can be hardwired to Vdd. If mode 0 is desired and full chip power down is not required, the CB0 pin can be hardwired to Vss.

In Bellcore's off-hook protocol, a Type 2 CPE should restore the voicepath within 50 ms after the end of the FSK signal. Due to noise, end of carrier detection is not always reliable. The TIA Type 2 standard stipulates that the CPE must detect the end of FSK when any one of the following occurs:

- absence of carrier signal or,
- more than five framing errors (trailing stop bit a 0 instead of a 1) have been detected in the FSK message or,
- more than 150 ms of continuous mark signal or space signal has been detected.

Mode 0 - Bit Stream Mode

This mode is selected when the CB0 pin is low. In this mode the FSK data is output directly to the DATA pin. DCLK and DR pins are timing signal outputs (see Figure 13.

For each received stop and start bit sequence, the MT88E45B outputs a fixed frequency clock string of 8 pulses at the DCLK pin. Each DCLK rising edge occurs in the middle of a DATA bit cell. DCLK is not generated for the start and stop bits. Consequently, DCLK will clock only valid data into a peripheral device such as a serial to parallel shift register or a microcontroller. The MT88E45B also outputs an end of word pulse (Data Ready) at the DR pin. DR goes low for half a nominal bit time at the beginning of the trailing stop bit. It can be used to interrupt a microcontroller or cause a serial to parallel converter to parallel load its data into the microcontroller. Since the DR rising edge occurs in the middle of the stop bit, it can also be used to read the stop bit to check for framing error.

Alternatively, DCLK and DATA may occupy 2 bits of a microcontroller's input port. The microcontroller polls the input port and saves the DATA bit whenever DCLK changes from low to high. When DR goes low, the word may then be assembled from the last 8 saved bits.

DATA may also be connected to a personal computer's serial communication port after conversion from CMOS to RS-232 voltage levels.

Mode 1 - Buffer Mode

This mode is selected when the CB0 pin is high. In this mode the received byte is stored on chip. At the end of a byte DR goes low to indicate that a new byte has become available. The microcontroller applies DCLK pulses to read the register contents serially out of the DATA pin (see Figure 1414).

Internal to the MT88E45B, the start bit is stripped off, the data bits and the trailing stop bit are sampled and stored. Midway through the stop bit, the 8 data bits and the stop bit are parallel loaded into a 9 bit shift register and DR goes low. The register's contents are shifted out to the DATA pin on the supplied DCLK's rising edges in the order they were received. The last bit must be shifted out and DCLK returned to low before the next DR. DCLK must be low for t_{DDS} before DR goes low and must remain low for t_{DDH} after DR has gone low (see Figure 14).

If DCLK begins while $\overline{DR}$ is low, $\overline{DR}$ will return to high upon the first DCLK rising edge. If $\overline{DR}$ interrupts a microcontroller then this feature allows the interrupt to be cleared by the first read pulse. Otherwise $\overline{DR}$ is low for half a nominal bit time (1/2400 sec).

Reading the stop bit allows the software to check for framing errors. When framing error is not checked the microcontroller only needs to send 8 DCLK pulses to shift the data byte out.

Carrier Detect

The carrier detector provides an indication of the presence of a signal in the FSK frequency band. It detects the presence of a signal of sufficient amplitude at the output of the FSK bandpass filter. The signal is qualified by a frequency aware digital algorithm before the $\overline{CD}$ output is set low to indicate carrier detection. A 10 ms hysteresis is provided to allow for momentary signal dropout once $\overline{CD}$ has been activated. $\overline{CD}$ is released when there is no activity at the FSK bandpass filter output for 10 ms.

When $\overline{CD}$ is inactive (high), the raw output of the FSK demodulator is ignored by the internal data timing recovery circuit. In mode 0 the DATA, DCLK and $\overline{DR}$ pins are forced high. In mode 1 the output shift register is not updated and $\overline{DR}$ is high; if DCLK is clocked, DATA is undefined.

Note that signals such as speech, CAS and DTMF tones also lie in the FSK frequency band and the carrier detector may be activated by these signals. They will be demodulated and presented as data. To avoid the false data, the MT88E45B should be put into CAS or power down mode when FSK is not expected. Ringing, on the other hand, does not pose a problem as it is ignored by the carrier detector.

Interrupt

The $\overline{DR}/\overline{STD}$ output can be used to interrupt a microcontroller. When the MT88E45B is the only interrupt source, $\overline{DR}/\overline{STD}$ can be connected directly to the microcontroller's interrupt input. Figure 9 shows the necessary connections when the MT88E45B is one of many interrupt sources. The diodes and resistors implement a wired-or so that the microcontroller is interrupted (INT low active or falling edge triggered) when one or more of INT1, INT2 or $\overline{DR}/\overline{STD}$ is low. The microcontroller can determine which one of $\overline{DR}/\overline{STD}$, INT1 or INT2 caused the interrupt by reading them into an input port.

When system power is first applied and CB0/1/2 have already been configured to select CAS detection, $\overline{DR}/\overline{STD}$ will power up as logic low. This is because there is no charge across the ST/GT capacitor in Figure 55, hence ST/GT is at Vdd which causes $\overline{STD}$ to be low. If $\overline{DR}/\overline{STD}$ is used to interrupt a microcontroller the interrupt will not clear until the capacitor has charged up. Therefore upon initial power up the microcontroller should ignore this interrupt source until there is sufficient time to charge the capacitor. Alternatively, the MT88E45B can be put into power down mode: $\overline{DR}/\overline{STD}$ goes high and clears the interrupt, ST/GT goes low and the capacitor will charge up quickly.

Power Down

The MT88E45B can be powered down to consume virtually no power supply current via a state of the CB0/1/2 pins. Momentary transition of CB0/1/2 into the power down code will not activate power down.

In power down mode both input op-amps, V_{REF} and the oscillator are non functional. DCLK becomes an input because to select the power down state CB0 is 1 which will select FSK interface mode 1. If the application uses FSK interface mode 0 and the MT88E45B needs to be powered down then a pull down resistor should be added at the DCLK pin to define its state during power down (R15 in Figure 7). When the MT88E45B is powered down DATA, $\overline{DR}/\overline{STD}$, $\overline{CD}$ are high; EST and ST/GT are low.

To reduce the operating current an Intelligent Power Down feature has been incorporated. When FSK is selected, the CAS detector is powered down. When CAS is selected the FSK demodulator is powered down. The two input op-amps are not affected and both will remain operational.

Oscillator

The MT88E45B requires a 3.579545 MHz crystal or ceramic resonator to generate its oscillator clock. To meet the CAS detection frequency tolerance specifications the crystal or resonator must have a 0.1% frequency tolerance. The crystal specification is as follows: (e.g., CTS MP036S)

Frequency:	3.579545 MHz
Frequency Tolerance:	± 0.1% (over temperature range of the application)
Resonance Mode:	Parallel
Load Capacitance:	18 pF
Maximum Series Resistance:	150 Ω
Maximum Drive Level:	2 mW

Alternatively an external clock source can be used. In which case the OSC1 pin should be driven directly from a CMOS buffer and the OSC2 pin left open.

For 5V+/-10% applications any number of MT88E45B's can be connected as shown in Figure 6 6 so that only one crystal is required.

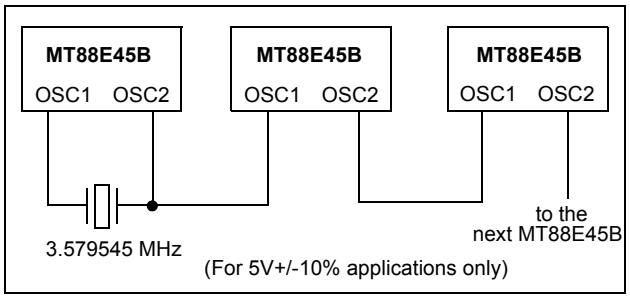
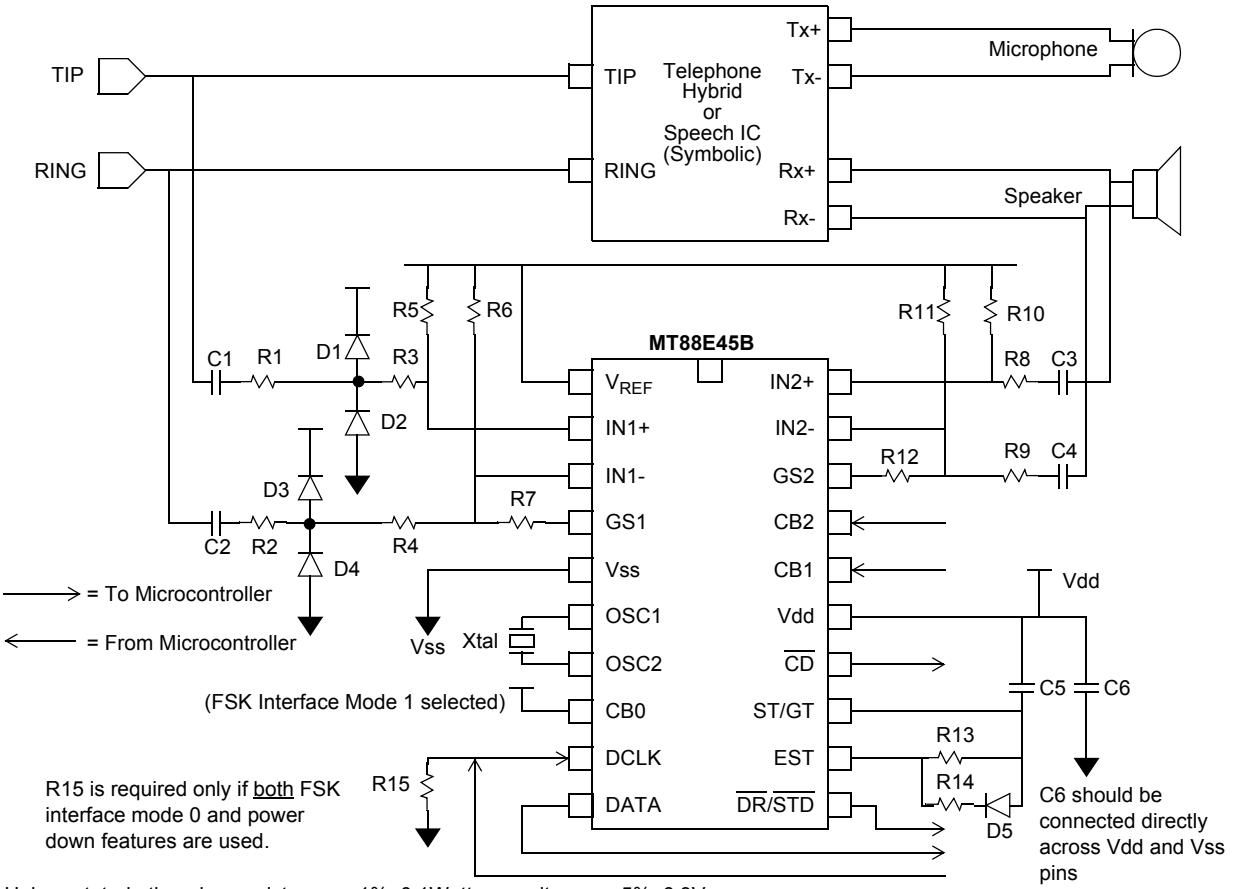


Figure 6 - Common Crystal Connection

Application Circuits



Unless stated otherwise, resistors are 1%, 0.1Watt; capacitors are 5%, 6.3V.

For 1000Vrms, 60Hz isolation from Tip to Earth and Ring to Earth:

R1,R2	430K, 0.5W, 5%, 475V min. (e.g. IRC type GS-3)	C1,C2	2n2, 1332V min.

If the 1000Vrms is handled by other methods then this circuit has to meet the FCC Part 68 Type B Ringer requirements:

R1,R2	432K, 0.1W, 1%, 56V min.	C1,C2	2n2, 212V min.

Common to both sets of R1,R2:

					5V, 0dB gain	3V, -3.5dB gain
R3,R4	34K	C3,C4	2n2	R5,R10	53K6	35K7
R8,R9	464K	C5	100n	R6,R11	60K4	40K2
R13	825K	C6	100n, 20%	R7,R12	464K	309K
R14	226K or 26K1	D1-D4	Diodes. 1N4148 or equivalent			
R15	100K, 20%	D5	Diode. 1N4148 or equivalent			
		Xtal	3.579545MHz, 0.1% crystal or ceramic resonator			

Figure 7 - Application Circuit: Bellcore MEI Compatible Type 2 Telephone

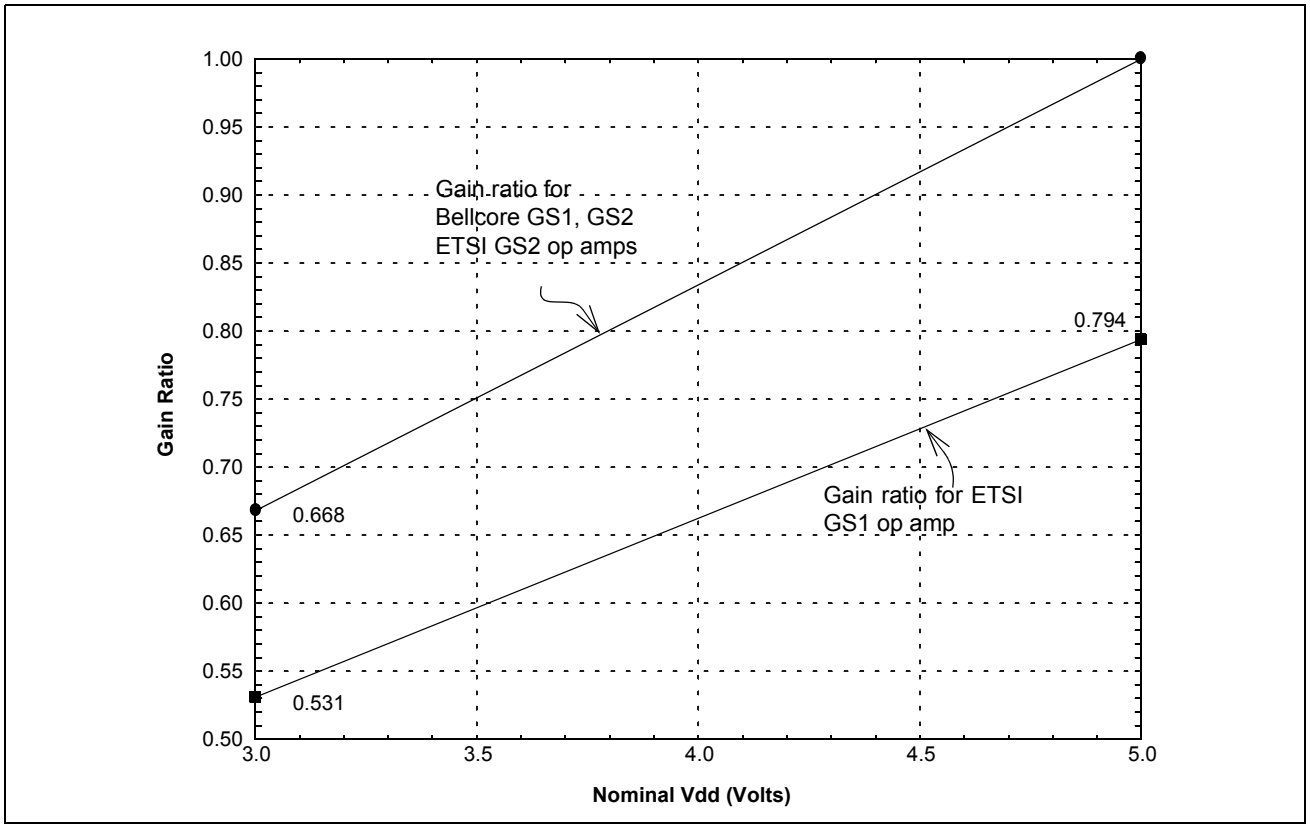


Figure 8 - Gain Ratio as a Function of Nominal Vdd

Gain Setting Resistor Calculation Example for Figure 8:

- For the desired nominal Vdd, use Figure 8 to determine approximate A_v.
- For the GS1 op-amp, start with the 0 dB gain setting resistor values of $R5_{0dB}$, $R6_{0dB}$ and $R7_{0dB}$. In Figure 7 these values are 53K7, 60K4 and 464 K respectively. Keep C1,C2,R1,R2,R3,R4 as in Figure 7 to maintain the highpass corner frequency constant for all gain settings.
- For the desired gain setting of A_v:

$R7_{Av} = R7_{0dB} \times A_V$	Scaled for desired gain. Choose the closest standard resistor value as $R7_{Av}$. Actual A_v from now on is $R7_{Av}/R7_{0db}$
$R5_{Av} = R5_{0dB} \times A_V$	Scaled for good common mode range. Choose the closest standard resistor value as $R5_{Av}$.
$1/R6_{Av} = 1/R5_{Av} - 1/R7_{Av}$	Calculate $R6_{Av}$ so that $R5_{Av}=R6_{Av} \parallel R7_{Av}$. Choose the closest standard resistor value as $R6_{Av}$.

- Repeat for R_{10}, R_{11}, R_{12} for the GS2 op-amp.

Example:

- For a gain of -3.5 dB, $A_V=10^{-3.5/20}$ = 0.668
- $R7_{-3.5dB}$= 464 K x 0.668 = 309K9, the closest standard resistor value is 309 K.
  A_V is now 309 K/464 K = 0.666
- $R5_{-3.5dB}$= 53K6 x 0.666 = 35K7, the closest standard resistor value is 35K7.
  Therefore $R6_{-3.5dB}$ is calculated to be 40K4, the closest standard resistor value is 40K2.

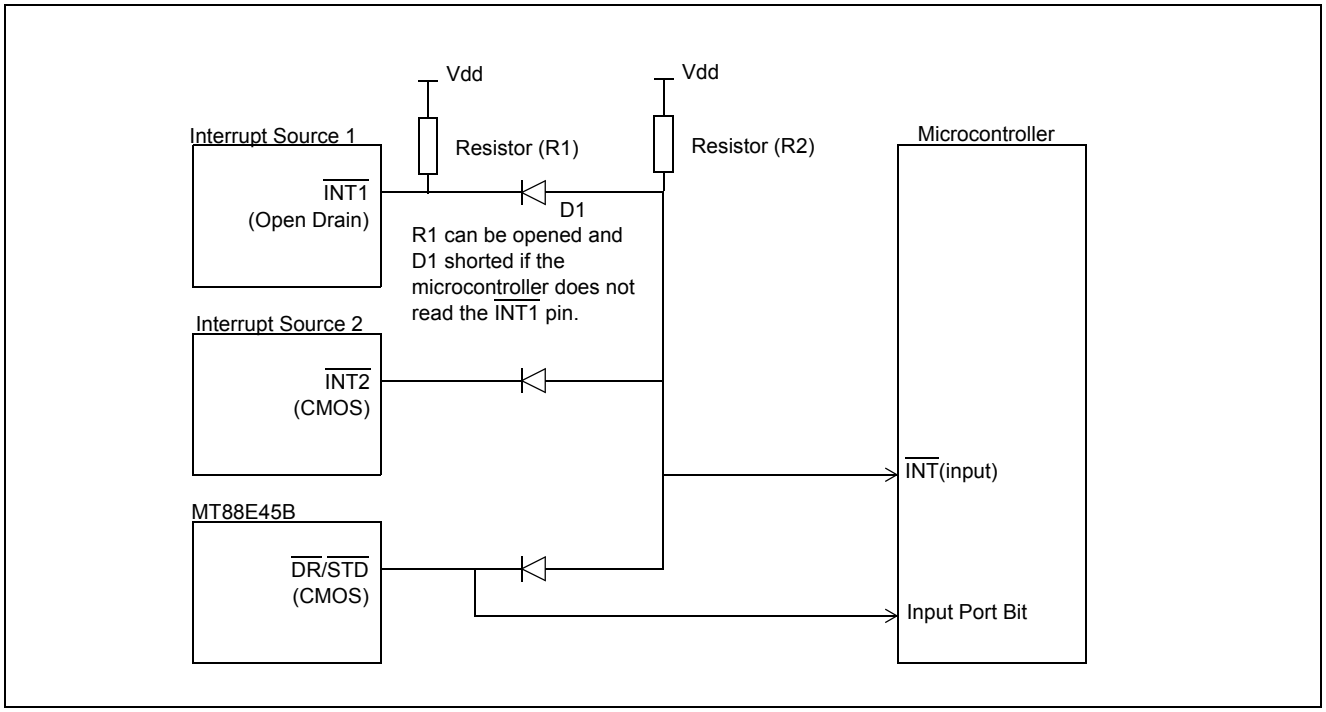


Figure 9 - Application Circuit: Multiple Interrupt Source

Absolute Maximum Ratings* - Voltages are with respect to V_{SS} unless otherwise stated

	Parameter	Symbol	Min.	Max.	Units
1	Supply voltage with respect to V_{ss}	V_{DD}	-0.3	6	V
2	Voltage on any pin other than supplies **	V_{PIN}	V_{ss}-0.3	V_{DD}+0.3	V
3	Current at any pin other than supplies	I_{PIN}		10	mA
4	Storage Temperature	T_{ST}	-65	150	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

** Under normal operating conditions voltage on any pin except supplies can be minimum V_{SS}-1V to maximum V_{DD}+1V for an input current limited to less than 200 μA

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units
1	Power Supplies	V_{DD}	2.7		5.5	V
2	Clock Frequency	f_{OSC}		3.579545		MHz
3	Tolerance on Clock Frequency	Δf_{OSC}	-0.1		+0.1	%
4	Operating Temperature	T_{OP}	-40		85	°C

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics†

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	SUPPLY	Standby Supply Current	I_{DDQ}		0.1	15	μA	All inputs are V_{DD}/V_{SS} except for oscillator pins. No analog input. outputs unloaded. CB0/1/2 = 1/0/0
2		Operating Supply Current V_{DD} = 5V ±10% V_{DD} = 3V ±10%	I_{DD}		 2.8 1.5	 8 4.5	 mA mA	All inputs are V_{DD}/V_{SS} except for oscillator pins. No analog input. outputs unloaded.
3		Power Consumption	PO			44	mW	
4	DCLK	Schmitt Input High Threshold	V_{T+}	0.44*V_{DD}		0.64*V_{DD}	V	
		Schmitt Input Low Threshold	V_{T-}	0.27*V_{DD}		0.47*V_{DD}	V	
5		Schmitt Hysteresis	V_{HYS}	0.2			V	
6	CB0 CB1 CB2	CMOS Input High Voltage	V_{IH}	0.7*V_{DD}		V_{DD}	V	
		CMOS Input Low Voltage	V_{IL}	V_{SS}		0.3*V_{DD}	V	
7	DCLK DATA $\overline{DR}$/STD $\overline{CD}$, EST ST/GT	Output High Source Current	I_{OH}	0.8			mA	V_{OH}=0.9*V_{DD}

DC Electrical Characteristics† (continued)

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
8	DCLK DATA $\overline{DR}$/STD $\overline{CD}$, EST ST/GT	Output Low Sink Current	I_{OL}	2			mA	V_{OL}=0.1*V_{DD}
9	IN1+ IN1- IN2+ IN2-	Input Current	Iin1			1	µA	V_{in}=V_{DD} to V_{SS}
	DCLK CB0 CB1 CB2		Iin2			10	µA	V_{in}=V_{DD} to V_{SS}
10	ST/GT	Output High-Impedance Current	Ioz1			5	µA	V_{out} =V_{DD} to V_{SS}
11	V_{REF}	Output Voltage	V_{REF}	0.5V_{DD} -0.1		0.5V_{DD}+0.1	V	No Load
12		Output Resistance	R_{REF}			2	kΩ	
13	ST/GT	Comparator Threshold Voltage	V_{TGt}	0.5V_{DD}-0.05		0.5V_{DD}+0.05	V	

† DC Electrical Characteristics are over recommended operating conditions, unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - CAS Detection

	Characteristic	Sym.	Min.	Typ.‡	Max.	Unit	Notes*
1	Lower Tone Frequency	f_L		2130		Hz	
2	Upper Tone Frequency	f_H		2750		Hz	
3	Frequency Deviation: Accept		1.1%				range within which tones are accepted
4	Frequency Deviation: Reject		3.5%				range outside of which tones are rejected
5	Accept Signal Level (per tone)		-40 -37.78		-2 0.22	dBV dBm	1, 5, 6
6	Reject Signal Level (per tone) Vdd=5V +/-10% only				-46 -43.78	dBV dBm	2, 5, 6
7	Reject Signal Level (per tone) Vdd=3V+/-10% or 5V+/-10%				-47.22 -45	dBV dBm	1, 5, 6
8	Twist: 20 log (V_{2130Hz}/V_{2750Hz})		-7		+7	dB	
9	Signal to Noise Ratio	SNR_{CAS}	20			dB	3,4

† AC Electrical Characteristics are over recommended operating conditions, unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing
*Notes:
1. Tip/Ring signal level. Input op-amp configured to 0dB gain at Vdd=5V+/-10%, -3.5dB at Vdd=3V+/-10%.
2. Tip/Ring signal level. Input op-amp configured to 0dB gain at Vdd=5V+/-10%.
3. Both tones have the same amplitude.
4. Band limited random noise 300-3400Hz. Measurement valid only when tone is present.
5. dBV - Decibels above or below a reference voltage of 1 Vrms. 0 dBV = 1 Vrms. Signal level is per tone.
6. dBm - Decibels above or below a reference power of 1 mW into 600 ohms. 0 dBm = 0.7746 Vrms. Signal level is per tone.

AC Electrical Characteristics† - FSK Demodulation

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes*
1	Accept Signal Level Range		-40 -37.78 10.0		-6.45 -4.23 476	dBV dBm mVrms	1, 2, 4, 5
2	Bell 202 Format Reject Signal Level				-48.24 -50.46 3	dBm dBV mVrms	1, 2, 4, 5
3	Transmission Rate		1188	1200	1212	baud	
4	Mark and Space Frequencies Bell 202 1 (Mark) Bell 202 0 (Space) CCITT V.23 1 (Mark) CCITT V.23 0 (Space)		 1188 2178 1280.5 2068.5	 1200 2200 1300 2100	 1212 2222 1319.5 2131.5	 Hz Hz Hz Hz	
5	Twist: 20 log (V_{MARK}/V_{SPACE})		-6		+10	dB	
6	Signal to Noise Ratio	SNR_{FSK}	20			dB	1,3

† AC Electrical Characteristics are over recommended operating conditions, unless otherwise stated.
‡ Typical figures are nominal values and are for design aid only: not guaranteed and not subject to production testing.
*Notes:
1. Both mark and space have the same amplitude.
2. Tip/Ring signal level. Input op-amp configured to 0dB gain at Vdd=5V+/-10%, -3.5dB at Vdd=3V+/-10%.
3. Band limited random noise (200-3400Hz). Present when FSK signal is present. Note that the BT band is 300-3400Hz, the Bellcore band is 0-4kHz.
4. dBV - Decibels above or below a reference voltage of 1 Vrms. 0 dBV = 1 Vrms.
5. dBm - Decibels above or below a reference power of 1 mW into 600 ohms. 0 dBm = 0.7746 Vrms.

Electrical Characteristics† - Gain Setting Amplifiers

	Characteristics	Sym.	Min.	Max.	Units	Test Conditions
1	Input Leakage Current	I_{IN}		1	µA	$V_{SS} \le V_{IN} \le V_{DD}$
2	Input Resistance	R_{in}	10		MΩ	
3	Input Offset Voltage	V_{OS}		25	mV	
4	Power Supply Rejection Ratio	PSRR	30		dB	1kHz ripple on V_{DD}
5	Common Mode Rejection Ratio	CMRR	40		dB	$V_{CMmin} \le V_{IN} \le V_{CMmax}$
6	DC Open Loop Voltage Gain	A_{VOL}	40		dB	
7	Unity Gain Bandwidth	f_C	0.3		MHz	
8	Output Voltage Swing	V_O	0.5	V_{DD}-0.5	V	Load ≥ 100kΩ
9	Capacitive Load (GS1,GS2)	C_L		50	pF	
10	Resistive Load (GS1,GS2)	R_L	100		kΩ	
11	Common Mode Range Voltage	V_{CM}	1.0	V_{DD}-1.0	V	

† Electrical characteristics are over recommended operating conditions, unless otherwise stated.

AC Electrical Characteristics† - CAS Detection Timing

	Characteristics	Sym.	Min.	Max.	Units	Notes
1	Tone present detect time	t_{DP}	0.5	10	ms	See Figures16 16, 1717
2	Tone absent detect time	t_{DA}	0.1	8	ms	See Figures16 16, 1717

† AC Electrical Characteristics are over recommended operating conditions unless otherwise stated.

AC Electrical Characteristics† - Oscillator and Carrier Detect Timing

		Characteristics	Sym.	Min.	Max.	Units	Notes
1	OSC2	Power-up time	t_{PU}		50	ms	
2		Power-down time	t_{PD}		10	ms	
3	$\overline{CD}$	Input FSK to $\overline{CD}$ low delay	t_{CP}		25	ms	
4		Input FSK to $\overline{CD}$ high delay	t_{CA}	10		ms	
5		Hysteresis		10		ms	

† AC Electrical Characteristics are over recommended operating conditions unless otherwise stated.

AC Electrical Characteristics† - 3-Wire FSK Data Interface Timing (Mode 0)

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes*
1	$\overline{DR}/\overline{STD}$	Rise time	t_{RR}			200	ns	into 50 pF Load
2		Fall time	t_{RF}			200	ns	into 50 pF Load
3		Low time	t_{RL}	415	416	417	µs	2
4	DATA	Rate		1188	1200	1212	baud	1
5		Input FSK to DATA delay	t_{IDD}		1	5	ms	
6	DATA DCLK	Rise time	t_R			200	ns	into 50 pF Load
7		Fall time	t_F			200	ns	into 50 pF Load
8		DATA to DCLK delay	t_{DCD}	6	416		µs	1, 2, 3
9		DCLK to DATA delay	t_{CDD}	6	416		µs	1, 2, 3
10	DCLK	Frequency	f_{DCLK0}	1201.6	1202.8	1204	Hz	2
11		High time	t_{CH}	415	416	417	µs	2
12		Low time	t_{CL}	415	416	417	µs	2
13	DCLK / $\overline{DR}/\overline{STD}$	DCLK to $\overline{DR}$ delay	t_{CRD}	415	416	417	µs	2

† AC Electrical Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
*Notes:
1. FSK input data at 1200 ±12 baud.
2. OSC1 at 3.579545 MHz ±0.1%.
3. Function of signal condition.

AC Electrical Characteristics† - 3-Wire FSK Data Interface Timing (Mode 1)

		Characteristics	Sym.	Min.	Max.	Units	Notes
1	DCLK	Frequency	f_{DCLK1}		1	MHz	
2		Duty cycle		30	70	%	
3		Rise time	t_{R1}		100	ns	
4	DCLK / $\overline{DR}$/STD	DCLK low set up before $\overline{DR}$	t_{DDS}	500		ns	
5		DCLK low hold time after $\overline{DR}$	t_{DDH}	500		ns	

† AC Electrical Characteristics are over recommended operating conditions unless otherwise stated.

AC Electrical Characteristics - Timing Parameter Measurement Voltage Levels

	Characteristics	Sym.	Level	Units	Notes
1	CMOS Threshold Voltage	V_{CT}	$0.5*V_{DD}$	V	
2	Rise/Fall Threshold Voltage High	V_{HM}	$0.7*V_{DD}$	V	
3	Rise/Fall Threshold Voltage Low	V_{LM}	$0.3*V_{DD}$	V	

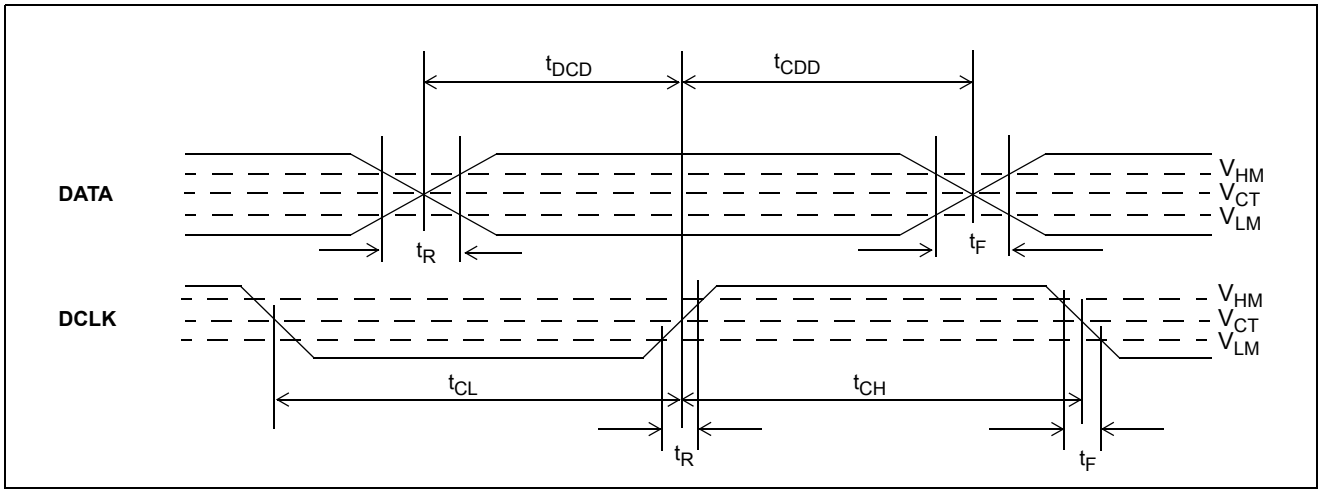


Figure 10 - DATA and DCLK Mode 0 Output Timing

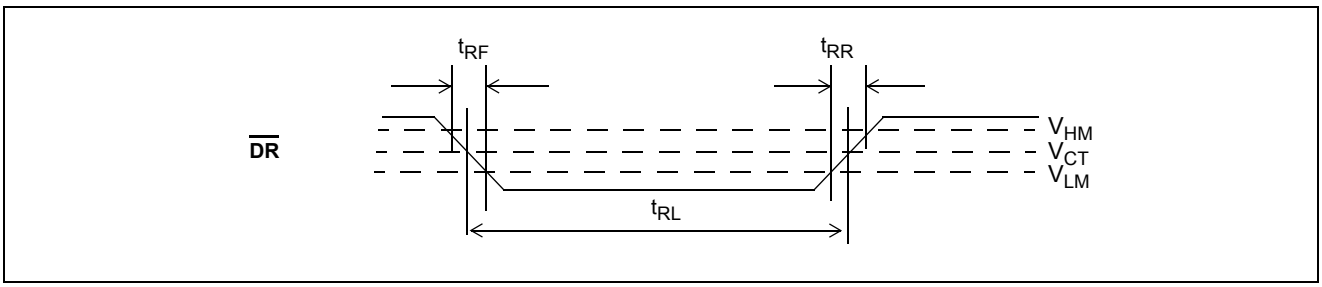


Figure 11 - $\overline{DR}$ Output Timing

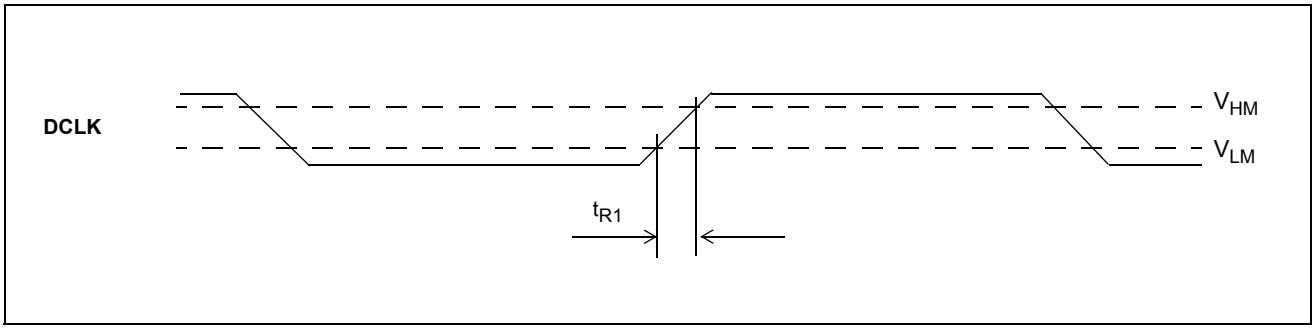


Figure 12 - DCLK Mode 1 Input Timing

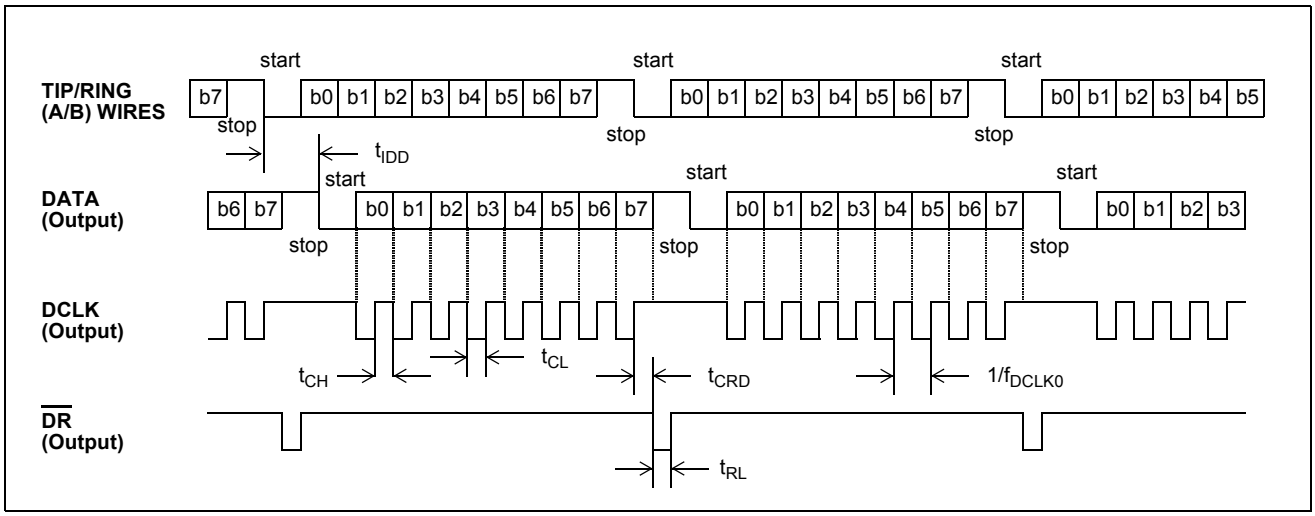
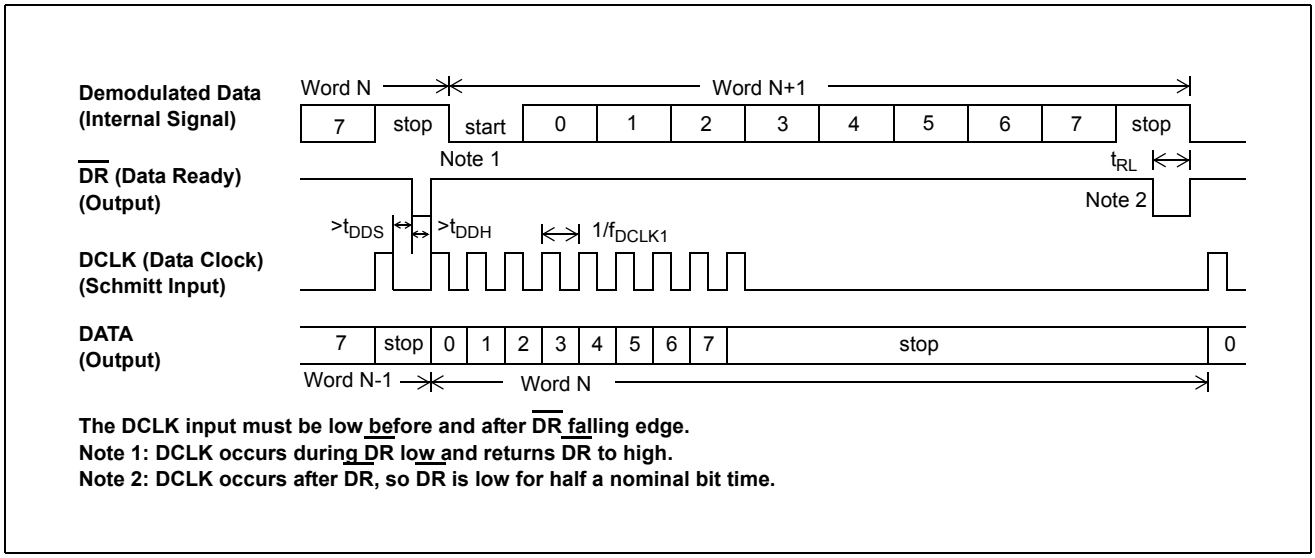


Figure 13 - 3-Wire FSK Data Interface Timing (Mode 0)



The DCLK input must be low before and after DR falling edge.
Note 1: DCLK occurs during DR low and returns DR to high.
Note 2: DCLK occurs after DR, so DR is low for half a nominal bit time.

Figure 14 - 3-Wire FSK Data Interface Timing (Mode 1)

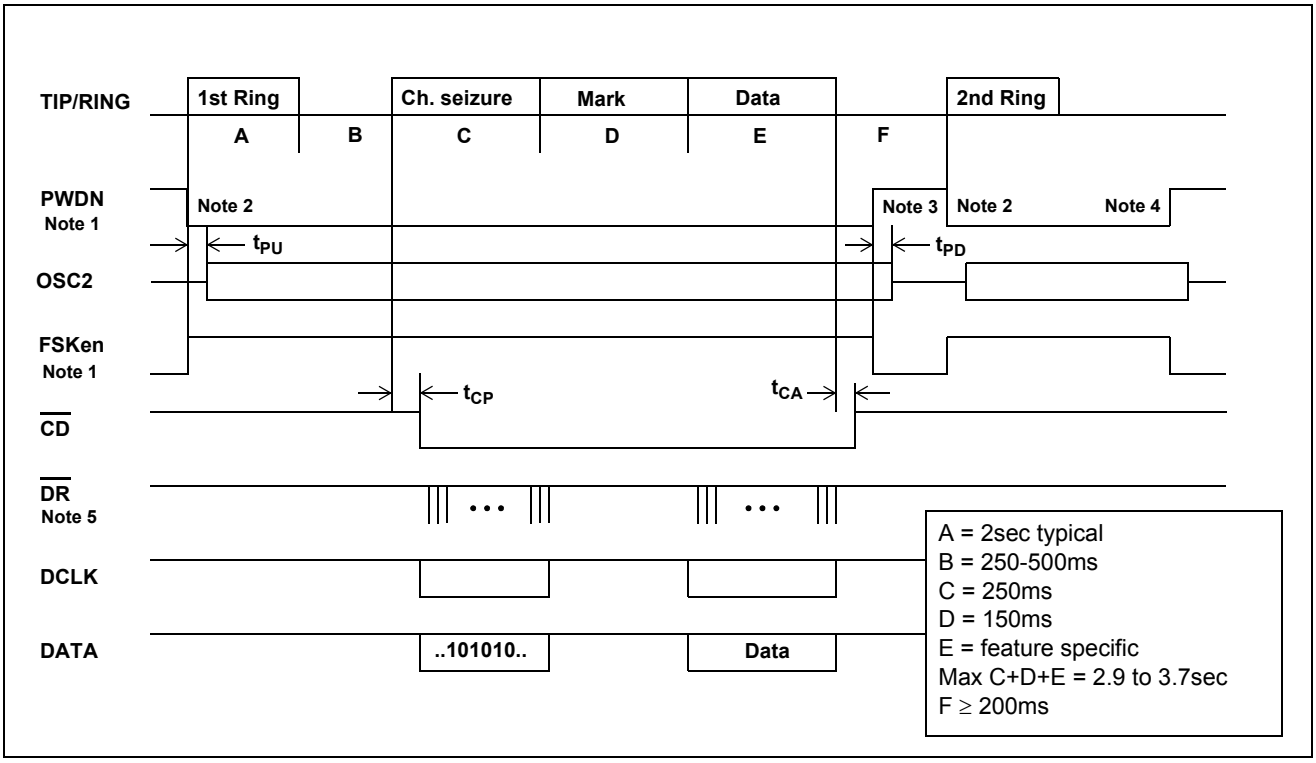


Figure 15 - Application Timing for Bellcore On-hook Data Transmission Associated with Ringing, e.g., CID

Notes:
This on-hook case application is included because a CIDCW (off-hook) CPE must be also capable of receiving on-hook data transmission (with ringing) from the end office.

1) PWDN and FSKen are internal signals decoded from CB0/1/2.
2) The CPE designer may choose to enable the MT88E45B only after the end of ringing to conserve power in a battery operated CPE. CD is not activated by ringing.
3) The microcontroller in the CPE powers down the MT88E45B after CD has become inactive.
4) The microcontroller times out if CD is not activated.
5) This signal represents the mode of the DR/STD pin.

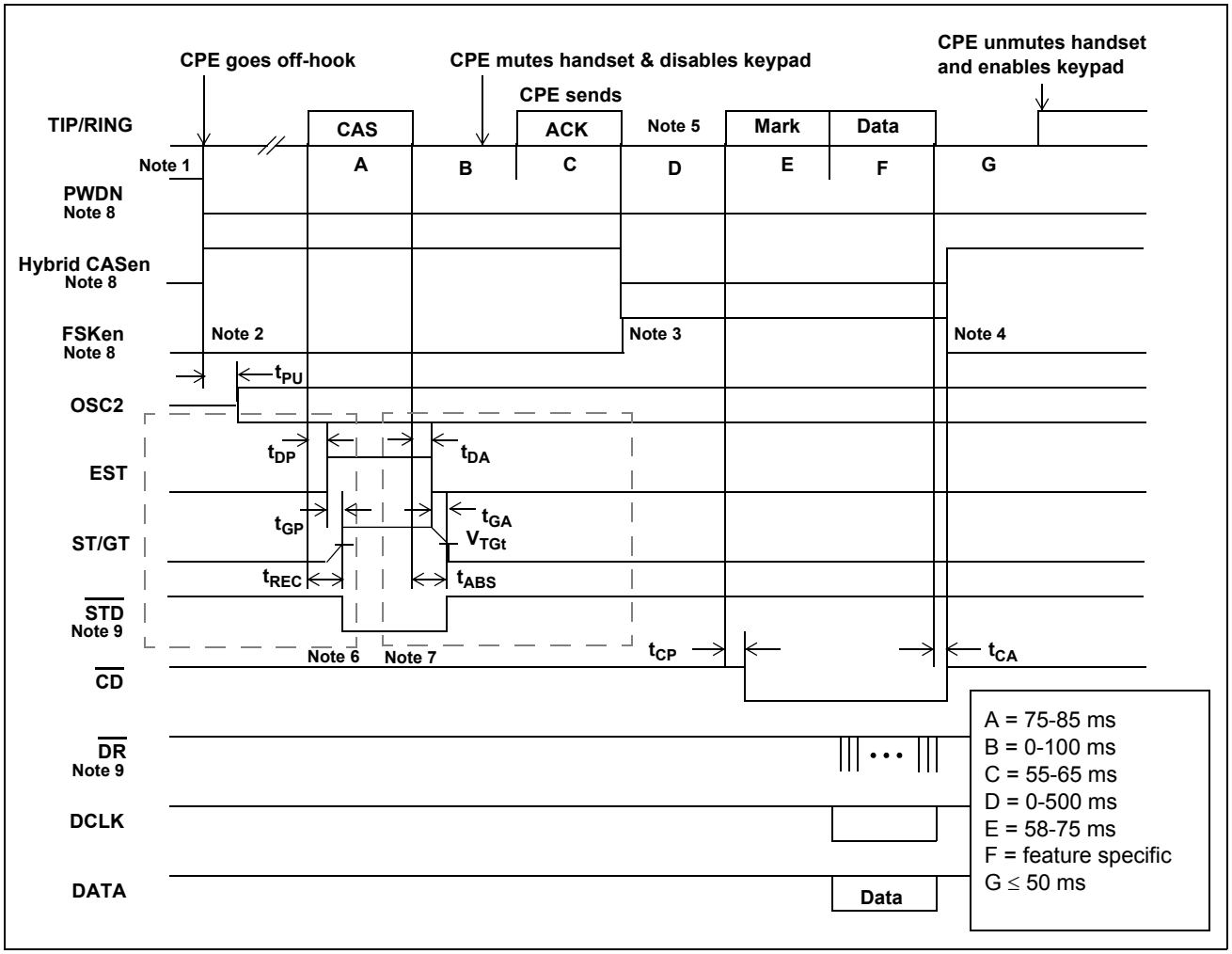


Figure 16 - Application Timing for Bellcore Off-hook Data Transmission, e.g., CIDCW

Notes:

1) In a CPE where AC power is not available, the designer may choose to switch over to line power when the CPE goes off-hook and use battery power while on-hook. The CPE must also be CID (on-hook) capable because a CIDCW CPE includes CID functionality.
2) Non-FSK signals such as CAS, speech and DTMF tones are in the same frequency band as FSK. They will be demodulated and give false data. Therefore the MT88E45B should be taken out of FSK mode when FSK is not expected.
3) The MT88E45B may be put into FSK mode as soon as the CPE has finished sending the acknowledgment signal ACK. TR-NWT-000575 specifies that ACK = DTMF 'D' for non-ADSI CPE, 'A' for ADSI CPE.
4) The MT88E45B should be taken out of FSK mode when $\overline{CD}$ has become inactive, or after 5 framing errors have been detected, or after 150ms of continuous mark signal or space signal has been received. The framing errors need not be consecutive.
5) In an unsuccessful attempt where the end office does not send the FSK signal, the CPE should unmute the handset and enable the keypad after interval D has expired.
6) The total recognition time is $t_{REC} = t_{GP} + t_{DP}$, where t_{GP} is the tone present guard time and t_{DP} is the tone present detect time. V_{TGt} is the comparator threshold (refer to Figure 55 for details).
7) The total tone absent time is $t_{ABS} = t_{GA} + t_{DA}$, where t_{GA} is the tone absent guard time and t_{DA} is the tone absent detect time. V_{TGt} is the comparator threshold (refer to Figure5 5 for details).
8) PWDN, Hybrid CASen and FSKen are $\overline{internal}$ signals decoded from CB0/1/2.
9) This signal represents the mode of the $\overline{DR}/\overline{STD}$ pin.

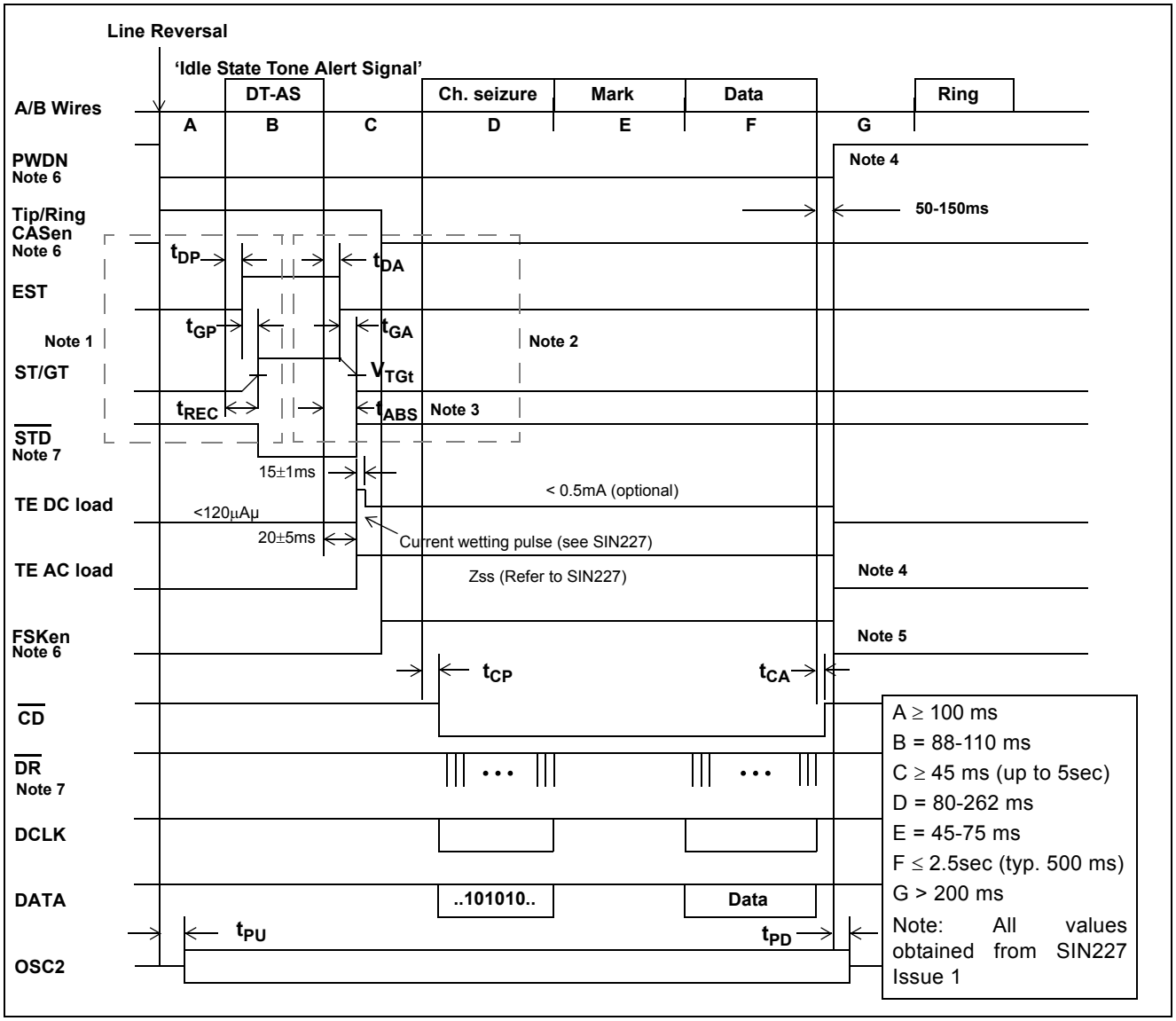


Figure 17 - Application Timing for BT Caller Display Service (CDS), e.g., CLIP

Notes:

1) The total recognition time is $t_{REC} = t_{GP} + t_{DP}$, where t_{GP} is the tone present guard time and t_{DP} is the tone present detect time. V_{TGt} is the comparator threshold (refer to Figure 55 for details).
2) The total tone absent time is $t_{ABS} = t_{GA} + t_{DA}$, where t_{GA} is the tone absent guard time and t_{DA} is the tone absent detect time. V_{TGt} is the comparator threshold (refer to Figure 55 for details).
3) By choosing t_{GA}=15ms, t_{ABS} will be 15-25ms so that the current wetting pulse and AC load can be applied right after the $\overline{STD}$ rising edge.
4) SIN227 specifies that the AC and DC loads should be removed between 50-150ms after the end of the FSK signal, indicated by $\overline{CD}$ returning to high. The MT88E45B may also be powered down at this time.
5) The MT88E45B should be taken out of FSK mode when FSK is not expected to prevent the FSK demodulator from reacting to other in-band signals such as speech, DT-AS/CAS and DTMF tones.
6) PWDN, Tip/Ring CASen, FSKen are internal signals decoded from CB0/1/2.
7) This signal represents the mode of the $\overline{DR}/\overline{STD}$ pin.

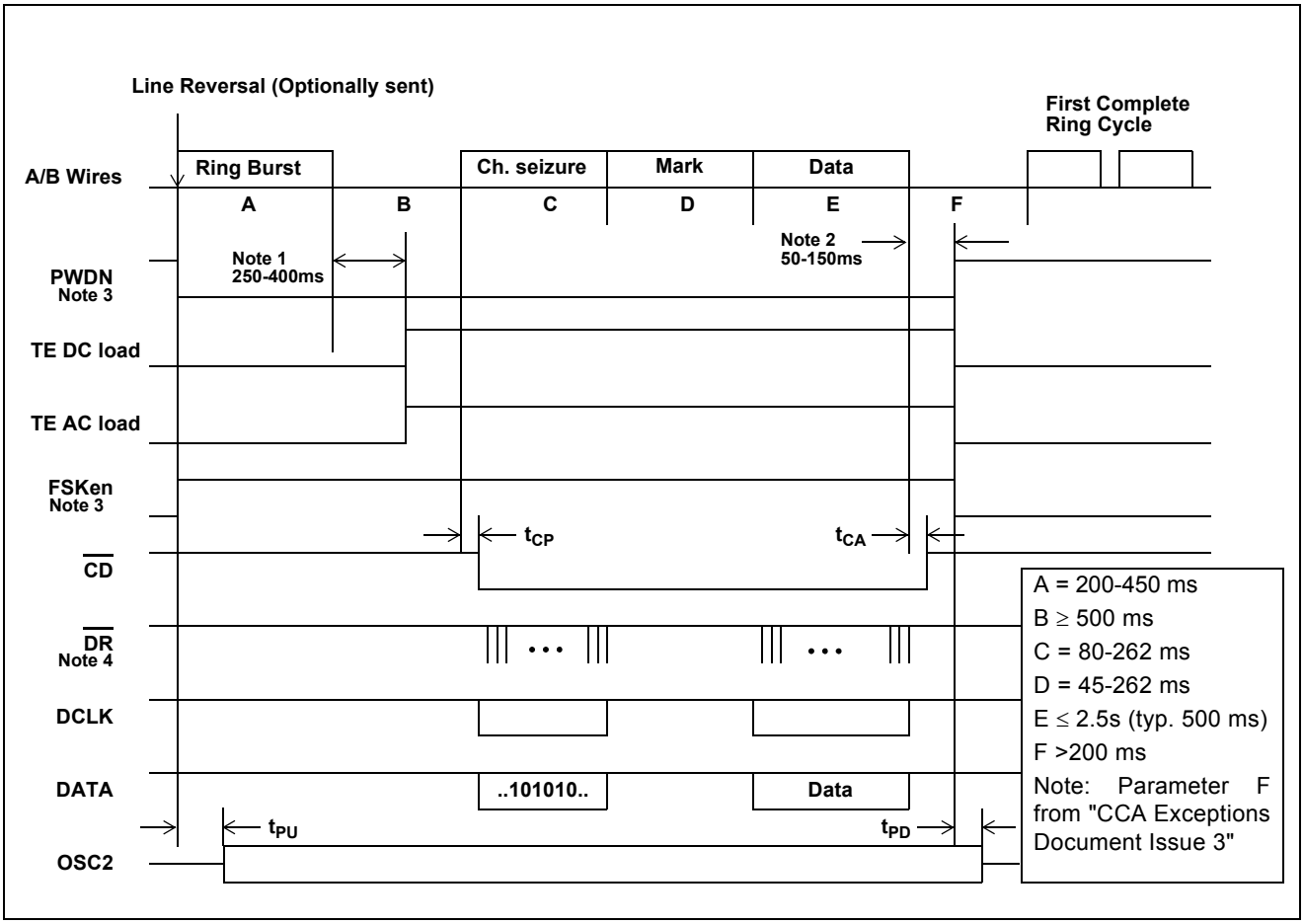
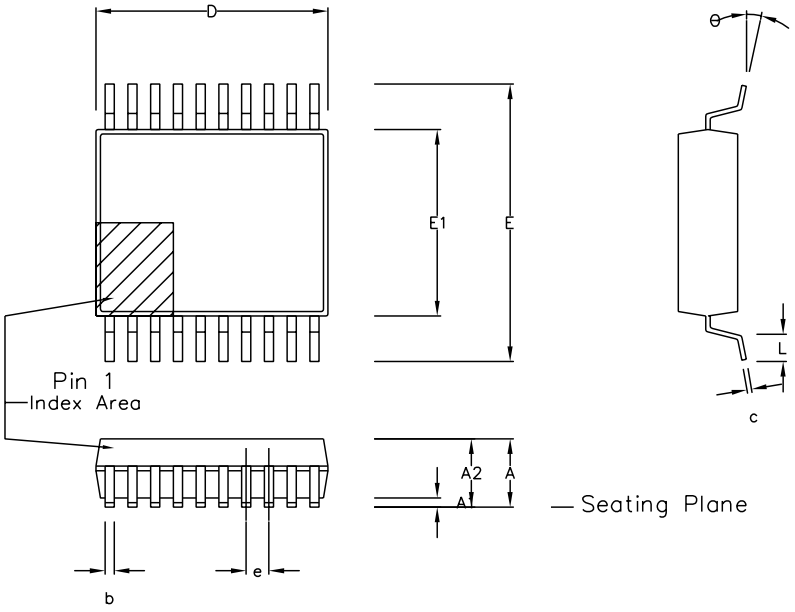


Figure 18 - Application Timing for UK's CCA Caller Display Service (CDS), e.g., CLIP

Notes:
1) From TW/P&E/312. Start time: The CPE should enter the signalling state by applying the DC and AC terminations within this time after the end of the ring burst.
2) End time: The CPE should leave the signalling state by removing the DC and AC terminations within this time after the end of Data, indicated by $\overline{CD}$ returning to high. The MT88E45B should also be taken out of FSK mode at this time to prevent the FSK demodulator from reacting to other in-band signals such as speech, and DTMF tones.
3) PWDN and FSKen are internal signals decoded from CB0/1/2.
4) This signal represents the mode of the $\overline{DR}$/$\overline{STD}$ pin.



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	1.70		2.00		0.067		0.079
A1	0.05		0.20		0.002		0.008
A2	1.65		1.85		0.065		0.073
D	6.90		7.50		0.272		0.295
E	7.40		8.20		0.291		0.323
E1	5.00		5.60		0.197		0.220
L	0.55		0.95		0.022		0.037
e	0.65 BSC.				0.026 BSC.		
b	0.22		0.38		0.009		0.015
c	0.09		0.25		0.004		0.010
θ	0°		8°		0°		8°
	Pin features						
N	20						
Conforms to JEDEC MO-150 AE Iss. B							

This drawing supersedes:-
418/ED/51481/002 (Swindon/Plymouth)

Notes:
1. A visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimensions D and E1 do not include mould flash or protusion. Mould flash or protusion shall not exceed 0.20 mm per side. D and E1 are maximum plastic body size dimensions including mould mismatch.
4. Dimension b does not include dambar protusion/intrusion. Allowable dambar protusion shall be 0.13 mm total in excess of b dimension. Dambar intrusion shall not reduce dimension b by more than 0.07 mm.

ISSUE	1	2	3	
ACN	201933	205234	212477	
DATE	27Feb97	25Sep98	3Apr02	
APPRD.				

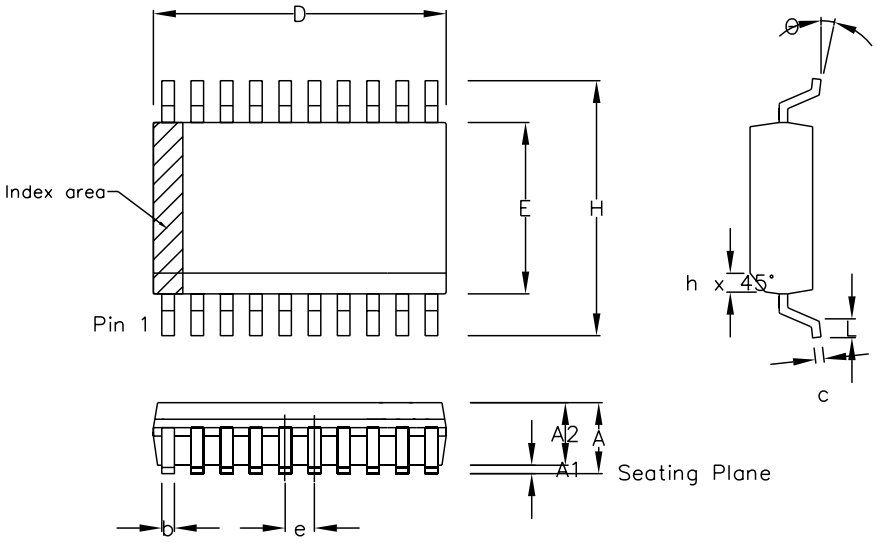
ZARLINK SEMICONDUCTOR

Previous package codes
NP / N

Package Code DD

Package Outline for 20 lead SSOP (5.3mm Body Width)

GPD00294



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	2.35		2.65		0.093		0.104
A1	0.10		0.30		0.004		0.012
A2	2.25		2.35		0.089		0.092
D	12.60		13.00		0.496		0.512
H	10.00		10.65		0.394		0.419
E	7.40		7.60		0.291		0.299
L	0.40		1.27		0.016		0.050
e	1.27 BSC.				0.050 BSC.		
b	0.33		0.51		0.013		0.020
c	0.23		0.32		0.009		0.013
Θ	0°		8°		0°		8°
h	0.25		0.75		0.010		0.029
	Pin features						
N	20						
Conforms to JEDEC MS-013AC Iss. C							

Notes:
1. The chamfer on the body is optional. If it not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimension D do not include mould flash, protrusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protrusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.004" total in excess of b dimension.

ISSUE	1	2	3	
ACN	6746	201941	213098	
DATE	7Apr95	27Feb97	15Jul02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

MP / S

Package Code DC

Package Outline for 20 lead SOIC (0.300" Body Width)

GPD00015

For more information about all Zarlink products visit our Web Site at

www.zarlink.com

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