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OKI Semiconductor

ML86V7668A

NTSC/PAL/SECAM Digital Video Decoder

GENERAL DESCRIPTION

The ML86V7668A is an LSI that converts NTSC, PAL and SECAM analog video signals into the YCbCr standard digital format defined by ITU-R recommendations BT.601/BT.656 and RGB digital data.
The device has two built-in 10-bit A/D converter channels and can accept composite video or S-video signal as input.
The composite video signal is separated into a luminance signal and chrominance signals by a 2-dimensional Y/C separation filter (adaptive comb filter) and are then converted to a general-purpose video data format.
In addition to the asynchronous sampling that is a special feature of Oki decoders, video signals can also be sampled using digital PLL for line lock clock sampling.
Further, with the built-in pixel position correction circuit and the FIFO for correcting the pixel count, the video jitter that can be a problem with asynchronous sampling is eliminated and jitter-free output data is ensured.
The ML86V7668A is a synchronous-performance-improved version of the ML86V7668. It is a product in which the synchronous performance in a weak electromagnetic field has specially been enhanced.
The ML86V7668A is fully pin-compatible with the ML86V7668.

USES AND APPLICATIONS

The ML86V7668A is an IC that can be used as an interface for video signal input of any digital video processing system. The device can be operated with a digital PLL line lock clock for applications where image quality is of utmost importance. Further, for applications where sync speed is important, such as switching between multiple input channels, an asynchronous clock allows high-speed synchronous operation.

Applications

- TVs and TV reception equipment
  Panel TVs such as TFT/PDP, PC TVs, digital TVs, set top boxes for receiving TV broadcasts
- Video recording equipment
  DVD-R/W, HDD recorders, digital VTRs, digital video cameras, and digital cameras
- Monitoring systems
  Multi-display equipment, long-playing video recording equipment, and transmission equipment for remote monitoring
- PC peripheral equipment
  Video capture boards, video editing equipment, and internet monitoring cameras

FEATURES

Input Section

- Accepts NTSC/PAL/SECAM composite video signals and S-video signals (NTSC/PAL)
- 4 composite inputs or 1 composite input + 3 S-video inputs can be connected
- Built-in clamp circuits and video amps
- Built-in 10-bit A/D converters (2 channels)
- Switchable between line lock clock sampling mode and asynchronous sampling mode
- Supported operating modes: Pixel frequency (sampling clock):
  NTSC/PAL/SECAM ITU-R BT.601 : 13.5 MHz (27 MHz)
  NTSC Square Pixel : 12.272727 MHz (24.545454 MHz)

Digital Processing Section

- 2-dimensional Y/C separation using an adaptive filter
  NTSC: Adaptive filter
  PAL: Adaptive filter
  SECAM: Trap filter
- Recognition of data in the VBI period (closed caption, CGMS, WSS) and function of reading from I^2C-bus (detection possible in all operating modes)
- Copy protection (analog copy protection signal) detection
- Capable of decoding specially standardized signals such as NTSC443, PAL-Nc, M, and 60
  Automatic determinations can also be made partially by register settings.
- Built-in AGC/ACC circuits (automatic luminance level control/automatic color level control)
- Automatic NTSC/PAL/SECAM recognition (only in ITU-R BT.601 mode)

Output Section

- Four selectable output interfaces:

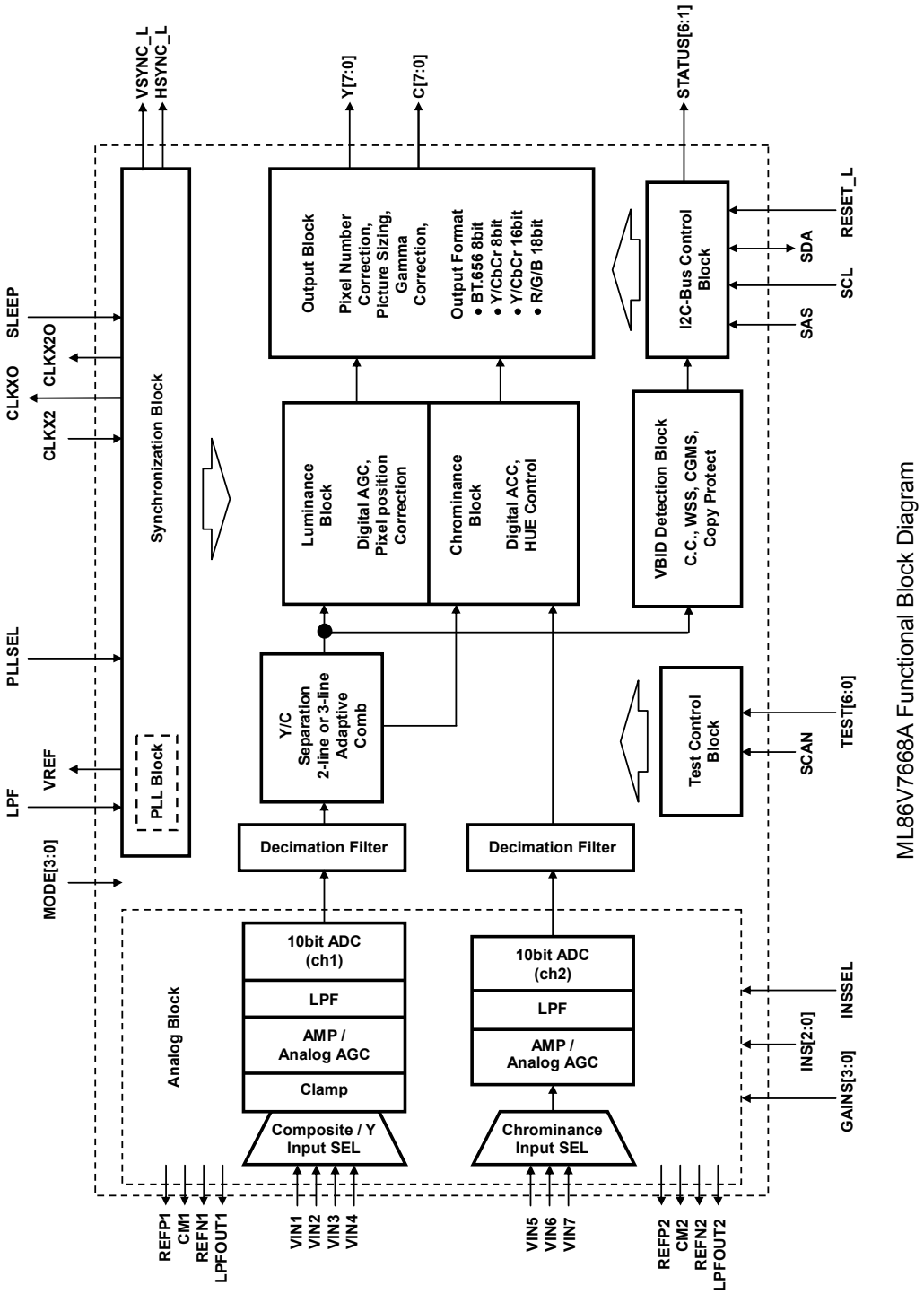
ITU-R BT.656-4 (8 bits (Y/CbCr))	: ITU-R BT.656 mode
Y/CbCr (8 bits (Y/CbCr) (4:2:2) + Sync.)	: 8-bit mode
Y/CbCr (8 bits (Y) + 8 bits (CbCr) (4:2:2)/(4:1:1) + Sync.)	: 16-bit mode
RGB (6 bits (R) + 6 bits (G) + 6 bits (B) + Sync.)	: 18-bit RGB mode

- Output pixel count correction via internal FIFO
- Screen scaling (QVGA)
- Gamma correction (only in RGB output mode)
- Sleep mode
- Output pins go to Hi-Z during reset period (excluding SDA, CLKXO, and CLKX2O)
- Polarity inversion of the field signal and vertical sync signal

Other Sections

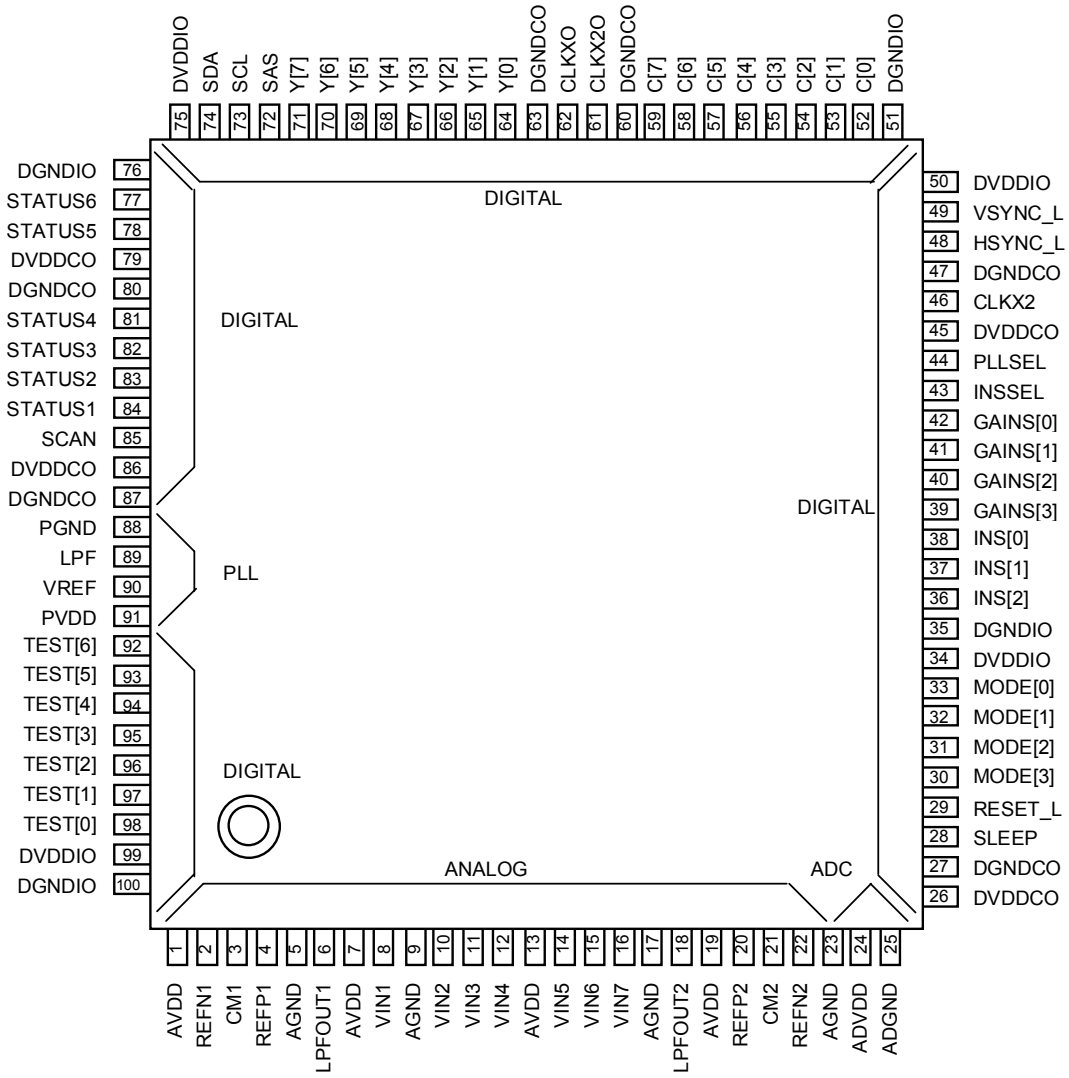
- I^2C-bus interface
- I/O: 3.3 V power supply, Core: 2.5 V power supply
- Package: 100-pin plastic TQFP (TQFP100-P-1414-0.50-K)

BLOCK DIAGRAM



ML86V7668A Functional Block Diagram

PIN CONFIGURATION (TOP VIEW)



100-Pin Plastic TQFP (TQFP100-P-1414-0.50-K)

PIN DESCRIPTIONS

No.	Symbol	I/O	PAD	Function
1	AVDD	—	—	Analog power supply (3.3 V)
2	REFN1	O	—	ADC1 reference voltage (Normally leave open)
3	CM1	O	—	
4	REFP1	O	—	
5	AGND	—	—	Analog ground
6	LPFOUT1	O	—	Analog amplifier output 1 (Normally leave open)
7	AVDD	—	—	Analog power supply (3.3 V)
8	VIN1	I		Analog Video Signal input 1 (Composite)
9	AGND	—	—	Analog ground
10	VIN2	I		Analog Video Signal input 2 (Composite or Lum)
11	VIN3	I		Analog Video Signal input 3 (Composite or Lum)
12	VIN4	I		Analog Video Signal input 4 (Composite or Lum)
13	AVDD	—	—	Analog power supply (3.3 V)
14	VIN5	I		Analog Video Signal input 5 (Chroma)
15	VIN6	I		Analog Video Signal input 6 (Chroma)
16	VIN7	I		Analog Video Signal input 7 (Chroma)
17	AGND	—	—	Analog ground
18	LPFOUT2	O	—	Analog amplifier output 2 (Normally leave open)
19	AVDD	—	—	Analog power supply (3.3 V)
20	REFP2	O	—	ADC2 reference voltage (Normally leave open)
21	CM2	O	—	
22	REFN2	O	—	
23	AGND	—	—	Analog ground
24	ADVDD	—	—	Digital power supply at Analog Block (3.3 V)
25	ADGND	—	—	Digital ground at Analog Block
26	DVDDCO	—	—	Digital core power supply (2.5 V)
27	DGNDCO	—	—	Digital core ground
28	SLEEP	I	Internal pull-down 50 kΩ	Sleep signal input
29	RESET_L	I		Reset signal input
30	MODE[3]	I	Internal pull-down 50 kΩ	Mode setting 3
31	MODE[2]	I	Internal pull-down 50 kΩ	Mode setting 2
32	MODE[1]	I	Internal pull-down 50 kΩ	Mode setting 1
33	MODE[0]	I	Internal pull-down 50 kΩ	Mode setting 0
34	DVDDIO	—	—	Digital IO power supply (3.3 V)
35	DGNDIO	—	—	Digital IO ground
36	INS[2]	I	Internal pull-down 50 kΩ	Input signal select 2
37	INS[1]	I	Internal pull-down 50 kΩ	Input signal select 1
38	INS[0]	I	Internal pull-down 50 kΩ	Input signal select 0
39	GAINS[3]	I	Internal pull-down 50 kΩ	Analog amplifier gain setting 3
40	GAINS[2]	I	Internal pull-down 50 kΩ	Analog amplifier gain setting 2
41	GAINS[1]	I	Internal pull-down 50 kΩ	Analog amplifier gain setting 1
42	GAINS[0]	I	Internal pull-down 50 kΩ	Analog amplifier gain setting 0
43	INSSEL	I	Internal pull-down 50 kΩ	Input signal select control pin
44	PLLSEL	I	Internal pull-down 50 kΩ	PLL clock select
45	DVDDCO	—	—	Digital core power supply (2.5 V)
46	CLKX2	I		External clock input
47	DGNDCO	—	—	Digital core ground
48	HSYNC_L	O		Horizontal sync signal output
49	VSYNC_L	O		Vertical sync signal output
50	DVDDIO	—	—	Digital IO power supply (3.3 V)

No.	Symbol	I/O	PAD	Function
51	DGNDIO	—	—	Digital IO ground
52	C[0]	O		Chroma data output 0 (LSB)
53	C[1]	O		Chroma data output 1
54	C[2]	O		Chroma data output 2
55	C[3]	O		Chroma data output 3
56	C[4]	O		Chroma data output 4
57	C[5]	O		Chroma data output 5
58	C[6]	O		Chroma data output 6
59	C[7]	O		Chroma data output 7 (MSB)
60	DGNDCO	—	—	Digital core ground
61	CLKX2O	O		System clock output
62	CLKXO	O		Pixel clock output
63	DGNDCO	—	—	Digital core ground
64	Y[0]	O		Luminance data output 0 (LSB)
65	Y[1]	O		Luminance data output 1
66	Y[2]	O		Luminance data output 2
67	Y[3]	O		Luminance data output 3
68	Y[4]	O		Luminance data output 4
69	Y[5]	O		Luminance data output 5
70	Y[6]	O		Luminance data output 6
71	Y[7]	O		Luminance data output 7 (MSB)
72	SAS	I	Internal pull-down 50 kΩ	Slave address select
73	SCL	I		I2C bus clock input
74	SDA	I/O	Schmitt	I2C bus data input/output
75	DVDDIO	—	—	Digital IO power supply (3.3 V)
76	DGNDIO	—	—	Digital IO ground
77	STATUS6	O		STATUS output pin 6
78	STATUS5	O		STATUS output pin 5
79	DVDDCO	—	—	Digital core power supply (2.5 V)
80	DGNDCO	—	—	Digital core ground
81	STATUS4	O		STATUS4 output
82	STATUS3	O		STATUS3 output
83	STATUS2	O		STATUS2 output
84	STATUS1	O		STATUS1 output
85	SCAN	I	Internal pull-down 50 kΩ	Test pin (Normally leave open)
86	DVDDCO	—	—	Digital core power supply (2.5 V)
87	DGNDCO	—	—	Digital core ground
88	PGND	—	—	PLL ground
89	LPF	I		LPF connection (Leave open when PLL is used; connect to PVDD when PLL not used)
90	VREF	O		Center frequency select (Leave open when PLL is used; connect to PVDD when PLL not used)
91	PVDD	—	—	PLL power supply (3.3 V)
92	TEST[6]	I	Internal pull-down 50 kΩ	Test pins (Normally leave open)
93	TEST[5]	I	Internal pull-down 50 kΩ	
94	TEST[4]	I	Internal pull-down 50 kΩ	
95	TEST[3]	I	Internal pull-down 50 kΩ	
96	TEST[2]	I	Internal pull-down 50 kΩ	
97	TEST[1]	I	Internal pull-down 50 kΩ	
98	TEST[0]	I	Internal pull-down 50 kΩ	
99	DVDDIO	—	—	Digital IO power supply (3.3 V)
100	DGNDIO	—	—	Digital IO ground

FUNCTIONAL DESCRIPTION

This section explains the basic functions of the IC in terms of the blocks shown in the block diagram.
Refer to the User's Manual for detailed explanations of the internal registers and any functions that are not covered in this data sheet.

Analog Section

The analog section inputs video signals. The analog section uses the video signal channel selector, AMP and 10-bit ADC to select the desired channel from among several video signals and convert the input to digital video data.

- Analog input selector

  The analog input selector is compatible with composite signals and S-video signals. The maximum allowable number of input connections is 4 channels of composite signals or 3 channels of S-video signals + 1 channel of composite signal. The selection of these input connections can be changed by external pins or by register controls using the I^2C-bus, as shown in the table below.

  # Related register: $68/ADC1[2:0]

Analog Input Controls

Input signal	Control pin	Register	Input pin							ADC operation setting
	Pin 43:INSSEL=0	Pin 43:INSSEL=1								
	INS Pins 36–38	$68/ADC1 [2:0]	VIN1 Pin 8	VIN2 Pin 10	VIN3 Pin 11	VIN4 Pin 12	VIN5 Pin 14	VIN6 Pin 15	VIN7 Pin 16	
*Composite-1 input	[000]	[000]	Composite							ADC1: ON ADC2: OFF
Composite-2 input	[001]	[001]		Composite						ADC1: ON ADC2: OFF
Composite-3 input	[010]	[010]			Composite					ADC1: ON ADC2: OFF
Composite-4 input	[011]	[011]				Composite				ADC1: ON ADC2: OFF
S-Video-1 input	[100]	[100]		Luminance			Chroma			ADC1: ON ADC2: ON
S-Video-2 input	[101]	[101]			Luminance			Chroma		ADC1: ON ADC2: ON
S-Video-3 input	[110]	[110]				Luminance			Chroma	ADC1: ON ADC2: ON
ADOFF	[111]	[111]	OFF (ADC sleep)							OFF

Blank: Selection disabled *: Default setting used for every register after the LSI is reset.

- AMP/analog AGC function

  This function converts video input signals to the optimum level for the ADC using the analog AMP of the AGC function. The AGC function has an output level adjustment function in the luminance block of the digital section in addition to the AMP input level adjustment function. Manual setting of the AMP gain is also possible.

  # Related register: $69/ADC2

  The analog AMP gain can be set also by using the AMP gain external setting pins GAINS[3:0] (pins 39-42), as shown in the table below. This method is enabled when INSSEL (pin 43) = "0". The gain values in the table are design target values.

Pins 39-42	Register	Gain factor
GAINS[3:0]	$69/ADC2[5:0]	
0000	11_1111	1.014
0001	11_0001	1.263
0010	10_0110	1.565
0011	01_1101	1.946
0100	01_0110	2.400
0101	01_0000	3.000
0110	00_1011	3.789
0111	00_0111	4.800
1000	00_0100	6.000
(1001)	(00_0010)	(Setting prohibited)
(1010)	(00_0000)	
(1011)	--	
(1100)		
(1101)		
(1110)		
(1111)		

• Clamp function
The clamp fixes the video input signal in the ADC input range. Clamping is performed by sync chip clamp.

• A/D converter
This 10-bit A/D converter (ADC) converts analog video signals to digital video data. There are 2 channels built into the ADC. Sampling is performed at the pixel frequency or double-speed.
Related registers: $68/ADC1, $69/ADC2, $6A/ADC3

Digital Section
The digital section separates the video data digitized by the ADC into Y and C data, converts these data to various data formats and outputs them. The digital section also performs output level adjustment, image quality adjustment and various corrections.

• Decimation filter
Since internal processing is performed at a single speed, this filter is needed to reduce the data that has been doubled by one-half. Using the decimation filter after double-speed sampling reduces high-frequency noise .
Related register: $08/FIFOBC[7]

2-dimensional Y/C Separation Block
This block separates composite data into Y (luminance) data and C (chrominance) data. For S-Video input, the Y/C separation circuit is bypassed.

• 2-Dimensional Y/C Separation Function
With the Y/C separation filter, composite data is separated into Y (luminance) data and C (chrominance) data. There are various Y/C separation filters available, which can be selected in an internal register.
Y/C separation of the SECAM signal is performed by the trap filter.
Related registers: $10/YC1, $11/YC2, $12/YC3

YC1[6:4]	NTSC Y/C separation	PAL Y/C separation
*000	Adaptive filter	Adaptive filter
001	3-line comb filter	2-line comb filter
010	Trap filter	Trap filter
011	3-line comb or trap adaptive filter	Undefined
100	Undefined	Undefined
101	2-line or 3-line adaptive transition filter	Undefined
110	Undefined	Undefined
111	Undefined	2-line comb or trap adaptive transition filter

Luminance Block

The luminance block removes sync signals from the luminance data after Y/C separation, and performs adjustments such as luminance level adjustment and luminance image quality correction and adjustment. Digital decoded data that conforms to ITU-R BT.601 can be output.

- Pixel Position Correction Function

  This function corrects sampling error in asynchronous sampling and loss of PLL synchronization. Error correction is made in the horizontal direction, which improves vertical line jitter on the screen.

  # Related register: $22/SYNC3

- Digital AGC Function

  This function adjusts the output level of luminance signals.

  Adjustment is automatically performed by the digital AGC, but the adjustment can also be set manually by using an internal register to set digital MGC. In the digital AGC mode, the sync level is compared with a reference value to determine the amplification ratio of the luminance level. The default is automatically adjusted to sync level 40IRE, but the level can also be adjusted by an internal register. In the digital MGC mode, the signal amplification ratio and the black level are adjusted with register settings. The black level is adjusted by means of pedestal level adjustment.

  Regarding the AGC function, in addition to the output level adjustment function in the digital section, the input level adjustment function of the AMP in the analog section also operate separately.

  # Related registers: $30/AGCC, $31/AGCRC, $37/LOFLC, $36/CLC

- Image Quality Adjustment

  The following image filters are provided for adjusting luminance image quality.
  Refer to the User's Manual for the characteristics of each filter.

  - Edge enhancement pre-filter
  This filter is for enhancing the edge of a luminance signal
  The two filters of a pre-filter and a sharp filter operate simultaneously.
  # Related register: $35/LUMC4[7]
  - Aperture bandpass filter and coring filter that are used for contour compensation
  These filters are adjusted using the following registers:
  - For setting the aperture band-pass filter coefficient:
  # Related register: $35/LUMC4[6:5]
  - For setting the range of coring
  # Related registers: $35/LUMC4[4:3]
  - For setting aperture weight
  # Related register: $35/LUMC4[2:0]

Chrominance Block

This block decodes chroma data to Cb/Cr data and performs level adjustment and color adjustment. To eliminate unnecessary bands, this block first passes data through a bandpass filter (bypass is possible) and then through an ACC correction circuit to maintain a stable chroma level, before performing UV decoding. The result of the UV decoding is passed through a low-pass filter and output as a chrominance signal.

Related registers: $46/CHRSC1, $47/CHRSC2

- Digital ACC Function

  The digital ACC is the gain adjustment for the chrominance signal output level. Adjustment is automatically performed by the digital ACC (Auto Chrominance Control), but adjustment can also be made manually by using an internal register to set digital MCC (Manual Chrominance Control). In the digital ACC mode, the burst level is compared with a reference value to determine the amplification ratio of the chrominance level. The default is automatically adjusted to sync level 40IRE, but the level can also be adjusted by an internal register. Separate U/V level adjustment is also possible.

  # Related registers: $40/ACCC, $41/ACCRC

- Hue Adjustment Function

  The function for adjusting hue.

  Hue can be adjusted by setting the HUE register.

  # Related register: $45/HUE

Output Block

The output block performs output timing adjustment, picture sizing, output format conversion and other types of output conversion.

- Pixel Count Correction Function

  This function uses the internal FIFO to correct the total number of pixels in a line. It corrects the 1-line sampling error generated in asynchronous sampling mode or when PLL synchronization is lost, and fixes the pixel count for a line within the active screen. Refer to Active Pixel Timing for more on the pixel count for one line.

  # Related register: $08/FIFOBC

- Output Format Conversion Function

  This function converts output data to a desired output format.

  The output formats listed in the table below are supported.

  # Related register: $01/IOC2

Output Formats

Output mode (i): interlace		Register IOC2[0] = "0" *	Register IOC2[0] = "1"	Register
		Control pin (Pins 30, 31)	Register	
		MODE[3:2]	IOC2[5:4]	IOC2[1]
ITU-R BT.656	(i) 4:2:2	[00]	[00] *	0
Y/CbCr 8 bits	(i) 4:2:2	[01]	[01]	0
Y/CbCr 16 bits	(i) 4:2:2	[10]	[10]	0
Y/CbCr 16 bits	(i) 4:1:1	[10]	[10]	1
RGB 18 bits	(i) 4:4:4	[11]	[11]	0

*: Default

Synchronization Block

This block controls the sync signals for internal operation, output sync signals, and the timing for each block. Synchronization detection levels, output timing, and various other functions can be adjusted by the registers listed below.

- PLL Function

  The digital PLL circuit generates an operating clock synchronized with the horizontal sync signals of the video signals. With the input of a 25 MHz or 32 MHz reference clock, the double-speed pixel clock for each mode is provided as a line lock clock and used as the sampling clock.

  The asynchronous sampling mode, which uses a fixed clock directly, can be used without using PLL.

  # Related registers: $70/PLLC1, $71/PLLC2, $72/PLLC3, $73/PLLC4

Input Clock Settings

Control pin Pin 44 PLLSEL	Input clock		Sampling
PLLSEL = "0" Fixed clock	Input the sampling clock according to the operating mode. (See the table below)		Asynchronous
PLLSEL = "1" PLL clock	$70/PLLC1[6] = "0" * 32 MHz	$70/PLLC1[6] = "1" 25 MHz	$70/PLLC1[7] = "0" * Line lock
			$70/PLLC1[7] = "1" Fixed PLL clock

In the PLL mode, a double-speed line lock clock is generated by setting the operating mode.

Operating Modes/Sampling Clock Settings

Operating mode	$01/IOC2[0] = "0" *	$01/IOC2[0] = "1"	Sampling clock (double-speed)
	Control pin (Pin 33)	Register	
	MODE[0]	$00/IOC1[1]	Pin 46 CLKX2
ITU-R BT.601 13.5 MHz	0	0 *	27 MHz
NTSC Square pixel 12.272727 MHz	1	1	24.545454 MHz

*: Default

VBID Detection Block

This block detects data information and copy protection information from the VBI (Vertical Blanking Interval) of the input luminance signals. The following five types of VBID data can be detected, and the detection line and detection level can be changed by altering register settings.

Note: Data may not be read correctly depending on the I2C read timing.
When this detection function is used, information as to presence or absence of a VBID signal or the content of VBID signal may be output incorrectly depending on the input signal status. To ensure the stable operation of this function, read the VBID signal over several fields and then confirm that the read contents are stable. Detection data should be used thereafter.

- VBID Detection Function

(1) Analog copy protection pulse
Detects whether specified lines include an analog copy protection pulse (NTSC/PAL) and sets a flag.
Related registers: $86/AGCD1, $87/AGCD2, $81/VBIDM, $89/RSTVBID, $92/VFLAG

(2) C. C. (Closed Caption)
Detects whether specified lines include closed caption data (NTSC/PAL), keeps separately the data of even and odd lines, and sets individual flags.
Related registers: $82/CCD, $81/VBIDM, $89/RSTVBID, $92/VFLAG, $93/CCDO0, $94/CCDO1, $95/CCDE0, $96/CCDE1

(3) WSS (Wide Screen Signaling)
Detects the WSS data in the lines specified by ETSI (European Telecommunications Standards Institute) and sets a flag (PAL only).
Related registers: $88/WSSD, $81/VBIDM, $89/RSTVBID, $92/VFLAG, $9D/WSS0, $9E/WSS1

(4) CGMS (Copy Generation Management System)
Detects the CGMS data in the lines specified by IEC61880 and sets a flag (NTSC only).
Related registers: $84/CGMS1, $85/CGMS2, $81/VBIDM, $89/RSTVBID, $92/VFLAG, $97/CGMSO0, $98/CGMSO1, $99/CGMSO2, $9A/CGMSE0, $9B/CGMSE1, $9C/CGMSE2

(5) Other copy protection detection functions
Detects color stripes, false pulses, and MV protection and sets flags.
MV protection: Outdated copy protedction signal that was being used in VTRs. It is a specicial signal whose vertical-serration-pulse width is 10 μs.
Related registers: $81/VBIDM, $89/RSTVBID, $90/STATUS1, $91/STATUS2, $92/VFLAG
Note: This function does not detect SECAM color stripes.

I²C-bus Control Block
This serial interface block is based on the I²C standard of Phillips Corporation. The registers at up to subaddress 89h are write/read, while the registers at 90h and onwards are read-only.

Test Control Block
This block is used to test the LSI chip. It is not intended for user use.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	VDD1(*1)	Ta = 25°C	–0.3 to +4.6	V
	VDD2(*2)		–0.3 to +3.6	V
Input voltage	Vi	Ta = 25°C	–0.3 to +3.9	V
Power consumption	Pw	Ta = 25°C	800	mW
Short output current	Ios	—	50	mA
Storage temperature	Tstg	—	–55 to +150	°C

Warning: Stresses beyond those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device.

*1 VDD1 (DVDDIO, AVDD, ADVDD, PVDD)

*2 VDD2 (DVDDCO)

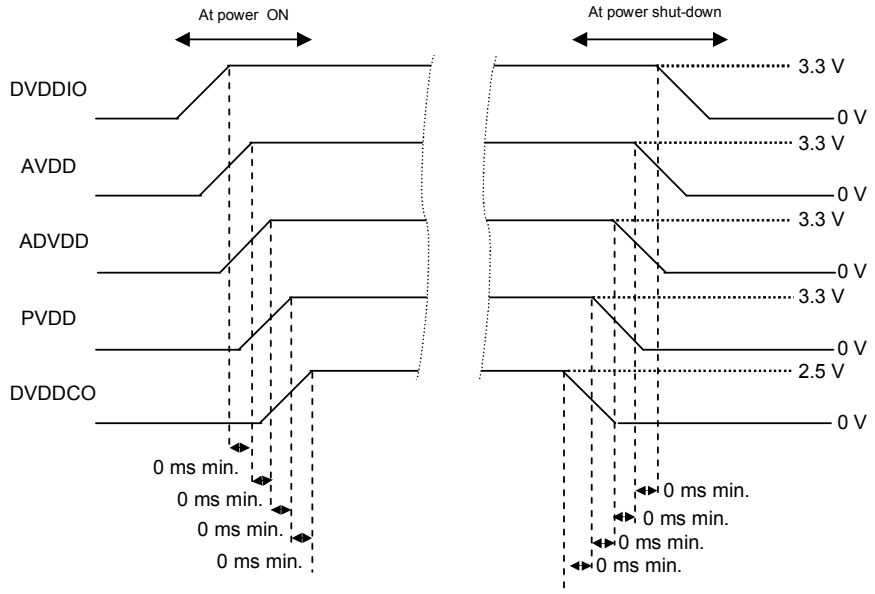
RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	DVDDIO	—	3.0	3.3	3.6	V
	DVDDCO	—	2.25	2.5	2.75	V
	AVDD	—	3.0	3.3	3.6	V
	ADVDD	—	3.0	3.3	3.6	V
	PVDD	—	3.0	3.3	3.6	V
	GND	—	—	0	—	V
Digital "H" level input voltage	Vih	—	0.8 VDD1	—	VDD1 + 0.3	V
Digital "L" level input voltage	Vil	—	–0.3	—	+0.6	V
Operating temperature	Ta	—	–40	—	+85	°C

Reset after all power supply voltages reach the specified values and confirming that CLKX2 has been input.

POWER-ON SEQUENCE

Follow the sequence shown below when turning the power on.



ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta = –40 to +85°C, VDD1 (DVDDIO, ADVDD, AVDD, PVDD) = 3.0 to 3.6 V, VDD2 (DVDDCO) = 2.25 to 2.75 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" level output voltage	VOH	Ioh = –4 mA(*1)	0.7 VDD1	—	—	V
"L" level output voltage	VOL	Iol = 4 mA(*2)	—	—	0.6	V
Input leakage current	Ii	Vi = GND or VDD1	–10	—	+10	μA
Output leakage current	Io	Vi = GND or VDD1	–10	—	+10	μA
Input leakage current (pull-down)	Iipl	Vi = VDD1	20	—	200	μA
VIN	Vivin	C Coupling	0.4	—	1.3	Vp-p

*1: Y[7:0], C[7:0], HSYNC_L, VSYNC_L, CLKXO, CLKX2O, STATUS1, STATUS2, STATUS3, STATUS4, STATUS5, STATUS6

*2: Y[7:0], C[7:0], HSYNC_L, VSYNC_L, CLKXO, CLKX2O, STATUS1, STATUS2, STATUS3, STATUS4, STATUS5, STATUS6, SDA

Current Characteristics

(Ta = –40 to +85°C, VDD1 (DVDDIO, ADVDD, AVDD, PVDD) = 3.0 to 3.6 V, VDD2 (DVDDCO) = 2.25 to 2.75 V)

Parameter	Symbol	Condition	Max. [mA]
Power supply (operating)	IDDO	—	200
Power supply (standby)	IDDS	SLEEP = "1" INS[2:0] = "111"	10

AC Characteristics

(Ta = –40 to +85°C, VDD1 (DVDDIO, ADVDD, AVDD, PVDD) = 3.0 to 3.6 V, VDD2 (DVDDCO) = 2.25 to 2.75 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CLKX2 Cycle Frequency	1/tclkx2	ITU-R BT.601	—	27	—	MHz
		NTSC Square Pixel	—	24.545454	—	MHz
CLKX2 Duty	td_d2	—	45	—	55	%
CLKX2-Output DATA Delay Time(*)	todx2	—	—	—	16	ns
Output Clock Delay Time(*) (CLKX2-CLKX20)	tcdx2o	—	—	—	8	ns
Output Clock Delay Time(*) (CLKX2-CLKX0)	tcdxo	—	—	—	10	ns
RESET_L width	rst_w	—	200	—	—	ns

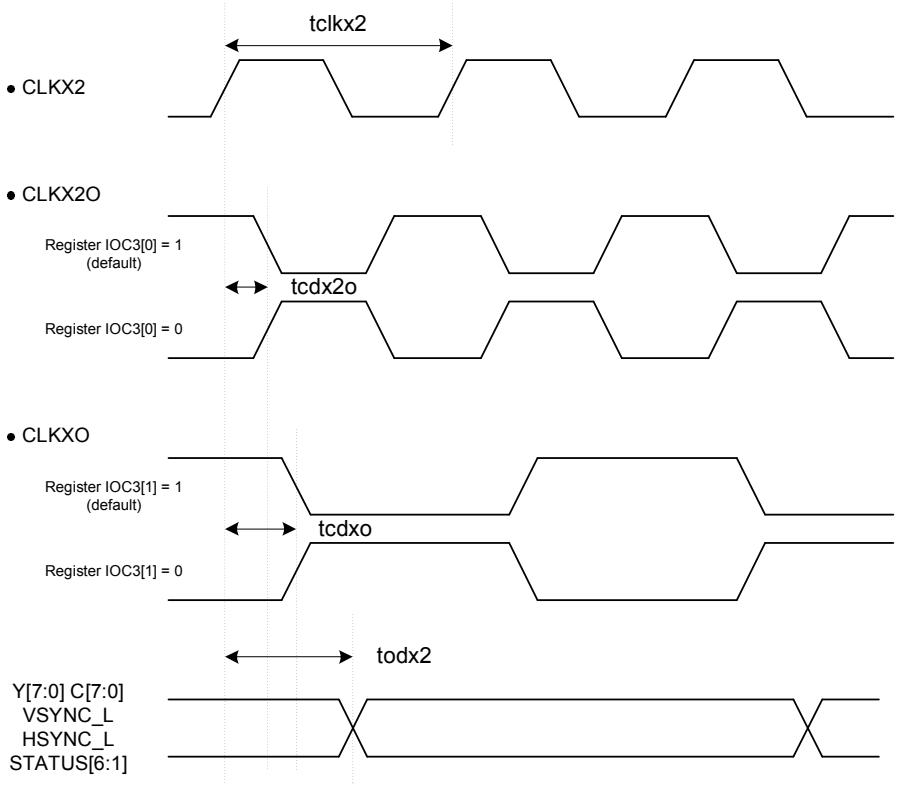
*: Output load: 20 pF

Use a clock frequency accuracy of ± 100 ppm.

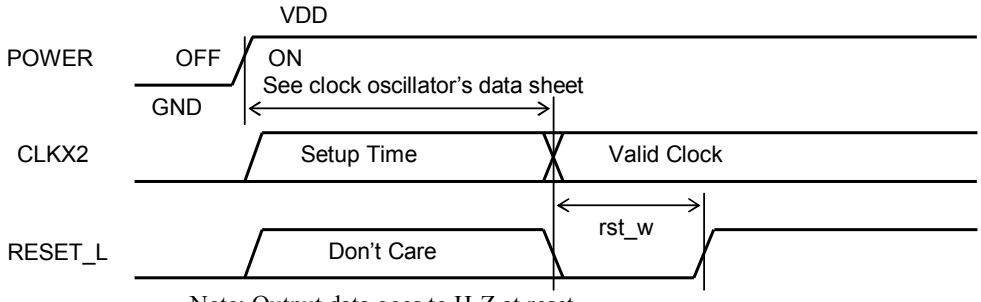
Timings of these output signals have been measured at the 50% point of VDD1.

INPUT AND OUTPUT TIMING DIAGRAMS

Data Output Timing (Pin 44: PLLSEL = "0")

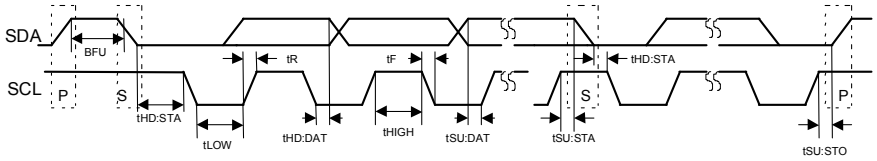


Reset Timing



Note: Output data goes to H-Z at reset.

I²C-bus Timing



I²C Specifications (Fast Mode)

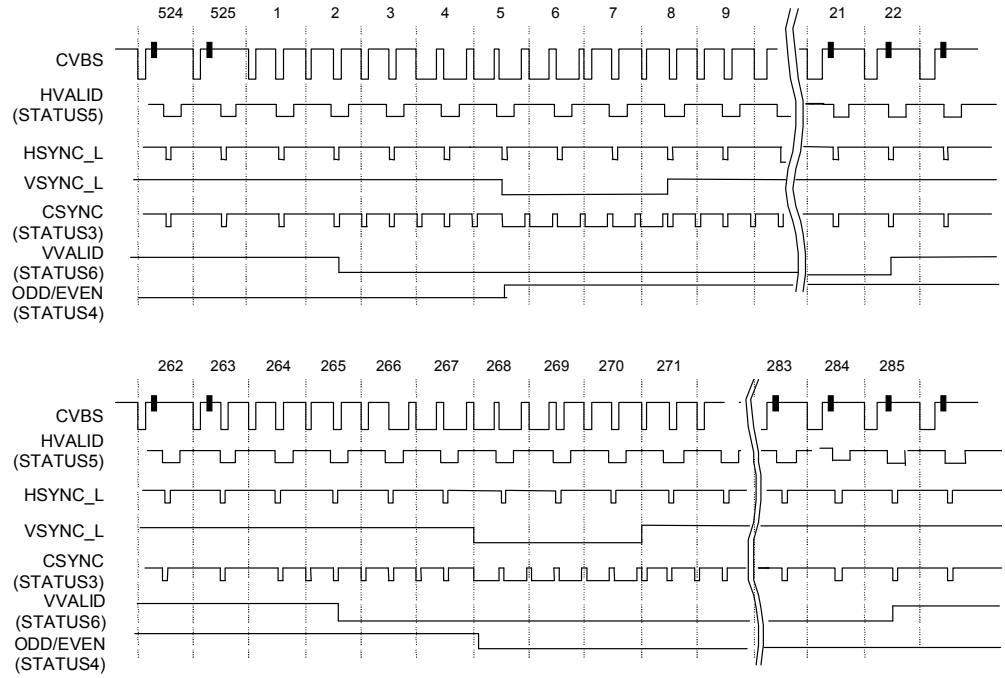
Symbol	Parameter	Min.	Typ.	Max.	Unit
fSCL	SCL frequency	0		100	kHz
tBUF	Bus open time	4.7			µs
tHD:STA	Start condition hold time	4.0			µs
tLOW	Clock LOW period	4.7			µs
tHIGH	Clock HIGH period	4.0			µs
tSU:STA	Start condition setup time	4.7			µs
tHD:DAT	Data hold time	0 (300)			ns
tSU:DAT	Data setup time	250			ns
tR	Line rise time			1	µs
tF	Line fall time			300	ns
tSU:STO	Stop condition setup time	4.0			µs

I²C Specifications (High Speed Mode)

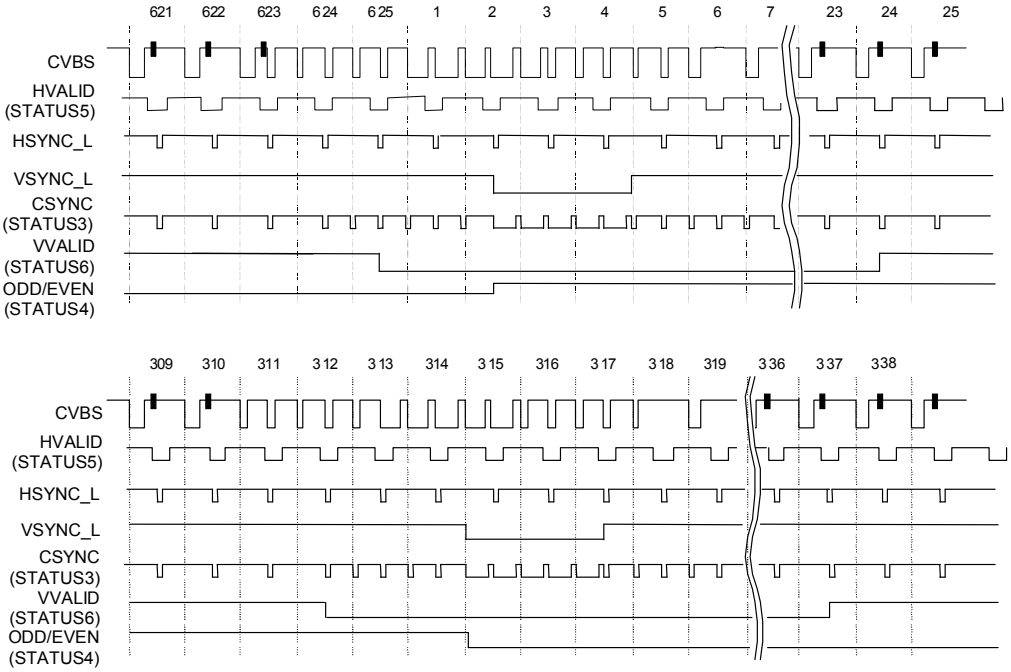
Symbol	Parameter	Min.	Typ.	Max.	Unit
fSCL	SCL frequency	0		400	kHz
tBUF	Bus open time	1.3			µs
tHD:STA	Start condition hold time	0.6			µs
tLOW	Clock LOW period	1.3			µs
tHIGH	Clock HIGH period	0.6			µs
tSU:STA	Start condition setup time	0.6			µs
tHD:DAT	Data hold time	0 (300)			ns
tSU:DAT	Data setup time	100			ns
tR	Line rise time			300	ns
tF	Line fall time			300	ns
tSU:STO	Stop condition setup time	0.6			µs

Sync Signal Input and Output Timings (Default)

The following illustrations show the timing of vertical sync signals.



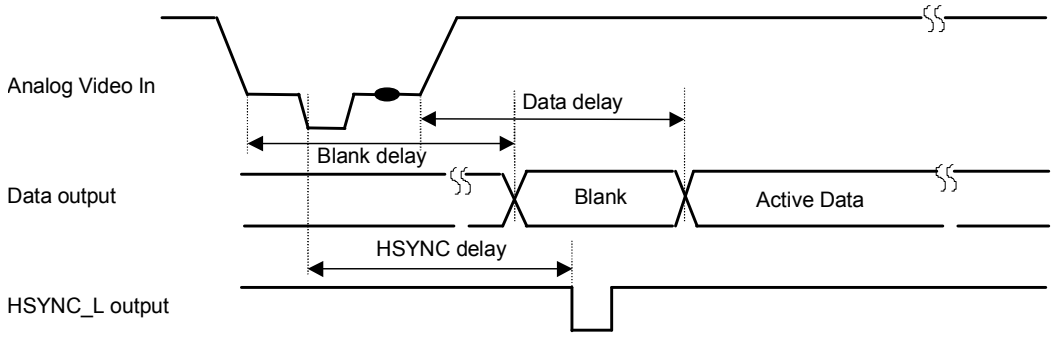
Vertical Sync Signals (NTSC)



Vertical Sync Signals (PAL)

Input/Output Delays (at Standard Signal Input)

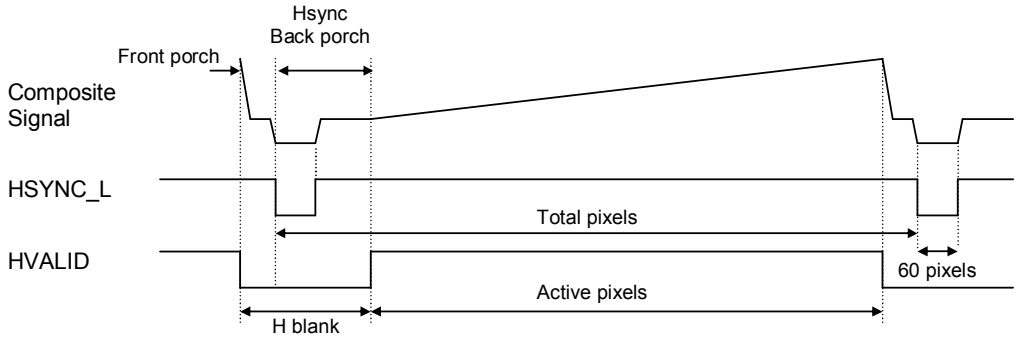
The illustration below shows the time delay between the input of a video signal and the output of digital data.



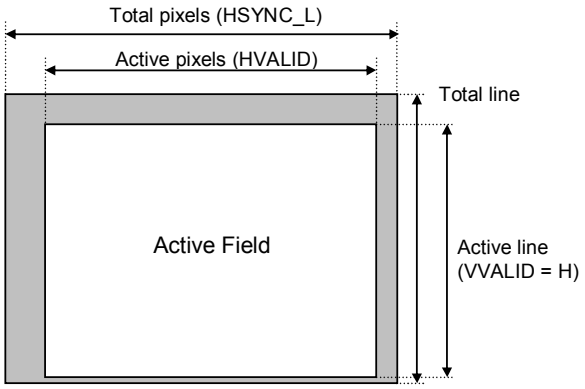
Video mode	Input signal	Mode	Delay
NTSC	Composite	FIFO-1, 2	Approx. 1.5H
NTSC	Composite	FIFO through	Approx. 1.5H
PAL/SECAM	Composite	FIFO-1, 2	Approx. 1.5H
PAL/SECAM	Composite	FIFO through	Approx. 1.5H

The data delay, blank delay, and sync signal delay are the same length.
In FIFO mode, the output cycle is fixed, so the delay varies.
The delay value becomes approx. 2.5H only when the adaptive filter (register $10/YC1[6:4] = "000") is selected as the Y/C separation filter in PAL mode.

Active Pixel Timing



Note: Actually, there is an output delay of about 1.5H after video signal input.



Video Modes and Pixel/Line Counts (at Standard Signal Input)

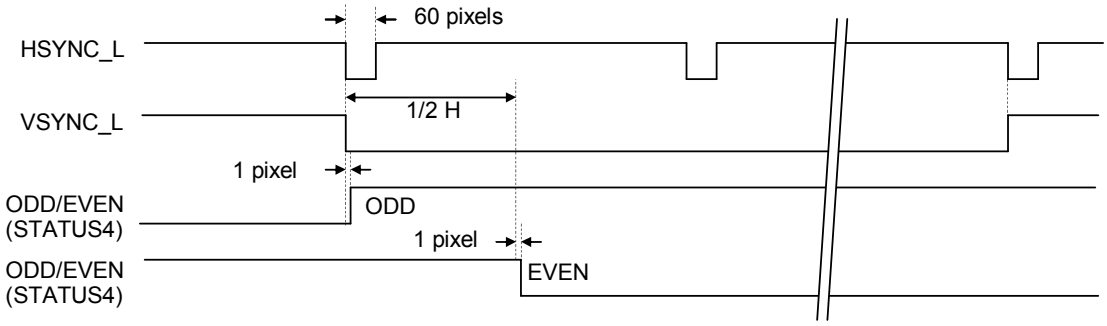
Video mode	Sampling pixel mode	Output pixel rate (MHz)	H					V		
			Front porch	Hsync Back porch	H blank	Active pixels	Total pixels	V blank	Active line	Total line
NTSC	ITUR.601	13.5	16	122	138	720	858	Odd/20 Even/20	Odd/243 Even/242	Odd/262.5 Even/262.5
	Square pixel	12.272727	22	118	140	640	780			
PAL/ SECAM	ITUR.601	13.5	12	132	144	720	864	Odd/24 Even/25	Odd/288 Even/288	Odd/312.5 Even/312.5

Note: Where the FIFO mode is used in asynchronous sampling operations with fixed clock, the 1-field sampling error accumulated in the line immediately following the fall of VVALID is reset. Therefore, the pixel count for the line that was reset will change. In addition, where the condition of VTR and other signals is poor in the FIFO-2 mode, the FIFO reset line might break in before the fall of VVALID.
In the above table, "V blank" indicates the line count during the "L" period of the VVALID signal, "Active line" the line count during the "H" period of the VVALID signal, and "Total line" the line count in 1 field.

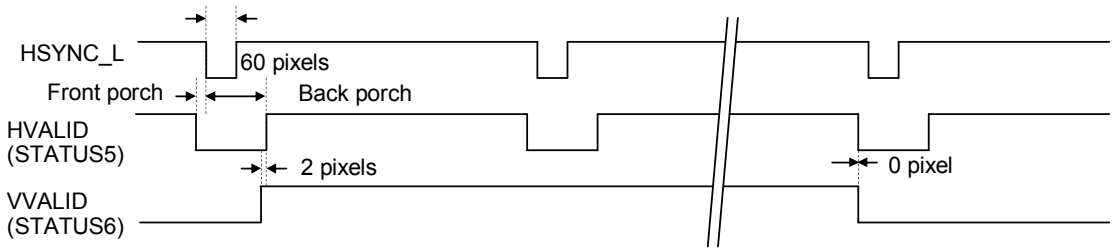
Sync Signals Output Timing (at Default/Standard Signal Input)

Each VALID signal and the ODD/EVEN signal are selected by the STATUS signal.

VSYNC_L, ODD/EVEN

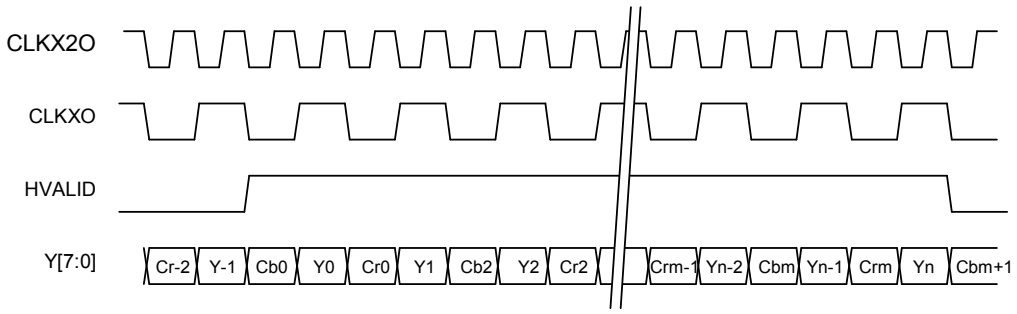


VALID Signal

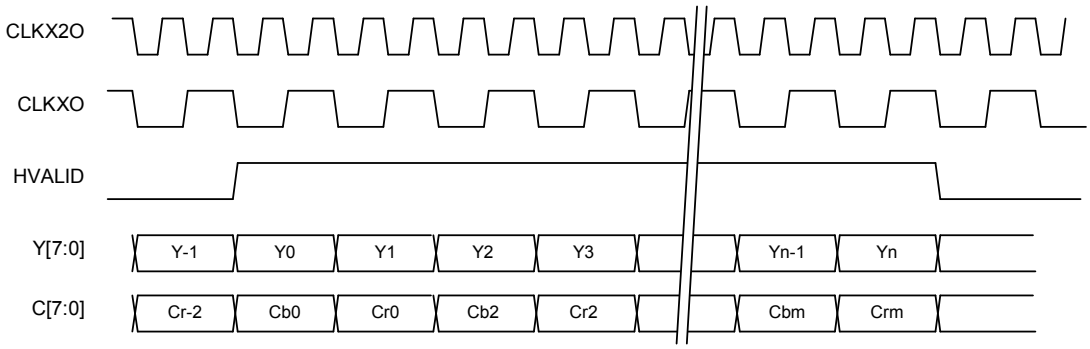


Output Timing by Mode

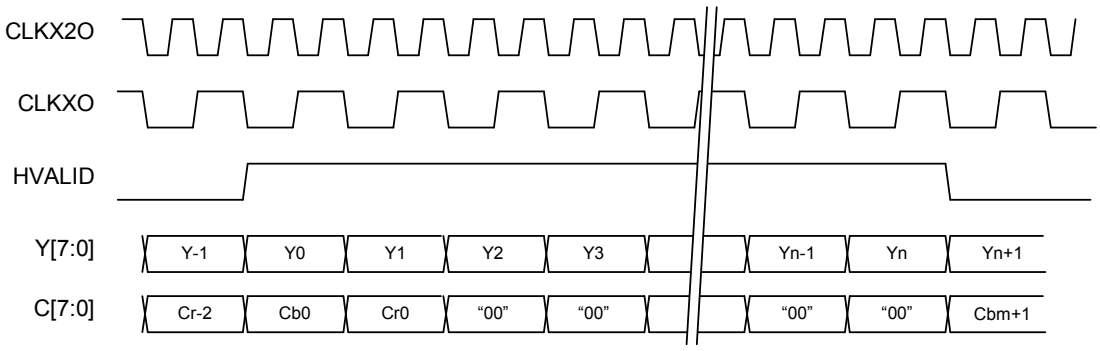
8-bit Y/CbCr (8 bits (Y/CbCr) (4:2:2))
(CLKX2O and CLKXO output setting ($02/IOC3 [1:0]): default)



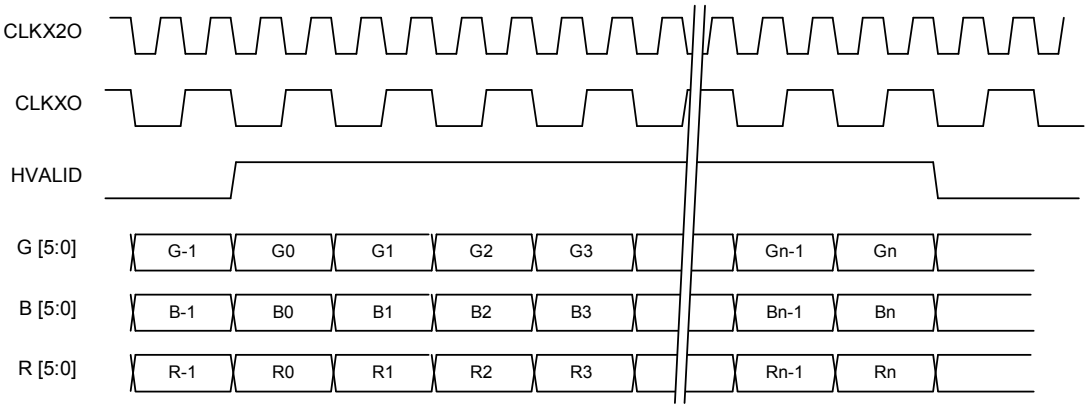
16-bit Y/CbCr (8 bits (Y) + 8 bits (CbCr) (4:2:2))
(CLKX2O and CLKXO output setting ($02/IOC3 [1:0]): default)



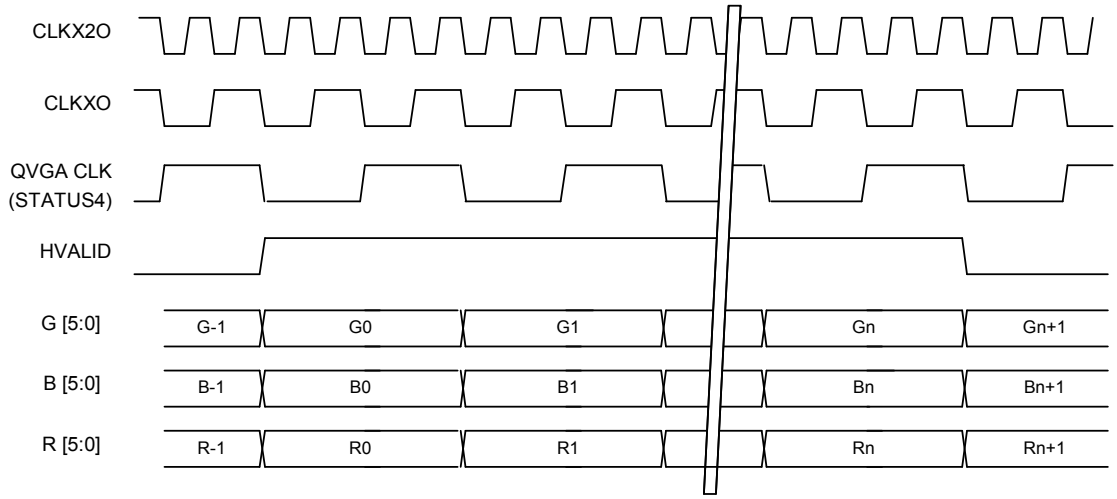
16-bit Y/CbCr (8 bits (Y) + 8 bits (CbCr) (4:1:1))
(CLKX2O and CLKXO output setting ($02/IOC3 [1:0]): default)



18-bit RGB (6 bits (R) + 6 bits (G) + 6 bits (B))
(CLKX2O and CLKXO output setting ($02/IOC3 [1:0]): default)

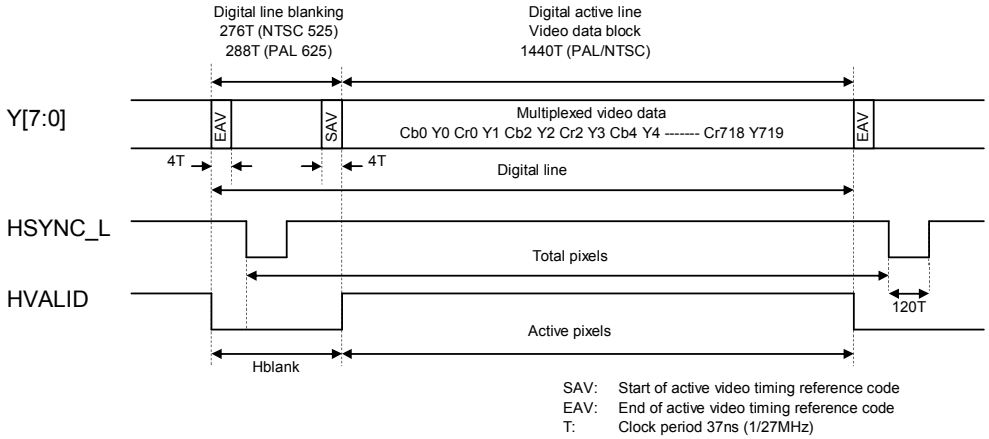


18-bit RGB (6 bits (R) + 6 bits (G) + 6 bits (B)) QVGA output
(CLKX2O, CLKXO, and QVGA output clock setting ($02/IOC3 [2:0]): default)



ITU-R BT.656-4 output:

Output is performed based on BT.656 of the ITU standards. Since sync signal information (SAV, EAV) is multiplexed with video data, for the interface that complies with BT.656, data can be transferred by connecting to 8-bit data lines, without connecting to the sync signal.
(When ITU-R BT.601 samplling mode is selected)



Note: When operating in asynchronous sampling mode, digital lines 1716T (NTSC, 525) and 1728T (PAL, 625) will change due to a sampling error.
In FIFO mode, the pixel count correction function ensures that there is no fluctuation in the pixel count between active lines, but the line immediately following the fall of VVALID will change due to a FIFO reset.
In particular, when non-standard signals such as VTR signals are input, the line immediately following the fall of VVALID will vary greatly in accordance with the degree of the instability of the input signal. Where the sampling error is large, the line will change immediately before the fall of VVALID.
In addition, in the case of such signals as non-standard signals where the line count increases or decreases with respect to the reference, even EAV and SAV may not be guaranteed.

INTERNAL REGISTERS

The following is a list of registers. Be sure to use only the subaddresses specified in the table below.
Refer to the User's Manual for details of each register.

Register	W/R	Sub Address	Bit								HEX
			MSB	Default Value						LSB	
			[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
IOC1	W/R	00	0	0	0	1	0	0	0	1	11
IOC2	W/R	01	0	0	0	0	0	0	0	0	00
IOC3	W/R	02	0	0	0	0	1	0	1	1	0B
IOC4	W/R	04	0	0	0	0	0	0	1	0	02
IOC5	W/R	05	0	0	0	0	0	0	0	0	00
FIFOBC	W/R	08	0	0	0	1	0	0	0	0	10
RR1	W/R	09	0	0	0	0	0	0	0	0	00
RR2	W/R	0A	0	0	0	0	0	0	0	0	00
YC1	W/R	10	0	0	0	0	0	0	0	0	00
YC2	W/R	11	0	0	0	1	0	0	0	0	10
YC3	W/R	12	0	0	0	0	0	0	0	0	00
SYNC1	W/R	20	0	0	0	1	0	0	0	0	10
SYNC2	W/R	21	0	0	0	0	0	0	1	0	02
SYNC3	W/R	22	0	0	0	0	0	0	1	0	82
HSTHR	W/R	23	1	0	0	1	1	1	1	1	9F
VSTHR	W/R	24	0	0	0	0	0	0	0	0	00
HSDL	W/R	25	0	0	0	0	0	0	0	0	00
HVALT	W/R	26	0	0	0	0	0	0	0	0	00
VVALT1	W/R	27	0	0	0	0	0	0	0	0	00
VVALT2	W/R	28	0	0	0	0	0	0	0	0	00
AGCC	W/R	30	0	1	0	0	0	0	0	1	41
AGCRC	W/R	31	0	0	0	0	0	0	0	0	00
LUMC1	W/R	32	0	0	0	0	0	0	0	0	00
LUMC2	W/R	33	1	0	0	0	0	1	0	0	84
LUMC3	W/R	34	0	0	0	0	0	0	0	0	00
LUMC4	W/R	35	0	0	0	0	0	0	0	0	00
CLC	W/R	36	0	0	0	0	0	0	0	0	00
LOFLC	W/R	37	0	0	0	0	0	0	0	0	00
ACCC	W/R	40	0	1	0	0	0	0	0	0	40
ACCRC	W/R	41	0	0	0	0	0	0	0	0	00
CHRC	W/R	42	0	0	0	0	0	0	0	0	00
CKILL1	W/R	43	0	1	0	0	1	0	0	0	48
CKILL2	W/R	44	0	0	0	1	0	1	0	0	14
HUE	W/R	45	0	0	0	0	0	0	0	0	00
CHRSC1	W/R	46	0	0	0	0	0	0	0	0	00
CHRSC2	W/R	47	0	0	0	0	0	0	0	0	00
BURSTD	W/R	48	1	0	0	0	0	0	0	0	80
CHRC2	W/R	49	0	0	0	0	0	0	0	0	00

Register	W/R	Sub Address	Bit								HEX
			MSB	Default Value						LSB	
			[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
BBHC1	W/R	50	1	0	0	0	1	0	0	1	89
BBHC2	W/R	51	0	0	0	0	0	0	0	0	00
RGBC	W/R	54	0	0	0	0	0	0	0	0	00
QVGAC	W/R	58	0	0	0	0	0	0	0	0	00
ADC1	W/R	68	1	1	1	0	0	0	0	0	E0
ADC2	W/R	69	0	0	1	1	1	1	1	1	3F
ADC3	W/R	6A	0	0	1	1	0	0	0	0	30
RR4	W/R	6B	0	0	0	0	0	0	0	0	00
RR5	W/R	6C	1	1	1	1	0	0	1	1	F3
PLLC1	W/R	70	0	0	0	0	0	0	0	0	00
PLLC2	W/R	71	0	0	0	0	0	0	0	0	00
PLLC3	W/R	72	0	0	0	0	0	0	0	0	00
PLLC4	W/R	73	0	0	0	0	0	0	0	0	00
STA1	W/R	78	0	1	1	0	0	1	0	0	64
STA2	W/R	79	0	0	1	1	0	0	1	0	32
STA3	W/R	7A	0	0	0	1	0	0	0	0	10
VBIDC	W/R	80	0	0	0	0	0	0	0	0	00
VBIDM	W/R	81	1	0	0	0	0	1	1	0	86
CCD	W/R	82	0	0	0	0	0	0	0	0	00
CGMS1	W/R	84	0	0	0	0	0	0	0	0	00
CGMS2	W/R	85	0	0	0	0	0	0	0	0	00
AGCD1	W/R	86	0	0	0	0	0	0	0	0	00
AGCD2	W/R	87	0	0	0	0	0	0	0	0	00
WSSD	W/R	88	0	0	0	0	0	0	0	0	00
RSTVBID	W/R	89	0	0	0	0	0	0	0	0	00
STATUS1	R	90	—	—	—	—	—	—	—	—	—
STATUS2	R	91	—	—	—	—	—	—	—	—	—
VFLAG	R	92	—	—	—	—	—	—	—	—	—
CCDO0	R	93	—	—	—	—	—	—	—	—	—
CCDO1	R	94	—	—	—	—	—	—	—	—	—
CCDE0	R	95	—	—	—	—	—	—	—	—	—
CCDE1	R	96	—	—	—	—	—	—	—	—	—
CGMSO0	R	97	—	—	—	—	—	—	—	—	—
CGMSO1	R	98	—	—	—	—	—	—	—	—	—
CGMSO2	R	99	—	—	—	—	—	—	—	—	—
CGMSE0	R	9A	—	—	—	—	—	—	—	—	—
CGMSE1	R	9B	—	—	—	—	—	—	—	—	—
CGMSE2	R	9C	—	—	—	—	—	—	—	—	—
WSS0	R	9D	—	—	—	—	—	—	—	—	—
WSS1	R	9E	—	—	—	—	—	—	—	—	—

NOTES ON USE

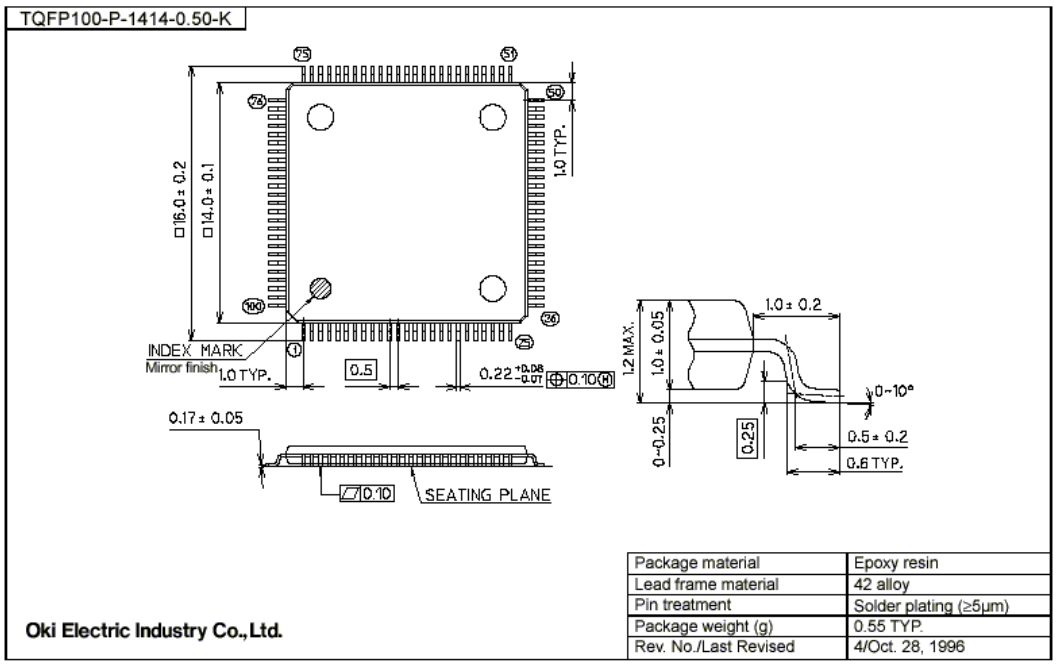
The ML86V7668A Video Decoder is being developed based on standard signals. Improvements are being made to ensure stable operation even with non-standard signals. However, the signal conditions and usage environments differ widely for signals such as those having a weak electromagnetic field, VTR playback signals, signals with numerous signal switching or a large amount of noise, and simple video signals from various cameras. As a result, stable operation for all signals has not yet been confirmed. Before using the decoder, please carefully evaluate and consider the signal conditions and usage environment of the intended use.

In addition to this Data Sheet, an ML86V7668A User's Manual is also available. The User's Manual explains each register and provides examples of adapted circuits as well as other information helpful in the design phase. Please read the User's Manual before embarking on design work.

Users are also requested to regularly download the most recent versions of this Data Sheet and the User's Manual from the Oki web site. Since the newest information, not included in printed materials, and the answers to frequently asked questions are published on the web site, users are recommended to check the site regularly for updates.

PACKAGE DIMENSIONS

(Unit: mm)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL86V7668A-01	Jan. 29, 2007	–	–	Final edition 1

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

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   Such applications include, but are not limited to, traffic and automotive equipment, safety devices, aerospace equipment, nuclear power control, medical equipment, and life-support systems.

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