FEDL87V5002-01
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OKI Semiconductor

ML87V5002

Audio Delay IC with Built-in 2-Mbit DRAM

GENERAL DESCRIPTION

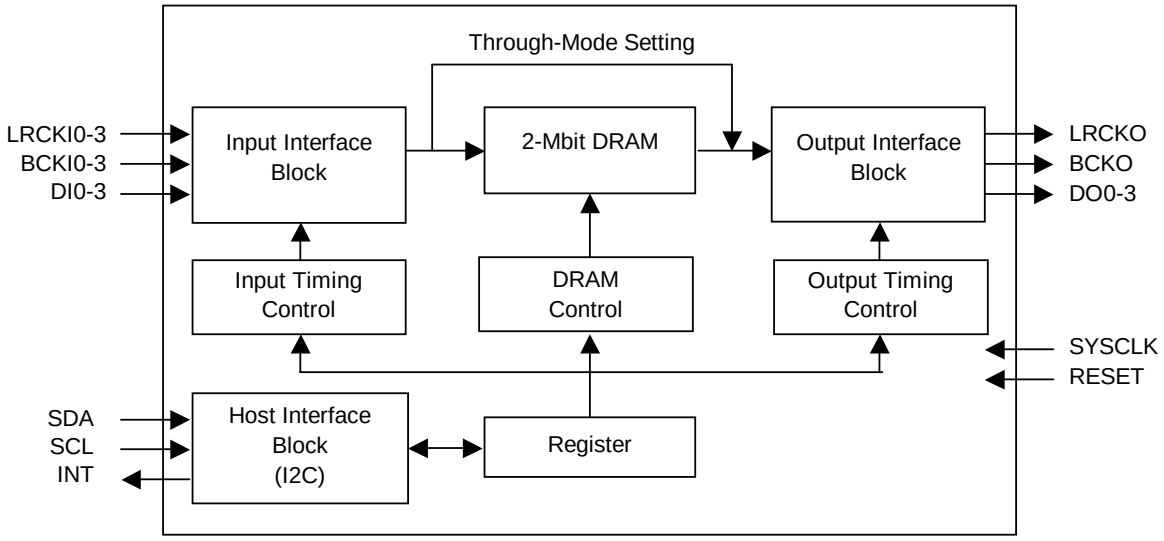
The ML87V5002 has been developed for solving "Lip-sync problems" in DVD systems, hard disc recording devices, digital TVs and Home Theater Systems. The ML87V5002 can delay the digital audio signal of each of eight channels by setting each register. The ML87V5002 is suitable for synchronizing sounds with motions when loads are too heavy for DSP to control audio delay.
The ML87V5002 does not require any external memory for the audio delay because the ML87V5002 has a built-in 2-Mbit DRAM. The maximum delay time is, for example, 341.3 ms at 48 kHz in 8-ch mode and 1.365 sec at 48 kHz in 2-ch mode. Supporting two to eight audio channels; the ML87V5002 is suitable for applications ranging from simple stereo systems to multi-channel systems. The granularity of the delay time is the sampling period, or Ts. The delay time of each channel can be set in steps of Ts.
The ML87V5002 interfaces to most audio LSIs since the ML87V5002 supports general digital audio formats, such as I^2S, right justified, and left justified. In addition, suitable digital audio formats can be selected as each of the input and output formats.

FEATURES

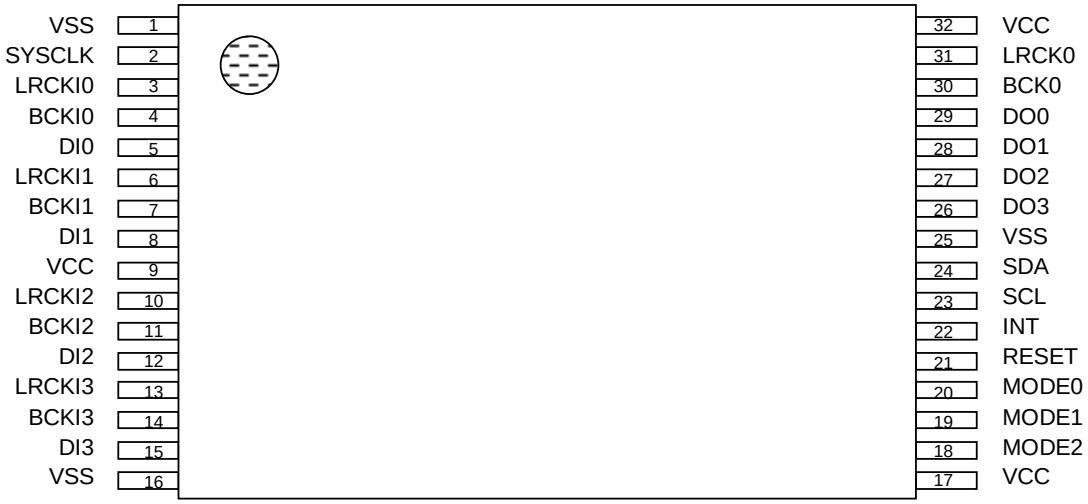
- **Digital audio delay control:** The digital audio signals input from the DI0-DI3 pins are delayed for specific delay times set by an external device and are output from the DO0-DO3 pins.
- **No external memory:** No external memory is required for the delay because the 2-Mbit DRAM is included.
- **Three digital-audio formats:** I^2S, right justified and left justified formats.
- **Input/output format settings:** I^2S, right justified, or left justified format can be selected as each of the input and output formats.
- **Data bit lengths:** 16/20/24/32 bits
- **Wide range sampling frequencies:** 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, and 192 kHz
- **Maximum audio delay time:**
  The maximum delay time (when the audio data length is 16 bits)
  - 1.365 sec (48 kHz, 2-ch mode)
  - 682.5 ms (96 kHz, 2-ch mode)
  - 341.3 ms (192 kHz, 2-ch mode)
  - 341.3 ms (48 kHz, 8-ch mode)
  - 170.7 ms (96 kHz, 8-ch mode)
  - 85.3 ms (192 kHz, 8-ch mode)
- Standard host interface: I^2C slave interface is supported.
- Minimum delay time step: The granularity of delay time is Ts.
- Independent delay time setting: The delay time of each channel can be set.
- General power supply voltage: 3.3 V ±0.3V
- 5V tolerant I/O: Audio interface inputs, I^2C, and INT are tolerant to 5 V.
- Package:
  32-pin plastic TSOP type I (TSOP(1)32-P-0814-0.50-1K)

Note:
- System clock requirements
  - Frequency
    The frequency of the system clock should be 128 times the sampling frequency or more. When the sampling frequency is 192 kHz, be sure to set the system clock frequency at 128 times the sampling frequency.
  - Phase
    The system clock should be synchronized with LRCK and the BCK. In synchronized condition, the phase variation is acceptable.

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



32-Pin Plastic TSOP Type I

PIN DESCRIPTION

Pin	Symbol	I/O	Description
3 6 10 13	LRCKI0 LRCKI1 LRCKI2 LRCKI3	I	The LRCK inputs of the input interface In the 2-channel mode, LRCKI0 to LRCKI3 correspond to DI0 to DI3, respectively. The polarity of LRCKI can be set by the internal register.
4 7 11 14	BCKI0 BCKI1 BCKI2 BCKI3	I	The BCK inputs of the input interface In the 2-channel mode, BCKI0 and BCKI3 correspond to DI0 to DI3, respectively. The number of BCK pulses in the 1LRCK should be 2× the number of the input bits or more.
5 8 12 15	DI0 DI1 DI2 DI3	I	The data input pins of the input interface The data is latched in at the rising edges of BCKI0-3.
31	LRCKO	O	The LRCK output pin of the output interface The polarity of LRCKO can be set by the internal register.
30	BCKO	O	The BCK output pin of the output interface In the internal generation mode, the number of BCK pulses in 1LRCK can be set by the internal register.
29 28 27 26	DO0 DO1 DO2 DO3	O	The data output pins of the output interface The data is output at the falling edge of BCKO.
20	SCL	I	The clock input pin of I^2C (SCL)
24	SDA	I/O	The address data pin of I^2C (SDA)
22	INT	O	The output pin for the interrupt signal to the host CPU Open drain output
2	SYSCLK	I	The input pin of system clock The system clock should be synchronized with LRCKI and BCKI and the frequency should be 128 times the sampling frequency or more.
21	RESET	I	The reset pin of the ML87V5002 Reset is continued while this pin is low.
20 19 18	MODE0 MODE1 MODE2	I	I^2C address setting pins
9,17,32	VCC	PW	Power supply
1,16,25	VSS	PW	Ground

Note: The equal supply voltage should be applied to each VCC pin.
The equal supply voltage should be applied to each VSS pin.
The input pins and I/O pins are tolerant to 5 V.
The output pins support 3.3 V and should not be connected to signal lines with voltages exceeding the supply voltage (VCC).

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating Value	Unit
Power Supply Voltage	VCC	Ta = 25°C	–0.3 to +4.6	V
Input Voltage	V_I	Ta = 25°C	–0.3 to +6.0	V
Short Circuit Output Current	I_{OS}	Ta = 25°C	50	mA
Power Dissipation	P_D	Ta = 25°C	1	W
Operating Temperature	T_{opr}	—	0 to 70	°C
Storage Temperature	T_{stg}	—	–50 to +150	°C

Note: Stressing the device beyond the “ABSOLUTE MAXIMUM RATINGS”, even momentarily, may cause permanent damage.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	VCC	3.0	3.3	3.6	V
Power Supply Voltage	VSS	0	0	0	V
Operating Temperature	Ta	0	—	70	°C

PIN CAPACITANCE

(VCC = 3.3 V ±0.3V, f = 1 MHz, Ta = 25°C)

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance	C_i	—	7	pF
Input Output Capacitance	C_{io}	—	7	pF
Output Capacitance	C_o	—	7	pF

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta = 0 to 70°C, VCC = 3.3 V ±0.3V, VSS = 0 V)

Parameter	Symbol	Condition	Min.	Max.	Unit
High-level input voltage	V_{IH1}	—	VCC×0.7	5.5	V
Low-level input voltage	V_{IL1}	—	–0.3	VCC×0.3	V
High-level input voltage (SDA, SCL)	V_{IH2}	—	VCC×0.75	5.5	V
Low-level input voltage (SDA, SCL)	V_{IL2}	—	–0.3	VCC×0.25	V
High-level output voltage	V_{OH}	I_{OH} = –4 mA	2.4	—	V
Low-level output voltage	V_{OL}	I_{OL} = 4 mA	—	0.4	V
Low-level output voltage (SDA, INT)	V_{OL2}	I_{OL} = 4 mA	—	0.4	V
Input Leakage Current	I_{LI}	V_{IN} = VCC or VSS	–10	+10	µA
Output Leakage Current	I_{LO}	V_{OUT} = VCC or VSS	–10	+10	µA
Supply Current (during operation)	I_{DD1}	SYSCLK = 24.576 MHz	—	30	mA
Supply Current (during standby)	I_{DD2}	Input pin = 0 V	—	4.5	mA

AC Characteristics

The SYSCLK (system clock) should be synchronized with inputs LRCK and BCK.

(Ta = 0 to 70°C, VCC = 3.3 V ±0.3V, VSS = 0 V)

Parameter	Symbol	Condition	Min.	Max.	Unit
SYSCLK Cycle Time	t_{SYSCLK}	—	40	—	ns
SYSCLK High-Level Time	t_{SYSCKH}	—	16	—	ns
SYSCLK Low-Level Time	t_{SYSCKL}	—	16	—	ns
BCKI Cycle Time	t_{BCLKI}	—	80		ns
BCKI High-Level Time	t_{BCKIH}	—	30		ns
BCKI Low-Level Time	t_{BCKIL}	—	30		ns
DI Setup Time (Ext. sync. / Int. gen.)	t_{DIS}	—	6	—	ns
DI Hold Time (Ext. sync. / Int. gen.)	t_{DIH}	—	8	—	ns
LRCKI Setup Time	t_{LCKIS}	—	6	—	ns
LRCKI Hold Time	t_{LCKIH}	—	8	—	ns
BCKO Delay Time (Ext. sync. / Through mode)	t_{BCKDT}	—	—	15	ns
DO Delay Time (Ext. sync. / Int. gen.)	t_{ODD}	C_L = 20pF	–7	12	ns
DO Delay Time (Through Mode)	t_{ODT}	C_L = 20pF	—	15	ns
LRCKO Delay Time (Int. gen.)	t_{LCKOD}	C_L = 20pF	–7	12	ns
LRCKO Delay Time (Ext. sync. / Through mode)	t_{LCKDT}	C_L = 20pF	—	15	ns
Input Rise Time, Input Fall Time	t_T	Except SDA and SCL	1	5	ns
Reset Pulse Time	t_{RSTP}	—	100	—	ns

Note: The input voltage level is measured at VCC/0V. The confront level of the output signal is measured at VCC/2.

Input/Output Waveforms

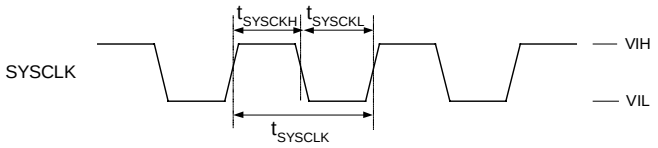


Figure 1 System Clock Diagram

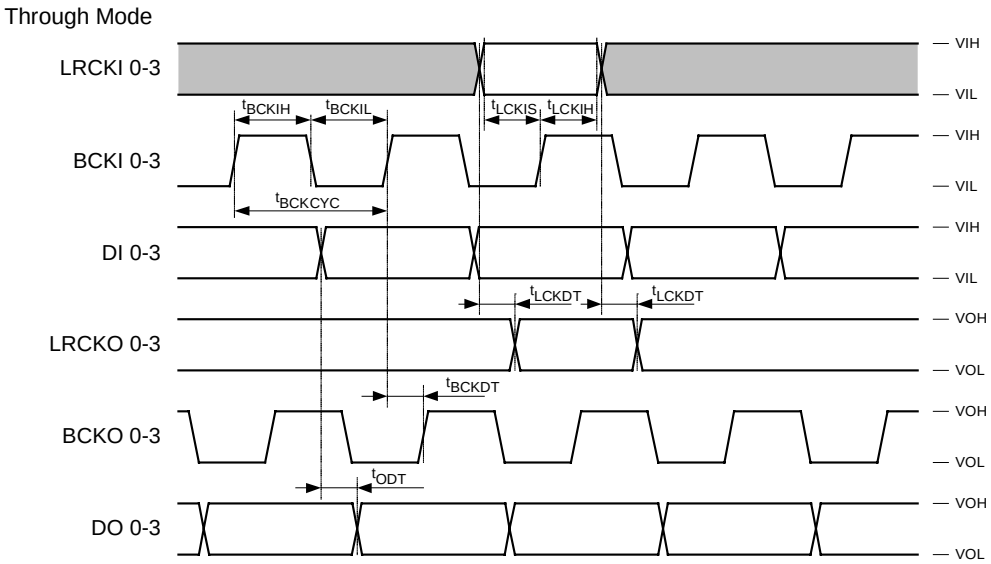


Figure 2 Through-Mode Input and Output Timing Diagram

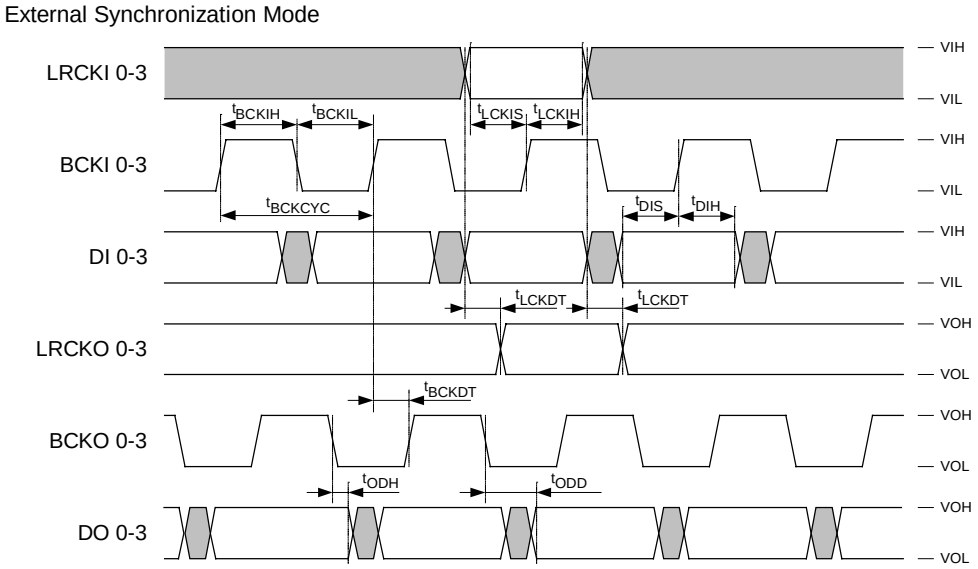


Figure 3 External Sync. Mode Input and Output Timing Diagram

Internal Generation Mode

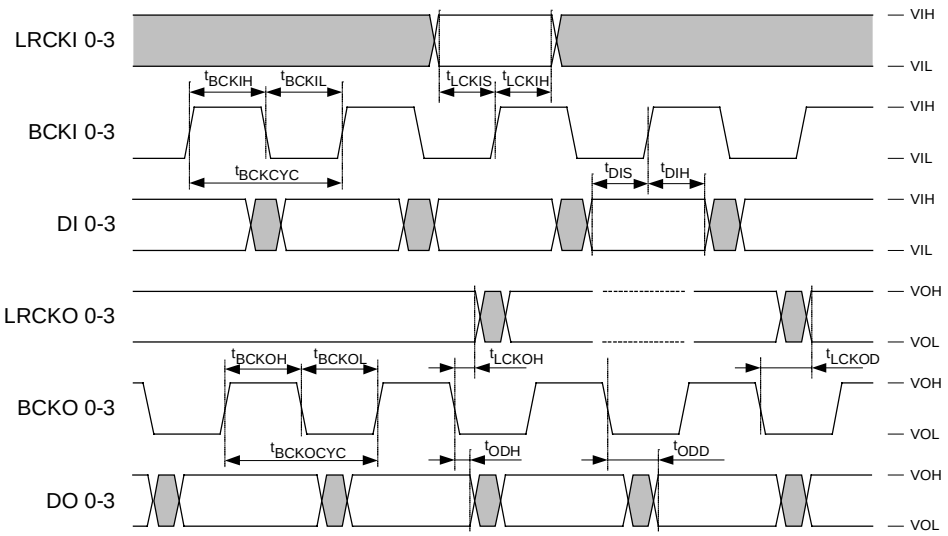


Figure 4 Internal Sync. Mode Input and Output Timing Diagram

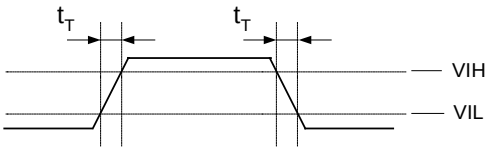


Figure 5 Rise Time, Fall Time (t_T)

I²C Interface Timing

The internal register setting is done via I²C Interface. The interface is based on the standard mode I²C bus (SCL frequency = 100 kHz).
Fig. 6 shows the basic timing. Table 1 summarizes the AC Characteristics of the standard mode I²C bus. Do not change the "SDA" level as long as the "SCL" is high except the stop or start condition. Refer to the "AC Characteristics" to know the values of timing parameters.

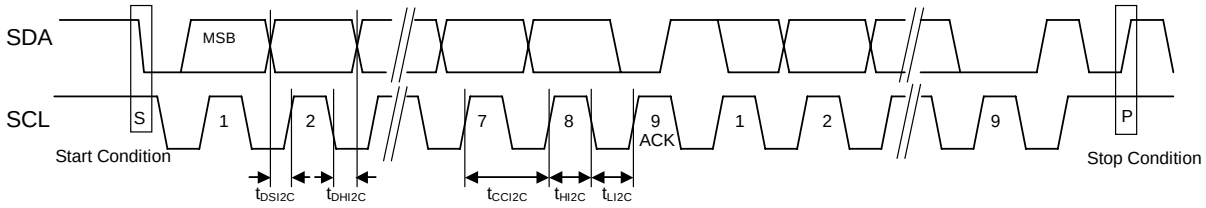


Figure 6 I²C Interface Basic Timing

Table 1 AC Characteristics of Standard Mode I²C Bus (SCL Frequency = 100 kHz)

Parameter	Symbol	Min.	Max.	Unit
Reset Pulse Time	t_{RSTP}	100	—	ns
I²C Clock Cycle Time	t_{CCI2C}	10	—	µs
I²C Clock High-Level Time	t_{HI2C}	4	—	µs
I²C Clock Low-Level Time	t_{LI2C}	4.7	—	µs
I²C Data Setup Time	t_{DSI2C}	250	—	ns
I²C Data Holdup Time	t_{DHI2C}	0	3.45	µs

Power-On

For the normal operation of the ML87V5002, the pins other than the RESET pin should be maintained at a low level until the VCC has reached the specified voltage level after powered on. Thereafter this LSI is reset by maintaining the RESET pin at a low level for 1 ms or more. The release of the RESET level leads to starting normal operation.
To reset this LSI during normal operation, set the RESET pin at a "L" level for a time t_{RSTP} or more.
To power on again after powered off, verify that VCC is 0 V.

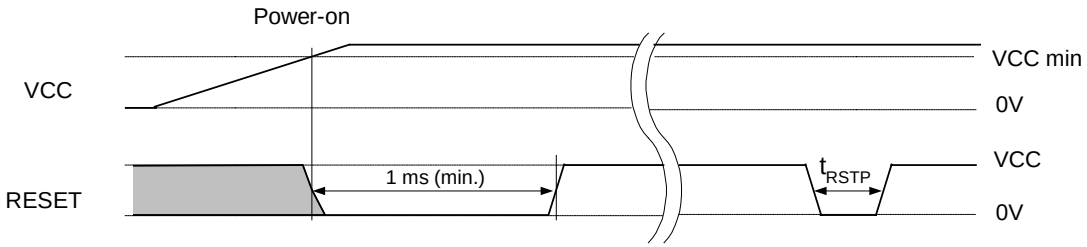


Figure 7 Power-On Sequence

FUNCTIONAL OPERATION

Mode of Operation

The ML87V5002 has two modes, 2-channel mode and 8-channel mode. Mode setting is done by the host CPU via the I^2C interface. When internal register "NOF_CH" (SUB:00h-bit[2]) is set to "0", the 2-channel mode is set. When "NOF_CH" is set to "1", the 8-channel mode is set.

- 2-channel mode

In the 2-channel mode, there are four input groups, group0-3. The inputs in group-0 are comprised of LRCK0,BCKI0 and DI0. The inputs in group-1 are LRCK1, BCK1 and DI1. The inputs in group-2 are LRCKI2, BCKI2 and DI2. The inputs in group-3 are LCRKI3, BCKI3 and DI3. That is, in the 2-channel mode, it looks four independent delay devices having a common 2-channel input can be provided. The common 2-channel input is connected to the output terminal of the selector that has four input as shown in Fig.7. One of the four inputs can be selected by the setting of the internal register "DI_SEL" (SUB:00h-bit[1:0]) as shown in the Table 2.

Table 2 Input Source Selection (SUB:00h-bit[1:0])

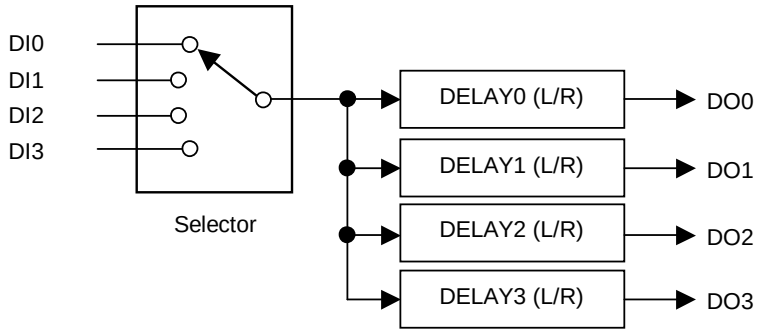
DI_SEL		Selectable Input Source
[1]	[0]	
0	0	DI0
0	1	DI1
1	0	DI2
1	1	DI3

The 2-channel input audio data is selected and transferred to the four delay devices via the common input terminal and being delayed for certain periods. The delayed data are output from DO0 - DO3 controlled by LRCKO and BCKO. Each delay time for the DO0 - DO3 can be set independently by the setting of internal regisiter, "DLYx_L" (x=0 - 7, SUB:10h-bit[7:0] - SUB:1fh-bit[7:0]) and "DLYx_H" (x=0 - 7, SUB:10h-bit[7:0] - SUB:1fh-bit[7:0]). The settings are shown in the Table 3.

Table 3 Delay Time Setting of Each Output

	L/R	Channel	Register Name	SUB
DO0 Delay Time DELAY0	Lch	CH0	DLY0_L	10h-bit[7:0]
			DLY0_H	11h-bit[7:0]
	Rch	CH1	DLY1_L	12h-bit[7:0]
			DLY1_H	13h-bit[7:0]
DO1 Delay Time DELAY1	Lch	CH2	DLY2_L	14h-bit[7:0]
			DLY2_H	15h-bit[7:0]
	Rch	CH3	DLY3_L	16h-bit[7:0]
			DLY3_H	17h-bit[7:0]
DO2 Delay Time DELAY2	Lch	CH4	DLY4_L	18h-bit[7:0]
			DLY4_H	19h-bit[7:0]
	Rch	CH5	DLY5_L	1ah-bit[7:0]
			DLY5_H	1bh-bit[7:0]
DO3 Delay Time DELAY3	Lch	CH6	DLY6_L	1ch-bit[7:0]
			DLY6_H	1dh-bit[7:0]
	Rch	CH7	DLY7_L	1eh-bit[7:0]
			DLY7_H	1fh-bit[7:0]

Figure 8 shows the concept of the 2-channel mode.



*1. DELAY0 (L/R), DELAY1 (L/R), DELAY2 (L/R), and DELAY3 (L/R) can be set independently.

*2. The input format and sampling frequency for each of DI0 to DI3 can be set.

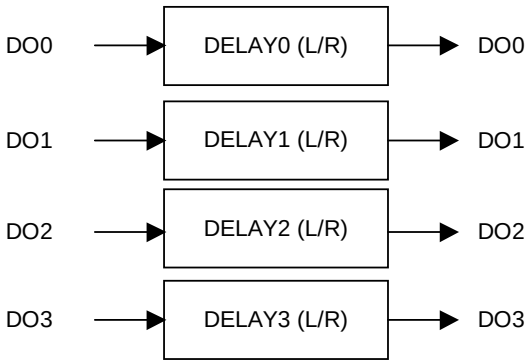
*3. The output format and the input format can be set independently, however, the output format for DO0 to DO3 is equal.

Figure 8 Conceptual Diagram of 2-Channel Mode

• 8-channel mode

In the 8-channel mode the ML87V5002 operates as an 8-channel audio interface input. In this case, LRCKI0 and BCKI0 are used. Note that LRCKI1, LRCKI2, LRCKI3, BCKI1, BCKI2 and BCKI3 are not used in the 8-channel mode. The data of each channel is input to DI0 to DI3 and is delayed for the set delay time. The data input to DI0 to DI3 are output from DO0 to DO3 having certain delay times, respectively. The delay time of each input can be set by the internal registers "DLYx_L" (x=0 to 7, SUB:10h-bit[7:0] to SUB:1fh-bit[7:0]) and "DLYx_H" (x=0 to 7, SUB:10h-bit[7:0] to SUB:1fh-bit[7:0]).

Figure 9 shows the concept of 8-channel mode



*4. DELAY0 (L/R), DELAY1 (L/R), DELAY2 (L/R), and DELAY3 (L/R) can be set independently.

*5. The output format and the input format can be set independently.

Figure 9 Conceptual Diagram of 8-Channel Mode

Operation Sequence

When reset is released, the internal register INIT(SUB:08h-bit[0]) is set to "1" and the ML87V5002 starts the initial sequence and then starts its normal operation.
The ML87V5002 keeps the command-wait state (waiting for the register setting of the host CPU) after the initial sequence. In this command-wait state, the delay operation is not started and the output keeps mute states. The delay operation is started by writing each parameter from the host CPU to the internal register and setting internal register "ENBL" (SUB:07h-bit[7]) to "1".
When internal register "ENBL" (SUB:07h-bit[7]) is set to "1", the ML87V5002 starts to investigate the validity of the settings. If the settings are proper, internal register "RUN" (SUB:08h-bit[7]) is set to "1", the mute state is released, and the delay operation is started.

• Suspension of the delay operation

This LSI sets the ENBL and RUN bits to "0" and suspends the delay operation when any of the following events occurs:

1. "0" is written to internal register ENBL (SUB:07h-bit[7]).
2. The signals of LRCKI and BCK become out of synchronization.
3. The setting of the audio format except the delay parameters is changed.
4. Input source channel is changed.
5. Operation mode is changed.
6. The operation is started on condition that parameters at settings are not proper.
7. The BCK pulses less than the data length are input.
8. Overrun or underrun occurs due to a mismatch in clock between the input and output.

When the suspension is caused by event 2, 6, 7, or 8 above, the LSI mutes the output immediately and sets the corresponding error bits in the internal registers shown in Table 4 to "1".

Table 4 Error Status Registers

Register Name	Error Description	SUB
TMG_ERR	Set when any change is detected in the input timing after resuming the operation and the LSI suspends the delay operation.	09h-bit[7]
CFG_ERR	Indicates the delay operation is suspended due to inconsistency of the setting values.	09h-bit[6]
BCK_ERR	Set when the number of BCK pulses in LRCK is less than the input data length or the output data length in external synchronization mode after starting the operation. The delay operation is suspended.	09h-bit[5]
OVRN	Set when the output data cycle is slower than the input cycle and the delay buffer overflows, and the delay operation is suspended.	09h-bit[4]
UDRN	Set when the output data cycle is faster than the input cycle and the delay buffer becomes empty, and the delay operation is suspended.	09h-bit[3]

• Restart of delay operation (restart by a command / auto-restart)

There are two options, “restart by a command” and “auto-restart”, for restarting the delay operation by setting the internal register.
In the case of the “restart by a command”, the INT output is set at “L” at athe same time as error detection. The delay operation is restarted by removing the cause of the error and writing “1” to the “ENBL” bit.
In the case of the “auto-restart” option (the internal register AUTORSTRT (SUB 07h-bit[1] = “1”), if the suspension is due to an error [TMG_ERR, OVRN, or UDRN] excluding CFG_ERR and BCK_ERR, set the error bit to “1” to restart the delay operation. (In this case, this LSI does not set the INT output at “L” or not generate the interrupt even if the interrupt mask register is cleared.)
In the case of the “auto-restart” option, if an error is detected and CFG_ERR or BCK_ERR is set to “1”, the LSI clears the ENBL bit to “0” and stops the delay operation. (In this case, this LSI sets the INT output at “L” and generates the interrupt if the interrupt mask register has been cleared.) Since the error bit is not automatically cleared, the host CPU writes “0” to the corresponding bit and clears the error bit.

• Change of the delay parameters during the delay operation

When the newly set value of the delay time is less than the previously set value, the reading pointer is moved forward and the operation is performed with a new delay time. In this case, the data existing between the times before and after the change is not output phonetically. (Figure 10)

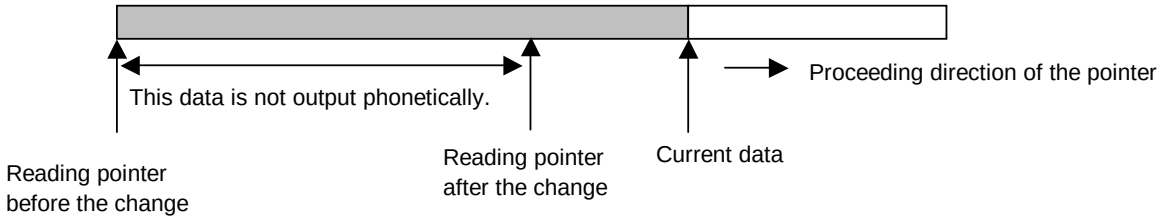


Figure 10 When a delay time is changed (when the delay time is shorter than the previously set time.)

Meanwhile, when the newly set value is longer than the former set value, the reading pointer should be moved backward and the operation should be performed with a new delay length. Output is muted (“0” output) for the insufficient data (Figure 11).

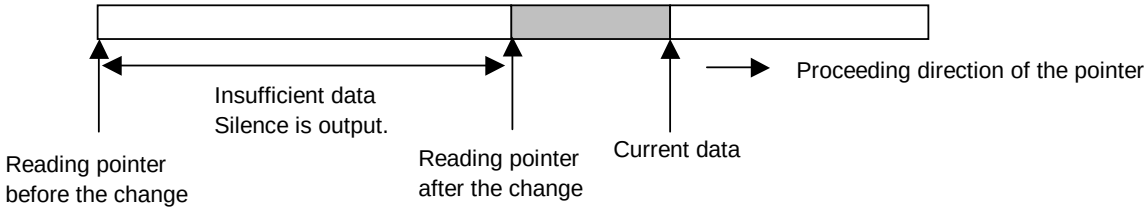


Figure 11 When a delay time is changed (when the delay time is longer than the previously set time.)

When a delay time is shortened once and then it is lengthened, the audio data is output when the valid audio data is in the memory. Output is muted (“0” output) until the pointer reaches the valid data when no valid audio data is in the memory.(Figure 12)

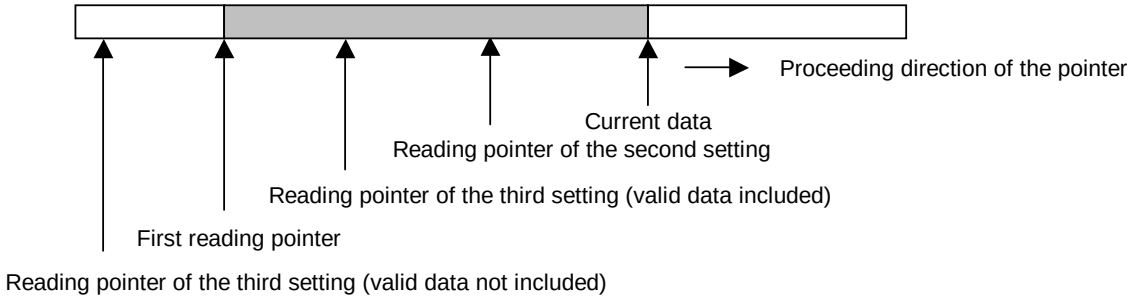


Figure 12 When a delay time is shortened once and then lengthened

Operation of Audio Input/Output Port

By setting the audio input ports (DI0 to DI3, LRCKI0 to LRCKI3, and BCKI0 to BCKI3) and the audio output port (DO0 to DO3, LRCKO, and BCKO) according to the internal register provided in the table 5-10, the formats can be changed. Figure 12 shows the formats supported by the ML87V5002.

Table 5 LRCKI Polarity Specification (SUB:01h-bit[4])

POLI	LRCKI polarity
[0]	
0	Non-inverted
1	Inverted

Table 6 Input Format Specification (SUB:01h-bit[3:2])

FMTI		Format
[1]	[0]	
0	0	Left justified
0	1	Right justified
1	0	I^2S
1	1	I^2S

Table 7 Input Data Bit Length Specification (SUB:01h-bit[1:0])

DI_LEN		Data bit length
[1]	[0]	
0	0	16 bits
0	1	20 bits
1	0	24 bits
1	1	32 bits

Table 8 LRCKO Polarity Specification (SUB:02h-bit[4])

POLO	LRCKI polarity
[0]	
0	Non-inverted
1	Inverted

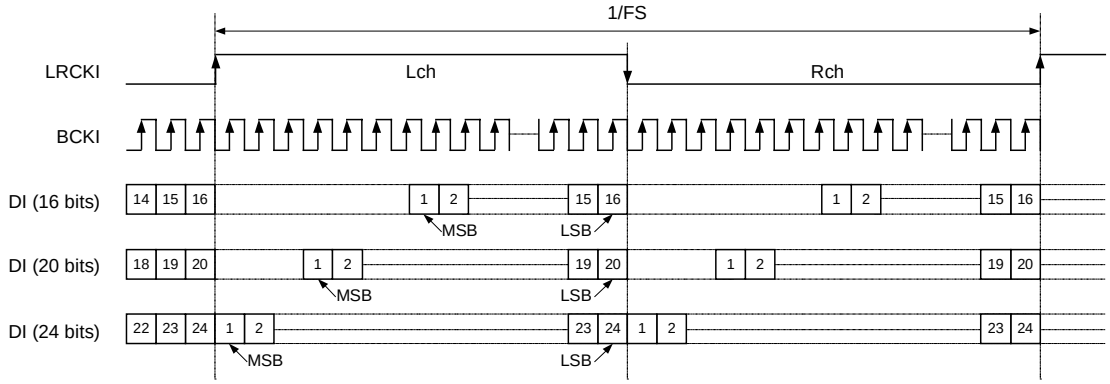
Table 9 Output Format Specification (SUB:02h-bit[3:2])

FMTO		Format
[1]	[0]	
0	0	Left justified
0	1	Right justified
1	0	I^2S
1	1	I^2S

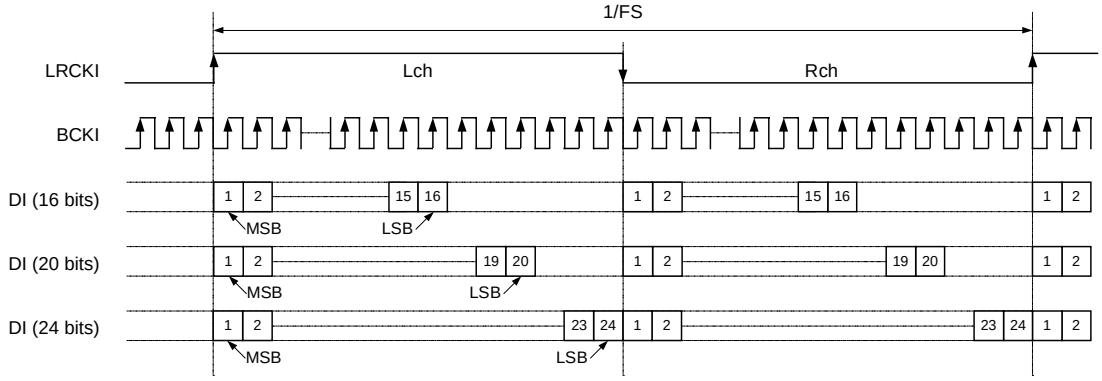
Table 10 Output Data Bit Length Specification (SUB:02h-bit[1:0])

DO_LEN		Data bit length
[1]	[0]	
0	0	16 bits
0	1	20 bits
1	0	24 bits
1	1	32 bits

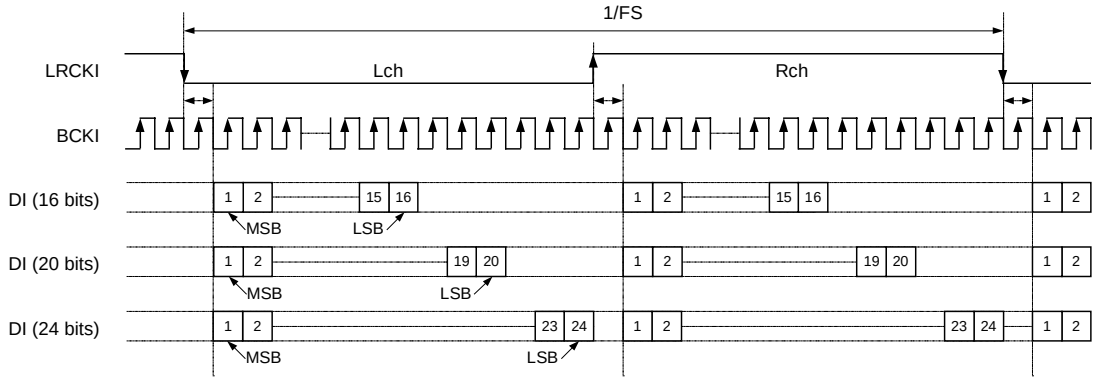
• Right justified format



• Left justified format



• I^2S format



Notes:

1. In the I^2S format, the MSB data is fixed with a delay of 1 BCK from left justify, and LRCK is inverted.
2. The data and LRCK alter on the falling edge of BCK.
3. The number of BCK pulses to LRCK requires twice the data length or more.
4. This figure shows the case where LRCK is not inverted.

Figure 13 Supported Format

Input and Output Data Lengths of DI0-3/DO0-3

This LSI can output data by changing the data length of input data. For instance, the LSI can output the 16-bit data that is input as 20-bit data. When the output bit count is greater than the input bit count, the same value as MSB is output for the lower-order bits. For instance, when the data that is input in a 16-bit length is output in a 20-bit length, the higher-order 16 bits contain the value of the input data and '0' is output in the lower-order 4 bits if MSB is '0' and '1' if MSB is '1'. When the input bit count is greater than the output bit count, the lower-order bits are ignored at output.
However, the data length must be equal to or less than 1/2 of the BCK clock count per LRCK. For instance, when 1 LRCK contains 40 BCKs, the data length must not exceed 20 bits. When the length exceeds 20 bits, BCK_ERR is set during checking performed at the start of operation, the LSI does not start operation, but activates the INT signal, and reports the occurrence of an error to the host CPU. However, when INTMASK is set (SUB:07h-bit[0] ='1'), the INT signal is not output.

External Synchronization Mode/Internal Generation Mode of LRCK/BCK

Two modes are available for signals LRCKO and BCKO, "external synchronous mode (including Through mode)" and "internal generation mode".
In external synchronous mode [INT_EXT (SUB:00h-bit[3])='0' or THRU (SUB:00h-bit[4])='1'], BCKIx that is selected by a combination of NOF_CH and DI_SEL is output through the BCKO pin.
For LRCKO, polarity reversal is performed by POLI, POLO, FMTI, or FMTO for LRCKIx that is selected by a combination of NOF_CH and DI_SEL and the result is output.
LRCKO and BCKO are definitely output regardless of the status of the RUN bit when LRCKIx and BCKIx are input.
In internal generation mode [INT_EXT (SUB:00h-bit[3])='1' and THRU (SUB:00h-bit[4])='0'], LRCKO and BCKO are generated from SYSCLK. As a result, a format different from that of input can be set without being restricted by [output data length ≤ number of BCKIs in LRCK/2] in external synchronous mode.
The LRCKO period can be set in internal register LRCK_DIV (SUB:04h-bit[3:0]) and the BCKO period can be set in internal register BCK_DIV (SUB:03h-bit[3:0]). (However, the LRCKO period that is generated by the setting of LRCK_DIV and BCK_DIV must match the LRCKI period). In internal generation mode, LRCKO and BCKO are not output while internal register RUN (SUB:08h-bit[7]) is set to '0'. For instance, when the internal generation mode is set immediately after reset, internal register ENBL (SUB:07h-bit[7]) is set to '1' and the RUN bit is set to '0' until delay operation starts. Therefore, LRCKO and BCKO are not output. When operation is stopped due to an error detected during normal operation and the RUN bit is cleared to '0', output of LRCKO and BCKO is stopped. When output of LRCKO and BCKO is stopped due to detection of an error, abnormal LRCKO and BCKO may be output while the operation shifts to a stop state. When the LSI stops operation by writing '0' in the ENBL bit during normal operation, audio data of '0' is output for at least one period of LRCKO and then the LSI stops the operation.

Through Mode

This LSI can output audio data by performing delay processing by setting internal register THRU (SUB:00h-bit[4]) to '1'. When transition between through modes is performed by setting or resetting the THRU bit, the relationship among DOx, LRCKO, and BCKO may collapse and abnormal LRCKO, LRCKO, and BCKO may be output.
This mode is made available to output audio data without delay when output delay by 1 LRCK causes a problem even if delay time = 0 is set in normal delay operation. Since polarity reversal for LRCK is performed by input and output format registers, POLx and FMTx, set the mode according to the input/output.

SYSCLK

SYSCLK requires a frequency that is 128 times the sampling frequency and within 12 times BCK. However, since the maximum operation frequency of this LSI is 25MHz, the frequency must not exceed the limit.
For instance, when the sampling frequency is 96 kHz, the frequency of 128 times is 12.288 MHz and the frequency of 256 times is 24.576 MHz. Therefore, either frequency can be used.

When the sampling frequency is 192kHz, the frequency of 128 times is 24.576 MHz. In this case, only this frequency can be selected.
LRCKI0 to LRCKI3 and BCKI0 toBCKI3 must synchronize with SYSCLK. As long as the synchronization is maintained, the phase with SYSCLK is irrelevant.

I^2C Address

This LSI can set two types of I2C addresses by the setting of MODE0 to MODE2.

- The I2C address is 0x8C/8D when MODE0 = '0', MODE1 = '0', and MODE2 = '0'
- The I2C address is 0x8E/8F when MODE0= '1', MODE1 = '0', and MODE2 = '0'

Modes other than those indicated above are not allowed since they are test modes of this LSI.

INTERNAL REGISTERS

Register Map

SA	DATA								Default Value	Function
	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0		
00h	-	-	CMN_DLY	THRU	INT_EXT	NOF_CH	DI_SEL 1	DI_SEL 0	xx00_0100b	Mode setting
01h	-	-	-	POLI	FMTI 1	FMTI 0	DI_LEN 1	DI_LEN 0	xxx0_0000b	Input data format setting
02h	-	-	-	POLO	FMTO 1	FMTO 0	DO_LEN 1	DO_LEN 0	xxx0_0000b	Output data format setting
03h	-	-	-	-	BCK_DIV 3	BCK_DIV 2	BCK_DIV 1	BCK_DIV 0	xxxx_0100b	BCKO cycle setting
04h	-	-	LRCK_DIV 5	LRCK_DIV 4	LRCK_DIV 3	LRCK_DIV 2	LRCK_DIV 1	LRCK_DIV 0	xx01_0000b	LRCKO cycle setting
05h	-	-	REF_INTVL 5	REF_INTVL 4	REF_INTVL 3	REF_INTVL 2	REF_INTVL 1	REF_INTVL 0	xx01_0110b	DRAM refresh interval setting
06h	SFT_RST	-	-	-	-	-	-	-	0xxx_xxxxb	Software reset
07h	ENBL	-	-	-	-	-	AUTO RSTRT	INT_MASK	0xxx_xx01b	Delay operation control
08h	RUN	SRC_CHG	SRC_CLK	-	-	CFG_ERS	DRAM RDY	INIT	000x_x001b	Operation status
09h	TMG_ERR	CFG_ERR	BCK_ERR	OVRN	UDRN	-	-	-	0000_0xxxb	Eorror status
0ah	MASK 7	MASK 6	MASK 5	MASK 4	MASK 3	MASK 2	MASK 1	MASK 0	0000_0000b	Output data mask
10h	DLY0_L 7	DLY0_L 6	DLY0_L 5	DLY0_L 4	DLY0_L 3	DLY0_L 2	DLY0_L 1	DLY0_L 0	0000_0000b	CH0 delay value setting lower-order 8 bits
11h	DLY0_H 7	DLY0_H 6	DLY0_H 5	DLY0_H 4	DLY0_H 3	DLY0_H 2	DLY0_H 1	DLY0_H 0	0000_0000b	CH0 delay value setting higher-order 8 bits
12h	DLY1_L 7	DLY1_L 6	DLY1_L 5	DLY1_L 4	DLY1_L 3	DLY1_L 2	DLY1_L 1	DLY1_L 0	0000_0000b	CH1 delay value setting lower-order 8 bits
13h	DLY1_H 7	DLY1_H 6	DLY1_H 5	DLY1_H 4	DLY1_H 3	DLY1_H 2	DLY1_H 1	DLY1_H 0	0000_0000b	CH1 delay value setting higher-order 8 bits
14h	DLY2_L 7	DLY2_L 6	DLY2_L 5	DLY2_L 4	DLY2_L 3	DLY2_L 2	DLY2_L 1	DLY2_L 0	0000_0000b	CH2 delay value setting lower-order 8 bits
15h	DLY2_H 7	DLY2_H 6	DLY2_H 5	DLY2_H 4	DLY2_H 3	DLY2_H 2	DLY2_H 1	DLY2_H 0	0000_0000b	CH2 delay value setting higher-order 8 bits
16h	DLY3_L 7	DLY3_L 6	DLY3_L 5	DLY3_L 4	DLY3_L 3	DLY3_L 2	DLY3_L 1	DLY3_L 0	0000_0000b	CH3 delay value setting lower-order 8 bits
17h	DLY3_H 7	DLY3_H 6	DLY3_H 5	DLY3_H 4	DLY3_H 3	DLY3_H 2	DLY3_H 1	DLY3_H 0	0000_0000b	CH3 delay value setting higher-order 8 bits
18h	DLY4_L 7	DLY4_L 6	DLY4_L 5	DLY4_L 4	DLY4_L 3	DLY4_L 2	DLY4_L 1	DLY4_L 0	0000_0000b	CH4 delay value setting lower-order 8 bits
19h	DLY4_H 7	DLY4_H 6	DLY4_H 5	DLY4_H 4	DLY4_H 3	DLY4_H 2	DLY4_H 1	DLY4_H 0	0000_0000b	CH4 delay value setting higher-order 8 bits
1ah	DLY5_L 7	DLY5_L 6	DLY5_L 5	DLY5_L 4	DLY5_L 3	DLY5_L 2	DLY5_L 1	DLY5_L 0	0000_0000b	CH5 delay value setting lower-order 8 bits
1bh	DLY5_H 7	DLY5_H 6	DLY5_H 5	DLY5_H 4	DLY5_H 3	DLY5_H 2	DLY5_H 1	DLY5_H 0	0000_0000b	CH5 delay value setting higher-order 8 bits
1ch	DLY6_L 7	DLY6_L 6	DLY6_L 5	DLY6_L 4	DLY6_L 3	DLY6_L 2	DLY6_L 1	DLY6_L 0	0000_0000b	CH6 delay value setting lower-order 8 bits
1dh	DLY6_H 7	DLY6_H 6	DLY6_H 5	DLY6_H 4	DLY6_H 3	DLY6_H 2	DLY6_H 1	DLY6_H 0	0000_0000b	CH6 delay value setting higher-order 8 bits
1eh	DLY7_L 7	DLY7_L 6	DLY7_L 5	DLY7_L 4	DLY7_L 3	DLY7_L 2	DLY7_L 1	DLY7_L 0	0000_0000b	CH7 delay value setting lower-order 8 bits
1fh	DLY7_H 7	DLY7_H 6	DLY7_H 5	DLY7_H 4	DLY7_H 3	DLY7_H 2	DLY7_H 1	DLY7_H 0	0000_0000b	CH7 delay value setting higher-order 8 bits

Register Descriptions

• Mode setting SUB_ADDRESS=00h(R/W)

Timing generation of LRCKO, BCKO, and DO0 - 3 outputs, delay register mode, 8-ch/2-ch mode switching and source selection in the 2-ch mode are performed.

Table 11 Mode Setting Register Map

DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register Name	—	—	CMN_DLY	THRU	INT_EXT	NOF_CH	DI_SEL	
WR	—	—	V	V	V	V	V	V
RD	0	0	V	V	V	V	V	V
Default Value	—	—	0	0	0	1	0	0

V = Valid Data

Table 12 Descriptions of the Mode Setting Register Functions

Register Name	Description
CMN_DLY	Specifies whether the delay value of each channel is set to an equal value or not. 0: Sets each channel to a delay value. 1: Sets each channel to the CH0 delay value.
THRU	Specifies the output mode. 1: Outputs the input signal specified by the “NOF_CH” or the “DI_SEL” at a delay time of 0. 0: Performs normal delay processing and outputs the input signal. * While the audio data are input to the DIx (x=0-3) pin (excluding LRCKx and BCKx pins), the setting from normal operation to Through mode and/or from Through mode to normal operation may results in output of the abnormal audio data from the DOx (x=0-3) pin. Therefore, when changing the output mode using this bit, setting the input data to all “0” is recommended.
INT_EXT	Specifies the output timing of LRCK0 / BCK0 / DO0 - 3. 1: Internal generation timing Outputs data at the timing specified by the TimingGenerate registers. 0: External input timing synchronization The DO0 - 3 signals are output synchronized to the LRCKIn / BCKn. LRCKO/BCKO outputs LRCKIn / BCKIn without modification. * When INT_EXT = “1”, set the register so that the FS generated by the TimingGenerate register is coincident with the input FS.
NOF_CH	Specifies the number of the delay processing channels. 1: 8-ch mode Samples the DI0 - 3 input pins, performs delay processing for each channel, and outputs data from the DO0 - 3 pins. 0: 2-ch mode Samples one input out of the DI0-3 pins selected by the “DI_SEL[1:0]” register, performs delay processing of the 4 outputs, and outputs data from the DO0-3 pins (2ch x 4 outputs). * This setting bit is also valid in Through mode when THRU = “1”

Register Name	Description
DI_SEL [1:0]	Specifies the audio source when ”NOF_CH” = “0”. 00: DI0 01: DI1 10: DI2 11: DI3 * When “NOF_CH” = “1”, this field is meaningless. This field is valid when THRU = “1”.

Table 13 Input and Output Relations by NOF_CH and DI_SEL[1:0]

NOF_CH	DI_SEL[1:0]	DO0	DO1	DO2	DO3	BCKO	LRCKO
“1”(8ch)	xx (Don’t Care)	DI0	DI1	DI2	DI3	BCKI0	LRCKI0
“0” (2ch)	00	DI0	DI0	DI0	DI0	BCKI0	LRCKI0
	01	DI1	DI1	DI1	DI1	BCKI1	LRCKI1
	10	DI2	DI2	DI2	DI2	BCKI2	LRCKI2
	11	DI3	DI3	DI3	DI3	BCKI3	LRCKI3

• Input data format setting SUB_ADDRESS=01h(R/W)

This register specifies the data bit length, I^2S, input data formats (left justified and right justified), and the polarity of the LRCK.

Table 14 Input Data Format Setting Register Map

DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register Name	—	—	—	POLI	FMTI		DI_LEN	
WR	—	—	—	V	V	V	V	V
RD	0	0	0	V	V	V	V	V
Default Value	—	—	—	0	0	0	0	0

Table 15 Descriptions of Input Data Format Setting Register Functions

Register Name	Description
POLI	Specifies the polarity of the LRCKI. 1: Inverted 0: Non-inverted
FMTI [1:0]	Specifies the input format. 00: Left justified (MSB) 00: Right justified (LSB) 10, 11: I^2S
DI_LEN [1:0]	Specifies the input data bit length. 00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits * This field is not valid in Through mode.

	POL=1		POL=0	
	LRCKI		LRCKI	
	LEFT	RIGHT	LEFT	RIGHT
I^2S	1	0	0	1
Left justified (MSB)	0	1	1	0
Right justified (LSB)	0	1	1	0

• Output data format setting SUB_ADDRESS=02h(R/W)

This register specifies the data bit length, I^2S, output data formats (left justified, and right justified), and the polarity of LRCK.

Table 16 Output Data Format Setting Register Map

DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register Name	—	—	—	POLO	FMTO		DO_LEN	
WR	—	—	—	V	V	V	V	V
RD	0	0	0	V	V	V	V	V
Default Value	—	—	—	0	0	0	0	0

Table 17 Descriptions of Output Data Format Setting Register Functions

<table>
<tr><th>Register Name</th><th>Description</th></tr>
<tr><td>POLO</td><td>Specifies the polarity of the LRCKO.
1: Inverted
0: Non-inverted
<table>
<tr><td rowspan="2"></td><td>POL=1</td><td colspan="2">POL=0</td></tr>
<tr><td>LRCKI</td><td colspan="2">LRCKI</td></tr>
<tr><td>LEFT</td><td>RIGHT</td><td>LEFT</td><td>RIGHT</td></tr>
<tr><td>I^2S</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Left justified (MSB)</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>Right justified (LSB)</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
</table></td></tr>
<tr><td>FMTO
[1:0]</td><td>Specifies the output format.
00: Left justified (MSB)
00: Right justified (LSB)
10, 11: I^2S</td></tr>
<tr><td>DO_LEN
[1:0]</td><td>Specifies the output data bit length.
00: 16 bits
01: 20 bits
10: 24 bits
11: 32 bits
* This field is not valid in Through mode.</td></tr>
</table>

• BCKO cycle setting SUB_ADDRESS=03h(R/W)

This register specifies the cycle of BCKO which is generated internally when INT_EXT of the mode setting register is “1”.

Table 18 BCKO Cycle Setting Register Map

DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register Name	—	—	—	—	BCK_DIV			
WR	—	—	—	—	V	V	V	V
RD	0	0	0	0	V	V	V	V
Default Value	—	—	—	—	0	1	0	0

• LRCKO Cycle Setting SUB_ADDRESS=04h(R/W)

This register specifies the cycle of LRCKO which is generated internally when INT_EXT of the mode setting register is “1”.

Table 19 LRCKO Cycle Setting Register Map

DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register Name	—	—	LRCK_DIV					
WR	—	—	V	V	V	V	V	V
RD	0	0	V	V	V	V	V	V
Default Value	—	—	0	1	0	0	0	0

Note: Both of the registers BCK_DIV and LRCK_DIV should be configured. The new data is valid if the both registers are configured. For example, when only the BCK_DIV register is to be changed, the BCK_DIV register is first configured, then the LRCK_DIV register should be configured with the value equal to the current value.

Table 20 Descriptions of BCKO/LRCKO Cycle Register Functions

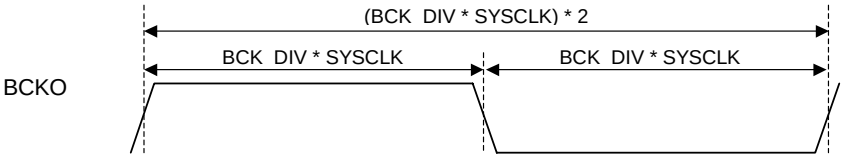
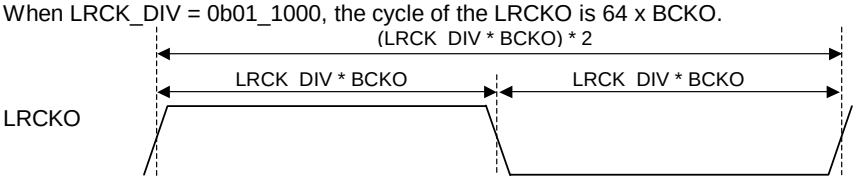
Register Name	Description
BCK_DIV [3:0]	Specifies the half cycle of the BCKO. The half cycle is specified according to the number of SYSCLK pulses. When BCK_DIV = 0b0001, the cycle of the BCKO is 2 x SYSCLK. When BCK_DIV = 0b0100, the cycle of the BCKO is 8 x SYSCLK. Set BCK_DIV to 6 or less. 
LRCK_DIV [5:0]	Specifies the half cycle of the LRCKO. The half cycle is specified according to the number of BCKO pulses. When LRCK_DIV = 0b01_0000, the cycle of the LRCKO is 32 x BCKO. When LRCK_DIV = 0b01_1000, the cycle of the LRCKO is 64 x BCKO. 

Table 21 Examples of Setting BCK_DIV and LRCK_DIV

	DO_LEN	00 (16 bits)	01 (20bits)	10 (24 bits)	11 (32 bits)
SYSCLK	Register Name				
512FS	BCK_DIV	--	0100 (4)	0100 (4)	0100 (4)
	LRCK_DIV	--	10_0000 (32)	10_0000 (32)	10_0000 (32)
384FS	BCK_DIV	0110 (6)	0100 (4)	0100 (4)	0011 (3)
	LRCK_DIV	01_0000 (16)	01_1000 (24)	01_1000 (24)	10_0000 (32)
256FS	BCK_DIV	0100 (4)	0010 (2)	0010 (2)	0010 (2)
	LRCK_DIV	01_0000 (16)	10_0000 (32)	10_0000 (32)	10_0000 (32)
192FS	BCK_DIV	0011 (3)	0010 (2)	0010 (2)	--
	LRCK_DIV	01_0000 (16)	01_1000 (24)	01_1000 (24)	--
128FS	BCK_DIV	0010 (2)	--	--	--
	LRCK_DIV	01_0000 (16)	--	--	--

*1: When ENBL is set to “1” with the configuration of BCK_DIV x LRCK_DIV over 192, the CFG_ERR bit is set to “1” and the delay operation is not started.

*2: Both of the registers BCK_DIV and LRCK_DIV should be configured. The new data is valid if the both registers are configured. For example, when only the BCK_DIV register is to be changed, the BCK_DIV register should be configured and then the LRCK_DIV register should be configured with the value equal to the current value.

• DRAM refresh interval setting SUB_ADDRESS=05h(R/W)

Table 22 DRAM Refresh Interval Setting Register Map

DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register Name	—	—	REF_ITVL					
WR	—	—	V	V	V	V	V	V
RD	0	0	V	V	V	V	V	V
Default Value	—	—	0	1	0	1	1	0

Table 23 Descriptions of DRAM Refresh Interval Setting Register Functions

Register Name	Description
REF_ITVL [5:0]	Specifies the DRAM refresh interval. The refresh interval is 8 x SYSCLK x REF_ITVL. The value (refresh interval) should be set around 14 µs (15.6µs x 0.9) by this register.

Table 24 Examples of REF_ITVL Setting by SYSCLK

	32kHz	44.1kHz	48kHz	96kHz	192kHz
512FS	01_1101 (29) (14.16 µs)	10_1000 (40) (14.17 µs)	10_1011 (43) (13.99 µs)	--	--
384FS	01_0110 (22) (14.32 µs)	01_1110 (30) (14.17 µs)	10_0000 (32) (13.88 µs)	--	--
256FS	00_1110 (14) (13.67 µs)	01_0100 (20) (14.17 µs)	01_0110 (22) (14.32 µs)	10_1011 (43) (13.99 µs)	--
192FS	00_1011 (11) (14.32 µs)	00_1111 (15) (14.17 µs)	01_0000 (16) (13.88 µs)	10_0000 (32) (13.88 µs)	--
128Fs	00_0111 (07) (13.67 µs)	00_1010 (10) (14.17 µs)	00_1011 (11) (14.32 µs)	01_0110 (22) (14.32 µs)	10_1011 (43) (13.99 µs)

Table 25 SYSCLK Cycle by SYSCLK Input

	32kHz	44.1kHz	48kHz	96kHz	192kHz
512FS	61.035 ns	44.289 ns	40.690 ns	--	--
384FS	81.380 ns	59.051 ns	54.253 ns	--	--
256FS	122.070 ns	88.577 ns	81.380 ns	40.690 ns	--
192FS	162.760 ns	118.103 ns	122.070 ns	54.253 ns	--
128Fs	244.141 ns	177.154 ns	162.760 ns	81.380 ns	40.690 ns

• Software reset SUB_ADDRESS=06h(R/W)

Table 26 Software Reset Register Map

DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register Name	SFT_RST	—	—	—	—	—	—	—
WR	V	—	—	—	—	—	—	—
RD	V	0	0	0	0	0	0	0
Default Value	0	—	—	—	—	—	—	—

Table 27 Descriptions of Software Reset Register Functions

Register Name	Description
SFT_RST	Specifies the execution of software reset. 0: NOP 1: Resets all the blocks except the I^2C block. This reset is done in the same manner as the hardware reset except that the I^2C block is not reset. When the reset is done, this bit is cleared automatically.

• Delay operation start/stop, interrupt mask control SUB_ADDRESS=07h(R/W)

Table 28 Delay Operation Control Register Map

DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register Name	ENBL	—	—	—	—	—	AUTOR STRT	INT MASK
WR	V	—	—	—	—	—	V	V
RD	V	0	0	0	0	0	V	V
Default Value	0	—	—	—	—	—	0	0

Table 29 Descriptions of Delay Operation Control Register Functions

Register Name	Description
ENBL	Controls the delay operation. 0: Stop 1: Start * When the CFG_ERR bit is set due to the inconsistency in the setting even if the ENBL register is set to “1”, the delay operation is not started. When the synchronization of LRCK and BCK is lost during the delay operation, the ENBL register is set to “0” and the operation is suspended (AUTORSTRT = 0).
AUTORSTRT	Performs resynchronization automatically when an input timing error occurs. 0: NOP 1: Automatic resynchronization * When this register is set to “1”, the INT output is fixed to a “H” level even if the INT_MASK is “0” except when the delay operation is suspended by CFG_ERR. However, the error statuses which cause interrupts are set.
INT_MASK	Masks interrupt outputs. 0: NOP 1: Mask * When this register is set to “1”, the error statuses which cause interrupts are masked though the INT output is fixed to a “H” level.

• Operation Status SUB_ADDRESS=08h(R/W)

Table 30 Operation Status Register Map

DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register Name	RUN	SRC_CHG	SRC_CLK	—	—	CFG_ERS	DRAM_RDY	INIT
WR	—	—	—	—	—	—	—	—
RD	V	V	V	0	0	V	V	V
Default Value	0	—	—	—	—	—	—	—

Table 31 Descriptions of Operation Status Register Functions

Register Name	Description
RUN	1: Indicates that the delay operation is being performed. 0: Indicates that the delay operation is being suspended. * When various settings are correct after the ENBL bit is set to '1' and input data formats are recognized correctly, the delay operation is started and the register is set to '1'. When an error is detected while the input data formats are recognized, the register is remained '0'. The register is set to '0' when the TMG_ERR bit is set to '1' by the change of the input signal or when the ENBL bit is cleared.
SRC_CHG	1: Indicates the input switching sequence is ready when switching 8ch → 2ch or switching the source in the 2-ch mode. 0: --- * This bit is changed to '1' when the input masking is performed by changing of input and output formats. When the ENBL bit is set while this bit is being set, the delay operation is not started until the interval operation is completed and this bit is cleared.
SRC_CLK	1: Indicates the clock of the clock source which is being selected is internally valid. 0: Indicates the clock of the clock which is being selected is internally invalid. * This bit is changed to '0' when the clock masking is performed by changing of input source.
CFG_ERS	1: Indicates any inconsistency arises from the various setting values. 0: --- * The delay operation is not started when the ENBL bit is set while this bit is being set. This bit is changed each time data is written in each setting register.
DRAM_RDY	1: Indicates the initialization of the internal DRAM is completed and normal operations are ready. 0: Indicates the internal DRAM is being initialized. * When the ENBL bit is set while this bit is being set, the delay operation is postponed until initialization of the internal DRAM is completed.
INIT	1: Indicates initialization is in progress. 0: ---

• Error status SUB_ADDRESS=09h(R/W)

Table 32 Error Status Register Map

DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register Name	TMG_ERR	CFG_ERR	BCK_ERR	OVRN	UDRN	—	—	—
WR	V	V	V	V	V	—	—	—
RD	V	V	V	V	V	0	0	0
Default Value	0	0	0	0	0	—	—	—

Table 33 Descriptions of the Status Register Functions

Register Name	Description
TMG_ERR	1: This bit is set to '1' when a change of the input timing (the relationship between LRCKI and BCKI) is detected after the operation is started, and the delay operation is stopped. 0: --- * Even if this bit is '1', the delay operation is started when the ENBL bit is set to '1'. This bit should be cleared by writing '0' to this bit since this bit is not cleared automatically.
CFG_ERR	1: Indicates delay operations are suspended due to any inconsistency in various setting values. 0: --- * The delay operation is stopped when this bit is set, regardless of the state of the AUTORSTRT bit. This bit is cleared by writing '0'.
BCK_ERR	1: This bit is set to '1' and the delay operation is stopped when the number of BCK pulses is less than the set input bit length or less than the set output data length in the external synchronization mode after the operation is started. 0: --- * This bit is cleared once at the time of operation start when the ENBL bit is set to '1'. If input signals are checked again when the initialization of the input signals is performed and the set register is not consistent with the input signals, the delay operation is stopped regardless of the state of the AUTORSTRT bit This bit is cleared by writing '0'.
OVRN	1: This bit is set to '1' when the delay buffer overflows due to the period of the input data that is shorter than that of the output data. 0: --- * When AUTORSTRT==0, the delay operation is stopped. When AUTORSTRT==0, the delay operation is started after the synchronization of input signals is performed again. This bit is cleared by writing '0'.
UDRN	1: This bit is set to '1' when the delay buffer underflows due to the period of the input data that is longer than that of the output data. 0: --- * When AUTORSTRT==0, the delay operation is stopped. When AUTORSTRT==0, the delay operation is started after the synchronization of input signals is performed again. This bit is not set to '1' when 0s are output while data equivalent to the delay time is has not been written in the delay buffer due to the change of the delay register. This bit is cleared by writing '0'.

• Output data mask control SUB_ADDRESS=0ah(R/W)

Table 34 Output Data Mask Register Map

DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register Name	MASK							
WR	V	V	V	V	V	V	V	V
RD	V	V	V	V	V	V	V	V
Default Value	0	0	0	0	0	0	0	0

Table 35 Descriptions of the Output Data Mask Register Function

Register Name	Description
MASK	Controls the output masking (output data = all “0”). 0: No masking (data is output). 1: Masking. * When this bit is set to '1' during the delay operation, the output data of the selected channel is set to '0' synchronized to LRCK. When the bit is set to '0' during the delay operation, the output masking is released synchronized to LRCK.

- CH delay value setting register

CH0(DO0 Lch)	Delay Value Setting (Lower-order 8 bits)	SUB_ADDRESS=10h(R/W)
CH0(DO0 Lch)	Delay Value Setting (Higher-order 8bits)	SUB_ADDRESS=11h(R/W)
CH1(DO0 Rch)	Delay Value Setting (Lower-order 8 bits)	SUB_ADDRESS=12h(R/W)
CH1(DO0 Rch)	Delay Value Setting (Higher-order 8bits)	SUB_ADDRESS=13h(R/W)
CH2(DO1 Lch)	Delay Value Setting (Lower-order 8 bits)	SUB_ADDRESS=14h(R/W)
CH2(DO1 Lch)	Delay Value Setting (Higher-order 8bits)	SUB_ADDRESS=15h(R/W)
CH3(DO1 Rch)	Delay Value Setting (Lower-order 8 bits)	SUB_ADDRESS=16h(R/W)
CH3(DO1 Rch)	Delay Value Setting (Higher-order 8bits)	SUB_ADDRESS=17h(R/W)
CH4(DO2 Lch)	Delay Value Setting (Lower-order 8 bits)	SUB_ADDRESS=18h(R/W)
CH4(DO2 Lch)	Delay Value Setting (Higher-order 8bits)	SUB_ADDRESS=19h(R/W)
CH5(DO2 Rch)	Delay Value Setting (Lower-order 8 bits)	SUB_ADDRESS=1ah(R/W)
CH5(DO2 Rch)	Delay Value Setting (Higher-order 8bits)	SUB_ADDRESS=1bh(R/W)
CH6(DO3 Lch)	Delay Value Setting (Lower-order 8 bits)	SUB_ADDRESS=1ch(R/W)
CH6(DO3 Lch)	Delay Value Setting (Higher-order 8bits)	SUB_ADDRESS=1dh(R/W)
CH7(DO3 Rch)	Delay Value Setting (Lower-order 8 bits)	SUB_ADDRESS=1eh(R/W)
CH7(DO3 Rch)	Delay Value Setting (Higher-order 8bits)	SUB_ADDRESS=1fh(R/W)

Table 36 CH Delay Value Setting (Lower-Order 8 Bits) Register Map

DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register Name	DLYx_L							
WR	V	V	V	V	V	V	V	V
RD	V	V	V	V	V	V	V	V
Default Value	0	0	0	0	0	0	0	0

Table 37 CH Delay Value Setting (Higher-Order 8 Bits) Register Map

DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register Name	DLYx_H							
WR	V	V	V	V	V	V	V	V
RD	V	V	V	V	V	V	V	V
Default Value	0	0	0	0	0	0	0	0

Table 38 Description of the CH Delay Value Setting Register Function

Register Name	Description
DLYx_H[7:0] **DLYx_L[7:0]**	Sets the delay time. The delay time is controlled in units of FS and set in a 16-bit length (DLYx_H = higher-order 8 bits / DLYx_L = lower-order 8 bits). * 2-ch mode When the input data length = 16 bits, the maximum delay is 65535. When the input data length > 16 bits, the maximum delay is 32767. * 8-ch mode When the input data length = 16 bits, the maximum delay is 16383. When the input data length > 16 bits, the maximum delay is 8191. When the value is set to reduce the maximum delay time (for example, 2-ch mode is changed to 8-ch mode), the maximum value is adopted as the delay value for the channel value which exceeds the maximum value. However, the value read from the register is the current value set, not the value limited with the maximum delay value.

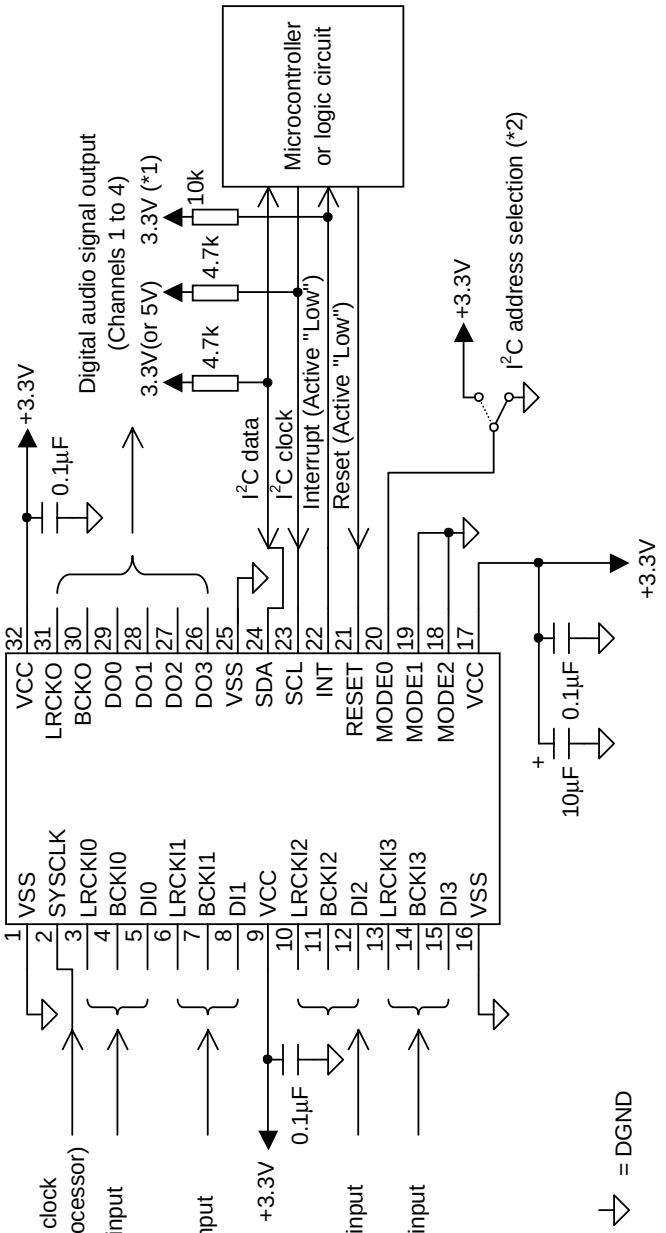
x = 0, 1, 2, 3, 4, 5, 6, 7

Table 39 Maximum Delay Times by Mode

Mode \ FS		32 kHz	44.1 kHz	48 kHz	88.2 kHz	96 kHz	192 kHz
2-ch	= 16 bits	2.048 s	1.486 s	1.365 s	743 ms	682.6 ms	341.3 ms
	> 16 bits	1.024 s	743 ms	682.6 ms	371.5 ms	341.3 ms	170.6 ms
8-ch	= 16 bits	512 ms	371.5 ms	341.3 ms	185.7 ms	170.6 ms	85.33 ms
	> 16 bits	256 ms	185.7 ms	170.6 ms	92.87 ms	85.33 ms	42.66 ms

* The delay times are calculated using equation (Maximum delay value + 1)/FS.

ML87V5002 APPLICATION CIRCUIT EXAMPLE



Notes:
This application circuit example is for reference. So the application circuit is not guaranteed for operation.

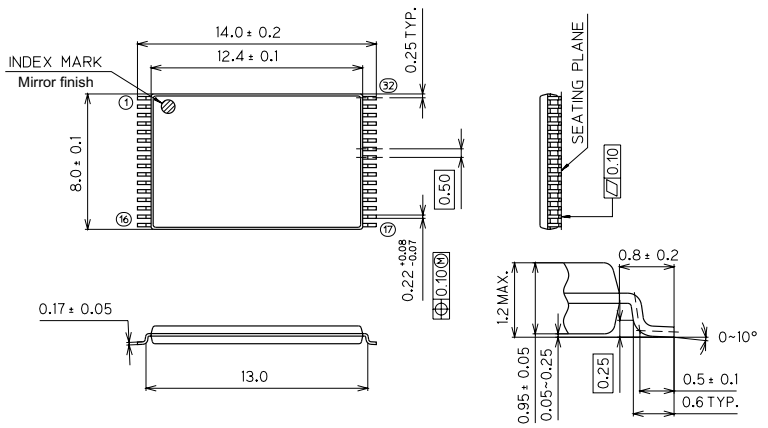
*1: The voltage depends on the supply voltage of the microcontroller.

*2: The I^{2}C address is determined by the input level of MODE0. See the "I^{2}C addresses" Section on Page 17.

PACKAGE DIMENSIONS

(Unit: mm)

TSOP(1)32-P-0814-0.50-1K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.27 TYP.
Rev. No./Last Revised	3/Dec. 10, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL87V5002-01	Sep. 1, 2005	–	–	Final edition 1

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