ML87V21071 Preliminary

Video Signal Noise Reduction IC with a Built-in Frame Memory

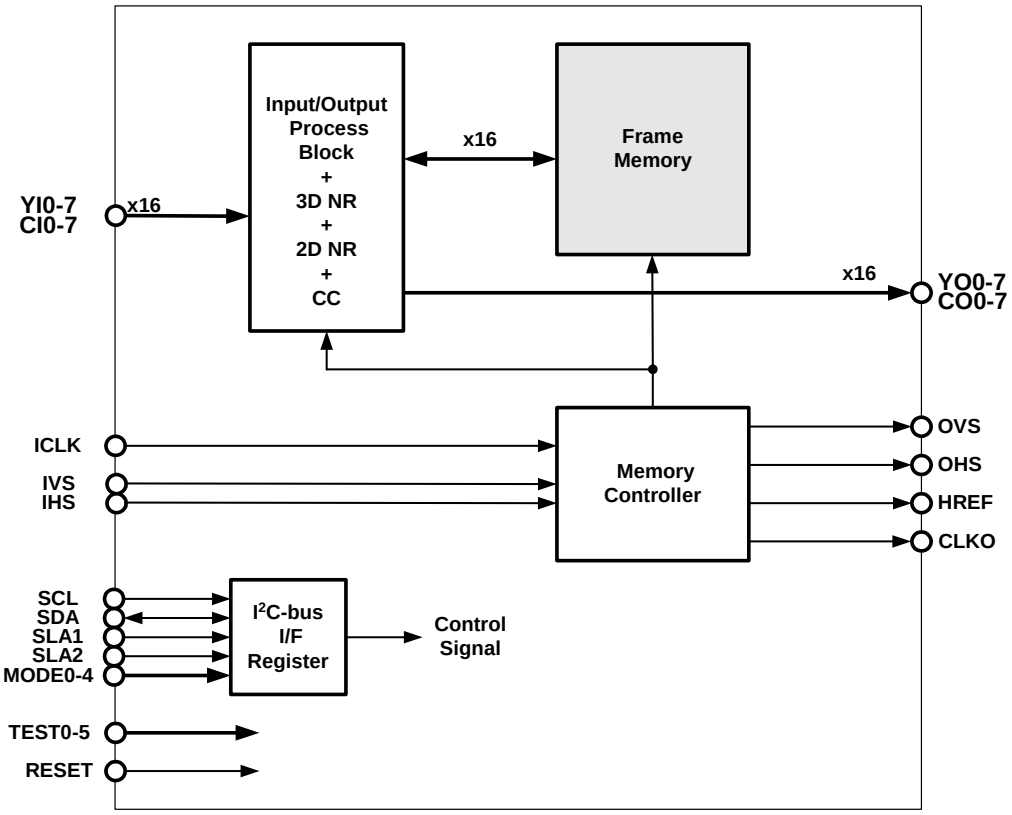
GENERAL DESCRIPTION

The ML87V21071, which comprises a frame memory and signal processing and memory control logic circuits, has achieved motion-adaptive 3D noise reduction.
To perform noise reduction with afterimage suppression, the ML87V21071 also enables noise reduction using the edge-adaptive 2D noise reduction filter.
Each noise reduction function allows setting an automatic mode. In automatic mode, noise of a vertical blanking period and a valid data period is detected to reduce noise according to the noise status from which the noise reduction setting value is detected.
The ML87V21071 also has a cross-color cancellation function that uses the motion-adaptive 3D comb filter method that removes cross colors occurring at two-dimensional YC separation in the NTSC/PAL system.
Since the same format as the input can be selected for output, noise reduction can easily be achieved by inserting the IC into the conventional system.

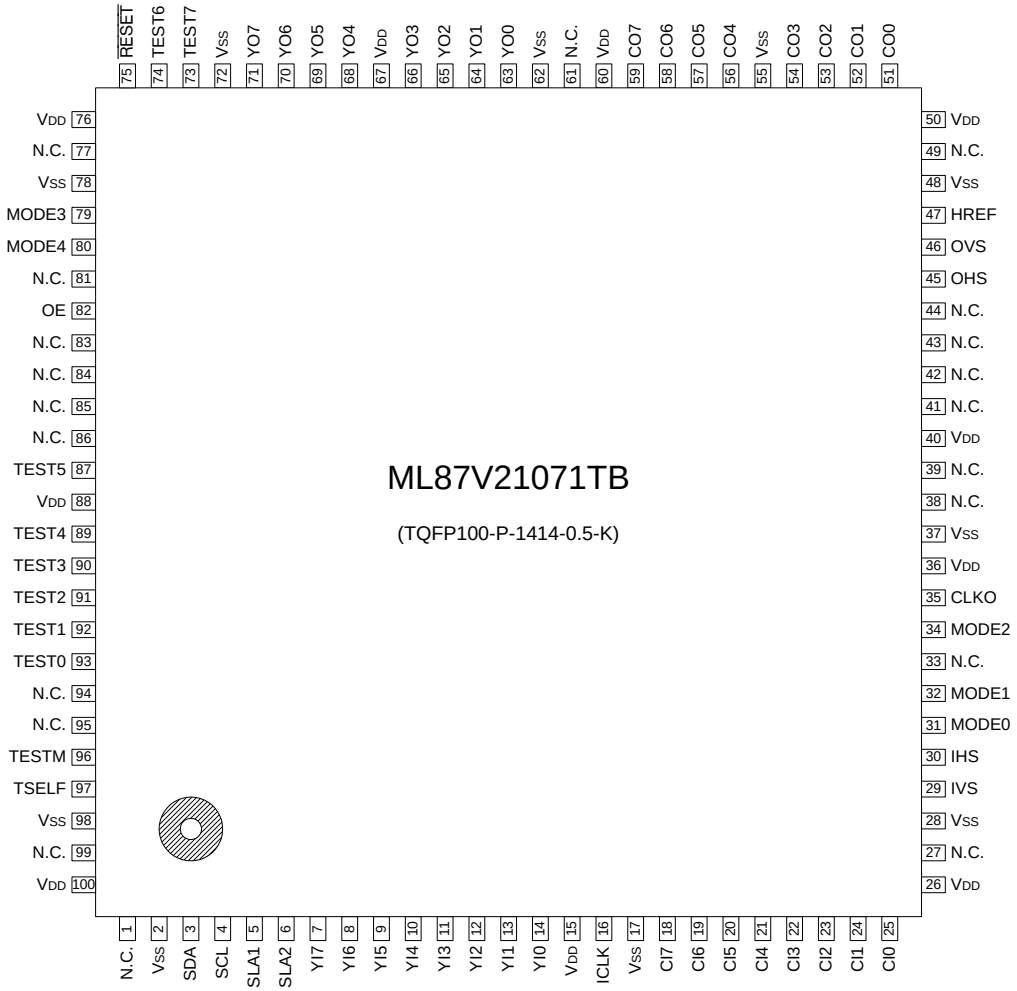
FEATURES

- Built-in memory:
  Frame memory (78 × 608 × 16-bit) × 1 unit
- Maximum input and output operating frequencies (16-bit/8-bit, ITU-R BT.656):
  14.75/29.5 MHz
  * For 525p/625p, only 16-bit input mode is supported (Max.: 29.5 MHz).
- Power supply voltage:
  3.3 V ± 0.3 V
- Input/ouput pin:
  LVCMOS (3.3 V)
- Input/ouput data format:
  YCbCr (8 bit (Y) + 8 bit (CbCr))(4:2:2): 16-bit mode
  YCbCr (8 bit (YCbCr))(4:2:2): 8-bit mode
  ITU-R656 (8 bit (YCbCr)): ITU-R BT.656 mode
  * In 16-bit input mode, neither 8-bit mode nor ITU-R BT.656 mode can be selected for output.
- Serial bus:
  I^2C-bus interface: (400 kHz, 100 kHz)
- Memory controller:
  Compatible with 625/50Hz 2:1(625i), 525/60Hz 2:1(525i), 625/50Hz 1:1(625p), and 525/60Hz 1:1(525p)
- Motion-adaptive 3D noise reduction:
  Frame-field-line-correlation noise detection and noise subtraction method
  Supports automatic noise reduction setting
- Edge-adaptive 2D noise reduction:
  Edge-adaptive space filter used
- Chrominance signal cross color cancelling:
  Motion-adaptive 3D comb filter used
  Compatible with 525i (NTSC decode signal)/625i (PAL decode signal)
- Package:
  100-pin TQFP (TQFP100-P-1414-0.50-K) (ML87V21071TB)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



PIN DESCRIPTIONS

No.	Symbol	I/O	Pad Remarks	Pin Description	Termination of unused pin
1	N.C.	—		Unused pin	Not used
2	V_{SS}	—		Ground	X
3	SDA	I/O	Schmitt(IN)/ OpenDrain(OUT)	I^2C-bus data pin	X
4	SCL	I	Schmitt	I^2C-bus clock pin	X
5	SLA1	I	Schmitt pull-down 50k	Slave address setting pin bit 1	Not used or connected to GND
6	SLA2	I	Schmitt pull-down 50k	Slave address setting pin bit 2	Not used or connected to GND
7	YI7	I		Luminance signal input pin bit 7 (MSB)	X
8	YI6	I		Luminance signal input pin bit 6	X
9	YI5	I		Luminance signal input pin bit 5	X
10	YI4	I		Luminance signal input pin bit 4	X
11	YI3	I		Luminance signal input pin bit 3	X
12	YI2	I		Luminance signal input pin bit 2	X
13	YI1	I		Luminance signal input pin bit 1	X
14	YI0	I		Luminance signal input pin bit 0 (LSB)	X
15	V_{DD}	—		3.3 V power supply	X
16	ICLK	I		System clock Input pin	X
17	V_{SS}	—		Ground	X
18	CI7	I	pull-down 50k	Chrominance signal input pin bit 7 (MSB)	Not used or connected to GND
19	CI6	I	pull-down 50k	Chrominance signal input pin bit 6	Not used or connected to GND
20	CI5	I	pull-down 50k	Chrominance signal input pin bit 5	Not used or connected to GND
21	CI4	I	pull-down 50k	Chrominance signal input pin bit 4	Not used or connected to GND
22	CI3	I	pull-down 50k	Chrominance signal input pin bit 3	Not used or connected to GND
23	CI2	I	pull-down 50k	Chrominance signal input pin bit 2	Not used or connected to GND
24	CI1	I	pull-down 50k	Chrominance signal input pin bit 1	Not used or connected to GND
25	CI0	I	pull-down 50k	Chrominance signal input pin bit 0 (LSB)	Not used or connected to GND
26	V_{DD}	—		3.3 V power supply	X
27	N.C.	—		Unused pin	Not used
28	V_{SS}	—		Ground	X
29	IVS	I	Schmitt pull-down 50k	Input system vertical Sync. signal input pin	Not used or connected to GND
30	IHS	I	Schmitt pull-down 50k	Input system horizontal Sync. signal input pin	Not used or connected to GND
31	MODE0	I	Schmitt pull-down 50k	Mode setting pin bit 0 (Equivalent to internal register VMD[0])	Not used or connected to GND
32	MODE1	I	Schmitt pull-down 50k	Mode setting pin bit 1 (Equivalent to internal register HMD[0])	Not used or connected to GND
33	N.C.	—		Unused pin	Not used

No.	Symbol	I/O	Pad Remarks	Pin Description	Termination of unused pin
34	MODE2	I	Schmitt pull-down 50k	Mode setting pin bit 2 (Equivalent to internal register DISEL[0])	Not used or connected to GND
35	CLKO	O		Clock output (I^2C-bus control possible)	Not used
36	V_{DD}	—		3.3 V power supply	X
37	V_{SS}	—		Ground	X
38	N.C.	—		Unused pin	Not used
39	N.C.	—		Unused pin	Not used
40	V_{DD}	—		3.3 V power supply	X
41	N.C.	—		Unused pin	Not used
42	N.C.	—		Unused pin	Not used
43	N.C.	—		Unused pin	Not used
44	N.C.	—		Unused pin	Not used
45	OHS	O		Horizontal Sync. signal output pin	Not used
46	OVS	O		Vertical Sync. signal output pin	Not used
47	HREF	O		Data output horizontal reference signal output pin	Not used
48	V_{SS}	—		Ground	X
49	N.C.	—		Unused pin	Not used
50	V_{DD}	—		3.3 V power supply	X
51	CO0	O		Chrominance signal output pin bit 0 (LSB)	Not used
52	CO1	O		Chrominance signal output pin bit 1	Not used
53	CO2	O		Chrominance signal output pin bit 2	Not used
54	CO3	O		Chrominance signal output pin bit 3	Not used
55	V_{SS}	—		Ground	X
56	CO4	O		Chrominance signal output pin bit 4	Not used
57	CO5	O		Chrominance signal output pin bit 5	Not used
58	CO6	O		Chrominance signal output pin bit 6	Not used
59	CO7	O		Chrominance signal output pin bit 7 (MSB)	Not used
60	V_{DD}	—		3.3 V power supply	X
61	N.C.	—		Unused pin	Not used
62	V_{SS}	—		Ground	X
63	YO0	O		Luminance signal output pin bit 0 (LSB)	X
64	YO1	O		Luminance signal output pin bit 1	X
65	YO2	O		Luminance signal output pin bit 2	X
66	YO3	O		Luminance signal output pin bit 3	X
67	V_{DD}	—		3.3 V power supply	X
68	YO4	O		Luminance signal output pin bit 4	X
69	YO5	O		Luminance signal output pin bit 5	X
70	YO6	O		Luminance signal output pin bit 6	X
71	YO7	O		Luminance signal output pin bit 7 (MSB)	X
72	V_{SS}	—		Ground	X
73	TEST7	I	Schmitt pull-down 50k	Test input pin bit 7 (1: Test mode)	Not used or connected to GND
74	TEST6	I	Schmitt pull-down 50k	Test input pin bit 6 (1: Test mode)	Not used or connected to GND
75	$\overline{\text{RESET}}$	I	Schmitt	System reset/input pin 0: System reset 1: Operation	X
76	V_{DD}	—		3.3 V power supply	X

No.	Symbol	I/O	Pad Remarks	Pin Description	Termination of unused pin
77	N.C.	—		Unused pin	Not used
78	V_{SS}	—		Ground	X
79	MODE3	I	Schmitt pull-down 50k	Mode setting pin bit 3 (Equivalent to internal register R656I)	Not used or connected to GND
80	MODE4	I	Schmitt pull-down 50k	Mode setting pin bit 4 (Equivalent to internal register DOSEL)	Not used or connected to GND
81	N.C.	—		Unused pin	Not used
82	OE	—	Schmitt pull-down 50k	Output enable input pin	Not used or connected to GND
83	N.C.	—		Unused pin	Not used
84	N.C.	—		Unused pin	Not used
85	N.C.	—		Unused pin	Not used
86	N.C.	—		Unused pin	Not used
87	TEST5	I	Schmitt pull-down 50k	Test input pin bit 5 (1: test mode)	Not used or connected to GND
88	V_{DD}	—		3.3 V power supply	X
89	TEST4	I	Schmitt pull-down 50k	Test input pin bit 4 (1: test mode)	Not used or connected to GND
90	TEST3	I	Schmitt pull-down 50k	Test input pin bit 3 (1: test mode)	Not used or connected to GND
91	TEST2	I	Schmitt pull-down 50k	Test input pin bit 2 (1: test mode)	Not used or connected to GND
92	TEST1	I	Schmitt pull-down 50k	Test input pin bit 1 (1: test mode)	Not used or connected to GND
93	TEST0	I	Schmitt pull-down 50k	Test input pin bit 0 (1: test mode)	Not used or connected to GND
94	N.C.	—		Unused pin	Not used
95	N.C.	—		Unused pin	Not used
96	TESTM	I	Schmitt pull-down 50k	Memory test input pin (1: test mode)	Not used or connected to GND
97	SELF	I	Schmitt pull-down 50k	Self refresh test input setting pin	Not used or connected to GND
98	V_{SS}	—		Ground	X
99	N.C.	—		Unused pin	Not used
100	VDD	—		3.3 V power supply	X

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta = 25°C	–0.5 to +4.6	V
Input pin voltage	V_I	Ta = 25°C	–0.5 to V_{DD} + 0.5 ≤ 4.6	V
Output pin short-circuit current	I_{OS}	Ta = 25°C	50	mA
Power dissipation	P_D	Ta = 25°C	1	W
Operating temperature	T_{opr}	—	0 to 70	°C
Storage temperature	T_{stg}	—	–50 to +150	°C

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	3.0	3.3	3.6	V
Power supply voltage	V_{SS}	0	0	0	V
Operating temperature	Ta	0	—	70	°C

Pin Capacitance

(V_{CC} = 3.3 V ± 0.3 V, f = 1 MHz, Ta = 25°C)

Parameter	Symbol	Min.	Max.	Unit
Input capacitance	C_i	—	7	pF
Input/output capacitance (SDA)	C_{io}	—	7	pF
Output capacitance	C_o	—	7	pF

DC Characteristics

(Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
"H" level input voltage	V_{IH1}	—	$V_{DD} \times 0.7$	V_{DD}+0.3	V
"L" level input voltage	V_{IL1}	—	–0.3	$V_{DD} \times 0.3$	V
"H" level input voltage (TEST1–TEST7, TESTM, SELF)	V_{IH2}	—	$V_{DD} \times 0.75$	V_{DD}+0.3	V
"L" level input voltage (TEST1–TEST7, TESTM, SELF)	V_{IL2}	—	–0.3	$V_{DD} \times 0.25$	V
"H" level input voltage (SDA, SCL, IVS, IHS, $\overline{\text{RESET}}$)	V_{IH3}	Schmitt	$V_{DD} \times 0.75$	V_{DD}+0.3	V
"L" level input voltage (SDA, SCL, IVS, IHS, $\overline{\text{RESET}}$)	V_{IL3}	Schmitt	–0.3	$V_{DD} \times 0.25$	V
"H" level input current (pull-down)	I_{IH}	50 kΩ pull down	20	200	µA
Input leakage current	I_{IL}	—	–10	+10	µA
"H" level output voltage (other than SDA)	V_{OH}	I_{OH} = –4 mA	2.4	V_{DD}	V
"L" level output voltage (other than SDA)	V_{OL}	I_{OL} = 4 mA	0	0.4	V
"L" level output voltage (N-Ch. OD) (SDA)	V_{OOL}	I_{OL} = 4 mA	0	0.4	V
Output leakage current	I_{OL}	$0 \le V_{out} \le V_{DD}$ Output disabled	–10	+10	µA
Supply current (during operation)	I_{DD1}	ICLK: 29.5MHz Output disabled	—	100 (TBD)	mA
Supply current (during standby)	I_{DD2}	Input pin = 0 V	—	5	mA

AC Characteristics

(Ta = 0 to 70°C)

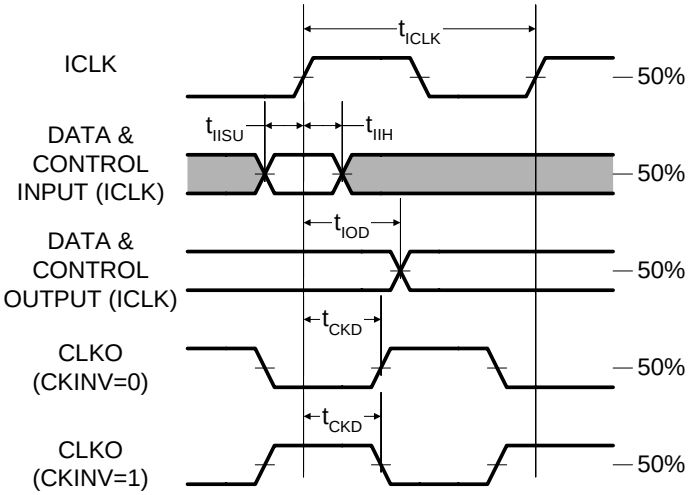
Parameter	Symbol	Condition	Min.	Max.	Unit
ICLK clock cycle time	t_{ICLK}	—	33	—	ns
ICLK clock duty ratio	dt_{ICLK}	—	40	60	%
ICLK input set-up time	t_{IISU}	—	5	—	ns
ICLK input hold time	t_{IIH}	—	3	—	ns
ICLK output delay time	t_{IOD}	C_L = 30pF	2	25	ns
CLKO delay time	t_{CKD}	C_L = 30 pF (IICLK output)	2	25	ns
		C_L = 30 pF (ICLK output)	2	17	
Data through time	t_{DIDO}	C_L = 30 pF	2	17	ns

Note 1: Measurement conditions
Output comparison level: $V_{OH} = V_{DD}/2$, $V_{OL} = V_{DD}/2$
Input voltage level: $V_{IH} = V_{DD}$, V_{IL} = 0.0 V

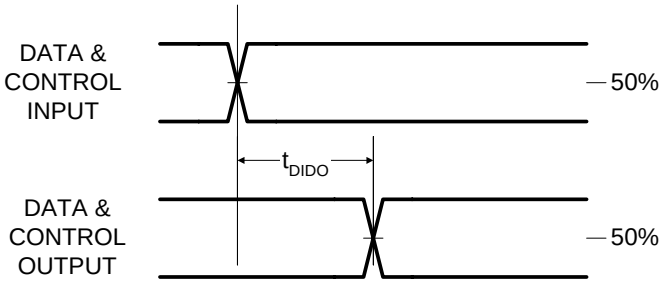
Note 2: Input/output data for the internal memory is guaranteed from the third input-system vertical synchronization signal with $\overline{\text{RESET}}$ = 1 after V_{DD} reaches 3.0 V after the power is turned on. (Due to memory initialization, the first and second data for two fields is not guaranteed.)

INPUT/OUTPUT TIMING

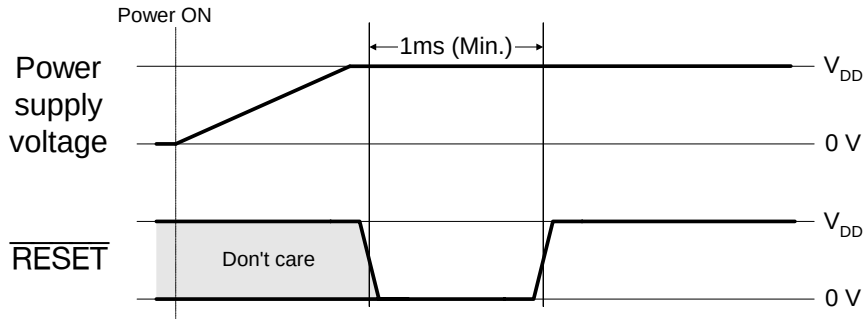
1. ICLK Input/Output Timing



2. Data through Mode Input/Output Timing



3. System Reset Timing



* When the power supply voltage reaches V_{DD} (3.0 to 3.6 V) from 0 V after power is turned on, input 0 to the $\overline{RESET}$ pin for 1 ms or more to initialize the internal circuits.

* After the $\overline{RESET}$ pin goes to 1, the I^2C-bus interface can be used while the input of ICLK is stable.

FUNCTIONAL DESCRIPTION

1. Input/Output

1.1 Memory Control

The ML87V21071 accesses data to the input data frame memory by generating a line access type memory control signal from Sync. signals of the IVS and IHS pin inputs or the Sync. signals separated from SAV and EAV, and achieves noise reduction of frame/field/line adaptation recursive type.

1.1.1 Input Control Mode Settings

As shown in the table below, this IC offers a choice of 12 input control modes including the progressive mode by the INPR setting (SUB:44h-bit[7]), which can be selected by setting either the external setting pin mode (IRMON = 0 (SUB: 40h–bit [7]) or internal register mode (IRMON = 1).
In ITU-R BT.656 input mode and in the mode of valid 720 pixels in the horizontal direction (HMD[1:0]=0h), the IC checks the mode by measuring the blanking period (between EAV and SAV) of the timing reference code of the input data (YI[7:0]) and automatically sets VMD[0] by setting APN656 = 1 (SUB: 41h-bit[2]).
During APN656=1, do not set any value other than HMD[1:0]=1.

Table F1-1-1 (1) Input Control Mode Setting Allocation 1

IRMON	VMD		HMD	
	[1]	[0]	[1]	[0]
0	SUB:40h-bit[1]	MODE 0 (External pin)	SUB:40h-bit[3]	MODE 1 (External pin)
1	SUB:40h-bit[1]	SUB:40h-bit[0]	SUB:40h-bit[3]	SUB:40h-bit[2]

Table F1-1-1 (2) Input Control Mode Setting Allocation 2

INPR	Mode
0	Interlace (525i/625i)
1	Progressive (525p/625p)

***** In progressive mode, neither 8-bit input mode nor ITU-R BT.656 input mode can be seected.

Table F1-1-1 (3) Input Control Mode Settings(INPR=0: Interlace)

VMD		HMD		Vertical mode	Number of valid lines	Standard clock frequency f_{ICLK} [MHz]	Standard pixels per line	Valid pixels
[1]	[0]	[1]	[0]					
0	0	0	0	625/50Hz 2:1	288	13.5/27	864	720
0	1	0	0	525/60Hz 2:1	243	13.5/27	858	720
0	0	0	1	625/50Hz 2:1	288	14.75/29.5	944	768
0	1	0	1	525/60Hz 2:1	243	12.272727/ 24.545454	780	640
0	0	1	0	625/50Hz 2:1	288	14.75/29.5	944	768
0	1	1	0	525/60Hz 2:1	243	14.31818/ 28.63636	910	768
Other than above				Test modes				

The input system internal clock frequency f_{IICLK} is as follows:
16-bit input mode: $f_{IICLK} = f_{ICLK}$
8-bit input mode/ITU-R BT.656 mode: $f_{IICLK} = f_{ICLK}/2$

Table F1-1-1 (4) Input Control Mode Settings(INPR=1: Progressive)

VMD		HMD		Vertical mode	Number of valid lines	Standard clock frequency f_{ICLK} [MHz]	Standard pixels per line	Valid pixels
[1]	[0]	[1]	[0]					
0	0	0	0	625/50Hz 1:1	288	27	864	720
0	1	0	0	525/60Hz 1:1	243	27	858	720
0	0	0	1	625/50Hz 1:1	288	29.5	944	768
0	1	0	1	525/60Hz 1:1	243	24.545454	780	640
0	0	1	0	625/50Hz 1:1	288	29.5	944	768
0	1	1	0	525/60Hz 1:1	243	28.63636	910	768
Other than above				Test modes				

The input system internal clock frequency f_{IICLK} is as follows:

16-bit input mode: $f_{IICLK} = f_{ICLK}$

1.1.2 Input System Field Detection

The IC detects the input data field from the phase of IVS and IHS and generates the input field pulse (IF) to control the internal memory.
The field detection pulse can be selected from the IHS (IFLS = 0) or from 0.5H pulse IHALF (IFLS = 1) by setting the I^2C-bus setting register IFLS (SUB:42h-bit[3]).
In the rear edge of judgment area, since the field judgment uncertainty area contains 10 clocks of IICLK (internal input system clock), external phase adjustment will be necessary if the phase of IVS lies in this area. (However, there is no problem if the change of IVS and IHS is in the same phase.)
When a single field Sync. signal is input (8 fields or more) while the output is in progressive mode, the inter-frame movement compensation stops.

The device also has the function to automatically generate a field pulse by judging a single field Sync. signal input (continuous for more than 8 fields) with the setting of FCON (SUB:42h-bit[7]) = 1. For example, if there is only field A input, the pulse toggled by IVS is regarded as the field pulse.

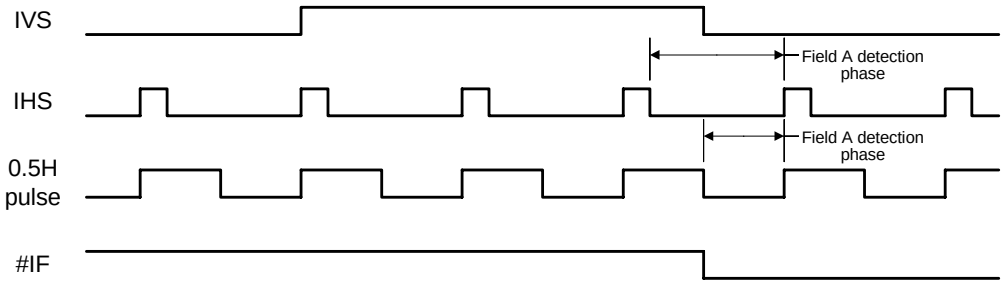


Figure F1-1-2 (1) Input System Field A Detection Timing

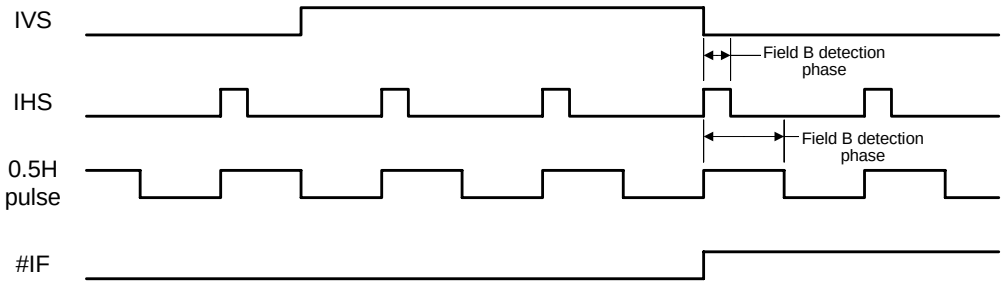


Figure F1-1-2 (2) Input System Field B Detection Timing

Figure F1-1-2 (3) Field Detection during Continuous Same Field Input (FCON = 1)

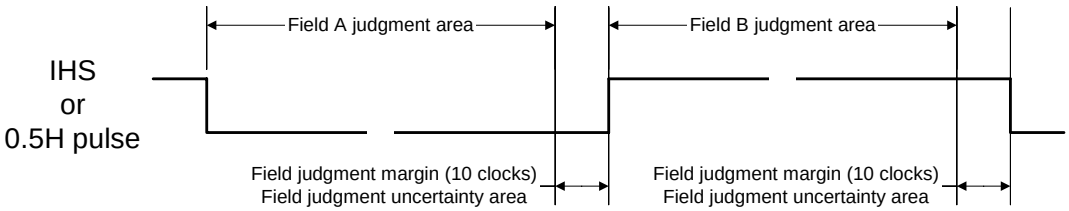


Figure F1-1-2 (4) Field Judgment Uncertainty Area

1.1.3 Setting Input System Write Enable and Read Enable

This IC generates the write enable signals (IWE) for writing data in the valid area made up of the valid vertical lines and the valid horizontal pixels defined by the input control mode settings to the write port of the frame memory.
With the write enable, it is possible to set the starting point in the vertical and horizontal directions. This setting makes it possible to position the areas of valid lines and valid pixels with non-standard phase Sync. signals.
This IC also generates a Read Enable (IRE) signal for Read operation to establish recursive noise reduction.
By setting PAOS (SUB:72h-bit[4]) to 1, the valid start offset, which is 2 lines at the setting of INPR=0 and 4 lines at the setting of INPR=1, is set and the number of valid lines is reduced by 2 lines or 4 lines from the normal condition.

Table F1-1-3(1) Valid Input Data Area (INPR=0: Interlace)

VMD		HMD		Valid lines	Valid pixels
[1]	[0]	[1]	[0]		
0	0	0	0	288(286)	720
0	1	0	0	243(241)	720
0	0	0	1	288(286)	768
0	1	0	1	243(241)	640
0	0	1	0	288(286)	768
0	1	1	0	243(241)	768
Other than above				Test modes (not settable)	

Table F1-1-3(2) Valid Input Data Area (INPR=1: Progressive)

VMD		HMD		Valid lines	Valid pixels
[1]	[0]	[1]	[0]		
0	0	0	0	576(572)	720
0	1	0	0	486(482)	720
0	0	0	1	576(572)	768
0	1	0	1	486(482)	640
0	0	1	0	576(572)	768
0	1	1	0	486(482)	768
Other than above				Test modes (not settable)	

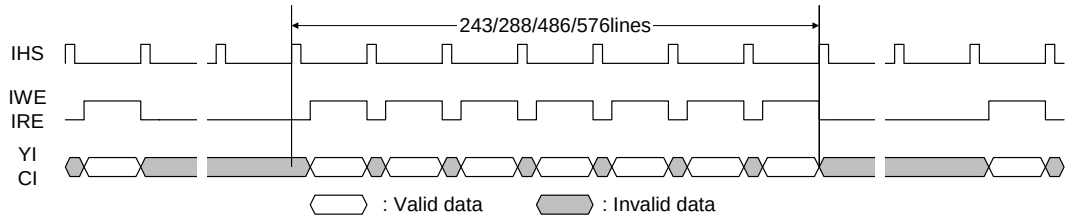


Figure F1-1-3(1) Input Vertical Valid Lines

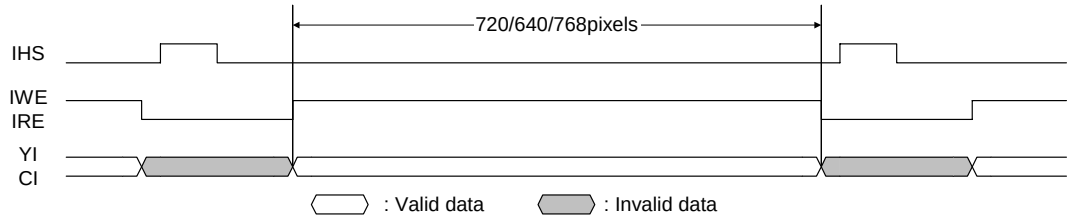


Figure F1-1-3(2) Input Horizontal Valid Pixels

- Setting of Input System Vertical Valid Line Start Position

  The input system vertical valid line start position (IVPS) is set in line unit with reference to the input system vertical reset (IVR: internal signal), generated from IVS, by setting NPVWE[4:0] (SUB:44h-bit[4:0]). Data of valid lines is written in the memory taking the input data subsequent to IVPS as valid data.
  For this value, ±7 lines (15 stages) can be set for the reference position (NPVWE[3:0]=8h) in interlace mode (INPR=0) and in progressive mode (INPR=1), ±15 lines (31 stages) can be set for the reference position (NPVWE[4:0]=10h).
  In interlace mode, NPVWE[4] is ignored.

Table F1-1-3 (3) Input System Vertical Valid Line Start Position (INPR=0: Interlace)

R656I	VMD		IVPS position (number of IHS's from IVR)				
	[1]	[0]	NPVWE=1h	……	NPVWE=8h	……	NPVWE=Fh
0	0	0	13 (–7 lines)	……	20 (default)	……	27 (+7 lines)
0	0	1	7 (–7 lines)	……	14 (default)	……	21 (+7 lines)
1	0	0	17 (–7 lines) (*1)	……	24 (default) (*1)	……	31 (+7 lines) (*1)
1	0	1	12 (–7 lines) (*1)	……	19 (default) (*1)	……	26 (+7 lines) (*1)
Other than above			Test modes (not settable)				

*1: In the case of field B, it is +1.

Table F1-1-3 (4) Input System Vertical Valid Line Start Position (INPR=1: Progressive)

R656I	VMD		IVPS position (number of IHS's from IVR)				
	[1]	[0]	NPVWE=1h	……	NPVWE=10h	……	NPVWE=1Fh
0	0	0	24 (–15 lines)	……	49 (default)	……	54 (+15 lines)
0	0	1	12 (–15 lines)	……	27 (default)	……	42 (+15 lines)

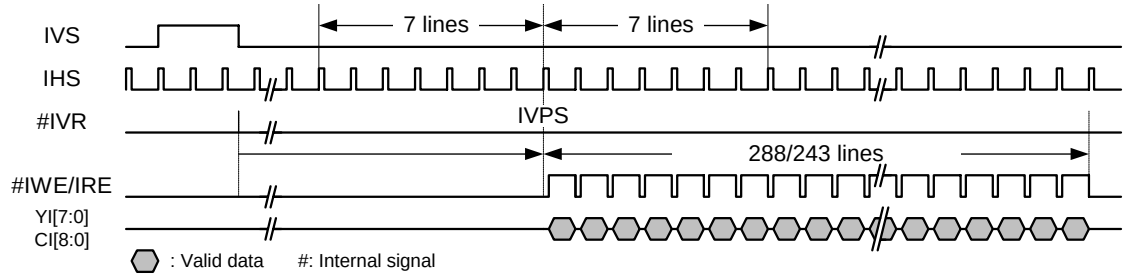


Figure F1-1-3 (3) Input System Vertical Valid Line Start Timing (INPR=0)

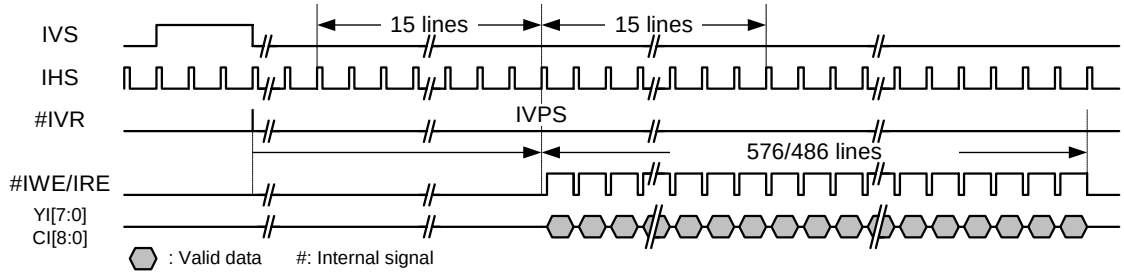


Figure F1-1-3 (4) Input System Vertical Valid Line Start Timing (INPR=1)

- Setting of Input System Horizontal Valid Pixel Start Position

The input system horizontal valid pixel start position (IHPS) is set in pixel unit with reference to the input system horizontal reset (IHR: internal signal), generated from IHS, by setting NPHWE[7:0] (SUB:45h-bit[7:0]).
The data subsequent to IHPS is written in the data memory of valid pixels as the valid data.
This value can be set in 255 levels of ±127 pixels with regard to the initial value (NPHWE[7:0] = 80h).
In the ITU-R BT.656 mode, the value cannot be set. Write enable with regard to valid data is generated on the basis of detected SAV, EAV.

Table F1-1-3 (5) Input System Horizontal Valid Pixel Start Position

HMD		VMD	IHPS position (Number of pixels from IHS)				
[1]	[0]	[0]	NPHWE=01h	……	NPHWE=80h	……	NHPWE=FFh
0	0	0	17 (–127 pixels)	……	144 (default)	……	271 (+127 pixels)
0	0	1	11 (–127 pixels)	……	138 (default)	……	265 (+127 pixels)
0	1	0	49 (–127 pixels)	……	176 (default)	……	303 (+127 pixels)
0	1	1	13 (–127 pixels)	……	140 (default)	……	267 (+127 pixels)
1	0	0	49 (–127 pixels)	……	176 (default)	……	303 (+127 pixels)
1	0	1	15 (–127 pixels)	……	142 (default)	……	269 (+127 pixels)
Other than above			Test modes (Setting inhibited)				

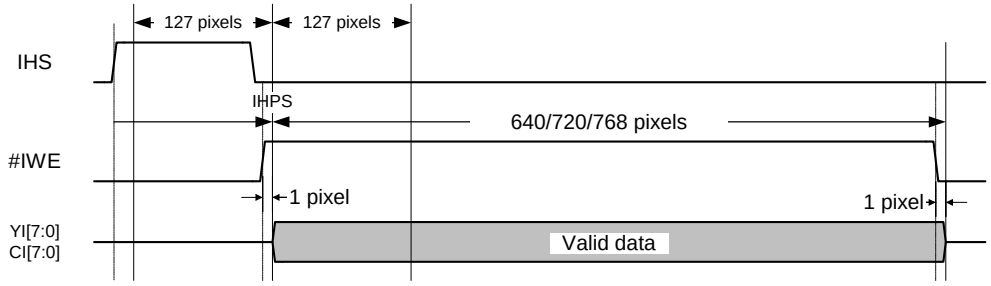


Figure F1-1-3 (5) Input System Horizontal Valid Pixel Start Timing

1.1.4 Input System Sync. Signal Polarity Inversion Setting

Negative polarity IVS can also be supported by setting the I^2C-bus setting register IVSINV (SUB:42h-bit[0]). Moreover, with regard to field detection, setting is possible even when setting the internal IVR generation edge.

Table F1-1-4 (1) IVINV Setting

IVSINV	Recommended input IVS polarity	IVR generation edge
0	Positive (default)	Rising edge
1	Negative	Falling edge

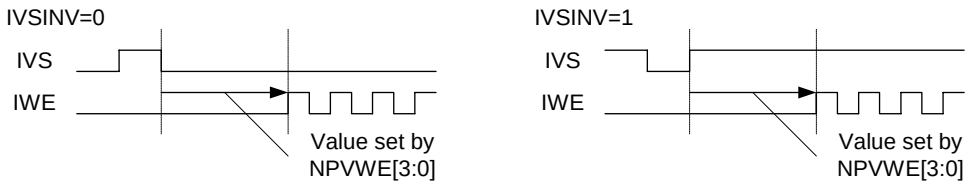


Figure F1-1-4 (1) Support of Input System Vertical Sync. Signal Polarity Inversion

Negative polarity IHS can also be supported by setting the I^2C-bus setting register IHSINV (SUB:42h-bit[1]).

Table F1-1-4 (2) IHSINV Setting

IHSINV	Input IHS polarity
0	Positive (default)
1	Negative

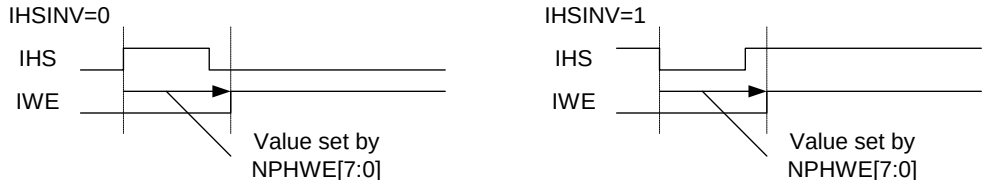


Figure F1-1-4 (2) Support of Input System Horizontal Sync. Signal Polarity Inversion

1.1.5 Input System Detection Field Inversion Setting

Inversion of input system internal field detection is possible by setting IFINV (SUB:42h-bit[2]) by I^2C-bus interface. However, setting is not necessary if there is no problem in normal detection.

Table F1-1-5 IFIND Setting

IFINV	Input field	
	Field A	Field B
0	0	1
1	1	0

* PAL : Field A = 1st, 3rd, 5th, 7th color field
Field B = 2nd, 4th, 6th, 8th color field
* NTSC : Field A = 2nd, 4th color field
Field B = 1st, 3rd color field

1.1.6 Input System Vertical Reset Compensation Mode Setting

In this IC, the rear edge (in the case of standard signal, 625 lines; A-3 line, 0.5H position, in between B-315 and B-316 lines, 525 lines; A-6 line, 0.5H position, in between B-6 and B-7 lines) of normally standard vertical Sync. signal (IVS) is regarded as the reference position (IVR generating position) to perform field detection and memory control.
If a Sync. signal with unspecified phase of the IVS rear edge and horizontal Sync. signal (IHS) is input, the front edge can be used with the setting IVSINV = 1. But if the front edge is used in standard 626-line mode, the detection filed reverses in normal operation and field B gets written in the memory with one line earlier phase.
Therefore, by setting the I^2C-bus setting register IVEM (SUB:42h-bit[4]), the detection field is inverted (A→B, B→A) and the vertical phase with regard to field B of the inverted result is delayed by 1H.
This allows compensation for field detection and IVR which is the typical front edge phase of IVS of 625-line mode.
In practice, this allows compliance with the Sync. signal examples shown in Table F1-1-6 and Figure F1-1-6.

Note: Use it in case the phase of field-detecting IVS and IHS reverses in the IC standard setting.

Table F1-1-6 Input System Vertical Reset Compensation by IVEM Setting

Condition	Vertical reference	Input data field	Internal decision field	IVEM setting	Field after compensation	Valid data start position
Phase 1	Rear edge IVSINV = 0	A	A	0	No compensation	n
		B	B			n
Phase 2	Rear edge IVSINV = 0	A	B	1	A	n
		B	A		B	n + 1
Phase 3	Front edge IVSINV = 1	A	A	0	No compensation	n
		B	B			n
Phase 4	Front edge IVSINV = 1	A	B	1	A	n
		B	A		B	n + 1

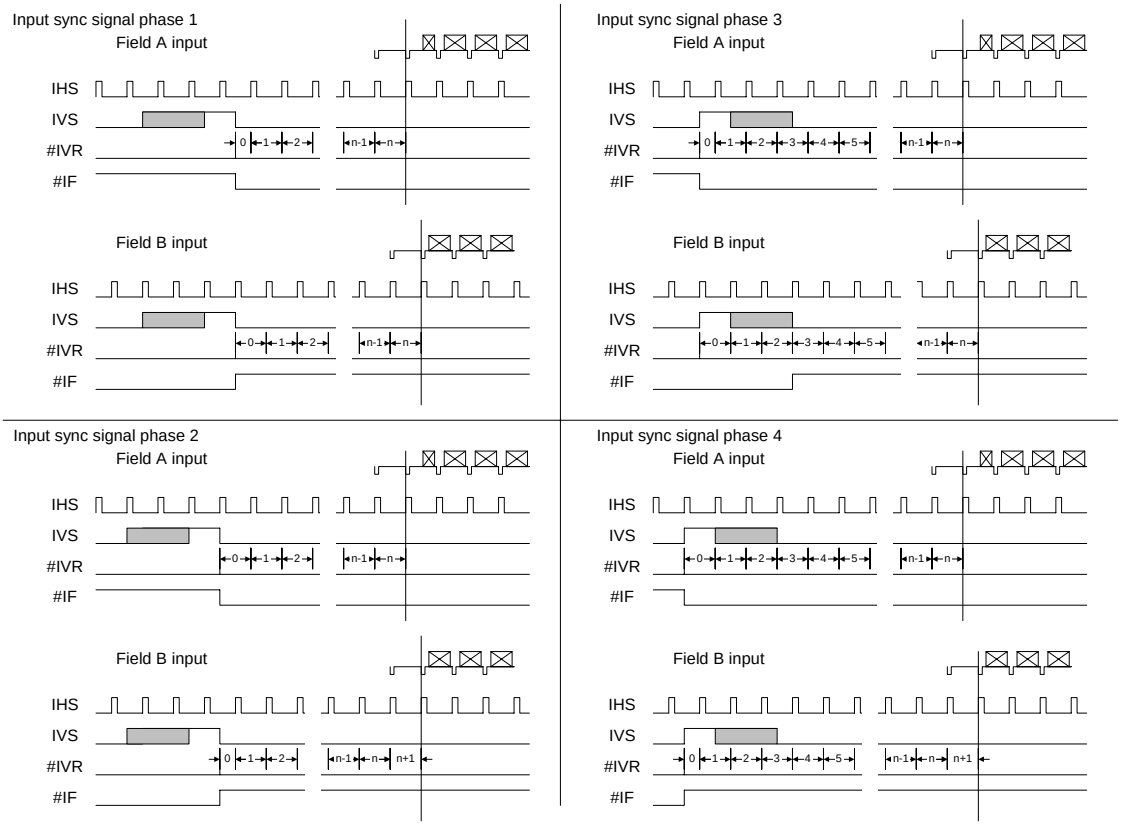


Figure F1-1-6 Input System Vertical Reset Compensation by IVEM Setting

1.1.7 Stop Memory Write Setting (Freeze Function)

By setting the I^2C-bus settings register STL[2:0] (SUB:43h-bit[2:0]), you can stop writing data to the memory. When you do this, the noise reduction feature stops.
Further, by setting STLM[1:0] (SUB:43h-bit[4:3]), field still image output, frame still image output, or frame still median) image output can be selected.
The still image data output is achieved by rewriting only the signals read from the memory for the valid data period selected by the IBLK signal, which indicates the valid data. Therefore, it is necessary to input the input Sync. signals as normal.
The data output as a field or frame (median) still image is based on the most recent data written to the memory (before the writing was stopped).
The timing of the writing stop and restoration can be set in one of the following three modes: selected field A/B timing, field A timing, and field B timing.
In the mode of selected field A/B timing, writing is stopped after data for the next frame (field A + field B) after writing stop is set is written. Writing is restored from the next frame after writing restoration is set. In this mode, the field still image output depends on the writing stop setting timing.
In the mode of field A timing, after data for one frame (field B + field A) is written from the field B after writing stop is set, writing is stopped from the next field B vertical Sync. signal. Writing is restored with the field B vertical Sync. signal. In this mode, field A is always output for the field still image output.
In the mode of field B timing, after data for one frame (field A + field B) is written from the field A after writing stop is set, writing is stopped from the next field A vertical Sync. signal. Writing is restored with the field A vertical Sync. signal. In this mode, field B is always output for the field still image output.
When INPR is set to 1, the setting of field timing STL[2:1] is ignored and only STL[0] stop operation is performed.

Table F1-1-7(1) Writing Stop Settings

STL			Input data writing
[2]	[1]	[0]	
0	0	0	Possible (field A restoration)
0	1	0	Possible (field B restoration)
1	X	0	Possible (either field restoration)
0	0	1	Stopped (field A maintained)
0	1	1	Stopped (field B maintained)
1	X	1	Stopped (either field output maintained)

Table F1-1-7 (2) Still Image Output Mode Settings

STLM		Output still image
[1]	[0]	
0	X	Field image
1	0	Frame image
1	1	Frame image (median)

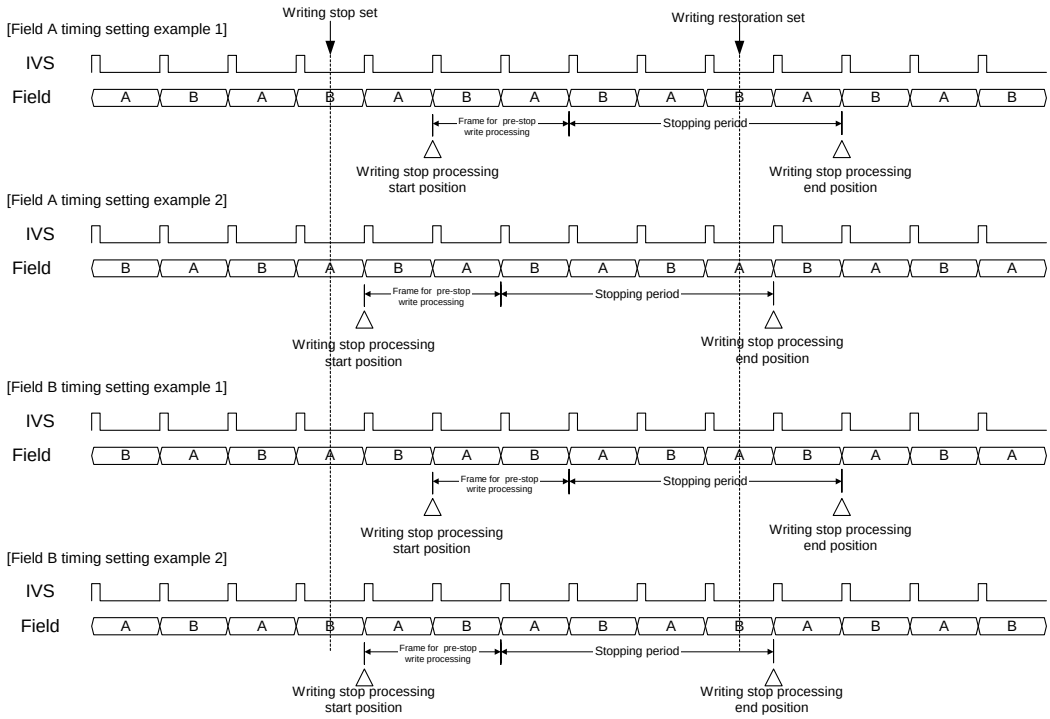


Figure F1-1-7 (1) Writing Stop/Restoration Timing

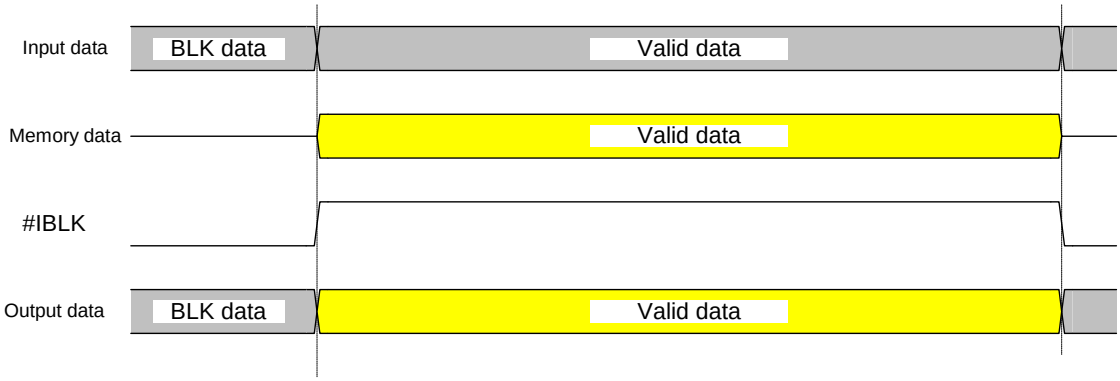


Figure F1-1-7(2) Output Data in Still Image Mode

* When MEM411 is set to 1, output data from the memory is converted to 4:2:2 data (pseudo conversion) through linear interpolation of chrominance data since the output data is 4:1:1 data. Therefore, the band of the data on the chrominance side deteriorates from that of the normal data.

1.2 Input/Output Format

1.2.1 Input Data Format

The input of this IC complies with 16-bit 4:2:2 (YI[7:0] = Y-8bit, CI[7:0] = CbCr-8bit 4:2:2) format (input in 16-bit mode), 8-bit 4:2:2 (YI[7:0] = YCbCr-8bit 4:2:2, without SAV, EVA) format (input in 8-bit mode) and ITU-R BT.656 conforming (YI[7:0] = YCbCr-8bit 4:2:2, with SAV, EAV) format (ITU-R BT.656 mode).
However, when INPR is set to 1, neither 8-bit input mode nor ITU-R BT.656 input mode can be selected.
The input format mode is set by an external pin MODE 2 or I^2C-bus setting register DISEL (SUB:41h-bit[0]), or R656 (SUB:41h-bit[1]).
Switching of an external pin and a register is accomplished by setting the I^2C-bus setting register IRMON (SUB:40h-bit[7]).

Table F1-2-1 (1) Input Data Format Mode

IRMON	MODE2	DISEL	R656I	Mode
0	0	X	0	Input in 16-bit mode
1	X	0	0	
0	1	X	0	Input in 8-bit mode
1	X	1	0	
X	X	X	1	ITU-R BT.656 mode

Table F1-2-1(2) Input Data Format

Input pin	Input in 16-bit mode		Input in 8-bit mode ITU-R BT.656 mode			
YI7	Y07	Y17	Cb07	Y07	Cr07	Y17
YI6	Y06	Y16	Cb06	Y06	Cr06	Y16
YI5	Y05	Y15	Cb05	Y05	Cr05	Y15
YI4	Y04	Y14	Cb04	Y04	Cr04	Y14
YI3	Y03	Y13	Cb03	Y03	Cr03	Y13
YI2	Y02	Y12	Cb02	Y02	Cr02	Y12
YI1	Y01	Y11	Cb01	Y01	Cr01	Y11
YI0	Y00	Y10	Cb00	Y00	Cr00	Y10
CI7	Cb07	Cr07	—	—	—	—
CI6	Cb06	Cr06	—	—	—	—
CI5	Cb05	Cr05	—	—	—	—
CI4	Cb04	Cr04	—	—	—	—
CI3	Cb03	Cr03	—	—	—	—
CI2	Cb02	Cr02	—	—	—	—
CI1	Cb01	Cr01	—	—	—	—
CI0	Cb00	Cr00	—	—	—	—
Y point	0	1	0		1	
C point	0		0			

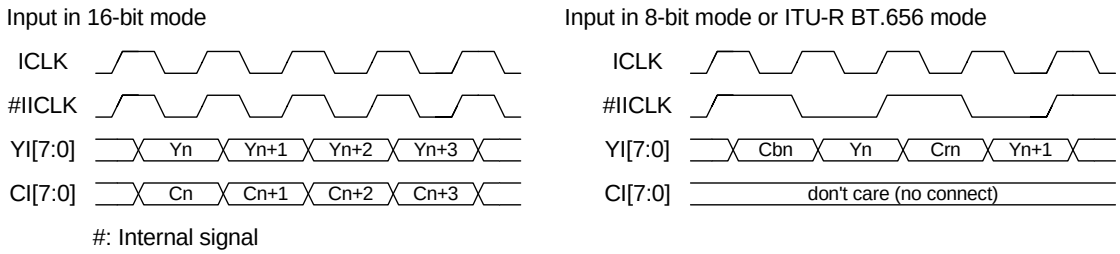


Figure F1-2-1 (1) Input Data Timing

The data and control signal interfaces according to input system modes are as follows.

- Input in 16-bit mode
  Vertical Sync. signal: IVS
  Horizontal Sync. signal: IHS
  Data input pin: YI[7:0], CI[7:0] (YCbCr-4:2:2)
  Input system clock frequency: f_{ICLK} = 12.2727272/13.5/14.31818/14.75 MHz
  Clip level: None

- Input in 8-bit mode
  Vertical Sync. signal: IVS
  Horizontal Sync. signal: IHS
  Data input pin: YI[7:0], (YCbCr-4:2:2)
  Input system clock frequency: f_{ICLK} = 24.545454/27/28.63636/29.5 MHz
  Clip level: None

- ITU-R BT.656 mode
  Vertical Sync. signal: SAV, EAV split
  Horizontal Sync. signal: SAV, EAV split
  Data input pin: YI[7:0] (YCbCr-4:2:2)
  Input system clock frequency: f_{ICLK} = 27 MHz
  Clip level: 00h → 01h, FFh → Feh
  * By setting POFF (SUB:41h-bit[6]) to 1, the parity bits of SAV and EAV can be disabled.

• Internal Input System Clock (IICLK)

The IICLK is IICLK = ICLK in 16-bit 4:2:2 mode whereas in 8-bit 4:2:2 mode and ITU-R BT.656 mode it is the clock pulse obtained by internally frequency-dividing ICLK to 1/2.

In 8-bit 4:2:2 mode, the position which is two ICLK clocks delayed from the rise of IHS is used for resetting and IICLK is generated by frequency-dividing ICLK to 1/2.

Normally reset of IICLK presumes the rise position of positive polarity IHS (IHSINV = 0), but by setting IHES (SUB:41h-bit[5]) and IHSINV, selection of compliance with negative polarity IHS and fall position is also possible.

In ITU-R BT 656 mode, ICLK is frequency-divided to 1/2 based on SAV.

In 8-bit 4:2:2 mode, if the phase of IHS for luminance and chrominance data reverses (number of ICLKs from IICLK reset to initial chrominance data is odd), it is possible to avoid the reversal by setting ICINV (SUB:41h-bit[4]).

Table F1-2-1 (3) IICLK Reset Position

IHES	IHSINV	Reset position
0	0	Positive polarity IHS rise (horizontal Sync. signal front edge)
1	0	Positive polarity IHS fall (horizontal Sync. signal rear edge)
0	1	Negative polarity IHS fall (horizontal Sync. signal front edge)
1	1	Negative polarity IHS rise (horizontal Sync. signal rear edge)

Table F1-2-1 (4) Compliance with Luminance-Chrominance Phase Reversal

ICINV	Usage conditions (8-bit 4:2:2 mode)
0	Number of ICLKs from IICLK reset to initial chrominance data is even.
1	Number of ICLKs from IICLK reset to initial chrominance data is odd.

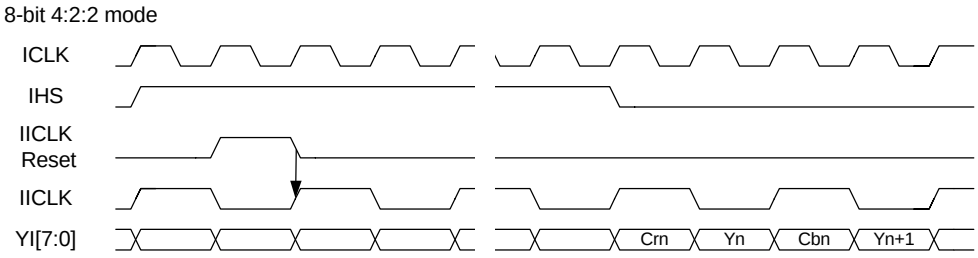


Figure F1-2-1 (2) IICLK Phase Timing Example

1.2.2 Output Data Format

Since internal signal processing is performed independently for luminance and chrominance signals, the output data format of basic output of this IC is YCbCr 16bit 4:2:2.
However, in YCbCr 8bit 4:2:2 mode and ITU-R BT.656 mode, selection of YCbCr 8bit 4:2:2 (same format as input) is enabled by setting DOSEL (SUB:60h-bit[1]) to 1. In this case, unused CO[7:0] becomes Hi-Z.
Table F1-2-2(2) shows the delay amount from input to output and the same delay amount occurs for all the data and Sync. signals.

Table F1-2-2 (1) Output Data Format

Output	Normal mode		8-bit input – 8-bit output mode (DOSEL =1)			
YO7	Y07	Y07	Cr07	Y17	Cb07	Y17
YO6	Y06	Y06	Cr06	Y16	Cb06	Y16
YO5	Y05	Y05	Cr05	Y15	Cb05	Y15
YO4	Y04	Y04	Cr04	Y14	Cb04	Y14
YO3	Y03	Y03	Cr03	Y13	Cb03	Y13
YO2	Y02	Y02	Cr02	Y12	Cb02	Y12
YD1	Y01	Y01	Cr01	Y11	Cb01	Y11
YD0	Y00	Y00	Cr00	Y10	Cb00	Y10
CO7	Cb07	Cr07	—	—	—	—
CO6	Cb06	Cr06	—	—	—	—
CO5	Cb05	Cr05	—	—	—	—
CO4	Cb04	Cr04	—	—	—	—
CO3	Cb03	Cr03	—	—	—	—
CO2	Cb02	Cr02	—	—	—	—
CO1	Cb01	Cr01	—	—	—	—
CO0	Cb00	Cr00	—	—	—	—

Table F1-2-2(2) Combinations for Input/Output Data Format

DISEL	R656I	DOSEL	Input	Output	Input/output delay amount
0	0	X	16-bit + Sync (H, V)	16-bit + Sync (H, V)	32 (ICLK)
1	0	0	8-bit + Sync (H, V)	8-bit + Sync (H, V)	64 (ICLK)
1	0	1	8-bit + Sync (H, V)	8-bit + Sync (H, V)	66 (ICLK)
X	1	0	ITU-R BT.656	16-bit + Sync (H, V)	64 (ICLK)
X	1	1	ITU-R BT.656	ITU-R BT.656 + Sync (H, V)	66 (ICLK)

* When input is ITU-R BT.656, Sync (H, V) on the output side is output to OVS and OHS as the Sync. signal separated from SAV and EAV.

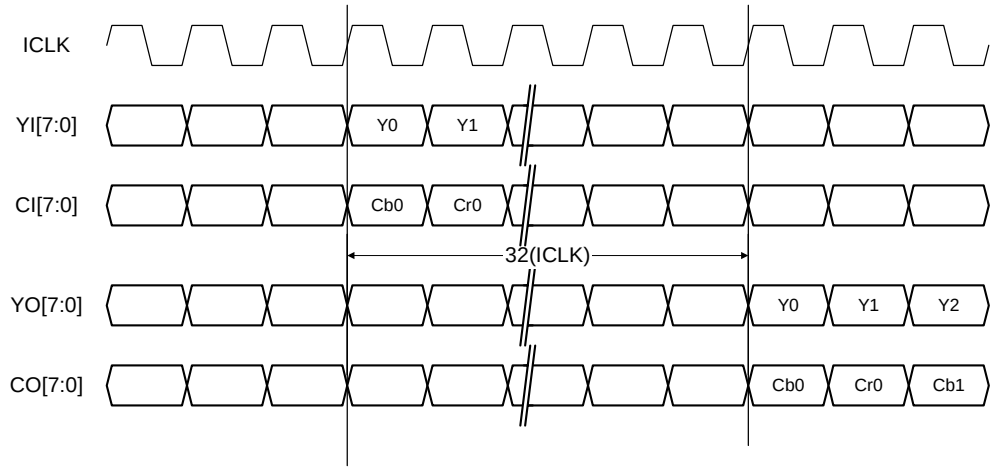


Figure F1-2-2(1) Input/Output Delay in 16-Bit Input Mode

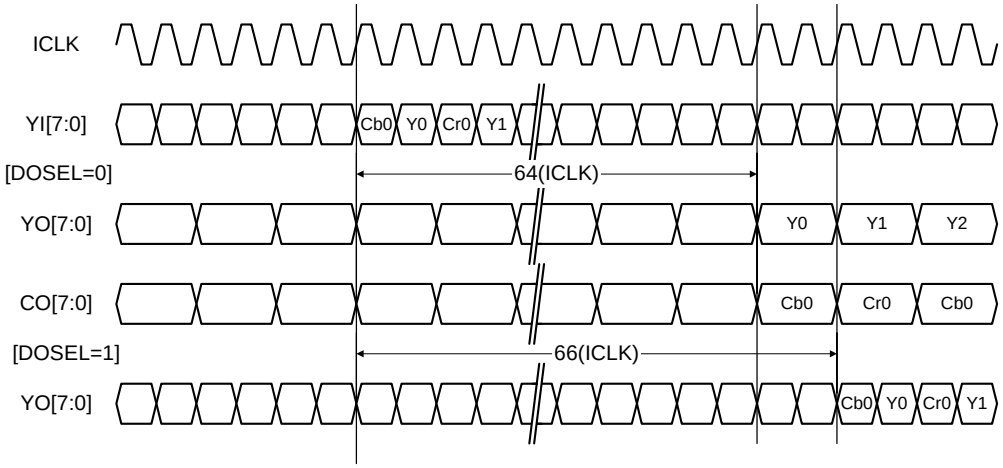


Figure F1-2-2(2) Input/Output Delay in 8-Bit Input Mode

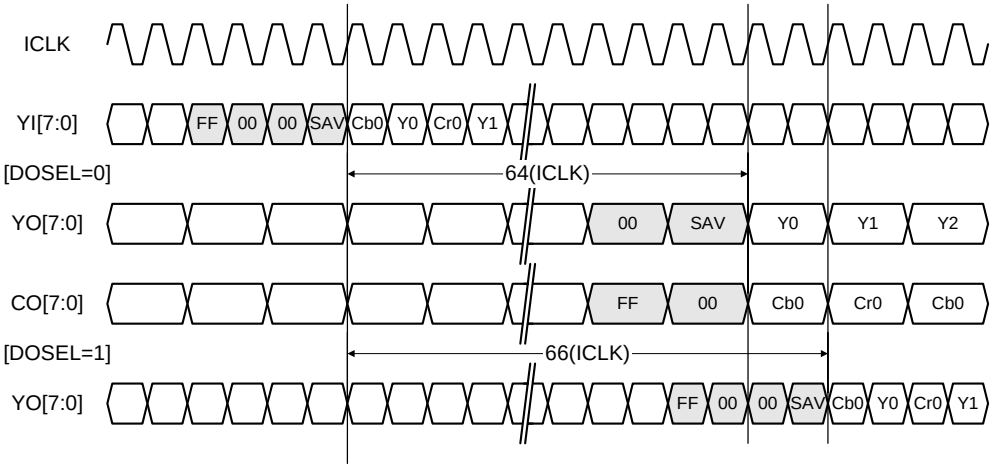


Figure F1-2-2(3) Input/Output Delay in ITU-R BT.656 Mode

2. Video Signal Processing Functions

2.1 Motion-Adaptive 3D Noise Reduction

This IC performs noise reduction first by detecting noise and predicting motion using frame recursion, field recursion, and line correlation, then by performing noise subtraction while performing motion compensation for the detected noise. Moreover, it achieves adaptive noise reduction by synthesizing four NR data items based on prediction of motion.
However, when INPR is set to 1, the field recursion stops and adaptive noise reduction is performed by the two NR data items, frame recursion and line correlation.

- Principle of Noise Reduction
  Difference between the current field data and the filed data preceding one frame, one field, or one line is extracted as time motion and noise independently for luminance and chrominance signals.
  The low gain portion of this data is judged to be noise and the high gain portion to be motion and is extracted as motion level detection noise.
  The noise component extracted here is subjected to motion prediction by adjacent motion level and adjacent code, then further subjected to compensation based on motion and is regarded as the final noise component.
  Finally, noise reduction is carried out by subtracting this final noise data from the current field data.

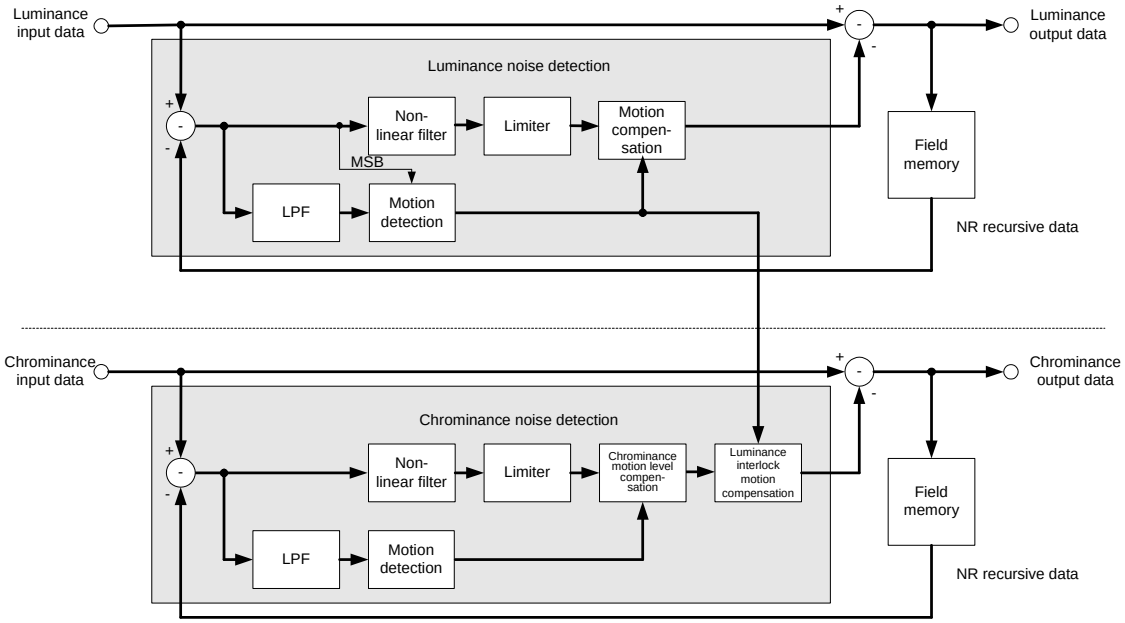


Figure F2-1 (1) Noise Detection Type Noise Reduction Configuration

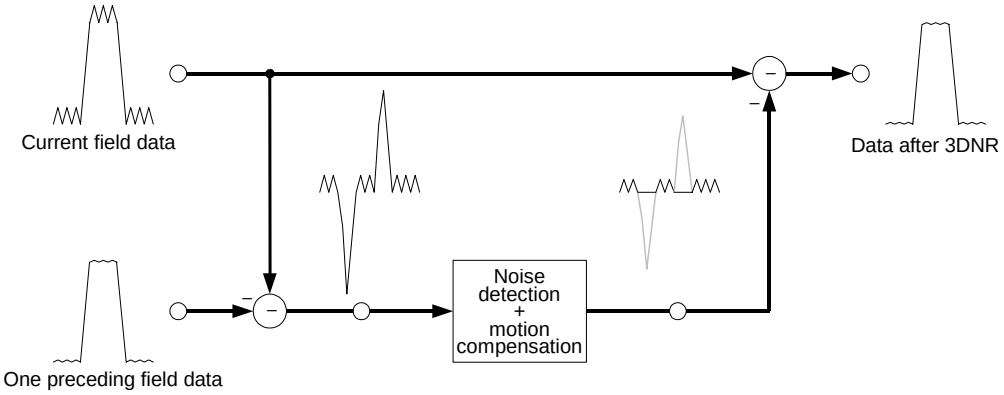


Figure F2-1(2) Noise Reduction by Noise Detection

- Principles of Adaptive Noise Reduction
  Adaptive noise reduction is achieved through the selection of noise reduction data, which utilizes the correlative relationships between frames, fields, and lines for the pixels for which noise reduction is to be performed, as shown in Figure F2-3 (3).

  The distinguishing characteristics of each correlation are as shown below.

  Between frames : Same position (most effective), time difference 2V (less effective)
  →Effective for still images (good NR, substantial afterimage)

  Between fields : Position 0.5H different (effective), time difference 1V(effective)
  →More effective for moving images than frames, more effective for still images than lines (medium NR, medium afterimage)

  Between lines : Position 1H different (less effective), time difference 0 (most effective)
  →Effective for moving images, but not effective for edges (medium NR, no afterimage, no NR for edges)

  This IC detects motions and edges between lines, frames, and fields, based on the features described above, to select data after better correlated NR and achieve effective noise reduction.

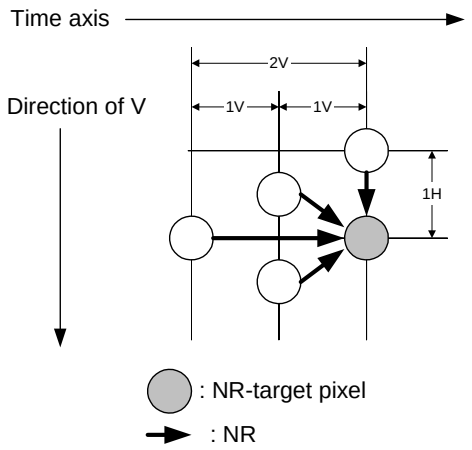


Figure F2-1 (3) Noise Reduction Correlation

2.1.1 Noise Reduction Mode

The noise reduction mode is set by NR2OFF(SUB:48h-bit[4]), FNRM[1:0] (SUB:48h-bit[6:5]), and you can select the noise reduction modes shown in Table F2-1-1.
Synthesis of an adaptive noise reduction mode is performed by checking motions that are predicted from the motion detection signal and differential signal level that are detected at noise reduction between frames, fields, or lines.
For determining the motion difference level, weighting factor can be applied to frames by setting the adaptive margin that is set by YFAM(SUB:4Ah-bit[1]), CFAM(SUB:4Bh-bit[1]). NR effect is improved by applying weighting factor to frames (however, afterimage will be more likely to occur).

Table F2-1-1 (1) Noise Reduction Modes

FNRM		NR2OFF	Noise Reduction Mode
[1]	[0]		
0	0	0	Fully adaptive frame-recursive NR (uses frames, fields, and lines)
0	0	1	3D adaptive frame-recursive NR (uses frames and fields)
0	1	0	2D adaptive frame-recursive NR (uses frames and lines)
0	1	1	Frame-recursive NR
1	X	0	2D adaptive field-recursive NR (uses fields and lines)
1	X	1	Field-recursive NR

Table F2-1-1 (2) Luminance Adaptive Margin Settings

YFAM	Luminance adaptive margin	Remarks
0	0	
1	–2	Frame NR performance emphasized (larger NR, larger afterimage)

F2-1-1 (3) Chrominance Adaptive Margin Settings

CFAM	Chrominance adaptive Margin	Remarks
0	0	
1	–2	Frame NR performance emphasized (larger NR, larger afterimage)

2.1.2 Detected Noise Between Frames, Fields and Lines

The differences are calculated between
- one pixel in the current field and one pixel preceding by one frame,
- one pixel in the current field and two pixels by one field, and
- one pixel in the current field and one pixel preceding by one line.

Among the absolute values of these differences, the smallest value is selected.

From the differential values between frames and between fields (ΔY, ΔC), the signal with a low level of absolute value for the differential values (|ΔY|, |ΔC|) is judged to be the noise component and the signal with a high level is judged to be the motion component. The data judged to be the noise is extracted as the motion level detection noise.

The detected noise is output after being filtered by the area covered by the input noise detection line, the noise convergence line, and the noise upper limit line. The inclination of the input noise detection line is set by YSLT[1:0](SUB:4Ah-bit[5:4]) and CSLT[1:0](SUB:4Bh-bit[5:4]), the inclination and offset of the noise convergence line are set by YSLT[3:2](SUB:4Ah-bit[7:6]), YNS[5:0] (SUB:4Ch-bit[5:0]), CSLT[3:2] (SUB:4Bh-bit[7:6]) and CNS[5:0] (SUB:4Dh-bit[5:0]), and the offset of the noise upper limit line, which has 0 inclination, is set by YLM[4:0] (SUB:4Eh-bit[4:0]) and CLM[4:0] (SUB:4Fh-bit[4:0]). (Figure F2-1-1)

Table F2-1-2 Non-Linear Filter Noise Detection Area Settings

YSLT/CSLT				Noise detection line		Noise convergence line		Noise upper limit line	
[3]	[1]	[2]	[0]	Inclination	Offset	Inclination	Offset	Inclination	Offset
0	0	0	0	1	0	–1	YNS[5:0] CNS[5:0]	0	YLM[4:0] CLM[4:0]
0	0	0	1	7/8					
0	1	0	0	3/4					
0	1	0	1	1/2					
0	0	1	0	1		–3/4			
0	0	1	1	7/8					
0	1	1	0	3/4					
0	1	1	1	1/2					
1	0	0	0	1		–1/2			
1	0	0	1	7/8					
1	1	0	0	3/4					
1	1	0	1	1/2					
1	0	1	0	1		–3/2			
1	0	1	1	7/8					
1	1	1	0	3/4					
1	1	1	1	1/2					

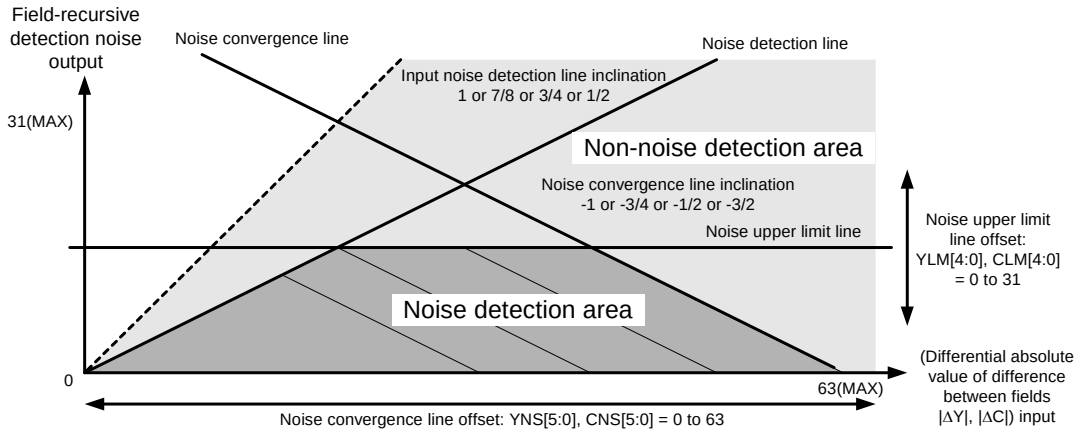


Figure F2-1-2 Field-Recursive Noise Motion Level Detection Noise Characteristics

2.1.3 Detection of Motion between Frames, Fields, and Lines

There are two types of luminance signal motion detection: level motion detection and continuous code motion detection.
Chrominance signal motion detection includes level motion detection.

① Luminance Level Motion Detection
From the differential data between fields, including luminance signal motion and noise, the high frequency component (ΔHY) is filtered with the LPF, extracting only the low frequency differential data (ΔLY).

Luminance LPF: $F(z) = (1/8)z^{-2} + (1/8)z^{-1} + (1/2)z^{0} + (1/8)z^{1} + (1/8)z^{2}$

The low frequency differential data is assumed to have a large proportion of the motion component, so the absolute value of that data (|ΔLY|) is compared with the luminance noise convergence level set in YNS[5:0] to determine the amount of motion.
If the result shows that the differential absolute value is greater than the noise convergence level, it is determined that there is a lot of motion in the data, and the motion flag (YMT) = 1 is set.
If the differential absolute value is less than the noise convergence level, it is determined that there is not much motion in the data, and the motion flag (YMT) = 0 is set.

Table F2-1-3 (1) Luminance Level Motion Detection

Motion Detection Conditions	Motion Flag (YMT)
|ΔLY| > 64	1
|ΔLY| > YNS[5:0]	1
|ΔLY| ≤ YNS[5:0]	0

② Luminance Continuous Code Motion Detection
This feature detects sequences of 3, 4, and 5 continuous codes in the differential data that includes the pixels for which noise detection is being performed. Where continuity is detected, the absolute value of the low frequency differential data and the continuous code motion detection level YMS[3:0](SUB:50h-bit[3:0]) are compared to determine the amount of motion.

- 3 Continuous Code Detection

If 3 continuous codes are detected to be the same and their low frequency differential data absolute values are equal to or greater than the continuous code motion detection level (YMS[3:0]), the data is judged to have much motion, and the 3 continuous code motion flag (YMT3) = 1 is set.
If the absolute value is less than the continuous motion detection level, the data is judged to have little motion, and the 3 continuous code motion flag (YMT3) = 0 is set.

Table F2-1-3 (2) Luminance 3 Continuous Code Motion Detection

Motion detection condition	Motion flag (YMT3)
|ΔLY| > 16	1
|ΔLY| ≥ YMS[3:0]	1
|ΔLY| < YMS[3:0]	0

• 4 Continuous Code Detection

If 4 continuous codes are detected to be the same and their low frequency differential data absolute values are equal to or greater than the continuous code motion detection level 1/2(YMS[3:1]), the data is judged to have much motion, and the 4 continuous code motion flag (YMT4) = 1 is set.
If the absolute value is less than the continuous motion detection level, the data is judged to have little motion, and the 4 continuous code motion flag (YMT4) = 0 is set.
By setting YMDM(SUB:50h-bit[4]) = 1, the detection precision of the 4-continuous code motion flag can be improved.

Table F2-1-3 (3) Luminance 4 Continuous Code Motion Detection

Motion detection condition	Motion flag (YMT4)
$\|\Delta LY\| > 8$	1
$\|\Delta LY\| \geq YMS[3:1]$	1
$\|\Delta LY\| < YMS[3:1]$	0

• 5 Continuous Code Detection

If 5 continuous codes are detected to be the same and their low frequency differential data absolute values are equal to or greater than the continuous code motion detection level 1/4 (YMS[3:2]), the data is judged to have much motion, and the 5 continuous code motion flag (YMT5) = 1 is set.
If the absolute value is less than the continuous motion detection level, the data is judged to have little motion, and the 5 continuous code motion flag (YMT5)=0 is raised.
By setting YMDM(SUB:50h-bit[4]) = 1, the detection precision of the 5-continuous code motion flag can be improved.

Table F2-1-3 (4) Luminance 5 Continuous Code Motion Detection

Motion detection condition	Motion flag (YMT5)
$\|\Delta LY\| > 4$	1
$\|\Delta LY\| \geq YMS[3:2]$	1
$\|\Delta LY\| < YMS[3:2]$	0

③ Chrominance Level Motion Detection

From the differential data between fields, including chrominance signal motion and noise, the high frequency component (ΔHC) is filtered with the LPF, extracting only the low frequency differential data (ΔLC).

Chrominance LPF: $F(z) = (1/4)z^{-2} + (1/2)z^{0} + (1/4)z^{2}$

The low frequency differential data is assumed to have a large proportion of the motion component, so the absolute value of that data ($|\Delta LC|$) is compared with the chrominance noise convergence level set in CNS[5:0] to determine the amount of motion.
If the result shows that the differential absolute value is greater than the noise convergence level, the data is judged to have a lot of motion, and the chrominance motion flag (CMT) = 1 is set.
If the differential absolute value is less than the noise convergence level, it is determined that there is not much motion in the data, and the motion flag (CMT) = 0 is set.
This motion flag is used in adjacent pixel motion compensation.

Table F2-1-3 (5) Chrominance Level Motion Detection

Motion detection condition	Motion flag (CMT)
$\|\Delta LC\| > 64$	1
$\|\Delta LC\| > CNS[5:0]$	1
$\|\Delta LC\| \leq CNS[5:0]$	0

2.1.4 Motion Compensation Processing

This IC performs the motion compensation described below in ① and ② for the noise detected in Section 2.1.2 It does this by creating the motion compensation flags YMA[3:0] and CMA[4:0] from the motion flags (YMT, YMT3, YMT4, YMT5, and CMT) detected in Section 2.1.3, the motion compensation stop settings YMOFF[3:0] (SUB:51h-bit[3:0]) and CMOFF[4:0](SUB:52h-bit[4:0]), and the luminance linked chrominance motion compensation setting CMY (SUB:52h-bit[7]).

Table F2-1-4 (1) Motion Compensation Flags

Motion compensation flag	Composite signal	Remarks
YMA[0]	YMT&YMOFF[0]	Luminance adjacent pixel level luminance motion compensation
YMA[1]	YMT&YMOFF[1]	Luminance 3 continuous codes luminance motion compensation
YMA[2]	YMT&YMOFF[2]	Luminance 4 continuous codes luminance motion compensation
YMA[3]	YMT&YMOFF[3]	Luminance 5 continuous codes luminance motion compensation
CMA[0]	CMT&CMOFF[0]	Chrominance adjacent pixel level chrominance motion compensation
CMA[1]	YMT&CMOFF[1]&CMY	Luminance adjacent pixel level chrominance motion compensation
CMA[2]	YMT3&CMOFF[2]&CMY	Luminance 3 continuous codes chrominance motion compensation
CMA[3]	YMT4&CMOFF[3]&CMY	Luminance 4 continuous codes chrominance motion compensation
CMA[4]	YMT5&CMOFF[4]&CMY	Luminance 5 continuous codes chrominance motion compensation

① Luminance Signal Noise Motion Compensation

This feature performs motion compensation for the detected noise using the motion compensation flag YMA[3:0].

As the method of motion compensation , you can select the reduction mode (YNRM = 0) or the noise 0 mode with YNRM(SUB:4Ah-bit[0]).

In the reduction mode, you can choose the normal reduction mode (YABN = 0) or the absolute noise reduction mode (YABN = 1) in register YABN(SUB:4Ah-bit[2]).

Table F2-1-4 (2) Luminance Motion Compensation Modes

YNRM	YABN	Motion compensation mode	Remarks
X	X	None	Detected noise as is
0	0	Normal reduction	(Detected noise) x (Reduction coefficient)
0	1	Absolute noise reduction	(Detected noise) x (Reduction coefficient)
1	X	Noise 0	Noise 0 judgment (NROFF)

Table F2-1-4 (3) Noise Reduction Coefficients

YMA				Reduction coefficient	
[3]	[2]	[1]	[0]	YABN = 0	YABN = 1
0	0	0	0	1	1
0	0	0	1	1/2	3/4
0	0	1	0	1/2	3/4
0	0	1	1	1/4	5/8
0	1	1	0	1/4	5/8
0	1	1	1	1/8	9/16
1	1	1	0	1/8	9/16
1	1	1	1	1/16	17/32

② Chrominance Signal Noise Motion Compensation

This feature performs motion compensation for the detected noise using the motion compensation flag CMA[4:0]. As the method of motion compensation , the reduction mode (CNRM = 0) or the noise 0 mode (CNRM = 1) can be selected by CNRM (SUB:4Bh-bit[0]).

In the reduction mode, the normal reduction mode (CABN = 0) or the absolute noise reduction mode (CABN = 1) can be selected by CABN (SUB:4Bh-bit[2]).

Table F2-1-4 (4) Chrominance Motion Compensation Mode

CNRM	CABN	Motion compensation mode	Remarks
X	X	None	Detected noise as is
0	0	Normal reduction	(Detected noise) x (Reduction coefficient)
0	1	Absolute noise reduction	(Detected noise) x (Reduction coefficient)
1	X	Noise 0	Noise 0 judgment (NROFF)

Table F2-1-4 (5) Chrominance Normal Reduction Mode Noise Reduction Coefficients

CMA					Reduction coefficient	
[4]	[3]	[2]	[1]	[0]	CABN=0	CABN=1
0	0	0	0	0	1	1
0	0	0	0	1	1/2	3/4
0	0	0	1	0	1/2	3/4
0	0	0	1	1	1/4	5/8
0	0	1	0	0	1/2	3/4
0	0	1	0	1	1/4	5/8
0	0	1	1	0	1/4	5/8
0	0	1	1	1	1/8	9/16
0	1	1	0	0	1/4	5/8
0	1	1	0	1	1/8	9/16
0	1	1	1	0	1/8	9/16
0	1	1	1	1	1/16	17/32
1	1	1	0	0	1/8	9/16
1	1	1	0	1	1/16	17/32
1	1	1	1	0	1/16	17/32
1	1	1	1	1	0	1/2

2.1.5 Noise Reduction Stop Setting

Noise reduction can be forcibly stopped by setting NROFF (SUB:48h-bit[0]) on the I^2C-bus interface.
However, data can be written into the memory even while noise reduction is stopped.

Table F2-1-5 NROFF Setting

NROFF	Noise Reduction
0	Operated
1	Stopped

2.1.6 Noise Reduction Demo Mode Setting

By setting NRDEMO[2:0] (SUB:48h-bit[2:0]), a screen can be split as shown in Figure F2-1-6 and noise reduction function can be confirmed as demo mode or the I^2C-bus interface.
However, the demo mode does not work when noise reduction is stopped by setting NROFF = 1.

Table F2-1-6 NRDEMO Setting

NROFF	NRDEMO			Left side of screen	Right side of screen
	[2]	[1]	[0]		
0	0	0	0	NR setting value	NR setting value
1	X	X	X	Stop NR	Stop NR
0	X	X	1	Stop NR	NR setting value
0	X	1	0	NR Setting value	Adaptive NR ON
0	1	0	0	NR Setting value	Adaptive line correlation NR ON

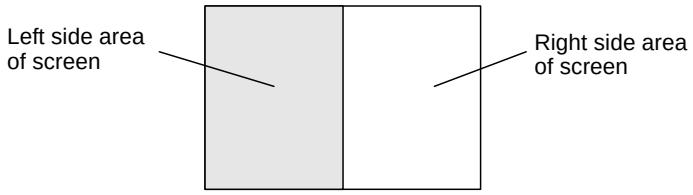


Figure F2-1-6 Noise Reduction Demo Screen

2.1.7 Noise Status Detection

In order to automatically optimize noise reduction setting, this IC has a function for detecting the overall video sample noise status during the motionless vertical blanking period.

- Detection of noise level (average and maximum values)

  Set NRDTON (SUB:49h-bit[1]) = 1 to detect the blanking period noise level for one line (NDTC = 0) of a vertical blanking period set by NRDTP[3:0](SUB:57h-bit[4:2]) and DTPSL (SUB:57h-bit[7]). Alternatively, you can set the same register to detect the blanking noise (average and maximum values) for one line (NDTC = 1) of the maximum noise level of multiple lines (a maximum of 16 lines not including valid lines) ending with line NRDTP[2:0]. The detection of blanking period noise (average and maximum values) and the noise on the line on which the average noise between fields for the valid data period is minimum can be performed frame by frame.

  The detection starting position is set in DTPSL. When DTPSL = 0, the starting position is immediately after the end of the valid lines; when DTPSL = 1, the starting position is one line after the end of the valid lines.

  In a blanking period, one line is divided into two sections, the noise levels of the two sections are detected, and the larger average noise value between the first 128 pixels and second 128 pixels is assumed as the average value and maximum value of the line.

  In a valid data period, one line is divided into four sections, the noise levels of the four 128-pixel periods are detected, and the lowest average noise value is assumed as the average value and maximum value of the line. During the valid data period, a luminance noise detection saturation level can be set through PYST[1:0](SUB:52h-bit[6:5]), thereby preventing deterioration of the noise detection level by luminance level saturation of CCD image input.

  When NRDTON = 0, the final status data for NRDTON = 1 is preserved. Initially, the average and maximum noise values are set at 0.

  The fields for which detection is to be performed are set in NRDTF (SUB:49h-bit[5]). When NRDTF = 0, field A vertical blanking period is set; when NRDTF = 1, field B vertical blanking period is set.

  By setting YNMAS (SUB:57-bit[0]) and CNMAS (SUB:57h-bit[1]), it is possible to select either an 8-frame average of the detected noise (YNMAS = 0, CNAMS = 0) or the level of detected noise in a single frame (YNMAS = 1, CNAMS = 1).

  For a noise detection area, a vertical blanking period, a valid data period, or a combination of both can be set using PODT (SUB:49h-bit[4]) and PNON (SUB:49h-bit[7]).

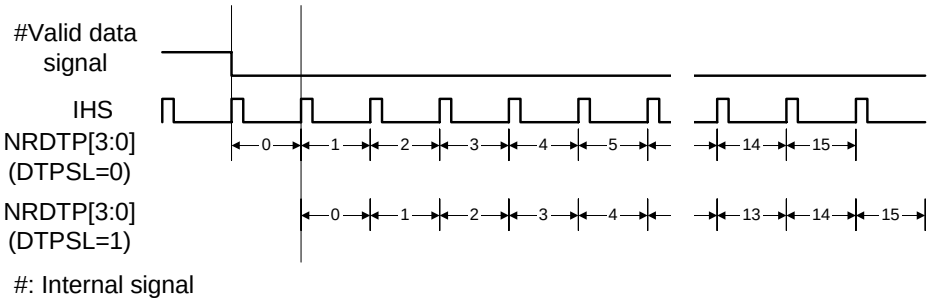


Figure F2-1-7 (1) Vertical Blanking Noise Status Detection timing (NDTC = 0)

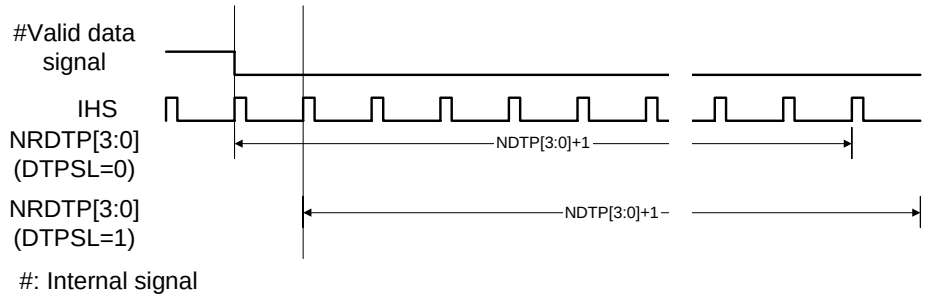


Figure F2-1-7 (2) Vertical Blanking Noise Status Detection timing (NDTC = 1)

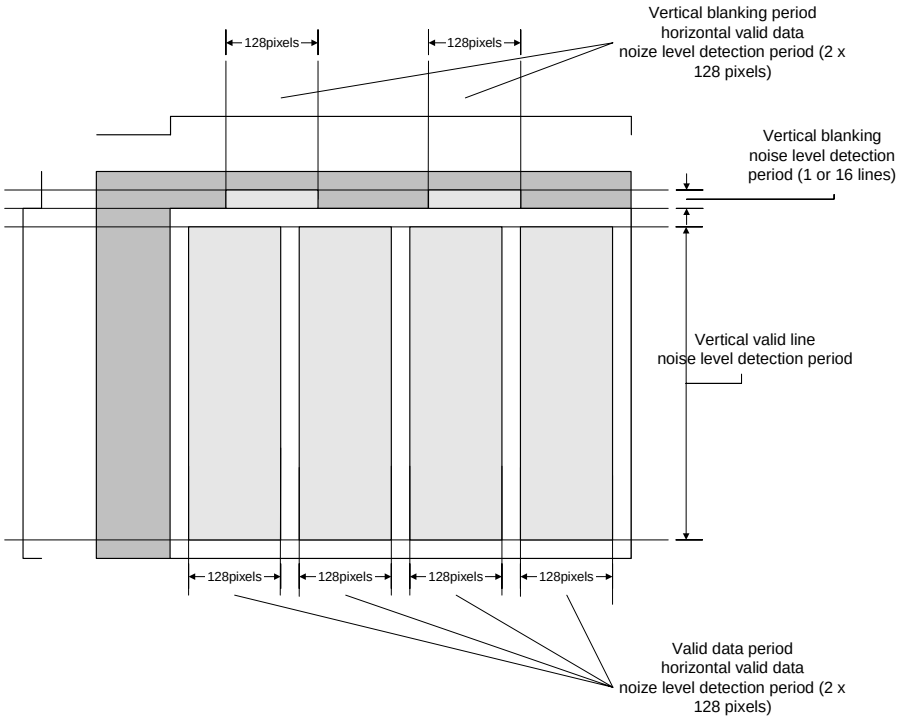


Figure F2-1-7(3) Noise Level Detection Area

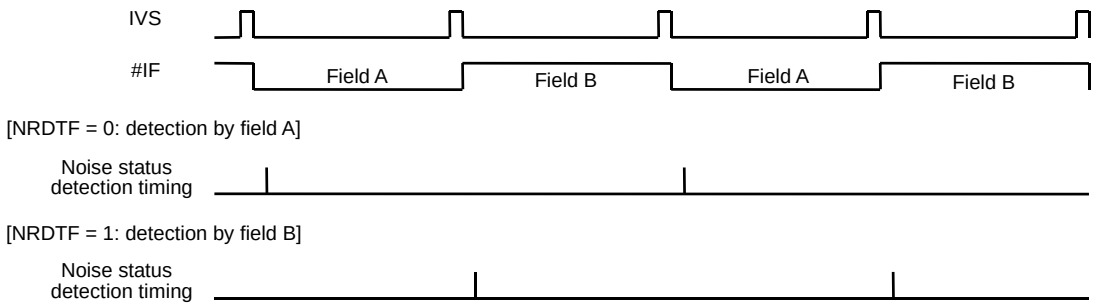


Figure F2-1-7 (4) Detection Field Based on NRDTF

Table F2-1-7 (1) Vertical Blanking Sample Noise Detection Settings

NRDTON	Noise detection
0	Stopped (previously detected data is maintained)
1	Operating

Table F2-1-7 (2) Noise Detection Field Settings

NRDTF	Noise detection field
0	Field A
1	Field B

Table F2-1-7 (3) Blanking Period Noise Detection Line Settings

NDTC	Noise detection line
0	1 line set at the NRDTP[3:0] position
1	Multiple lines (a maximum of 16 lines) from the line after the last valid line to NRDTP[3:0]

Table F2-1-7 (4) Noise Detection Value Select Settings

YNAMS CNAMS	Noise detection value
0	Average of 8 frames
1	Single frame

Table F2-1-7(5) Noise Detection Area Settings

PODT	PNON	Noise detection area
0	0	Vertical blanking only
0		Vertical blanking only + valid data period
1	X	Valid data period only

Table R2-1-7(6) Luminance Saturation Level Settings for Valid Data Area Noise Detection

PYST[1:0]	Luminance saturation level
0h	**No saturation level**
1h	E0h
2h	C0h
3h	80h

① Detection of Basic Noise Status Signals

Detection of the basic noise status signal (YBDTO, CBDTO) involves comparing the average noise value (YBAVRO[6:0], CBAVRO[6:0]) and the noise status comparison value (YAVR1[5:0] (SUB:53h-bit[5:0]), CAVR1[5:0] (SUB:54h-bit[5:0])) of the blanking period. The noise status is switched when the new status has continued for four frames or more.

The detection of the noise status signal has the hysteresis characteristic shown in Figure F2-1-6(4). You can select the characteristic with YAH1(SUB:53h-bit[7]) and CAH1 (SUB:54h-bit[7]).

Table F2-1-7 (5) Luminance Blanking Period Noise Status Detection

Before transition YBDTO	Condition	After transition YBDTO
0	YBAVRO[6:0] ≤ YAVR1[5:0]	0
0	YBAVRO[6:0] > YAVR1[5:0]	1
1	YBAVRO[6:0] ≤ YAVR1[5:0] x (hysteresis coefficient)	0
1	YBAVRO[6:0] > YAVR1[5:0] x (hysteresis coefficient)	1

Table F2-1-7 (6) Chrominance Blanking Period Noise Status Detection

Before transition CBDTO	Condition	After transition CBDTO
0	CBAVRO[6:0] ≤ CAVR1[5:0]	0
0	CBAVRO[6:0] > CAVR1[5:0]	1
1	CBAVRO[6:0] ≤ CAVR1[5:0] x (hysteresis coefficient)	0
1	CBAVRO[6:0] > CAVR1[5:0] x (hysteresis coefficient)	1

Table F2-1-7 (7) Noise Status Reduction Direction Detection Hysteresis Settings

YAH1 CAH1	Noise reduction direction switching coefficient
0	3/4
1	7/8

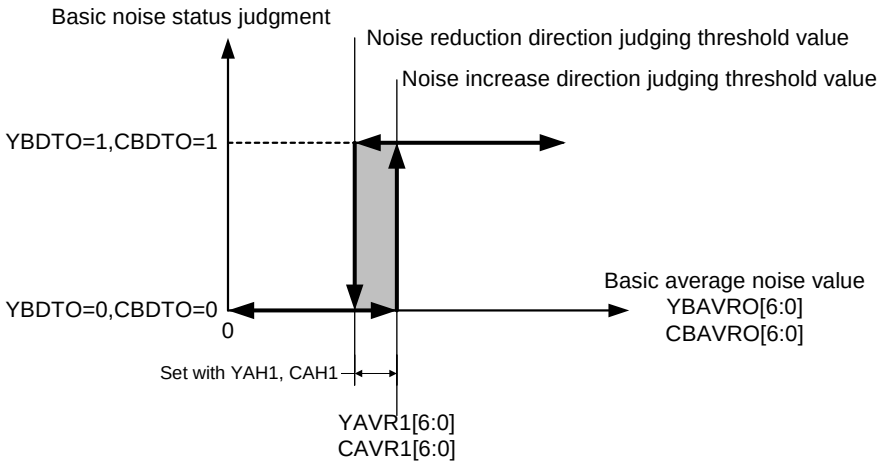


Figure F2-1-7 (4) Basic Noise Status Judgment Transition Diagram

② Judgment Noise Level Selection

Select the judgment noise level based on the procedure for basic noise level detection described above.
When PODT = 0 and PNON = 0, the blanking period noise level is referenced for the judgment noise level.
When PODT = 0 and PNON = 1, the overall noise status is referenced on the noise level of the valid data period when the noise status of the blanking period is judged to be low noise (YBDTO1 = 0, CBDTO1 = 0).
When the noise status of the blanking period is judged to be high (YBDTO1 = 1, CBDTO1 = 1), the average noise level of the blanking period and the average noise level of the valid period are compared and the smaller value is referenced for the overall noise status.
Switching between the blanking period and the valid data period occurs when the noise average value condition has continued for four frames or more.
When PODT = 1, the noise level of the valid data period is referenced for the judgment noise level.

Table F2-1-7 (8) Luminance Judgment Noise Level Selection

PODT	PNON	YBDTO1	Luminance noise average value noise level condition	Luminance judgment noise level
0	0	X	—	Blanking period noise level
0	1	0	—	Valid data period noise level
0	1	1	Blanking period ≤ Valid data period	Blanking period noise level
0	1	1	Blanking period > Valid data period	Valid data period noise level
1	X	X	—	Valid data period noise level

Table F2-1-7 (9) Chrominance Judgment Noise Level Selection

PODT	PNON	CBDTO1	Chrominance noise average value noise level condition	Chrominance judgment noise level
0	0	X	—	Blanking period noise level
0	1	0	—	Valid data period noise level
0	1	1	Blanking period ≤ Valid data period	Blanking period noise level
0	1	1	Blanking period > Valid data period	Valid data period noise level
1	X	X	—	Valid data period noise level

③ Judging noise status detection

Judgment of the noise status is achieved by comparing the average noise value (YAVRO[6:0], CAVRO[6:0]), the noise status comparison value (I^2C-bus setting registers YAVR1[5:0] (SUB:53h-bit[5:0]), CAVR1[5:0] (SUB:54h-bit[5:0]), YAVR2 [6:0] (SUB:55h-bit[6:0]), CAVR2[6:0] (SUB:56h-bit[6:0])). Based on this judgment, the noise status signals (YDTO1, CDTO1, YDTO2, CDTO2) are generated.

The detection of noise status signal has a hysteresis characteristic as shown in Figure F2-1-6 (5). Select the characteristic with YAH1 (SUB:53h-bit[7]), CAH1 (SUB:54h-bit[7]), YAH2 (SUB:55h-bit[7]), and CAH2 (SUB:56h-bit[7]).

It is also possible to mask the luminance detection in order to enable chrominance detection by setting ACY (SUB:49h-bit[2]. The chrominance detection is enabled when YDTO1 = 1 for CDTO1 and YDTO2 = 1 for CDTO2.

Table F2-1-7 (10) Luminance Judgment Noise Status Detection 1

Before transition YDTO1	Condition	After transition YDTO1
0	YAVRO[6:0] ≤ YAVR1[5:0]	0
0	YAVRO[6:0] > YAVR1[5:0]	1
1	YAVRO[6:0] ≤ YAVR1[5:0] x (hysteresis coefficient)	0
1	YAVRO[6:0] > YAVR1[5:0] x (hysteresis coefficient)	1

Table F2-1-7 (11) Chrominance Judgment Noise Status Detection 1

Before transition CDTO1	Condition	After transition CDTO1
0	CAVRO[6:0] ≤ CAVR1[5:0]	0
0	CAVRO[6:0] > CAVR1[5:0]	1
1	CAVRO[6:0] ≤ CAVR1[5:0] x (hysteresis coefficient)	0
1	CAVRO[6:0] > CAVR1[5:0] x (hysteresis coefficient)	1

Table F2-1-7 (12) Luminance Judgment Noise Level Detection 2

Before transition YDTO2	Condition	After transition YDTO2
0	YAVRO[6:0] ≤ YAVR2[6:0]	0
0	YAVRO[6:0] > YAVR2[6:0]	1
1	YAVRO[6:0] ≤ YAVR2[6:0] x (hysteresis coefficient)	0
1	YAVRO[6:0] > YAVR2[6:0] x (hysteresis coefficient)	1

Table F12-1-7 (13) Chrominance Judgment Noise Status Detection 2

Before transition CDTO2	Condition	After transition CDTO2
0	CAVRO[6:0] ≤ CAVR2[6:0]	0
0	CAVRO[6:0] > CAVR2[6:0]	1
1	CAVRO[6:0] ≤ CAVR2[6:0] x (hysteresis coefficient)	0
1	CAVRO[6:0] > CAVR2[6:0] x (hysteresis coefficient)	1

Table F2-1-7 (14) Chrominance Noise Status Detection Mask Setting

ACY	Chrominance noise status detection
0	Chrominance independent detection
1	Luminance detection mask detection

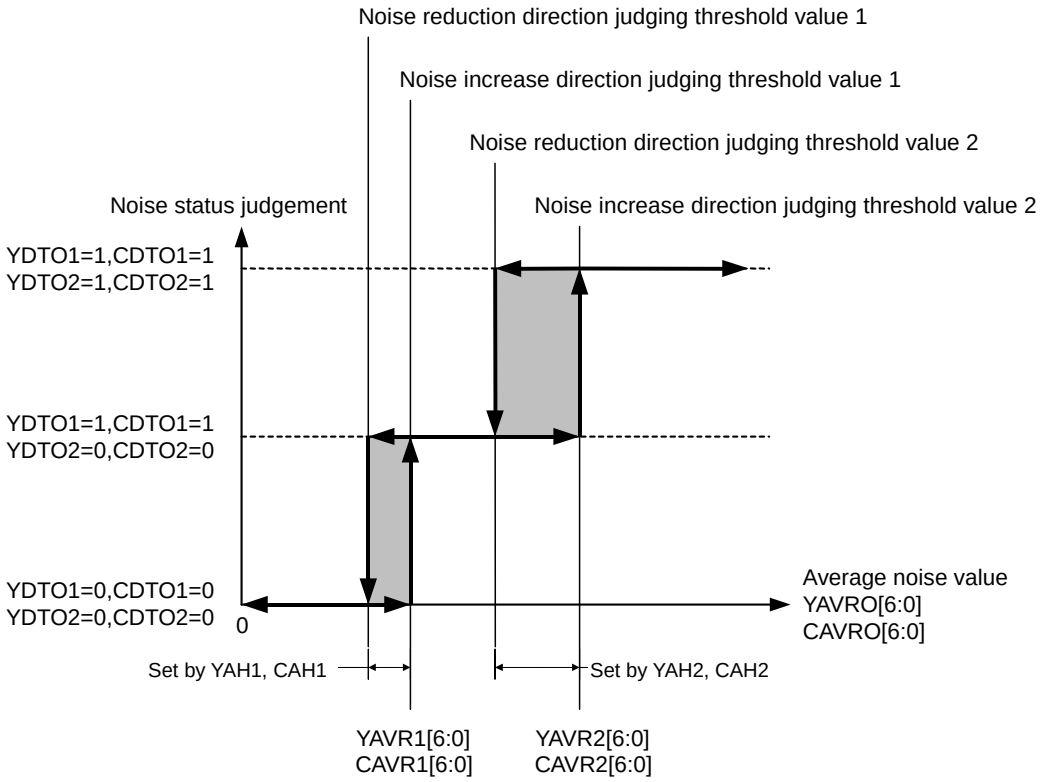


Figure F2-1-7 (5) Noise Status Judgment Transition Diagram

- I^2C-bus interface read of detected noise
  The detected judgment, the average and maximum detected noise values and the noise status signal in the blanking period can be read using the I^2C-bus interface.

Table F2-1-7 (15) I^2C-bus Interface Read of Detected Noise Data

Read data	Sub-address data bit	Data content
YAVRO[6:0]	SUB:58h-bit[6:0]	Luminance judgment average noise value
YDTO1	SUB:58h-bit[7]	Luminance judgment noise status 1 (noise low/medium judgment)
CAVRO[6:0]	SUB:59h-bit[6:0]	Chrominance judgment average noise value
CDTO1	SUB:59h-bit[7]	Chrominance judgment status 1 (noise low/medium judgment)
YMAXO[4:0]	SUB:5Ah-bit[4:0]	Luminance judgment maximum noise value
YDTO2	SUB:5Ah-bit[7]	Luminance judgment noise status 2 (noise medium/high judgment)
CMAXO[4:0]	SUB:5Bh-bit[4:0]	Chrominance judgment maximum noise value
CDTO2	SUB:5Bh-bit[7]	Chrominance judgment noise status 2 (noise medium/high judgment)
YBAVRO[6:0]	SUB:5Ch-bit[6:0]	Luminance blanking average noise value
YBDTO	SUB:5Ch-bit[7]	Luminance blanking noise status (basic noise judgment)
CBAVRO[6:0]	SUB:5Dh-bit[6:0]	Luminance blanking average noise value
CBDTO	SUB:5Dh-bit[7]	Luminance blanking noise status (basic noise judgment)

2.1.8 Noise Reduction Auto Mode

The noise reduction setting value of this IC is normally register fixed mode, but considering that the noise level may considerably exceed the set value or the noise level is almost zero, this IC is equipped with an auto mode to automatically perform setting of noise reduction by setting NRAUTO (SUB:49h-bit[0]) and using the maximum noise values (YMAXO[5:0], CMAXO[5:0]) and noise status signals (YDTO1, YDTO2, CDTO1, CDTO2) detected in section 1.3.7.

When NRAUTO = 1, the auto mode of 3-status transition shown in Tables F1-3-8 (1), (2) operates. In auto mode, any of status transition modes (auto mode 1, auto mode 2) can be selected by AMM (SUB:49h-bit[3]).

The noise reduction setting value in auto mode can be precisely set by AYABN (SUB:4Ah-bit[3]), ACABN (SUB:4Bh-bit[3]), AYNS[1:0] (SUB:4Ch-bit[7:6]), ACNS[1:0] (SUB:4Dh-bit[7:6]), AYLM [1:0] (SUB:4Eh-bit[7:6]), ACLM[1:0] (SUB:4Fh-bit[7:6]), AYMS [1:0] (SUB:50h-bit[7:6]), and AYMOFF[3:1] (SUB:51h-bit[7:5]).

Table F2-1-8 (1) Auto Mode (AMM = 0)

NRAUTO	YBDTO CBDTO	YDTO1 CDTO1	YDTO2 CDTO2	Noise reduction mode (Noise status)	Remarks
0	X	X	X	Register fixed value mode	
1	0	0	X	Auto mode (NROFF status)	Same as NROFF = 1
1	0	1	X	Auto mode (Noise low follow-up status) With upper limit Maximum motion compensation	AYNS [1:0], YCNA [1:0], AYLM [1:0], YCLM [1:0], and AYMS [1:0] are valid. YNRM, CNRM, YABN and CABN settings are ignored; operation is equivalent to YNRM = 1, CNRM = 1, YABN = 0, CABN = 0, and YMDM = 1.
1	1	X	0	Auto mode (Fixed register status)	All registers other than YMS [4:0] are the same as for the register fixed value mode. AYMS [1:0] is valid. Operation is equivalent to YMDM = 1.
1	1	X	1	Auto mode (Noise high follow-up status) With lower limit	AYABN, ACABN, AYNS[1:0], YCNS[1:0], AYLM[1:0], YCLM[1:0], AYMS[1:0], and AYMOFF[3:1] are valid.

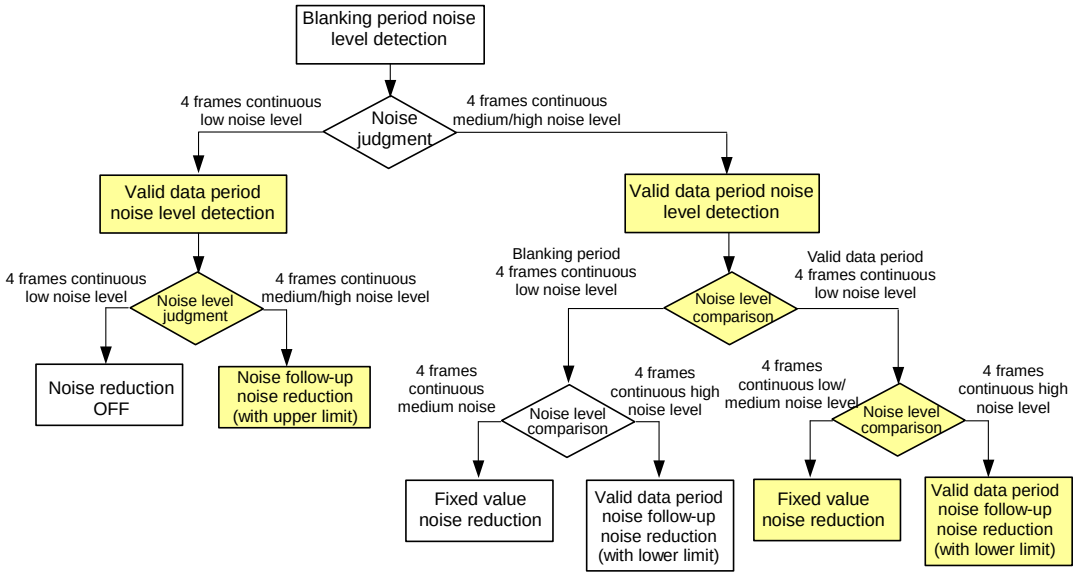


Figure F2-1-8 (1) Auto Mode Judgment Flow (AMM = 0)

Table F2-1-8 (2) Auto Mode 2 (AMM = 1)

NRAUTO	YBDTO CBDTO	YDTO1 CDTO1	YDTO2 CDTO2	Noise reduction mode	Remarks
0	X	X	X	Register fixed value mode	
1	0	0	X	Auto mode (Noise low follow-up status) With upper limit motion compensation maximum	AYNS [1:0], YCNA [1:0], AYLM [1:0], YCLM [1:0], and AYMS [1:0] are valid. YNRM, CNRM, YABN and CABN settings are ignored; operation is equivalent to YNRM = 1, CNRM = 1, YABN = 0, CABN = 0, and YMDM = 1.
1	0	1	X	Auto mode (Noise low follow-up status) With upper limit	AYNS[1:0], YCNA[1:0], AYLM[1:0], YCLM[1:0], and AYMS[1:0] are valid. Operation is equivalent to YMDM = 1.
1	1	X	0	Auto mode (Fixed register status)	AYMS[1:0] and AYOFF[3:1] are valid same as register fixed value mode other than YMS[4:0] and YMOFF[3:1]. Operation is equivalent to YMDM = 1.
1	1	X	1	Auto mode (Noise high follow-up status) With lower limit	AYABN, ACABN, AYNS[1:0], YCNA[1:0], AYLM[1:0], YCLM[1:0], and AYMOFF[3:1] are valid.

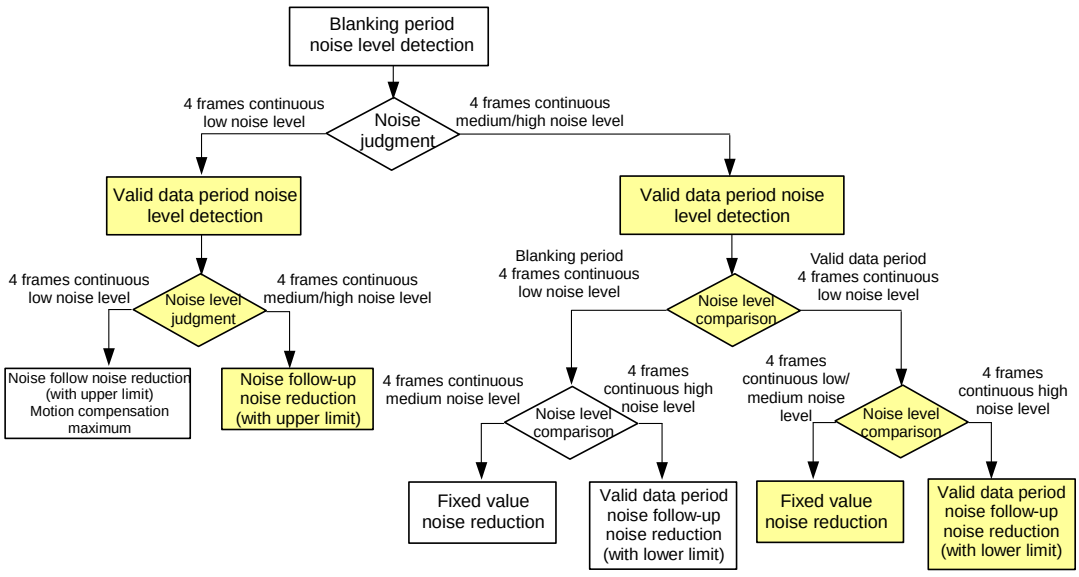


Figure F2-1-8 (2) Auto Mode Judgment Flow (AMM = 1)

(1) Auto Mode Luminance Noise Reduction Mode Settings (AYABN)
Sets whether or not to use the luminance absolute noise reduction mode in the auto mode luminance noise follow-up status (YDTO2 = 1).

Table F2-1-8 (3) Auto Mode Luminance Noise Reduction Mode Settings (YABN = 0)

YDTO2	AYABN	Luminance noise reduction mode
0	X	YABN dependent
1	0	YABN dependent
1	1	Absolute noise reduction mode (equivalent to YABN = 1 operation)

(2) Auto Mode Chrominance Noise Reduction Mode Settings (ACABN)
Sets whether or not to use the chrominance absolute noise reduction mode in the auto mode chrominance noise follow-up status (CDTO2 = 1).

Table F2-1-8 (4) Auto Mode Chrominance Noise Reduction Mode Settings (CABN = 0)

CDTO2	ACABN	Chrominance Noise Reduction Mode
0	X	CABN dependent
1	0	CABN dependent
1	1	Absolute noise reduction mode (equivalent to CABN = 1 operation)

(3) Auto Mode Luminance Noise Convergence Level Settings (AYNS[1:0])
Sets whether or not to use the luminance noise convergence level automatic setting in the auto mode luminance noise follow-up status (YDTO2 = 1).
When AMM = 0, noise reduction stops with YDTO1 = 0, so the luminance noise convergence level is ignored.

Table F2-1-8 (5) Auto Mode Luminance Noise Convergence Level Settings

YBDTO	YDTO1	YDTO2	AYNS		Luminance noise convergence level
			[1]	[0]	
0	X	X	0	X	YNS[5:0]
			1	0	YNS[5:0] + YMAXO[4:0](max:3Fh)
			1	1	Smaller of YMAXO[4:0] x 3(max:3Fh) and YNS[5:0]
1	X	0	X	X	YNS[5:0]
1	X	1	0	X	YNS[5:0]
			1	0	YNS[5:0] + YMAXO[4:0](max:3Fh)
			1	1	Larger of YMAXO[4:0] x 3(max:3Fh) and YNS[5:0]

(4) Auto Mode Chrominance Noise Convergence Level Settings (ACNS[1:0])
Sets whether or not to use the chrominance noise convergence level automatic setting in the auto mode noise follow-up status (CDTO2 = 1).
When AMM = 0, noise reduction stops with CDTO1 = 0, so the chrominance noise convergence level is ignored.

Table F2-1-8 (6) Auto Mode Chrominance Noise Convergence Level Settings

CBDTO	CDTO1	CDTO2	ACNS		Chrominance Noise Convergence Level
			[1]	[0]	
0	X	0	0	X	CNS[5:0]
			1	0	CNS[5:0] + CMAXO[4:0](max:3Fh)
			1	1	Smaller of CMAXO[4:0] x 3(max:3Fh) and CNS[5:0]
1	X	0	X	X	CNS[5:0]
1	X	1	0	X	CNS[5:0]
			1	0	CNS[5:0] + CMAXO[4:0](max:3Fh)
			1	1	Larger of CMAXO[4:0] x 3(max:3Fh) and CNS[5:0]

(5) Auto Mode Luminance Noise Upper Limit Level Settings (AYLM[1:0])
Sets whether or not to use the luminance noise upper limit level automatic setting in the auto mode luminance noise follow-up status (YDTO2 = 1).
When AMM = 0, noise reduction stops with YDTO1 = 0, so the luminance noise upper limit level is ignored.

Table F2-1-8 (7) Auto Mode Luminance Noise Upper Limit Level Settings

YBDTO	YDTO1	YDTO2	AYLM		Luminance noise upper limit level
			[1]	[0]	
0	X	0	0	X	YLM[4:0]
			1	0	Smaller of YMAXO[4:0] x 0.75(max:1Fh) and YLM[4:0]
			1	1	Smaller of YMAXO[4:0](mx:1Fh) and YLM[4:0]
1	X	0	X	X	YLM[4:0]
1	X	1	0	X	YLM[4:0]
			1	0	Larger of YMAXO[4:0] x 0.75(max:1Fh) and YLM[4:0]
			1	1	Larger of YMAXO[4:0](max:1Fh) and YLM[4:0]

(6) Auto Mode Chrominance Noise Upper Limit Level Settings (ACLM[1:0])
Sets whether or not to use the chrominance noise upper limit level automatic setting in the auto mode chrominance noise follow-up status (CDTO2 = 1).
When AMM = 0, noise reduction stops with CDTO1 = 0, so the chrominance noise upper limit level is ignored.

Table F2-1-8 (8) Auto Mode Chrominance Noise Upper Limit Level Settings

CBDTO	CDTO1	CDTO2	ACLM		Chrominance noise upper limit level
			[1]	[0]	
0	X	0	0	X	CLM[4:0]
			1	0	Smaller of CMAXO[4:0] x 0.75 (max:1Fh) and CLM[4:0]
			1	1	Smaller of CMAXO[4:0](max:1Fh) and CLM[4:0]
1	X	0	X	X	CLM[4:0]
1	X	1	0	X	CLM[4:0]
			1	0	Larger of CMAXO[4:0] x 0.75(max:1Fh) and CLM[4:0]
			1	1	Larger of CMAXO[4:0](max:1Fh) and CLM[4:0]

(7) Auto Mode Luminance Continuous Code Motion Detection Level Settings (AYMS[1:0])
Sets whether or not to use the luminance continuous code motion detection level automatic setting except in the auto mode luminance noise follow-up status (YDTO2 = 0).
When AMM = 0, noise reduction stops with YDTO1 = 0, so the luminance continuous code motion detection level is ignored.

Table F2-1-8 (9) Luminance Continuous Code Motion Detection Level Settings

YDTO2	AYMS		Luminance continuous code motion detection level
	[1]	[0]	
0	0	X	YMS[4:0]
0	1	0	Smaller of YMAXO[4:0](max:1Fh) and YMS[3:0]
0	1	1	Smaller of YMAXO[4:0]/2(max:1Fh) and YMS[3:0]
1	X	X	YMS[4:0]

(8) Auto Mode Luminance Motion Compensation Stop Settings (AYMOFF[3:1])
Sets whether or not to use the luminance motion compensation stop automatic setting in the auto mode 1 luminance noise follow-up status (YDTO2 = 1) and the auto mode 2 (AMM = 1) luminance fixed register 2 status (YDTO = 1).

Table F2-1-8 (10) Auto Mode 1 Luminance Motion Compensation Stop Settings (AMM = 0)

YDTO2	AYMOFF[a]	Luminance motion compensation
0	X	Motion compensation YMOFF[a] dependent
1	0	Motion compensation YMOFF[a] dependent
1	1	Motion compensation stopped (equivalent to YMOFF[a] = 1)

Table F2-1-8 (11) Auto Mode 2 Luminance Motion Compensation Stop Settings (AMM = 1)

YDTO1	AYMOFF[a]	Luminance motion compensation
0	X	Motion compensation YMOFF[a] dependent
1	0	Motion compensation YMOFF[a] dependent
1	1	Motion compensation stopped (equivalent to YMOFF[a] = 1)

(9) Auto Mode Luminance Adaptive Margin Settings
In the auto mode, the luminance adaptive margin is set independently of YFAM.

Table F2-1-8 (12) Luminance Adaptive Margin Settings

YDTO2	Luminance adaptive margin setting
0	YFAM dependent
1	Equivalent to YFAM = 1 operation

(10) Auto Mode Chrominance Adaptive Margin Settings
In the auto mode, the chrominance adaptive margin is set independently of CFAM.

Table F2-1-8 (13) Chrominance Adaptive Margin Settings

CDTO2	Chrominance adaptive margin setting
0	CFAM dependent
1	Equivalent to CFAM = 1 operation

(11) Auto Mode Line Correlation NR OFF Settings
When A2OFF = 1 is set, the noise status of the blanking period is the noise follow-up level and where YDTO1 or CDTO1 is 1, the line correlation NR is set to be OFF.

Table F2-1-8 (14) Line Correlation NR OFF Settings

Blanking period noise	YDTO1 or CDTO1	Line correlation NR setting
0	X	NR2OFF dependent
1	0	NR2OFF dependent
1	1	Line correlation NR OFF

[Notes on Using Noise State Detection and Auto Mode Noise Reduction]

Using the noise state detection and auto mode noise reduction functions of this IC can degrade picture quality because of the possibility of wrong detection of noise state due to persistence of vision . Therefore, check the following points beforehand and then use these functions:

1. Noise state detection is performed once in vertical blanking in one frame. Since it is not possible to correctly determine the noise detection position by factors such as TV system, area, input source (VTR, DVD), pre-stage tuner and video decoder, accurate detection of the noise state is disabled. Therefore, confirm the operation prior to using these functions.

2. Where the input source has been recorded by a home VTR, the data of the blanking period in particular is uncertain. Do not use noise reduction in the noise follow-up status (YDTO2 = 1, CDTO2 = 1) unless you have determined that there is no problem.
   (There are some cases where the VTR is input as RF input, so take appropriate measures such as preventing the noise follow-up status from operating on the RF channel for external input.)

3. In composite video input signal, if only that position is selectable in which data can be in the position of noise state detection, enable the luminance link mode for chrominance by setting ACY=1 considering that luminance data can enter the chrominance data or do not use the chrominance auto mode.

4. There are cases of no noise in the vertical blanking period, or a part of the vertical blanking period, by a pre-stage tuner or video decoder. Perform NRDTP[3:0] setting and make sure to select a position at which noise level is the same as the valid data.
   If noise is not detectable within the settable vertical blanking period at NRDTP[3:0] setting, then it is not possible to use the noise state detection and the auto mode noise reduction.

5. Regarding the video signals added later of devices such as DVD, cameras, and digital recording, the noise level of the added Sync. signals is detected as the noise state because the noise state detection is performed in the vertical blanking period.

6. Noise state detection is not performed at all times if the hysteresis characteristic of noise state detection is not valid (frequent occurrence of state switching). The noise detection is performed by NRDTON = 1 (8 frames or more) at the time of RF channels or input source switching only. Thereafter, settings to hold the noise state etc., at NRDTON = 0 up to the next switching become necessary.

2.2 Cross-Color Cancellation

The cross-color cancellation function of this IC removes the commingling of chrominance (cross color) of the fsc component in luminance in 2DYC separation method, by using an inter-frame comb filter through the video signal interleaving relationship. This IC has also the movement compensation function that checks luminance movements between frames and sets the cancellation function to OFF when detecting a movement.

[Notes on using the cross-color cancellation function]

- Supports cross-color due to NTSC and PAL and cancellation is not effective in SECAM .
- Cancellation is not effective for progressive input either.
- While the cross-color cancellation function is active, chrominance recursive type noise reduction does not function.
- When using the cross-color cancellation function, set MEM411 to “1” and the internal memory to the 4:1:1 use mode since two-frame chrominance data needs to be used.

2.2.1 Cross-Color Canceling in the NTSC System

In the NTSC system, when CCON (SUB:5Eh-bit[0]) is set to 1 in the I^2C-bus interface, the 3D comb filter between the data one frame prior to the chrominance and the input data operates, realizing the cross-color cancellation in the NTSC system, as shown in Figure F2-2-1.
By setting CCMON (SUB:5Eh-bit[0]) to 1, the cross-color cancellation function can perform movement compensation that is set to ON/OFF in pixel units according to the luminance movement. It allows detailed setting by selecting the movement detection coefficient (CCMDT: SUB:5Eh-bit[3]), luminance movement detection level (CCYMS[2:0]-SUB:5Eh-bit[6:4]), and cross-color level feedback (CCMM-SUB:5Eh-bit[7]).
Only the NTSC system supports movement compensation by detection of 0 degree (360 degree) phase by the data two frames prior to the chrominance, enabling adjustments of the chrominance 0 degree phase detection level.
When using the movement compensation function, be sure to set MEM411 (SUB:5Eh-bit[1]) to 1 and the memory use mode to 4:1:1.

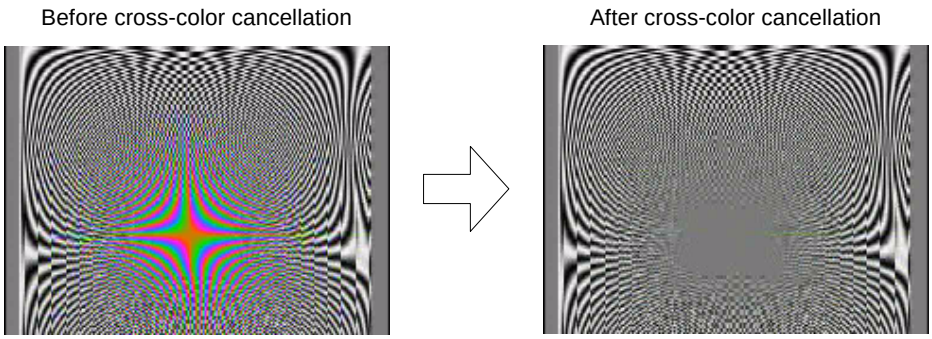


Figure F2-2-1 Cross-Color Cancellation in the NTSC System

2.2.2 Cross-Color Canceling in the PAL System

In the PAL system, when CCON (SUB:5Eh-bit[0]) is set to 1 in the I2C-bus interface, the 3D comb filter between the data two frames prior to the chrominance and the input data operates, realizing the cross-color cancellation in the PAL system, as shown in Figure F2-2-2 (CCON=1).
By setting CCMON (SUB:5Eh-bit[0]) to 1, the cross-color cancellation function can perform movement compensation that is set to ON/OFF in pixel units according to the luminance movement. It allows detailed settings by selecting the movement detection coefficient (CCMDT: SUB:5Eh-bit[3]), luminance movement detection level (CCYMS[2:0]-SUB:5Eh-bit[6:4]), and cross-color level feedback (CCMM-SUB:5Eh-bit[7]).
When using the cross-color cancellation function in the PAL system, be sure to set MEM411(SUB:5Eh-bit[1]) to 1 and the memory use mode to 4:1:1.

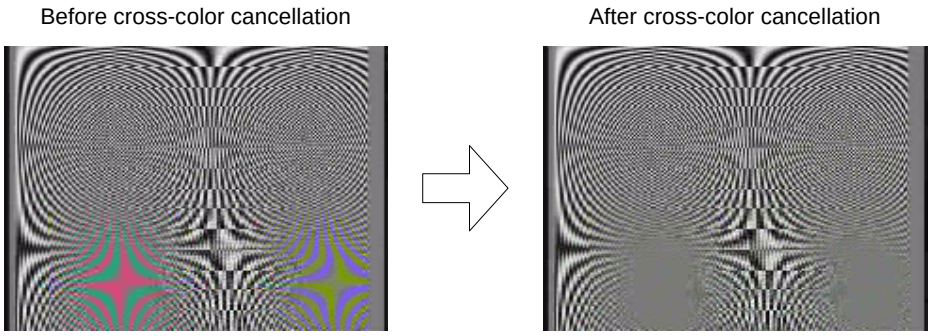


Figure F2-2-2 Cross-Color Cancellation in the PAL System

2.2.3 Cross-Color Cancellation Auto-OFF Setting

By setting ACC[1:0](SUB:5Fh-bit[5:4]) in the I^2C-bus interface, the cross-color cancellation can be stopped automatically by luminance noise level judgment.

Table F2-2-3 Cross-Color Cancellation Auto-OFF Setting

ACC		Cross-color cancellation
[1]	[0]	
0	X	Set by CCON
1	0	Goes OFF if YDT1 = 1 when CCON = 1
1	1	Goes OFF if YDT2 = 1 when CCON = 1

2.2.4 Cross-Color Cancellation Demonstration Mode

By setting CCT (SUB:5Fh-bit[6]) in the I^2C-bus interface, only chrominance signals can be displayed by fixing the luminance signal level to 80h.
By setting DMCC (SUB:5Fh-bit[7]) in the I^2C-bus interface, the cross-color cancellation function can be checked as a demonstration mode by splitting the screen as shown in Figure F2-2-4.

Table F2-2-4(1) Cross-Color Cancellation Demonstration Setting 1

CCT	Luminance signal
0	Input luminance signal
1	80h fixed

Table F2-2-4(2) Cross-Color Cancellation Demonstration Setting 2

DMCC	Left side on the screen	Right side on the screen
0	CC setting value	CC setting value
1	CCOFF	CC setting value

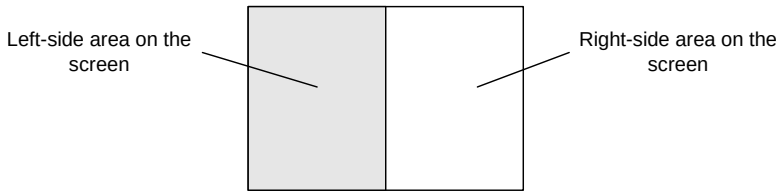


Figure F2-2-4 Cross-Color Cancellation Demonstration Screen

2.3 Edge-Adaptive 2D Noise Reduction

This IC has an edge-adaptive 2D noise reduction function that reduces residual noise after input type SNR processing and block noise and mosquito noise that occur due to compression such as MPEG.

2.3.1 Luminance Edge-Adaptive 2D Noise Reduction

By setting YLPFON (SUB:64h-bit[0]) = 1, 2D noise reduction of luminance data operates.
The edge-adaptive 2D noise reduction uses the surrounding 6 pixels (YHLPFM = 0) centering on the target pixel that is selected by YHLPFM (SUB:64h-bit[2]) or surrounding 10 pixels (YHLPFM = 1) centering on the target pixel (Figure 2-3-1) to form a filter with two-stage configuration (that is, vertical direction filter and horizontal direction filter), thereby achieving noise reduction.
The filter coefficient can be selected through YLPFM (SUB:64h-bit[1]).

[Vertical direction filter value processing]
YLPFM=0:f(z) = $(7/8)z^{0}+(1/8)z^{+1}$
YLPFM=1:f(z) = $(3/4)z^{0}+(1/4)z^{+1}$

[Horizontal direction filter value processing (YHLPFM=0)]
YLPFM=0: f(z) = $(1/8)z^{-1}+ (3/4)z^{0}+(1/8)z^{+1}$
YLPFM=1: f(z) = $(1/4)z^{-1}+ (1/2)z^{0}+(1/4)z^{+1}$

[Horizontal direction filter value processing (YHLPFM=1)]
YLPFM=0: f(z) = $(1/16)z^{-2}+(1/16)z^{-1}+(3/4)z^{0}+(1/16)z^{+1}+(1/16)z^{+2}$
YLPFM=1: f(z) = $(1/8)z^{-2}+(1/8)z^{-1}+(1/2)z^{0}+(1/8)z^{+1}+(1/8)z^{+2}$

As a countermeasure for band deterioration of edge sections, the difference between the target pixel (z^{0}) and surrounding pixels (z^{-2}, z^{-1}, z^{+1}, z^{+2}) is compared with YED[4:0] (SUB:65h-bit[4:0]). When the difference exceeds YED[4:0], the section is determined as an edge section and adaptive processing is performed using the edge adaptation method that replaces the surrounding pixel section in filter processing with the target pixel and removes the data from the filter data.

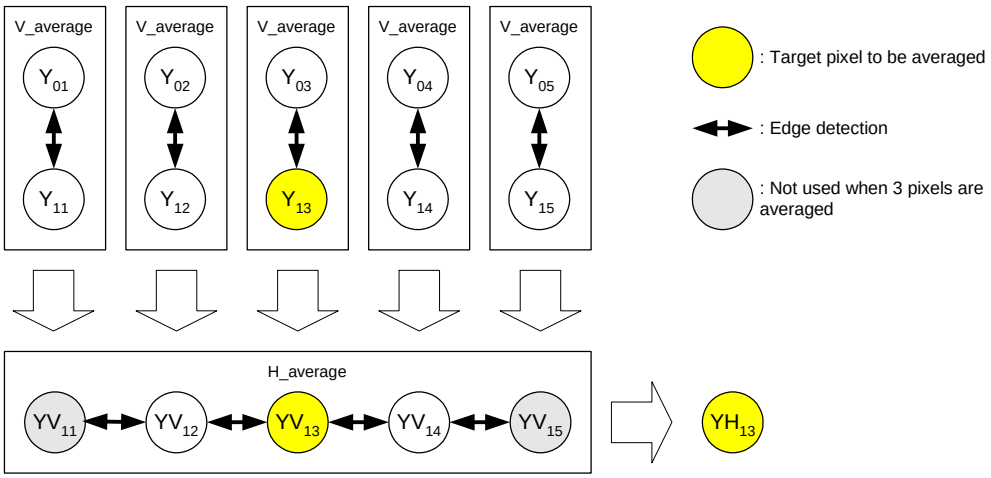


Figure F2-3-1 Luminance Edge-Adaptive 2D Noise Reduction

2.3.2 Chrominance Edge-Adaptive 2D Noise Reduction

By setting CLPFON(SUB:64h-bit[3]) = 1, edge-adaptive 2D noise reduction of chrominance data can be operated.
Chrominance edge-adaptive 2D noise reduction uses the surrounding 3 pixels skipping in the horizontal direction (Figure 2-3-2) and centering on the target pixel and forms only a horizontal direction filter, thereby achieving noise reduction.
The filter coefficient can be selected through CLPFM (SUB:65h-bit[4]).
This IC allows the setting of a compensation level of the edge section through the CED[4:0] (SUB:66h-bit[4:0]) level to prevent band deterioration of the edge section by LPF.
However, if edge compensation is enhanced, edge-adaptive 2D noise reduction deteriorates.

[Horizontal direction filter processing]
CLPFM=0: $f(z) = (1/8)z^{-2}+(3/4)z^{0}+(1/8)z^{+2}$
CLPFM=1: $f(z) = (1/4)z^{-2}+(1/2)z^{0}+(1/4)z^{+2}$

As a countermeasure for band deterioration of edge sections, the difference between the target pixel (z^0) and surrounding pixels (z^{-2}, z^{+2}) is compared with CED[4:0] (SUB:66h-bit[4:0]). When the difference exceeds CED[4:0], the section is determined as an edge section and adaptive processing is performed using the edge adaptation method that replaces the surrounding pixel section in filter processing with the target pixel and removes the data from the filter data.

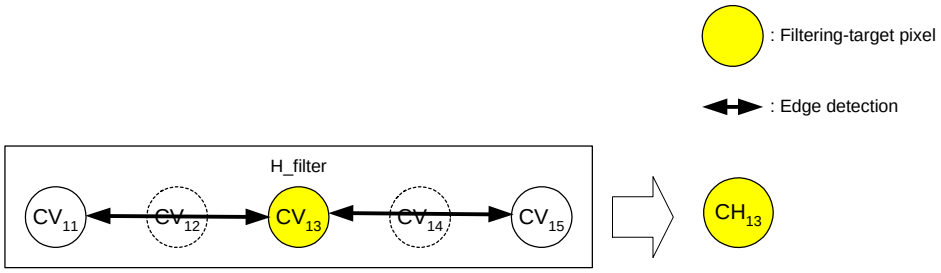


Figure F2-3-2 Chrominance Edge-Adaptive 2D Noise Reduction

2.3.3 Automatic Setting of Edge-Adaptive 2D Noise Reduction

By setting AYLPF[2:1](SUB:65h-bit[7:6]) and ACLPF[2:1](SUB:66h-bit[7:6]) in the I^2C-bus interface, the edge-adaptive 2D noise reduction ON/OFF can be set using the noise checking flag (YDTO1, YDTO2, CDTO1, CDTO2).
When using the automatic ON/OFF function, set YLPFON = 0 and CLPFON = 0.
By setting AYED (SUB:65h-bit[5]) and ACED (SUB:66h-bit[5]), it is possible to allow the edge adaptive level to follow the noise level.

Table F2-3-3(1) Luminance Edge-Adaptive 2D Noise Reduction Auto ON/OFF Setting

AYLPF		YDTO1	YDTO2	Luminance edge-adaptive 2D NR
[2]	[1]			
0	0	X	X	OFF
0	1	0	0	OFF
		1	0	ON
		1	1	ON
1	0	0	0	OFF
		1	0	OFF
		1	1	ON

Table F2-3-3(2) Chrominance Edge-Adaptive 2D Noise Reduction Auto ON/OFF Setting

ACLPF		CDTO1	CDTO2	Chrominance edge-adaptive 2D NR
[2]	[1]			
0	0	X	X	OFF
0	1	0	0	OFF
		1	0	ON
		1	1	ON
1	0	0	0	OFF
		1	0	OFF
		1	1	ON

2.3.4 Edge-Adaptive 2D Noise Reduction Demo Board

By setting ODEMO[1:0](SUB:64h-bit[7:6]) in the I^2C-bus interface, the edge-adaptive 2D noise reduction function can be checked as a demonstration mode by splitting the screen as shown in Figure F2-3-3.

Table F2-3-4 ODEMO Setting

ODEMO		Left side of screen	Right side of screen
[1]	[0]		
0	0	YLPFON, CLPFON setting	YLPFON, CLPFON setting
0	1	Edge-adaptive 2D OFF	YLPFON, CLPFON setting
1	0	Normal edge-adaptive 2D	YLPFON, CLPFON setting

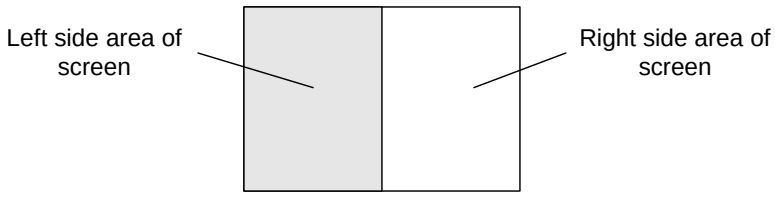


Figure F2-3-3 Edge-Adaptive 2D Noise Reduction Demo Screen

2.4 Luminance Edge Correction Processing

This IC has a luminance edge correction function that reduces the luminance band deterioration after 2D decoding in the input system.

2.4.1 Luminance Edge Correction

When YECON (SUB:64h-bit[5]) is set to 1, luminance data edge correction operates.
Undershoot or overshoot does not occur as a result of edge correction.

Table F2-4-1 Luminance Edge Correction Setting

YECON	Luminance edge correction
0	**OFF**
1	ON

3. Other Functions

3.1 REF Pin Output

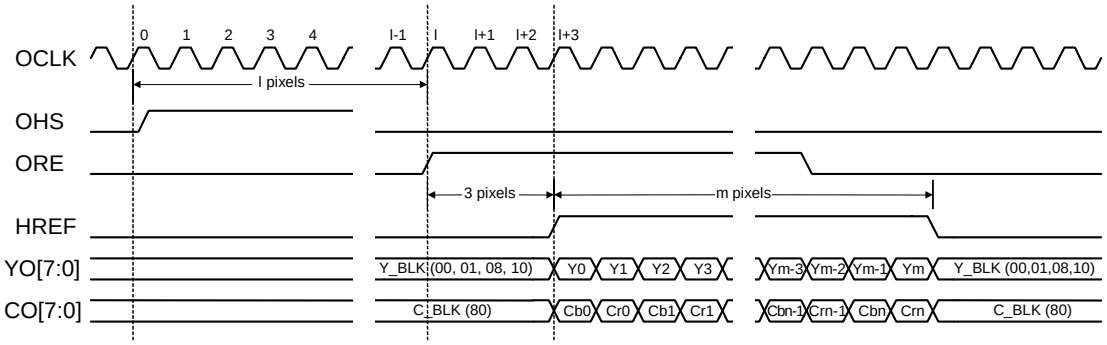
Set the I2C-bus setting register REFSL[1:0] (SUB:60h-bit[4:3]) to select a horizontal reference signal, chrominance select signal, or effective area signal for output from the HREF pin.

Table F3-1 REF Pin Output Selection

REFSL		REF pin output
[1]	[0]	
0	0	Horizontal reference signal
0	1	Chrominance select signal
1	0	Effective area signal (horizontal reference signal + vertical blanking signal)
1	1	Output system filed pulse signal

- Horizontal reference signal

  This signal is a signal for default valid data period 1 and blanking period 0. This signal can be used as the reference for separating Cb, Cr, etc.



I: Set at NPHRE[7:0].
m: Set at VMD, HMD.
n: m/2

Figure F3-1 (1) Horizontal Reference Signal

- Chrominance select signal

  The chrominance select signal is a signal that toggles between 0 (at valid period start) and ICLK. It can be used as a signal for separating Cb and Cr.

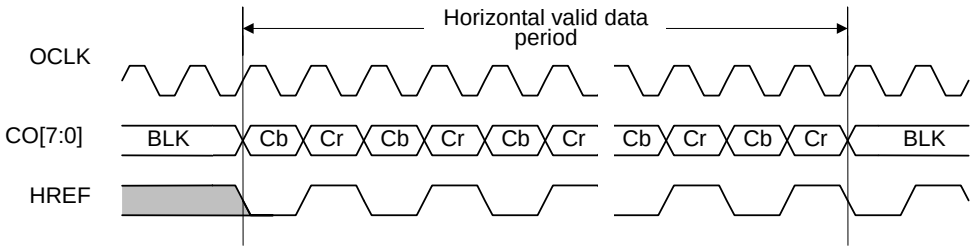


Figure F3-1 (2) Chrominance Select Signal Timing

- Effective area signal
  The effective area signal is created from a synthesis of the vertical valid blanking signal (vertical valid data period: 1, vertical blanking period: 0) and the horizontal reference signal (horizontal valid data period: 1, horizontal blanking period: 0). It is output as a signal with valid data period: 1, blanking period: 0.

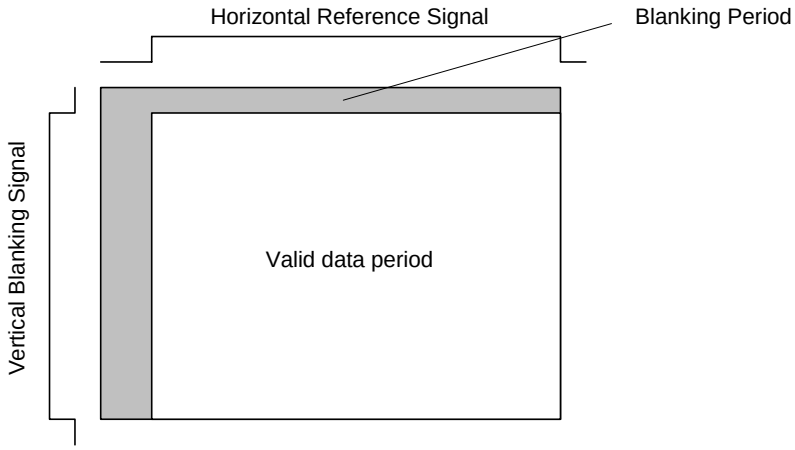


Figure F3-1 (3) Effective Area

- Field pulse signal
  Normally, the field pulse signal detected from the IVS and IHS phases is output.
  While R656I=1 is set, an F signal that complies with ITU-R BT.656 is output.

3.2 OVS, OHS, and HREF Pin Output Polarity Setting

The polarity of a group of Sync. signals that are output from the pins OVS, OHS, and HREF can be inverted by setting the I^2C-bus setting registers OVSINV (SUB:61h-bit[0]), OHSINV (SUB:61h-bit[1]), and HREFINV (SUB:61h-bit[2]).

Table F3-2(1) OVS Pin Polarity

OVSINV	OVS output
0	Input same polarity
1	Input opposite polarity

Table F3-2(2) OVS Pin Polarity

OHSINV	OHS output
0	Input same polarity
1	Input opposite polarity

Table F3-2(3) HREF Pin Polarity

HREFINV	HREF output
0	Internally generated same polarity
1	Internally generated opposite polarity

3.3 Output Signal Level Range Settings

ITU-R601 compliance is specified for the input signal level range for this IC. Output is normally the same as input, but where 00h and FFh are input for the valid data period, you can set the output signal level range to be 01h to FEh by setting the I^2C-bussettings register R601(SUB:40h-bit[6]) = 1.

Table F3-3 Output Signal Level Range

R601	Output signal level range
0	00h to FFh
1	01h to FEh

3.4 CLKO Output Setting

As a data latch for post-stage ICs of this IC, the CLKO pin can output a clock synchronized with data. Enable control of the CLKO pin is possible with CKEN (SUB:60h-bit[7]).
In normal mode, ICLK is output. When TEST7 is set to 1, IICLK (same as 16-bit mode: ICLK; 8-bit or ITU-R BT.656 mode:1 /2 division of ICLK) or ICLK can be selected in CKSL (SUB:60h-bit[6]).
Further, by setting CKINV (SUB:60h-bit[5]) as necessary, the polarity of the CLKO output clock can be inverted.

Table F3-4 CLKO Output

CKEN	CKSL	CKINV	CLKO output
0	**X**	**X**	**Hi-Z**
1	0	0	IICLK
1	0	1	IICLK inversion
1	1	0	ICLK
1	1	1	ICLK inversion

* In the 16-bit input mode, IICLK = ICLK.

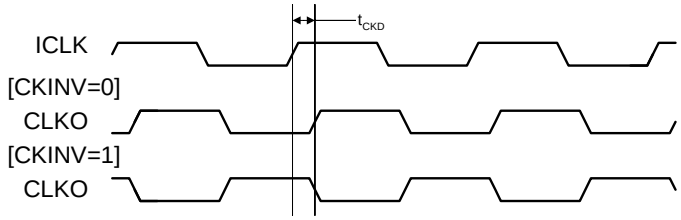


Figure F3-4 (1) CLKO Output Timing (16-Bit Mode)

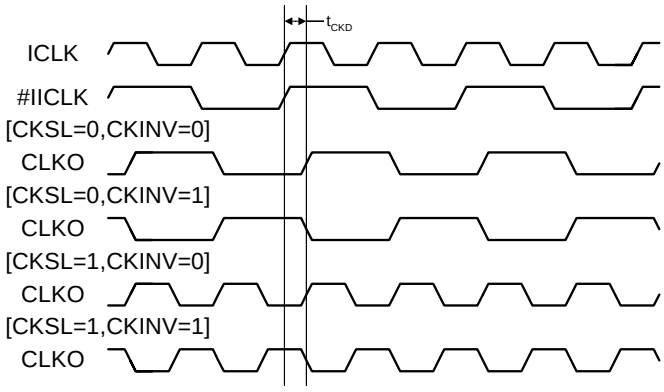


Figure F3-4 (2) CLKO Output Timing (8-Bit/ITU-R BT.656 Mode in Input)

3.5 Input Through Mode

By setting the register setting PASS (SUB:72h-bit[0]) = 1, the data (YI[7:0], CI[7:0]) and Sync. signals (IVS, IHS) that are input to the input system pins are directly output from the output system data (YO[7:0], CO[7:0]) and Sync. signal (OVS, OHS) pins. IHS is output from HREF pin at this time.
When both the RESET pin and the OE pin are set to a Low level, a through mode is set in the same way. In this case, input of the ICLK pin is output from the CLKO pin.

Table F3-5 Input Through Mode

Input pin	Output pin
YI[7:0]	YO[7:0]
CI[7:0]	CO[7:0]
IVS	OVS
IHS	OHS HREF

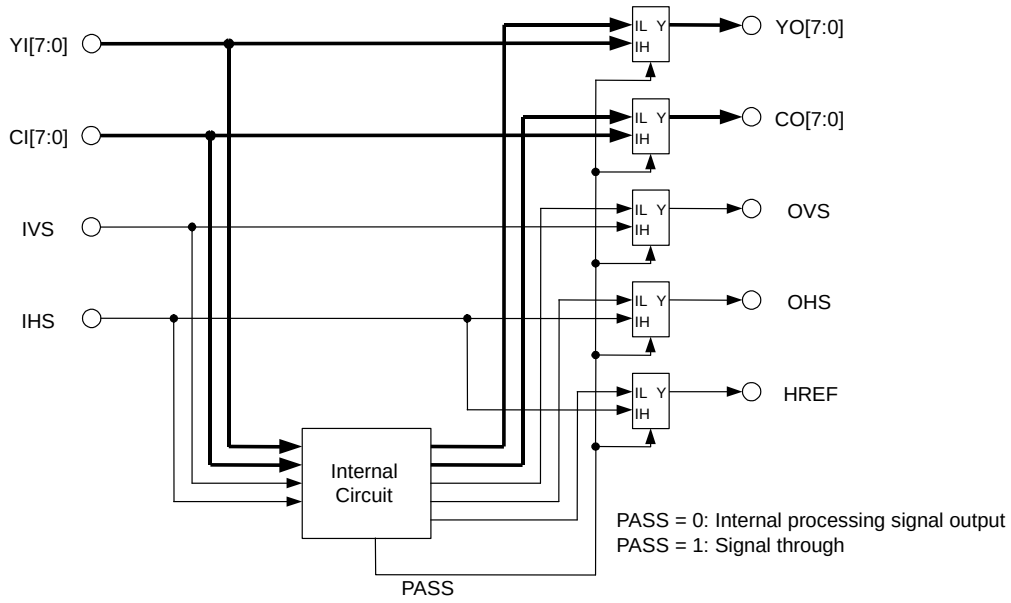


Figure F3-5 Input Through Mode

3.6 Output Enable/Disable Setting

By setting the OUTDS(SUB:72h-bit[1]) = 1, the output pins (YO[7:0], CO[7:0], OVS, OHS, HREF, CLKO) are put in the Hi-Z state.
At system reset (external pin RESET = 0), all the output pins can be set to Enable/Disable by the external pin OE regardless of the setting of OUTDS and output pin levels at power-on can be set.
By setting external pins OE and OEINV (SUB:72h-bit[3]), the output data pins (YO[7:0], CO[7:0]) can be put in the Hi-Z state.

Table F3-6 Output Pin Enable/Disable Setting

RST	OUTDS	OE	OEINV	Data output pin	Output pins other than data
1	0	0	0	Disable	Enable
1	0	0	1	Enable	Enable
1	0	1	0	Enable	Enable
1	0	1	1	Disable	Enable
1	1	X	X	Disable	Disable
0	0 (*1)	0	0 (*1)	Disable	Disable
0	0 (*1)	1	0 (*1)	Enable	Enable

*1: Fixed to 0 by system reset.

3.7 Release of Synchronization by Register Setting

Normally, the data that is set through I^2C interface is reflected in the IC internal section synchronously with IVS. However, as a test mode, using the I^2C-bus setting register RLTG (SUB:72h-bit[7]) can release the synchronization. Normally, synchronize with IVS by setting the register to 0.

Table F3-7 Synchronization Release Setting by Register

RLTG	Data reflection
0	Synchronized with IVS
1	When set by I^2C

4. I²C-Bus Interface

The IC incorporates an interface that conforms to the I²C-bus interface standards of Philips. This allows setting a filter selection etc., by an external micro-computer etc.
The slave address is set to 10111XX0 to write to and 10111XX1 to read from the IC.
Here, XX is set by the user with external setting pins. Namely, the slave address 10111, SLA2, SLA1, W/R is obtained by using SLA2 and SLA1.

Table F4 (1) Slave Address

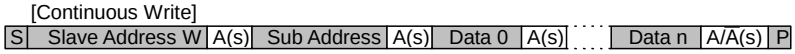
SLA2	SLA1	Slave Address (Write)	Slave Address (Read)
0	0	B8h	B9h
0	1	BAh	BBh
1	0	BCh	BDh
1	1	BEh	BFh

- I²C-bus format

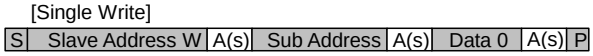
Input format of the I²C-bus interface is shown below.

Write Format

[Continuous Write]



[Single Write]

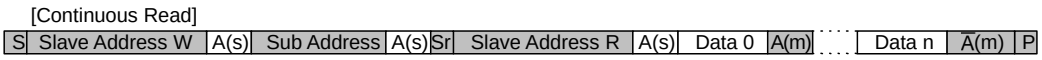


from master to slave

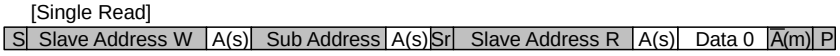
from slave to master

Read Format

[Continuous Read]



[Single Read]



from master to slave

from slave to master

Table F4 (2) Description of the I²C-bus Format

Symbol	Description
S	Start condition
Sr	Restart condition
Slave Address W	Slave address 1011_1XX0 (XX is set externally.)
Slave Address R	Slave address 1011_1XX1 (XX is set externally.)
A(s)	Acknowledge (Slave side generates.)
A(m)	Acknowledge (Master side generates.)
Sub Address	Sub-address byte
Data n	Data byte
P	Stop condition

As mentioned above, it is possible to read/write data at successive sub-addresses starting from a certain sub-address (continuous read/write). Read/write to a non-contiguous sub-address is performed by repeating the acknowledge and stop conditions of input format (single read/write) of the above-mentioned data 0.
The IC does not return acknowledge in the following cases:

Slave-address does not match.
Non-existing sub-address is specified.

The input timing diagram is shown below.

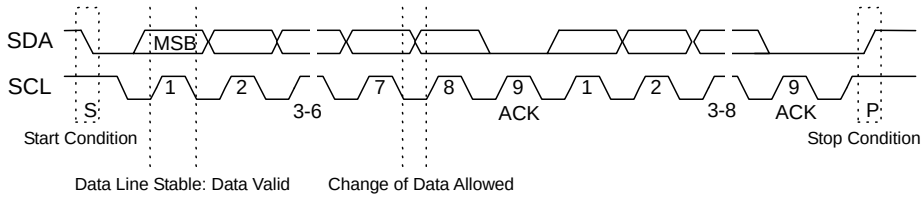


Figure F4 I²C-bus Interface Basic Timing

- Setting internal reflect timing
  Input System: IVS fall position (IVSINV = 0) or IVS rise position (IVSINV = 1).

* Settings by I²C-bus interface should be made by avoiding the position of above-mentioned setting internal reflect timing. If the setting is performed at a position that contains the above timing, the setting may not finish inside the same field.

DESCRIPTION OF THE REGISTERS

The IC is equipped with 64 bytes (sub-address 40h to 7Fh) of sub-address registers (8-bit unit) that can access by the I^2C-bus interface.
Write cycle of the I^2C-bus interface returns acknowledge by sub-addresses from 40h to 7Fh.
Regarding the read-only sub-addresses, acknowledge is returned but data write is not performed.
Settings such as mode setting, noise reduction function, memory control function, Sync. signals generation become possible by accessing these registers.
All writable registers become readable also.

The subaddress registers 40h to 7Fh of this IC are set to the initial values of the register map as a result of input of system reset (RESET pin = 0). For the reserved registers that are not included in the register map, 00h data is set as the initial value.

Note: Blank (reserved) registers must be set to 0.

1. Map of the Registers

Table R1 Map of the Registers (40h to 7Fh)

SA	DATA								Initial value	Sync
	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0		
40h	IRMON	R601	—	—	HMD		VMD		00h	IVS
					1	**0**	1	**0**		
41h	HBLKM	POFF	IHES	ICINV	—	APN656	**R656I**	**DISEL**	00h	—
42h	FCON	—	—	IVEM	IFLS	IFINV	IHSINV	IVSINV	00h	IVS
43h	—	—	—	STLM		STL			00h	IVS
				1	0	2	1	0		
44h	INPR	—	—	NPVWE					08h	IVS
				4	3	2	1	0		
45h	NPHWE								80h	IVS
	7	6	5	4	3	2	1	0		
46h	—								—	—
47h	—								—	—
48h	—	FNRM		NR2OFF	NRDEMO			NROFF	01h	IVS
		1	0		2	1	0			
49h	PNON	NDTC	NRDTF	PODT	AMM	ACY	NRDTON	NRAUTO	00h	IVS
4Ah	YSLT				AYABN	YABN	YFAM	YNRM	10h	IVS
	3	2	1	0						
4Bh	CSLT				ACABN	CABN	CFAM	CNRM	10h	IVS
	3	2	1	0						
4Ch	AYNS		YNS						18h	IVS
	1	0	5	4	3	2	1	0		
4Dh	ACNS		CNS						0Fh	IVS
	1	0	5	4	3	2	1	0		
4Eh	AYLM		AYNDL	YLM					06h	IVS
	1	0		4	3	2	1	0		
4Fh	ACLM		ACNDL	CLM					03h	IVS
	1	0		4	3	2	1	0		
50h	AYMS		A2OFF	—	YMS				04h	IVS
	1	0			3	2	1	0		
51h	AYMOFF			YMDM	YMOFF				06h	IVS
	3	2	1		3	2	1	0		
52h	CMY	PYST		CMOFF					80h	IVS
		1	0	4	3	2	1	0		
53h	YAH1	—	YAVR1						00h	IVS
			5	4	3	2	1	0		
54h	CAH1	—	CAVR1						00h	IVS
			5	4	3	2	1	0		
55h	YAH2	YAVR2							7Fh	IVS
		6	5	4	3	2	1	0		
56h	CAH2	CAVR2							7Fh	IVS
		6	5	4	3	2	1	0		
57h	DTPSL	—	NRDTP				CNAMS	YNAMS	00h	IVS
			3	2	1	0				
58h	YDTO1	YAVRO							00h	IVS (R)
		6	5	4	3	2	1	0		

SA	DATA								Initial value	Sync
	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0		
59h	CDTO1	CAVRO							00h	IVS (R)
		6	5	4	3	2	1	0		
5Ah	YDTO2	—	—	YMAXO					00h	IVS (R)
				4	3	2	1	0		
5Bh	CDTO2	—	—	CMAXO					00h	IVS (R)
				4	3	2	1	0		
5Ch	YBDTO	YBAVRO							00h	IVS (R)
		6	5	4	3	2	1	0		
5Dh	CBDTO	CBAVRO							00h	IVS (R)
		6	5	4	3	2	1	0		
5Eh	CCMM	CCYMS			CCMDT	CCMON	MEM411	CCON	00h	IVS
		2	1	0						
5Fh	DMCC	CCT	ACC		YCCNL				00h	IVS
			1	0	3	2	1	0		
60h	CKEN	CKSL	CKINV	REFSL		—	**DOSEL**	—	00h	—
				1	0					
61h	—	—	—	—	—	HREF INV	OHSINV	OVSINV	00h	—
62h	—								—	—
63h	—								—	—
64h	ODEMO		YECON	CLPFM	CLPFON	YHLPFM	YLPFM	YLPFON	00h	IVS
	1	0								
65h	AYLPF		AYED	YED					0Fh	IVS
	2	1		4	3	2	1	0		
66h	ACLPF		ACED	CED					0Fh	IVS
	2	1		4	3	2	1	0		
67h	—								—	—
68h	—								—	—
69h	—								—	—
6Ah	—								—	—
6Bh	—								—	—
6Ch	—								—	—
6Dh	—								—	—
6Eh	—								—	—
6Fh	—								—	—
70h	TST								00h	—
	7	6	5	4	3	2	1	0		
71h	TST								00h	—
	15	14	13	12	11	10	9	8		
72h	RLTG	—	—	AROS	—	OEINV	OUTDS	PASS	00h	—
73h	RYLPF	—	RYNS						00h	IVS (R)
			5	4	3	2	1	0		
74h	RCLPF	RCCON	RCNS						00h	IVS (R)
			5	4	3	2	1	0		
75h	RYABN	RYNRM	RYNR OFF	RYLM					00h	IVS (R)
				4	3	2	1	0		
76h	RCABN	RCNRM	RCNR OFF	RCLM					00h	IVS (R)
				4	3	2	1	0		

SA	DATA								Initial value	Sync
	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0		
77h	RYMOF			RNR2	RYMS				00h	IVS
	3	2	1	OFF	3	2	1	0		(R)
78h	—	—	—	—	—	—	HSSEL	ISYNC	00h	—
79h	SHSDL								00h	—
	7	6	5	4	3	2	1	0		
7Ah	TST								00h	—
	23	22	21	20	19	18	17	16		
7Bh	0	1	0	1	0	1	0	1	55h	(R)
7Ch	1	0	1	0	1	0	1	0	AAh	(R)
7Dh	1	1	1	1	1	1	1	1	FFh	(R)
7Eh	0	0	1	0	0	0	0	1	21h	(R)
7Fh	0	1	1	1	0	0	0	1	71h	(R)

* (-): Reserved register

2. Description of the Registers

2.1 Mode Setting

SUB_ADDRESS = 40h (W/R): Write/read common mode setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	IRMON	R601	(Reserved)	(Reserved)	HMD		VMD	
					1	0	1	0

VMD[1:0] Initial value: 00; Setting range: 00 to 11
Sets vertical lines operation mode.
In normal operation, 2 and 3 are not set.
VMD[0] is validated when IRMON = 1.

Table R2-1 (1) Vertical Line Operation Mode Setting

VMD		Vertical line operation mode setting
[1]	[0]	
0	**0**	**625-line mode**
0	1	525-line mode
1	0	Test mode
1	1	

HMD[1:0] Initial value: 00; Setting range: 00 to 11
Sets horizontal effective pixels (sampling frequency) mode.
In normal operation, 3 is not set.
HMD[0] is validated at IRMON = 1.

Table R2-1 (2) Horizontal Valid Pixel Mode Setting

HMD		Horizontal valid pixels mode setting	Sampling frequency
[1]	[0]		
0	**0**	**720-pixel mode**	13.5 MHz
0	1	Square (768/640) pixel mode	14.75/12.272727 MHz
1	0	768-pixel mode	14.75/14.31818 MHz
1	1	Test mode	—

R601 Initial value: 0; Setting range: 0 to 1
Sets input/output valid data signal level.
This setting is necessary if the input signal level conforms to ITU-R BT.601.

Table R2-1 (4) Input/Output Valid Data Signal Level Range

R601	Input signal level range
0	**00h to FFh**
1	ITU-R BT.601 (01h to FEh)

IRMON Initial value: 0; Setting range: 0 to 1
Sets external pin/internal registers switching for memory control mode setting

Table R2-1 (5) External Pin Setting Switching Setting

IRMON	Register set mode setting
0	**External pin (MODE[4:0])**
1	Internal registers (VMD[0], HMD[0], DISEL, R656I, DOSEL)

2.2 Input Settings

2.2.1 Input Data Setting

SUB_ADDRESS = 41h(W/R): Input data setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	HBLKM	POFF	IHES	ICINV	(Reserved)	APN656	R6561	DISEL

DISEL Initial value: 0; Setting range: 0 to 1

Sets input data format.

When R656 = 0, the input data format of 16-bit YCbCr 4:2:2 or 8-bit YCbCr 4:2:2 is selectable.

This register is valid when IRMON = 1. When IRMON = 0, external pin MODE2 performs the similar operation.

R656I Initial value: 0; Setting range: 0 to 1

Sets input data format.

By setting R656I = 1, the input data format supports the ITU-R BT.656 standards regardless of DISEL and MODE2 settings.

Table R2-2-1 (1) Input Data Format Setting

IRMON	MODE2	DISEL	R656I	Input data format
0	0	X	0	16-bit 4:2:2 YCbCr
1	X	0	0	
0	1	X	0	8-bit 4:2:2 YCbCr
1	X	1	0	
X	X	X	1	ITU-R BT.656 mode

APN656 Initial value: 1, Setting range: 0 to 1

Automatic setting of 625/525

In ITU-R BT.656 input/output mode, the IC checks the format of 625 lines/525 lines and automatically switches to the mode according to the setting VMD[0]. In this case, VMD[0] set due to external pin setting or internal register setting is ignored.

Table R2-2-1(2) Automatic 625/525 Setting

APN656	Automatic 625/525 setting
0	**OFF (VMD[0] setting)**
1	ON (automatic setting) * ITU-R BT.656 input mode only

ICINV Initial value: 0; Setting range: 0 to 1

Sets internal input system clock (IICLK) polarity.

Sets the polarity of IICLK (ICLK frequency-divided by 2) generated in the input 8-bit mode and ITU-R BT.656 mode.

This setting is not in synchronization with IVS.

Table R2-2-1 (3) IICLK Polarity Setting

ICINV	IICLK polarity
0	At IHS rise reset: 1
1	At IHS rise reset: 0

IHES Initial value: 0; Setting range: 0 to 1

Sets IHS edge for internal input system clock (IICLK) reset

Selects the reset timing of IICLK generated in 1H period at the fall or rise of IHS.

Table R2-2-1 (4) IHS Edge Setting for IICLK Reset

IHES	IHS edge for H reset
0	**Rise**
1	Fall

POFF Initial value: 0; Setting range: 0 to 1

Sets ITU-R BT.656 mode parity check.

Table R2-2-1 (5) ITU-R BT.656 Mode Parity Check Setting

POFF	Parity check
0	**ON**
1	OFF

HBLKM Initial value: 0; Setting range: 0 to 1

Sets an ITU-R BT.656 mode timing reference mask.

Invalid timing reference codes of horizontal blanking (between EAV and SAV) are ignored.

Table R2-2-1(6) Timing Reference Code Mask Setting

HBLKM	Timing reference code detection
0	All timing reference code enabled.
1	Timing reference code during horizontal blanking period disabled.

2.2.2 Input System Memory Control Mode Setting

SUB_ADDRESS = 42h(W/R): Input system memory control mode setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	FCON	(Reserved)	(Reserved)	IVEM	IFLS	IFINV	IHSINV	IVSINV

IVSINV Initial value: 0; Setting range: 0 to 1

Sets input polarity (timing edge) of input system vertical synchronization signal (IVS).
The IC operates with the fall of IVS positive polarity as a reference. However, in case the IVS input is of negative polarity, it is possible to match the polarity reference such as the rise of positive polarity.

Table R2-2-2 (1) IVS Input Polarity (Edge) Setting

IVSINV	IVS input polarity 1	IVS input polarity 2
0	**Positive polarity (Fall)**	**Negative polarity (Fall)**
1	Negative polarity (Rise)	Positive polarity (Rise)

IHSINV Initial value: 0; Setting range: 0 to 1

Sets input polarity (timing edge) of input system horizontal synchronization signal (IHS).
The IC operates with the rise of IHS positive polarity as a reference. However, if the IHS input is of negative polarity, it is possible to match the polarity reference such as making the fall of positive polarity.

Table R2-2-2 (2) IHS Input Polarity (Edge) Setting

IHSINV	IHS input polarity 1	IHS input polarity 2
0	**Positive polarity (Rise)**	**Negative polarity (Rise)**
1	Negative polarity (Fall)	Positive polarity (Fall)

IFINV Initial value: 0; Setting range: 0 to 1

Sets the polarity of input system detection field pulse.

Table R2-2-2 (3) Polarity Setting of Input System Detection Field Pulse

IFINV	Detection field pulse
0	**Decision result**
1	Decision result inversion

IFLS Initial value: 0; Setting range: 0 to 1

Sets input system field decision mode selection.

Table R2-2-2 (4) Input System Field Decision Mode Selection Setting

IFLS	Detection field pulse
0	**IHS decision**
1	0.5H pulse decision

IVEM Initial value: 0; Setting range: 0 to 1

Sets input system vertical reset compensation mode.

When IVEM = 1, inverts the detection field and performs 1 line delay reset for field B.

Table R2-2-2 (5) Input System Vertical Reset Compensation Mode Setting

IVEM	IVS reset compensation
0	**No compensation**
1	Compensation (Field inversion, field B 1 line delay vertical reset)

FCON Initial value: 0; Setting range: 0 to 1

Sets successive same field input countermeasure.

Automatically generates both fields by detecting 8 or more successive same fields.

Table R2-2-2 (6) Detection Field Pulse Polarity Setting

FCON	Detection field pulse
0	**Decision result mode**
1	Automatic field generation mode

2.2.3 Memory Control Setting 1 (write stop)

SUB_ADDRESS = 43h(W/R): Memory write stop setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	(Reserved)	(Reserved)	(Reserved)	STLM		STL		
				1	0	2	1	0

STL[2:0] Initial value: 000; Setting range: Refer to Table R2-2-3.
Sets input data write stop control.
When data write stops, holds the field data just before the data write stops.
While INPR is set to 1, the setting of SLT[2:1] is disabled.

Table R2-2-3 (1) Input Data Write Stop Setting

STL			Input data write
[2]	[1]	[0]	
0	0	0	Possible (field B recovery)
0	1	0	Possible (field A recovery)
1	X	0	Possible (arbitrary field recovery)
0	0	1	Stop (field A data hold)
0	1	1	Stop (field B data hold)
1	X	1	Stop (arbitrary field data hold)

STLM Initial value: 0; Setting range: 0 to 1
Sets output when input data writing stop is controlled.
While INPR is set to 1, this setting is disabled.

Table R2-2-3 (2) Output Mode Settings when Input Data Writing is Stopped

STLM		Output mode
[1]	[0]	
X	**0**	**Field output mode**
0	1	Frame output mode (normal)
1	1	Frame output mode (median)

2.2.4 Memory Control Setting 2 (phase adjustment)

SUB_ADDRESS = 44h(W/R): Input system memory control vertical phase adjustment setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	INPR	(Reserved)	(Reserved)	NPVWE				
				4	3	2	1	0
SUB_ADDRESS = 45h(W/R): Input system memory control horizontal phase adjustment setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	NPHWE							
	7	6	5	4	3	2	1	0

NPVWE[4:0] Initial value: 1000; Setting range: 00001 to 11111
When INSINV = 0, sets the number of lines (IHS input count) from the IVS fall position up to the vertical standard write start position.
When IVSINV = 1, the number of lines is set from the IVS rise position.
NPVWE[4]is enabled only when INPR = 1.

INPR Initial value: 0; Setting range: 0 to 1
Sets progressive input.

Table R2-2-4 Progressive Input Setting

INPR	Input
0	**Interlace (525i/625i)**
1	Progressive input (525p/625p)

NPHWE[7:0] Initial value: 1000_0000; Setting range: 0000_0001 to 1111_1111
When IHSINV = 0, sets the number of pixels from the IHS rise position up to the horizontal standard write start position.
When IHSINV = 1, sets the number of pixels from the IHS fall position.

2.3 Noise Reduction Settings

2.3.1 Noise Reduction Stop/Demo Mode Setting

SUB_ADDRESS = 48h(W/R): Noise reduction stop/demo mode setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	(Reserved)	FNRM		NR2OFF	NRDEMO			NROFF
		1	0		2	1	0	

NROFF Initial value: 1; Setting Range: 0 to 1

Sets On/Off of the 3D noise reduction function.

Although data is written to the memory when the setting is off, all the noise reduction functions are stopped.

NRDEMO[2:0] Initial value: 000; Setting range: Refer to Table R2-3-1(1).

Sets On/Off of noise reduction function demo mode.

Motion compensation stop is the same as YMOFF[3:0] = Fh, CMOFF[4:0] = 1Fh.

Table R2-3-1 (1) Noise Reduction Stop/Demo Mode On/Off Setting

NROFF	NRDEMO			Left side screen	Right side screen
	[2]	[1]	[0]		
0	0	0	0	NR setting value	NR setting value
1	**X**	**X**	**X**	**Stop NR.**	**Stop NR.**
0	X	X	1	Stop NR.	NR setting value
0	X	1	0	Stop motion compensation.	NR setting value
0	1	0	0	Stop auto mode.	NR setting value
0	1	1	0	Stop motion compensation. Stop auto mode.	NR setting value

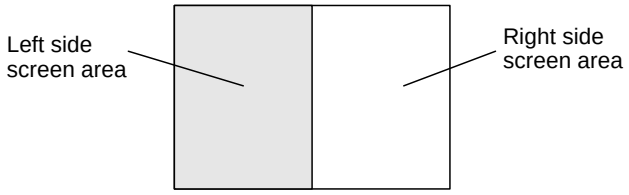


Figure R2-3-1 Noise Reduction Demo Screen

NR2OFF Initial value: 0; Setting range: 0 to 1
Sets the ON/OFF of the line correlation noise reduction feature.

Table R2-3-1 (2) Line Correlation Noise Reduction Settings

NR2OFF	line correlation noise reduction
0	**ON (adaptive)**
1	OFF

FNRM[1:0] Initial value:0; Setting range: 00 to 11
Sets the noise reduction recursive mode.

Table R2-3-1 (3) Recursive Mode Settings

FNRM		Mode
[1]	[0]	
0	**0**	**Frame / field adaptive mode**
0	1	Frame mode
1	X	Field mode

2.3.2 Noise Reduction Auto Mode Setting

SUB_ADDRESS = 49h(W/R): Noise reduction auto mode setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	PNON	NDTC	NRDTF	PODT	AMM	ACY	NRDTON	NRAUTO

NRAUTO Initial value: 0; Setting range: 0 to 1

Sets noise reduction auto mode.

When NRAUTO = 1, the noise reduction setting can be performed based on the noise state detected at NRDTON = 1.

Table R2-3-2 (1) Auto Level Setting Mode Setting

NRAUTO	Noise reduction mode
0	**Register fixed mode**
1	Auto mode

NRDTON Initial value: 0; Setting range: 0 to 1

Sets On/Off of noise detection.

When NRDTON = 1, performs noise detection on areas set by NRDTF, NRDTP[3:0], NDTC and PNON. The average and maximum detected noise values are updated every frame.

Table R2-3-2 (2) Noise Detection On/Off Setting

NRDTON	Noise detection
0	**Stop (Hold)**
1	Updated every frame

ACY Initial value: 0; Setting range: 0 to 1

Sets chrominance noise detection flag mode.

When ACY = 1, masking for the chrominance noise detection flags (CDTO1, CDTO2) is performed by luminance noise detection flags (YDTO1, YDTO2). Holds the noise detection flag to “0” even if the chrominance noise detection value has exceeded the setting level as far as the luminance noise detection value does not exceed the setting value.

Table R2-3-2(3) Chrominance Noise Detection Flag Mode Setting

ACY	Chrominance noise detection flag mode
0	**Chrominance independent**
1	Luminance linked

AMM Initial value: 0; Setting range: 0 to 1
Sets noise reduction auto mode transition.
Selects noise reduction transition mode at NRAUTO = 1.

Table R2-3-2 (4) Noise Reduction Auto Mode Status Transition Setting

AMM	Noise Reduction Status		
	YDTO1 = 0, YDTO2 = 0 CDTO1 = 0, CDTO2 = 0	YDTO1 = 1, YDTO2 = 0 CDTO1 = 1, CDTO2 = 0	YDTO1 = 1, YDTO2 = 1 CDTO1 = 1, CDTO2 = 1
0	**Noise reduction OFF**	**Fixed register state A (Without automatic motion compensation OFF)**	**Noise follow-up state (With automatic motion compensation OFF)**
1	Fixed register state B1 (Without automatic motion compensation OFF. Same as YNRM = 1, CNRM = 1)	Fixed register state B2 (With automatic motion compensation OFF)	Noise follow-up state (With automatic motion compensation OFF)

PODT Initial value: 0; Setting range: 0 to 1
Noise detection is set for valid data only.
The function operates regardless of PNON. * For monitor cameras

NRDTF Initial value: 0; Setting range: 0 to 1
Sets noise detection field.
Noise detection is performed once in one frame in the vertical blanking period of one side. Performs selection of that detection field.

Table R2-3-2 (5) Noise Detection Field Setting

NRDTF	Noise detection field
0	**Field A**
1	Field B

NDCT Initial value: 0; Setting range: 0 to 1
Sets noise detection area in the blanking period.
Selects the setting of the basic noise detection period.

Table R2-3-2 (6) Basic Noise Detection Period Setting

NDTCF	Basic noise detection period
0	**1 line set by NRDTP[3:0]**
1	Multiple lines set by NRDTP[3:0]

PNON Initial value: 0; Setting range: 0 to 1
Sets noise detection area.
Selects the use of "vertical blanking + valid data area" for noise detection.
* Priority is given to PODT=1.

Table R2-3-2 (7) Noise Detection Area Setting

PODT	PNON	Noise detection period
0	**0**	**Vertical blanking period only**
0	1	Vertical blanking period + valid data period
1	X	Valid data period only

2.3.3 Noise Reduction Motion Compensation Mode/Noise Detection Inclination Setting

SUB_ADDRESS = 4Ah(W/R): Luminance noise reduction motion compensation mode/Noise detection inclination setting

DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	YSLT				AYABN	YABN	YFAM	YNRM
	3	2	1	0				

SUB_ADDRESS = 4Bh(W/R): Chrominance noise reduction motion compensation mode/Noise detection inclination setting

DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	CSLT				ACABN	CABN	CFAM	CNRM
	3	2	1	0				

YNRM Initial value: 0; Setting range: Refer to Table R2-3-3 (1).
Sets luminance noise reduction motion compensation mode selection.

YFAM Initial value: 0; Setting range: Refer to Table R2-3-3 (3).
Sets luminance adaptive noise reduction mode.

YABN Initial value: 0; Setting range: Refer to Table R2-3-3 (5).
Sets luminance absolute noise mode.
It is possible not to perform 1/2 motion compensation as absolute noise with respect to the motion level detection noise of luminance signal.

AYABN Initial value: 0; Setting range: Refer to Table R2-3-3 (7).
Sets auto mode luminance absolute noise mode.
By setting to "1", the luminance absolute noise mode operates in luminance noise follow-up state (YDTO2 = 1) of the auto mode. (The same operation as YABN = 1.)

YSLT[3:0] Initial value: 0001; Setting range: Refer to Table R2-3-3 (9).
Sets luminance noise reduction noise detection lines/convergence lines inclination.

CNRM Initial value: 0; Setting range: Refer to Table R2-3-3 (2).
Sets chrominance noise reduction motion compensation mode selection.

CFAM Initial value: 0; Setting range: Refer to Table R2-3-3 (4).
Sets chrominance adaptive noise reduction mode.

CABN Initial value: 0; Setting range: Refer to Table R2-3-3 (6).
Sets chrominance absolute noise mode.
It is possible not to perform 1/2 motion compensation as absolute noise with respect to the motion level detection noise of chrominance signal.

ACABN Initial value: 0; Setting range: Refer to Table R2-3-3 (8).
Sets auto mode chrominance absolute noise mode.
By setting to "1", the chrominance absolute noise mode operates in the chrominance noise follow-up state (CDTO2 = 1) of the auto mode. (The same operation as CABN = 1.)

CSLT[3:0] Initial value: 0001; Setting range: Refer to Table R2-3-3 (10).
Sets chrominance noise reduction noise detection line/convergence line inclination.

Table R2-3-3 (1) Luminance Noise Reduction Motion Compensation Mode Setting

YNRM	Luminance motion decision noise processing (Motion compensation)
0	**(Non-linear filter detection noise) × (Attenuation coefficient)**
1	Fix to 0. (Decision without noise)

Table R2-3-3 (2) Chrominance Noise Reduction Motion Compensation Mode Setting

CNRM	Chrominance motion decision noise processing (Motion compensation)
0	**(Non-linear filter detection noise) × (Attenuation coefficient)**
1	Fix to 0. (Decision without noise)

Table R2-3-3 (3) Luminance Adaptive Noise Reduction Mode Settings

YFAM	Luminance adaptive noise reduction mode
0	**Without adaptive margin (weak NR, few afterimages)**
1	With adaptive margin (strong NR, many afterimages)

Table R2-3-3 (4) Chrominance Adaptive Noise Reduction Mode

CFAM	Chrominance adaptive noise reduction mode
0	**Without adaptive margin (weak NR, few afterimages)**
1	With adaptive margin (strong NR, many afterimages)

Table R2-3-3 (5) Luminance Absolute Noise Mode Setting

YABN	Luminance mode	Remarks
0	**Normal noise mode**	**(Detection noise) × (Motion compensation attenuation coefficient)**
1	Absolute noise mode	(Detection noise)/2 + {(Detection noise) × (Motion compensation attenuation coefficient)}/2

Table R2-3-3 (6) Chrominance Absolute Noise Mode Setting

CABN	Chrominance mode	Remarks
0	**Normal noise mode**	**(Detection noise) × (Motion compensation attenuation coefficient)**
1	Absolute noise mode	(Detection noise)/2 + {(Detection noise) × (Motion compensation attenuation coefficient)}/2

Table R2-3-3 (7) Auto Mode Luminance Absolute Noise Mode Setting (Valid when NRAUTO=1)

AYABN	Noise follow-up state luminance mode
0	**Normal noise mode**
1	Absolute noise mode

Table R2-3-3 (8) Auto mode Chrominance Absolute Noise Mode Setting (Valid when NRAUTO=1)

ACABN	Noise follow-up state chrominance mode
0	**Normal noise mode**
1	Absolute noise mode

Table R2-3-3 (9) Luminance Non-linear Filter Noise Detection/Convergence Line Inclination Setting

YSLT				Noise detection line coefficient (Inclination)	Noise convergence line coefficient (Inclination)
[3]	[2]	[1]	[0]		
X	X	0	0	1	–
X	**X**	**0**	**1**	**7/8**	**–**
X	X	1	0	3/4	–
X	X	1	1	1/2	–
0	**0**	**X**	**X**	**–**	**1 (–1)**
0	1	X	X	–	3/4 (–3/4)
1	0	X	X	–	1/2 (–1/2)
1	1	X	X	–	3/2 (–3/2)

Table R2-3-3 (10) Chrominance Non-linear Filter Noise Detection/Convergence Line Inclination Setting

CSLT				Noise detection line coefficient (Inclination)	Noise convergence line coefficient (Inclination)
[3]	[2]	[1]	[0]		
X	X	0	0	1	–
X	**X**	**0**	**1**	**7/8**	**–**
X	X	1	0	3/4	–
X	X	1	1	1/2	–
0	**0**	**X**	**X**	**–**	**1 (–1)**
0	1	X	X	–	3/4 (–3/4)
1	0	X	X	–	1/2 (–1/2)
1	1	X	X	–	3/2 (–3/2)

2.3.4 Noise Convergence Level Setting

SUB_ADDRESS = 4Ch(W/R): Luminance noise convergence level setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	AYNS		YNS					
	1	0	5	4	3	2	1	0
SUB_ADDRESS = 4Dh(W/R): Chrominance noise convergence level setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	ACNS		CNS					
	1	0	5	4	3	2	1	0

YNS[5:0] Initial value: 01_1000; Setting range: 00_0000 to 11_1111
Sets luminance noise convergence level.
This setting can be used also for the adjacent motion compensation level.
The setting can be adjusted in 0 to 63 levels for differential data of luminance signal fields. The detected noise level is limited to 1Fh as a result of combining the detection and convergence lines.

AYNS[1:0] Initial value: 00; Setting range: Refer to Table R2-3-4 (1).
Sets auto mode luminance noise convergence level.
Becomes valid in the auto mode noise follow-up state.

CNS[5:0] Initial value: 00_1111; Setting range: 00_0000 to 11_1111
Sets chrominance noise convergence level.
This setting can be used also for the adjacent motion compensation level.
The setting can be adjusted in 0 to 63 levels for differential data of the chrominance signal field. The detected noise level is limited to 1Fh as a result of combining the detection and convergence lines.

ACNS[1:0] Initial value: 00; Setting range: Refer to Table R2-3-4 (2).
Sets auto mode chrominance noise convergence level.
Becomes valid in the noise follow-up state in the auto mode.

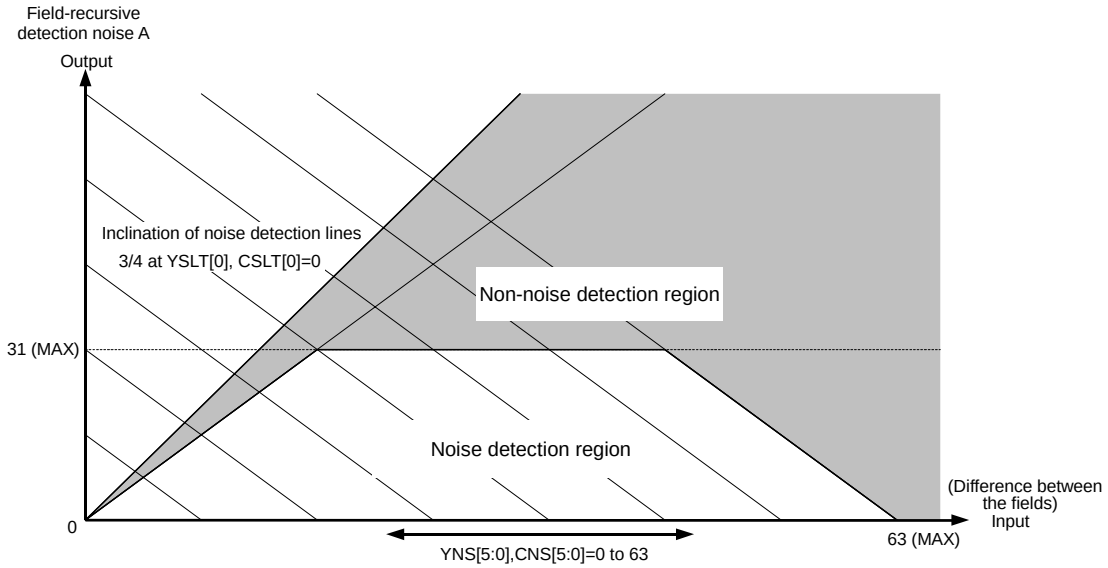


Figure R2-3-4 Example of Noise Detection by the YNS and CNS Settings

Table R2-3-4 (1) Auto Mode Luminance Noise Convergence Level Setting (Valid at NRAUTO=1)

AYNS		Noise Follow-up State Noise Convergence Level
[1]	[0]	
X	**0**	**YNS[5:0]**
0	1	YNS[5:0] + YMAXO[5:0] (Max.: 3Fh)
1	1	YMAXO[5:0] × 3 (Max.: 3Fh)

Table R2-3-4 (2) Auto Mode Chrominance Noise Convergence Level Setting (Valid at NRAUTO=1)

ACNS		Noise Follow-up State Noise Convergence Level
[1]	[0]	
X	**0**	**CNS[5:0]**
0	1	CNS[5:9] + CMAXO[5:0] (Max.: 3Fh)
1	1	CMAXO[5:0] × 4 (Max.: 3Fh)

2.3.5 Noise Upper Limit Setting

SUB_ADDRESS = 4Eh(W/R): Luminance noise upper limit level setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	AYLM		AYNDL	YLM				
	1	0		4	3	2	1	0
SUB_ADDRESS = 4Fh(W/R): Chrominance noise upper limit level setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	ACLM		ACNDL	CLM				
	1	0		4	3	2	1	0

YLM[4:0] Initial value: 0_0110; Setting range: 0_0000 to 1_1111
Sets luminance noise upper limit level.
The limit values are selected by 00h to 1Fh.

AYNDL Initial value: 0; Setting range: 0 to 1
Sets luminance noise upper limit level of noise detection.
By setting 1, unexpected noise at noise detection is restricted to control the rapid change in the noise detection amount.

AYLM[1:0] Initial value: 00; Setting range: Refer to table R2-3-5 (1).
Sets auto mode luminance noise upper limit level.
Becomes valid in noise follow-up state in the auto mode.

CLM[4:0] Initial value: 0_0011; Setting range: 0_0000 to 1_1111
Sets chrominance noise upper limit level.
The limit values are selected by 00h to 1Fh.

AYNDL Initial value: 0; Setting range: 0 to 1
Sets luminance noise upper limit level of noise detection.
By setting 1, unexpected noise at noise detection is restricted to control the rapid change in the noise detection amount is controlled.

ACLM[1:0] Initial value: 00; Setting range: Refer to table R2-3-5 (2).
Sets auto mode chrominance noise upper limit level.
Becomes valid in the auto mode noise follow-up state.

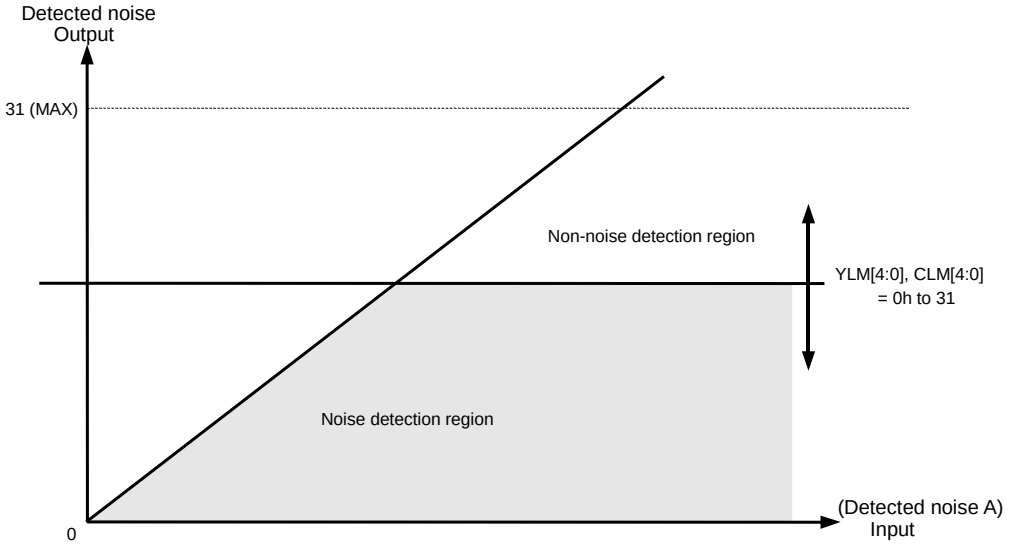


Figure R2-3-5 Noise Detection Limits by YLM and CLM Settings

Table R2-3-5 (1) Auto Mode Luminance Noise Upper Limit Level Setting (Valid at NRAUTO = 1)

AYLM		Noise Follow-up State Luminance Noise Upper Limit Level
[1]	[0]	
X	**0**	**YLM[4:0]**
0	1	YMAXO[5:0] × 0.75 (Max.: 1Fh)
1	1	YMAXO[5:0] (Max.: 1Fh)

Table R2-3-5 (2) Auto Mode Chrominance Noise Upper Limit Level Setting (Valid at NRAUTO = 1)

ACLM		Noise Follow-up State Chrominance Noise Upper Limit Level
[1]	[0]	
X	**0**	**CLM[4:0]**
0	1	CMAXO[5:0] × 0.75 (Max.: 1Fh)
1	1	CMAXO[5:0] (Max.: 1Fh)

2.3.6 Luminance Continuous Code Motion Compensation Level Setting

SUB_ADDRESS = 50h(W): Luminance Continuous Code Motion Compensation Level Setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	AYMS		A2OFF	(Reserved)	YMS			
	1	0			3	2	1	0

YMS[3:0] Initial value: 0100; Setting range: 0000 to 1111

Sets luminance signal continuous code motion compensation level.
Settable in 0 to 30 levels for the luminance signal field differential absolute value data.
Assigns respective setting values to the 3-continuous codes, 4-continuous codes and 5-continuous codes motion detection, decides data having large motion components for |ΔLY| exceeding the setting, and performs the noise attenuation compensation (YNRM = 0) or NROFF compensation (YNRM = 1).

Table R2-3-6 (1) 3-Continuous Code Motion Compensation Decision

Motion detection condition	Motion decision
|ΔLY| > 16	Large (Compensation operation)
|ΔLY| > YMS[3:0]	Large (Compensation operation)
|ΔLY| ≤ YMS[3:0]	Small (No compensation)

Table R2-3-6 (2) 4-Continuous Code Motion Compensation Decision

Motion detection condition	Motion decision
|ΔLY| > 8	Large (Compensation operation)
|ΔLY| > YMS[3:1]	Large (Compensation operation)
|ΔLY| ≤ YMS[3:1]	Small (No compensation)

Table R2-3-6 (3) 5-Continuous Code Motion Compensation Decision

Motion detection condition	Motion decision
|ΔLY| > 4	Large (Compensation operation)
|ΔLY| > YMS[3:2]	Large (Compensation operation)
|ΔLY| ≤ YMS[3:2]	Small (No compensation)

AYMS[1:0] Initial value: 00; Setting range: Refer to table R2-3-5 (4).

Sets auto mode luminance motion compensation level.
Valid in the auto mode noise follow-up state.

Table R2-3-6 (4) Auto Mode Motion Compensation Level Setting (Valid at NRAUTO = 1)

AYMS		Noise follow-up state motion compensation level
[1]	[0]	
X	**0**	**YMS[4:0]**
0	1	YMAXO[5:0] (Max.: Fh)
1	1	YMAXO[5:0]/2 (Max.: Fh)

A2OFF Initial value: 0; Setting range: 0 to 1

Sets the auto mode line correlation noise reduction OFF.

If there is a lot of noise in the auto mode, the line correlation noise reduction is turned OFF.

Table R2-3-6 (5) Auto Mode Line Correlation Noise Reduction OFF Setting

A2OFF	Line correlation noise reduction
0	**Depends on NR2OFF setting**
1	Line correlation OFF in noise status 2

2.3.7 Noise Reduction Motion Compensation ON/OFF Setting

SUB_ADDRESS = 51h(W/R): Luminance Noise Reduction Motion Compensation ON/OFF Setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	AYMOFF			YMDM	YMOFF			
	3	2	1		3	2	1	0
SUB_ADDRESS = 52h(W/R): Chrominance Noise Reduction Motion Compensation ON/OFF Setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	CMY	PYST		CMOFF				
		1	0	4	3	2	1	0

YMOFF[3:0] Initial value: 0000; Setting range: Refer to Table R2-3-7 (1).
Sets motion compensation ON/OFF of luminance signal field-recursive noise reduction detection noise.

Table R2-3-7 (1) Luminance Motion Compensation ON/OFF Setting 1

YMOFF				Luminance motion level detection noise motion compensation
[3]	[2]	[1]	[0]	
X	X	X	**0**	**Luminance horizontal contiguous motion level compensation - ON**
X	X	X	1	Luminance horizontal contiguous motion level compensation - OFF
X	X	0	X	Luminance horizontal contiguous 3-continuous code motion compensation - ON
X	X	**1**	X	**Luminance horizontal contiguous 3-continuous code motion compensation - OFF**
X	0	X	X	Luminance horizontal contiguous 4-continuous code motion compensation - ON
X	**1**	X	X	**Luminance horizontal contiguous 4-continuous code motion compensation - OFF**
0	X	X	X	**Luminance horizontal contiguous 5-continuous code motion compensation - ON**
1	X	X	X	Luminance horizontal contiguous 5-continuous code motion compensation – OFF

YMDM Initial value: 0; Setting range: 0 to 1
Sets movement detection for luminance motion compensation.

Table-R2-3-7(2) Motion Detection Setting for Luminance Motion Compensation

YMDM	Detection setting
0	**Detection setting weak**
1	Detection setting strong

AYMOFF[3:1] Initial value: 000; Setting range: Refer to Tables R2-3-7 (2), (3).
Sets auto mode motion compensation ON/OFF of luminance signal field recursive noise reduction detection noise.
Validates in auto mode 1 (AMM = 0) noise follow-up state or in auto mode 2 (AMM = 1) fixed register state B2/ noise follow-up state. (The same operation as of YMOFF[3:1].)

Table R2-3-7 (3) Auto Mode 1 Motion Compensation Setting (Valid at NRAUTO = 1)

AYMOFF[*]	Noise follow-up state motion compensation
0	**Motion compensation ON**
1	Motion compensation OFF

* is 1 to 3.

Table R2-3-7 (4) Auto Mode 2 Motion Compensation Setting (Valid at NRAUTO = 1)

AYMOFF[*]	Fixed register state B2/Noise follow-up state luminance mode
0	**Motion compensation ON**
1	Motion compensation OFF

* is 1 to 3.

CMOFF[4:0] Initial value: 0_0000; Setting range: Refer to Table R2-3-7 (5).
Sets motion compensation ON/OFF of chrominance signal field recursive noise reduction detection noise.

CMY Initial value: 0; Setting range: Refer to Table R2-3-7 (5).
Sets chrominance motion compensation mode.
Allows to use motion compensation for the chrominance signal also for the luminance signal.

Table R2-3-7 (5) Chrominance Motion Compensation ON/OFF Setting

CMOFF					CMY	Chrominance motion level detection noise motion compensation
[4]	[3]	[2]	[1]	[0]		
X	X	X	X	**0**	X	**Chrominance horizontal contiguous motion level compensation - ON**
X	X	X	X	1	X	Chrominance horizontal contiguous motion level compensation - OFF
X	X	X	**0**	X	0	Luminance horizontal contiguous motion level compensation - OFF
					1	**Luminance horizontal contiguous motion level compensation - ON**
X	X	X	1	X	X	Luminance horizontal contiguous motion level compensation - OFF
X	X	**0**	X	X	0	Luminance horizontal contiguous 3-continuous code motion compensation - OFF
					1	**Luminance horizontal contiguous 3-continuous code motion compensation - ON**
X	X	1	X	X	X	Luminance horizontal contiguous 3-continuous code motion compensation - OFF
X	**0**	X	X	X	0	Luminance horizontal contiguous 4-continuous code motion compensation - OFF
					1	**Luminance horizontal contiguous 4-continuous code motion compensation - ON**
X	1	X	1	X	X	Luminance horizontal contiguous 4-continuous code motion compensation - OFF
0	X	X	X	X	0	Luminance horizontal contiguous 5-continuous code motion compensation - OFF
					1	**Luminance horizontal contiguous 5-continuous code motion compensation - ON**
1	X	X	X	X	X	Luminance horizontal contiguous 5-continuous code motion compensation - OFF

PYST[1:0] Initial value: 0; Setting range: 0 to 3

Sets a noise detection luminance saturation level of the valid data area.

Sets a level that does not perform noise judgment in noise detection in a valid data area.

Table R2-3-7(6) Setting of a Noise Detection Luminance Saturation Level of Valid Data Area

PYST[1:0]	Luminance saturation level
0h	**No saturation level**
1h	E0h
2h	C0h
3h	80h

2.3.8 Noise State Detection Setting

SUB_ADDRESS = 53h(W/R): Luminance noise state 1 detection setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	YAH1	(Reserved)	YAVR1					
			5	4	3	2	1	0
SUB_ADDRESS = 54h(W/R): Chrominance noise state 1 detection setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	CAH1	(Reserved)	CAVR1					
			5	4	3	2	1	0
SUB_ADDRESS = 55h(W/R): Luminance noise state 2 detection setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	YAH2	YAVR2						
		6	5	4	3	2	1	0
SUB_ADDRESS = 56h(W/R): Chrominance noise state 2 detection setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	CAH2	CAVR2						
		6	5	4	3	2	1	0

YAVR1[5:0] Initial value: 00_0000; Setting range: 00_0000 to 11_1111
Sets increase direction decision average value level of luminance noise state 1.
Becomes the decision level when the noise level is in the increase direction.
YAVR1[5:4] is an integral part and YAVR1[3:0] is a decimal part.
Make sure to set a value smaller than YAVR2[6:0].

YAH1 Initial setting: 0; Setting range: 0 to 1
Sets decrease direction decision average value level hysteresis coefficient of luminance noise state 1.
The decision level of the noise level in decreasing direction is set by (YAVR1[5:0]) × (Coefficient).

CAVR1[5:0] Initial value: 00_0000; Setting range: 00_0000 to 11_1111
Sets increase direction decision average value level of chrominance noise state 1.
Becomes the decision level of the noise level in increasing direction.
CAVR1[5:4] is an integral part and CAVR1[3:0] is decimal part.
Make sure to set the value smaller than CAVR2[6:0].

CAH1 Initial value: 0; Setting range: 0 to 1
Sets decrease direction decision average value level hysteresis coefficient of chrominance noise state 1.
The decision level of the noise level in the decreasing direction is set by (CAVR1[5:0]) × (Coefficient)

YAVR2[6:0] Initial value: 111_1111; Setting range: 000_0000 to 111_1111
Sets increase direction decision average value level of luminance noise state 2.
Becomes the decision level of the noise level in increasing direction.
YAVR2[6:4] is an integral part and YAVR2[3:0] is a decimal part.
Make sure to set the value larger than YAVR1[5:0].

YAH2 Initial value: 0; Setting range: 0 to 1
Sets decrease direction decision average value level hysteresis coefficient of luminance noise state 2.
The decision level of the noise level in decreasing direction is set by (YAVR2[6:0]) × (Coefficient).

CAVR2[6:0] Initial value: 111_1111; Setting range: 000_0000 to 111_1111
Sets increase direction decision average value level of chrominance noise state 2.
Becomes the decision level of the noise level in increasing direction.
CAVR2[6:4] is an integral part and CAVR2[3:0] is a decimal part.
Make sure to set the value larger than CAVR1[5:0].

CAH2 Initial value: 0; Setting range: 0 to 1
Sets decrease direction decision average value level hysteresis coefficient of chrominance noise state 2.
The decision level of the noise level in decreasing direction is set by (CAVR2[6:0]) × (Coefficient)

Table R2-3-8 (1) Luminance Noise State 1 Decision Level Conditions

Level condition	State
YAVRO[6:0] > YAVR1[5:0]	YDTO1 = 0 → 1
YAVRO[6:0] ≤ (YAVR1[5:0] × Coefficient)	YDTO1 = 1 → 0

Table R2-3-8 (2) Chrominance Noise State 1 Decision Level Conditions

Level condition	State
CAVRO[6:0] > CAVR1[5:0]	CDTO1 = 0 → 1
CAVRO[6:0] ≤ (CAVR1[5:0] × Coefficient)	CDTO1 = 1 → 0

Table R2-3-8 (3) Luminance Noise State 2 Decision Level Conditions

Level condition	State
YAVRO[6:0] > YAVR2[6:0]	YDTO2 = 0 → 1
YAVRO[6:0] ≤ (YAVR2[6:0] × Coefficient)	YDTO2 = 1 → 0

Table R2-3-8 (4) Chrominance Noise State 2 Decision Level Conditions

Level condition	State
CAVRO[6:0] > CAVR2[6:0]	CDTO2 = 0 → 1
CAVRO[6:0] ≤ (CAVR2[6:0] × Coefficient)	CDTO2 = 1 → 0

Table R2-3-8 (5) Luminance Noise State 1 Hysteresis Coefficient

YAH1	Noise decrease direction switching coefficient
0	3/4
1	7/8

Table R2-3-8 (6) Chrominance Noise State 1 Hysteresis Coefficient

CAH1	Noise decrease direction switching coefficient
0	3/4
1	7/8

Table R2-3-8 (7) Luminance Noise State 2 Hysteresis Coefficient

YAH2	Noise decrease direction switching coefficient
0	3/4
1	7/8

Table R2-3-8 (8) Chrominance Noise State 2 Hysteresis Coefficient

CAH2	Noise decrease direction switching coefficient
0	3/4
1	7/8

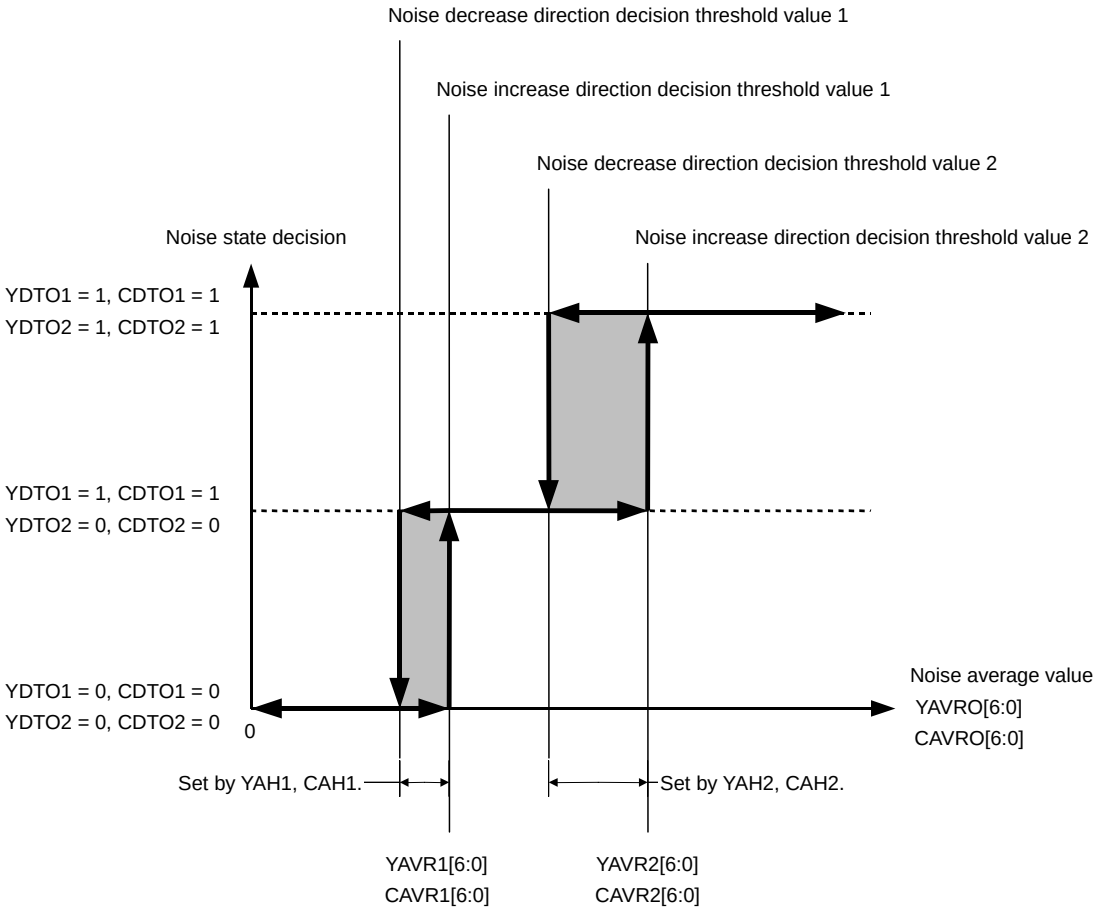


Figure R2-3-8 Noise State Decision Transition Diagram

2.3.9 Noise Read Data Select Setting

SUB_ADDRESS=57h(W/R): Noise read data select setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	DTPSL	(Reserved)	NRDTP				CNAMS	YNAMS
			3	2	1	0		

YNAMS Initial value: 0; Setting range: 0 to 1
Sets luminance signal noise data read selection.
Selects a value that is reflected on YAVRO[6:0] and YMAXO[5:0].

Table R2-3-9 (1) Luminance Signal Noise Data Read Select Setting

YNAMS	YAVRO [6:0], YMAXO[5:0]
0	**8 frames average**
1	1 frame detection

CNAMS Initial value: 0; Setting range: 0 to 1
Sets chrominance signal noise data read selection.
Selects a value that is reflected on CAVRO[6:0] and CMAXO[5:0].

Table R2-3-9 (2) Chrominance Signal Noise Data Read Select Setting

CNAMS	CAVRO [6:0], CMAXO[5:0]
0	**8 frames average**
1	1 frame detection

NRDTP[3:0] Initial value: 0000; Setting range: 0001 to 1111
Sets auto mode noise detection position.

DTPSL Initial value: 0; Setting range: 0 to 1
Sets noise detection reference position.

Table R2-3-9 (3) Noise Detection Reference Position Setting

DTPSL	Noise detection reference position
0	**1st line after valid data end line**
1	2nd line after valid data end line

2.3.10 Noise Level Read Registers (read only)

SUB_ADDRESS = 58h(R): Luminance noise average value level read register								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	YDTO1	YAVRO						
		6	5	4	3	2	1	0
SUB_ADDRESS = 59h(R): Chrominance noise average value level read register								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	CDTO1	CAVRO						
		6	5	4	3	2	1	0
SUB_ADDRESS = 5Ah(R): Luminance noise maximum value level read register								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	YDTO2	0	0	YMAXO				
				4	3	2	1	0
SUB_ADDRESS = 5Bh(R): Chrominance noise maximum value level read register								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	CDTO2	0	0	CMAXO				
				4	3	2	1	0
SUB_ADDRESS = 5Ch(R): Luminance base noise average value level read register								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	YBDTO	YBAVRO						
		6	5	4	3	2	1	0
SUB_ADDRESS = 5Dh(R): Chrominance base noise average value level read register								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	CBDTO	CBAVRO						
		6	5	4	3	2	1	0

YAVRO[6:0] Read value range: 000_0000 to 111_1111
Luminance noise level of 8 frames average (YNAMS = 0), or of 1 frame (YNAMS = 1), of noise absolute value average of lines detected at NRDTON = 1
Updated every frame. 7Fh is read out if the noise level exceeds 7Fh.
YAVRO[6:4] is an integral part and YAVRO[3:0] is a decimal part.

CAVRO[6:0] Read value range: 000_0000 to 111_1111
Chrominance noise level of 8 frames average (CNAMS = 0), or of 1 frame (CNAMS = 1), of noise absolute value average of lines detected at NRDTON = 1
Updated every frame. 7Fh is read out if the noise level exceeds 7Fh.
CAVRO[6:4] is an integral part and CAVRO[3:0] is a decimal part.

YDTO1 Read value range: 0 to 1
Luminance Noise Detection Flag
At NRDTON = 1, YDTO1 is set to “1” if YAVRO[6:0] > YAVR1[5:0] state continues in 4 frames.

CDTO1 Read value range: 0 to 1
Chrominance noise detection flag.
At NRDTON = 1, CDTO1 is set to “1” if CAVRO[6:0] > CAVR1[5:0] state continues in 4 frames.

YDTO2 Read value range: 0 to 1
Luminance noise detection flag.
At NRDTON = 1, YDTO2 is set to “1” if YAVRO[6:0] > YAVR2[6:0] state continues in 4 frames.
YDTO2 is fixed to “0” in the case of YAVR2[6:0] = 7Fh.

CDTO2 Read value range: 0 to 1
Chrominance noise detection flag.
At NRDTON = 1, CDTO2 is set to “1” if CAVRO[6:0] > CAVR2[6:0] state continues in 4 frames.
CDTO2 is fixed to “0” in the case of CAVR2[6:0] = 7Fh.

YMAXO[4:0] Read value range: 0_0000 to 1_1111
Luminance noise level of 8 frames average (YNAMS = 0), or of 1 frame (YNAMS = 1), of the noise maximum value of lines detected at NRDTON = 1.
Updated every frame. 3Fh is read out if the noise level exceeds 3Fh.

CMAXO[4:0] Read value range: 0_0000 to 1_1111
Chrominance noise level of 8 frames average (CNAMS = 0), or of 1 frame (CNAMS = 1), of the noise maximum value of lines detected at NRDTON = 1.
Updated every frame. 3Fh is read out if the noise level exceeds 3Fh.

YBAVRO[6:0] Read value range: 000_0000 to 111_1111
Luminance noise level of 8 frames average (YNAMS = 0), or of 1 frame (YNAMS = 1), of luminance base noise absolute value average of lines detected at NRDTON = 1
Updated every frame. 7Fh is read out if the noise level exceeds 7Fh.
YBAVRO[6:4] is an integral part and YBAVRO[3:0] is a decimal part.

CBAVRO[6:0] Read value range: 000_0000 to 111_1111
Chrominance noise level of 8 frames average (CNAMS = 0), or of 1 frame (CNAMS = 1), of chrominance base noise absolute value average of lines detected at NRDTON = 1
Updated every frame. 7Fh is read out if the noise level exceeds 7Fh.
CBAVRO[6:4] is an integral part and CBAVRO[3:0] is a decimal part.

YBDTO Read value range: 0 to 1
Luminance base noise detection flag.
At NRDTON = 1, YBDTO is set to “1” if YBAVRO[6:0] > YAVR1[5:0] state continues in 4 frames.

CBDTO Read value range: 0 to 1
Chrominance base noise detection flag.
At NRDTON = 1, CBDTO is set to “1” if CBAVRO[6:0] > CAVR1[5:0] state continues in 4 frames.

2.4 Output System Settings

2.4.1 Output Data Setting

SUB_ADDRESS=60h(W/R): Output data setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	CKEN	CKSL	CKINV	REFSL		(Reserved)	DOSEL	(Reserved)
				1	0			

DOSEL Initial value: 0; Setting range: 0 to 1
Sets the output format.

Table R2-4-1 (1) Output Format Mode Setting

DOSEL	Output data format
0	**16-bit output**
1	Same format for input and output

REFSL[1:0] Initial value: 00; Setting range: 00 to 11
Sets HREF pin output.
Selects and outputs any one of the horizontal reference signal, chrominance select signal, effective area signal, and field pulse signal.

Table R2-4-1 (2) HREF Pin Output Selection

REFSL		HREF pin output
[1]	[0]	
0	**0**	**Horizontal reference signal**
0	1	Chrominance select signal
1	0	Effective area signal
1	1	Field pulse signal

CKINV Initial value: 0; Setting range: Refer to Table R2-4-1 (3).
Sets CLKO output polarity.

CKSL Initial value: 0; Setting range: Refer to Table R2-4-1 (3)
Sets CLKO output selection.

CKEN Initial value: 0; Setting range: Refer to Table R2-4-1 (3).
Sets CLKO output enable.

Table R2-4-1 (3) CLKO Output Setting

CKEN	CKSL	CKINV	CLKO output
0	**X**	**X**	**Hi-Z**
1	0	0	IICLK
1	0	1	IICLK inverted
1	1	0	ICLK
1	1	1	ICLK inverted

* During 16-bit mode in input, IICLK = ICLK.

2.4.2 Sync. Signal Output Setting

SUB_ADDRESS=61h(W/R): Sync. signal output setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	(Reserved)	(Reserved)	(Reserved)	(Reserved)	(Reserved)	HREF INV	OHSINV	OVSINV

OVSINV Initial value: 0; Setting range: 0 to 1
Sets OVS output polarity.

Table-R2-4-2(1) OVS Polarity Setting

OVSINV	OVS Polarity
0	**Positive**
1	Negative

OHSINV Initial value: 0; Setting range: 0 to 1
Sets OHS output polarity.

Table-R2-4-2(2) OHS Polarity Setting

OHSINV	OHS Polarity
0	**Positive**
1	Negative

HREFINV Initial value: 0; Setting range: 0 to 1
Sets HREF output polarity.

Table R2-4-2(3) HREF Polarity Setting

HREFINV	HREF polarity
0	**Positive polarity**
1	Negative polarity

2.5 Other Image Adjustment Settings

2.5.1 Cross-Color Cancellation Setting

SUB_ADDRESS=5Eh (W/R): Cross-color cancellation setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	CCMM	CCYMS			CCMDT	CCMON	MEM411	CCON
		2	1	0				

SUB_ADDRESS=5Fh (W/R): Cross-color cancellation setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	DMCC	CCT	ACC		YCCNL			
			1	0	3	2	1	0

CCON Initial value: 0; Setting range: 0 to 1
Sets cross-color cancellation to ON/OFF.

Table R2-5-1(1) Cross-Color Cancellation ON/OFF Setting

CCON	Cross-color cancellation
0	**OFF**
1	ON

MEM411 Initial value: 0; Setting range: 0 to 1
Sets a memory format.
When operating the cross-color cancellation in 625 line mode, be sure to set this bit to 1.

Table R2-5-1(2) Memory Format Setting

MEM411	Memory Format
0	**4:2:2**
1	4:1:1

CCMON Initial value: 0; Setting range: 0 to 1
Sets cross-color cancellation movement compensation to ON/OFF.

Table R2-5-1(3) Cross-Color Cancellation Movement Compensation ON/OFF Setting

CCMON	Movement compensation
0	**OFF**
1	ON

CCMDT Initial value: 0; Setting range: 0 to 1
Sets cross-color cancellation movement detection.

Table R2-5-1(4) Cross-Color Cancellation Movement Detection

CCMDT	Movement detection
0	**Weak**
1	Strong

CCYMS[2:0] Initial value: 0; Setting range: 000 to 111
Sets a cross-color cancellation movement detection level.

CCMM Initial value: 0; Setting range: 0 to 1
Sets a cross-color cancellation movement compensation mode.

Table R2-5-1(5) Cross-Color Cancellation Movement Compensation Mode Setting

CCMDT	Movement compensation mode
0	**Cross-color level mask**
1	No cross-color level mask

YCCNL[3:0] Initial value: 0; Setting range: 0000 to 1111
Sets a cross-color cancellation 0° phase movement detection level.
Operation is enabled in 525 line mode and the memory format is 4:1:1.

ACC[1:0] Initial value: 0; Setting range: (see Table R2-5-1(6))
Sets cross-color cancellation to ON/OFF automatically.

Table R2-5-1(6) Cross-Color Cancellation Auto ON/OFF Setting

ACC		Cross-color cancellation auto ON/OFF setting
[1]	[0]	
0	**0**	Cross-color cancellation **auto ON/OFF disabled**
0	1	If YDTO1 = 1, cross-color cancellation OFF
1	1	If YDTO2 = 1, cross-color cancellation OFF

CCT Initial value: 0; Setting range: 0 to 1
Sets a cross-color cancellation test mode.

Table R2-5-1(7) Cross-Color Cancellation Test Mode Setting

CCT	Test mode
0	Normal mode
1	Test mode (luminance is fixed to 80h)

DMCC Initial value: 0; Setting range: 0 to 1
Sets a cross-color cancellation demonstration mode.

Table R2-5-1(8) Cross-Color Cancellation Demonstration Mode Setting

DMCC	Demonstration mode
0	Normal mode
1	Demonstration mode (Left: OFF, Right: ON)

2.5.2 Edge-Adaptive 2D Noise Reduction Settings

SUB_ADDRESS=64h (W/R): Sets edge-adaptive 2D noise reduction.								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	ODEMO		YECON	CLPFM	CLPFON	YHLPFM	YLPFM	YLPFON
	1	0						
SUB_ADDRESS=65h(W/R): Sets luminance edge-adaptive 2D noise reduction.								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	AYLPF		(Reserved)	YED				
	2	1		4	3	2	1	0
SUB_ADDRESS=66h(W/R): Sets chrominance edge-adaptive 2D noise reduction.								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	ACLPF		(Reserved)	CED				
	2	1		4	3	2	1	0

YLPFON Initial value: 0; Setting range: 0 to 1

Sets luminance edge-adaptive 2D noise reduction ON/OFF.

Table R2-5-2(1) Luminance Edge-Adaptive 2D Noise Reduction ON/OFF Setting

YLPFON	Luminance edge-adaptive 2D noise reduction
0	**OFF**
1	ON

YLPFM Initial value: 0; Setting range: 0 to 1

Sets luminance edge-adaptive 2D noise reduction.

Table R2-5-2(2) Luminance Edge-Adaptive 2D Noise Reduction Setting

YLPFM	Luminance edge-adaptive 2D noise reduction
0	**Filter weak**
1	Filter strong

YHLPFM Initial value: 0; Setting range: 0 to 1

Sets luminance edge-adaptive 2D noise reduction horizontal direction.

Table R2-5-2(3) Luminance Edge-Adaptive 2D Noise Reduction Horizontal Direction Setting

YHLPFM	Luminance edge-adaptive 2D noise reduction
0	**3-pixel filter**
1	5-pixel filter

CLPFON Initial value: 0; Setting range: 0 to 1

Sets chrominance edge-adaptive 2D noise reduction ON/OFF.

Table R2-5-2(4) Chrominance Edge-Adaptive 2D Noise Reduction ON/OFF Setting

CLPFON	Chrominance edge-adaptive 2D noise reduction
0	**OFF**
1	ON

CLPFM Initial value: 0; Setting range: 0 to 1
Sets the chrominance edge-adaptive 2D noise reduction .

Table R2-5-2(5) Chrominance Edge-Adaptive 2D Noise Reduction Setting

CLPFM	Chrominance edge-adaptive 2D noise reduction
0	**Filter weak**
1	Filter strong

YECON Initial value: 0; Setting range: 0 to 1
Sets luminance edge correction ON/OFF.

Table R2-5-2(6) Luminance Edge Correction ON/OFF Setting

LTION	Luminance edge correction
0	**OFF**
1	ON

ODEMO[1:0] Initial value: 00; Setting range: (Refer to Table R2-5-1(5).)
Sets edge-adaptive 2D noise reduction function demonstration mode ON/OFF.

Table R2-5-2(6) Demonstration Mode ON/OFF Setting

ODEMO		Left side of screen	Right side of screen
[1]	[0]		
0	**0**	**2D noise reduction setting value**	**2D noise reduction setting value**
0	1	2D noise reduction stop	2D noise reduction setting value
1	0	Edge-adaptation stop	2D noise reduction setting value

YED[4:0] Initial value: 0_0000; Setting range: 0_0000 to 1_1111
Sets the luminance edge-adaptive 2D noise reduction edge adaptation level.

AYED Initial value: 0; Setting range: 0 to 1
Sets luminance edge-adaptive 2D noise reduction edge adaptation level auto setting ON/OFF.

Table R2-5-2(7) Luminance Edge Adaptation Level Auto Setting ON/OFF Setting

AYED	Luminance edge adaptation level auto setting ON/OFF setting
0	**OFF (YED[4:0])**
1	ON (if YDTO2 = 1, noise level is set)

AYLPF[2:1] Initial value: 00; Setting range: See Table R2-5-2(8).
Sets luminance 2D noise reduction ON/OFF.

Table R2-5-2(8) Luminance Edge-Adaptive 2D Noise Reduction Auto ON/OFF Setting

AYLPF		Luminance edge-adaptive 2D noise reduction auto ON/OFF setting
[2]	[1]	
0	**0**	**Stop luminance 2D noise reduction auto ON/OFF.**
X	1	Noise reduction ON when YDTO1 = 1.
1	0	Noise reduction ON when YDTO2 = 1.

CED[4:0] Initial value: 0_0000; Setting range: 0_0000 to 1_1111
Sets a chrominance noise reduction edge adaptive level.

ACED Initial value: 0; Setting range: 0 to 1
Sets an adaptive level of chrominance edge adaptive 2D noise reduction edge to ON/OFF automatically.

Table R2-5-2(9) Chrominance Edge Adaptive Level Auto ON/OFF Setting

ACED	Chrominance edge adaptive level auto ON/OFF setting
0	**OFF (CED[4:0])**
1	ON (if CDTO2 = 1, noise level is set)

ACLPF[2:1] Initial value: 00; Setting range: See Table R2-5-2(10).
Sets to chrominance edge adaptive 2D noise reduction to ON/OFF automatically.

Table R2-5-2(10) Chrominance Edge-Adaptive 2d Noise Reduction Auto ON/OFF Setting

ACLPF		Chrominance edge-adaptive 2D noise reduction auto ON/OFF setting
[2]	[1]	
0	**0**	Chrominance edge-adaptive 2D noise reduction **auto ON/OFF disabled**
X	1	Chrominance 2D noise reduction ON when CDTO1 = 1
1	0	Chrominance 2D noise reduction ON when CDTO2 = 1

2.6 Other Settings

2.6.1 Other Mode Settings

SUB_ADDRESS = 72h(W/R): Other settings								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	RLTG	(Reserved)	(Reserved)	PAOS	(Reserved)	OEINV	OUTDS	PASS

PASS Initial value: 0; Setting range: 0 to 1

Sets data through mode.

The input pin is directly connected to the output pin. At this time, there is a delay generated equal to the time it takes for the output data to pass through the internal circuitry.

Table R2-6-1 (1) Data Through Mode Setting

PASS	Mode
0	**Normal operation**
1	Data through

OUTDS Initial value: 0; Setting range: 0 to 1

Sets to disable forcibly all outputs.

Table R2-6-1 (2) All Outputs Disable Setting

OUTDS	All output pins
0	**Dependent on other settings (OE, INT)**
1	Disable

OEINV Initial value: 0; Setting range: 0 to 1

Sets OE input pin polarity inversion.

Table R2-6-1(3) OE Input Pin Polarity Inversion Setting

OEINV	OE input pin
0	**OE = 0: Output data disable**
1	OE = 1: Output data disable

PAOS Initial value: 0; Setting range: 0 to 1

Sets a starting offset of vertical valid data.

Table R2-6-1(4) Vertical Valid Data Starting Offset Setting

PAOS	Offset
0	**No offset**
1	2H (INPR = 0)/4H (INPR = 1)

RLTG Initial value: 0; Setting range: 0 to 1

Sets the register setting synchronous mode. Normally 0; used only for tests.

Table R2-6-1 (5) Register Set Mode Setting

RLTG	Data reflection
0	**Synchronized to IVS and OVS**
1	When I^2C-bus is set

2.6.2 Test Mode Setting

SUB_ADDRESS = 70h (W/R): Test mode setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	TST							
	7	6	5	4	3	2	1	0
SUB_ADDRESS = 71h (W/R): Test mode setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	TST							
	15	14	13	12	11	10	9	8
SUB_ADDRESS = 7Ah (W/R): Test mode setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	TST							
	7	6	5	4	3	2	1	0

TST [7:0] Initial value: 0000_0000; Setting range: 0000_0000 to 1111_1111
TST [15:8] Initial value: 0000_0000; Setting range: 0000_0000 to 1111_1111
TST [23:16] Initial value: 0000_0000; Setting range: 0000_0000 to 1111_1111
Sets test mode:
Normally fixed to 0000_0000.

2.6.3 Synch. Signal Generation Adjustment Setting (for Demonstration)

SUB_ADDRESS=78h (W/R): Output system memory control mode setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	(Reserved)	(Reserved)	(Reserved)	(Reserved)	(Reserved)	(Reserved)	HSSEL	ISYNC
SUB_ADDRESS=79h(W/R): OHS generation start position setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	SHSDL							
	7	6	5	4	3	2	1	0

ISYNC Initial value: 0; Setting range: 0 to 1
Sets the generation of an OVS/OHS internal Sync. signal.
* Since this is a setting for demonstration, normally set this bit to 0.

Table R2-6-3(1) Internal Sync. Signal Generation Setting

ISYNC	OVS, OHS output
0	**Input (IVS, IHS)-delay output**
1	Internally generated output

HSSEL Initial value: 0; Setting range: 0 to 1
Sets internally generated OHS composite Sync.
* Since this is a setting for demonstration, normally set this bit to 0.

Table R2-6-3(2) Internally Generated OHS Composite Sync Setting

HSSEL	OHS phase
0	**Horizontal Sync. signal**
1	Composite Sync

SHSDL[7:0] Initial value: 0011_1111; Setting range: 0000_0001 to 1111_1111
Set an OHS generation starting position of the internal Sync generator.
* Since this is a setting for demonstration, normally set this bit to 0.

2.6.4 Read NR Setting Values

SUB_ADDRESS = 73h(R): Luminance noise convergence level read register								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	RYLPF	0	RYNS					
			5	4	3	2	1	0
SUB_ADDRESS = 74h(R): Chrominance noise convergence level read register								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	RCLPF	RCCON	RCNS					
			5	4	3	2	1	0
SUB_ADDRESS = 75h(R): Luminance noise upper limit level read register								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	RYABN	RYNRM	RYNR OFF	RYLM				
				4	3	2	1	0
SUB_ADDRESS = 76h(R): Chrominance noise upper limit level read register								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	RCABN	RCNRM	RCNR OFF	RCLM				
				4	3	2	1	0
SUB_ADDRESS = 77h(R): Luminance motion compensation level read register								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	RYMOF			RNR2 OFF	RYMS			
	3	2	1		3	2	1	0

RYNS[5:0] Read value range: 00_0000 to 11_1111
Reads luminance noise convergence level of an internal operation status.
RYNS[5:0] = YNS[5:0] in case either the auto mode is not set (NRAUTO = 0) or the follow-up is not set in the auto mode (AYNS[0] = 0).

RCNS[5:0] Read value range: 00_0000 to 11_1111
Reads chrominance noise convergence level of an internal operation status.
RCNS[5:0] = CNS[5:0] in case either the auto mode is not set (NRAUTO = 0) or the follow-up is not set in the auto mode (ACNS[0] = 0).

RYLM[5:0] Read value range: 0_0000 to 1_1111
Reads luminance noise upper limit level of an internal operation status.
RYLM[4:0] = YLM[4:0] in case either the auto mode is not set (NRAUTO = 0) or the follow-up is not set in the auto mode (AYLM[0] = 0).

RYNROF Read value range: 0 to 1
Reads luminance NR On/Off switching signal of an internal operation status.
In case the auto mode is not set (NRAUTO = 0): RYNROFF = NROFF

RYNRM Read value range: 0 to 1
Reads luminance motion detection noise mode 0 switching signal of an internal operation status.
In case the auto mode is not set (NRAUTO = 0): RYNRM = YNRM

RYABN Read value range: 0 to 1
Reads luminance absolute noise mode switching signal of an internal operation status.
RYABN = YABN in case either the auto mode is not set (NRAUTO = 0) or the follow-up setting is not set in the auto mode (AYABN = 0).

RCLM[4:0] Read value range: 0_0000 to 1_1111
Reads chrominance noise upper limit level of an internal operation status.
RCLM[4:0] = YCM[4:0] in case either the auto mode is not set (NRAUTO = 0) or the follow-up is not set in the auto mode (ACLM[0] = 0).

RYNROFF Read value range: 0 to 1
Reads chrominance NR ON/OFF switching signal of an internal operation status.
In case the auto mode is not set (NRAUTO = 0): RCNROFF = NROFF

RYNRM Read value range: 0 to 1
Reads chrominance motion detection noise mode 0 switching signal of an internal operation status.
In case the auto mode is not set (NRAUTO = 0): RCNRM = CNRM

RYABN Read value range: 0 to 1
Reads chrominance absolute noise mode switching signal of an internal operation status.
RCABN = CABN in case either the auto mode is not set (NRAUTO = 0) or the follow-up is not set in the auto mode (ACABN = 0).

RNR2OFF Read value range: 0 to 1
Reads adaptive line correlation noise reduction ON/OFF signal of internal operation status.
If the auto mode is not set (NRAUTO = 0) or if A2OFF = 1 is not set in the auto mode, RNR2OFF = NR2OFF is set.

RYMS[3:0] Read value range: 0_0000 to 1_1111
Reads luminance motion compensation level of an internal operation status.
RYMS[4:0] = YMS[4:0] in case either the auto mode is not set (NRAUTO = 0) or the follow-up is not set in the auto mode (AYMS[0] = 0).

RYMOF[3:1] Read value range: 000 to 111
Reads luminance motion compensation ON/OFF switching signal of an internal operation status.
RYMOF[*] = YMOFF[*] in case either the auto mode is not set (NRAUTO = 0) or the follow-up is not set in the auto mode (AYMOFF[*] = 0). (* is 1 to 3.)

RYLPF Read value range: 0 to 1
Reads luminance edge-adaptive 2D noise reduction ON/OFF switching signal of an internal operation status.

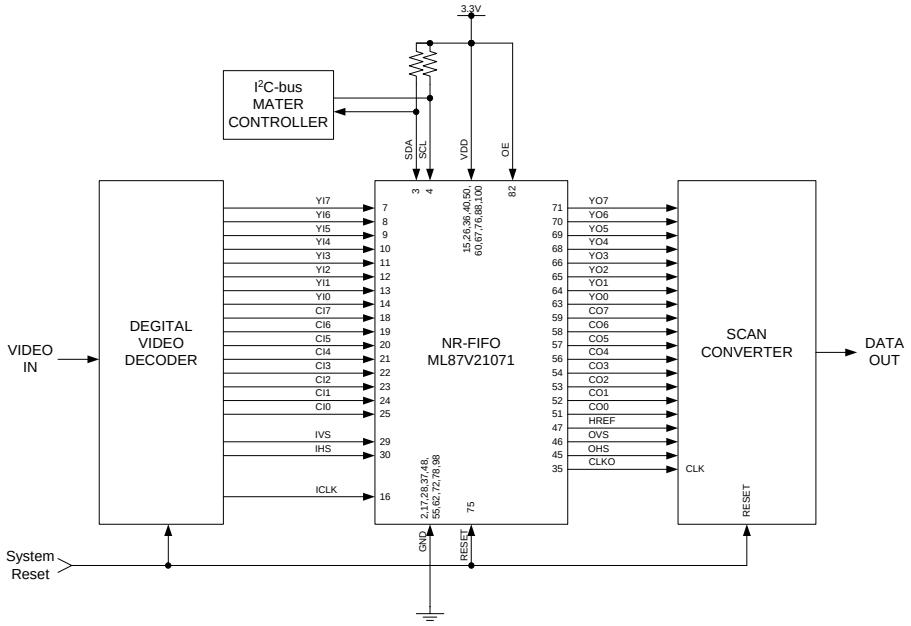
RCLPF Read value range: 0 to 1
Reads chrominance edge-adaptive 2D noise reduction ON/OFF switching signal of an internal operation status.

RCCON Read value range: 0 to 1
Reads cross-color cancellation ON/OFF switching signal of an internal operation status.

APPLICATION EXAMPLES

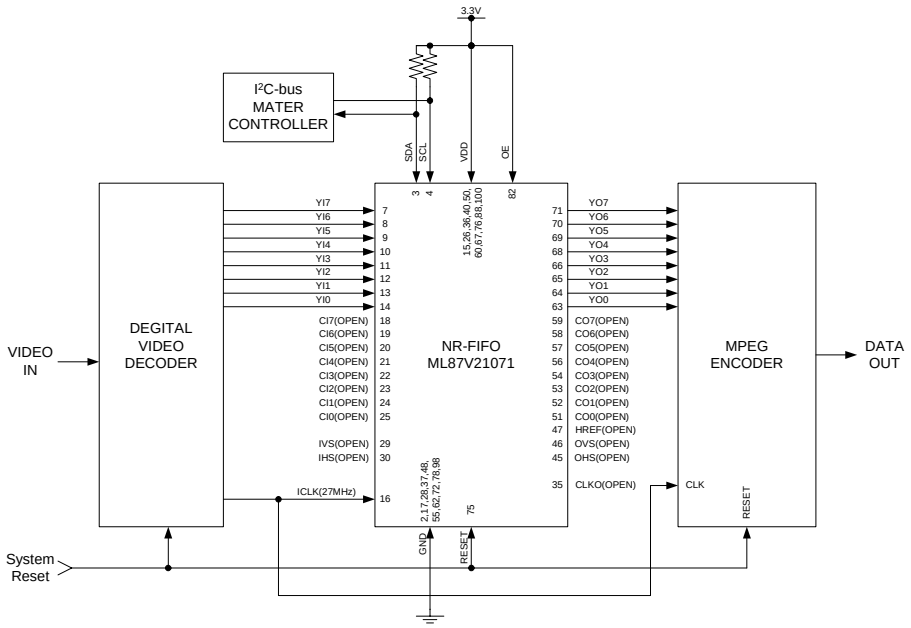
Application Example 1

Mode setting: Open
Slave address: 1011100
Input format: 16-bit YCbCr (Register setting: DISEL = 0, R656I = 0, DOSEL = 0)



Application Example 2

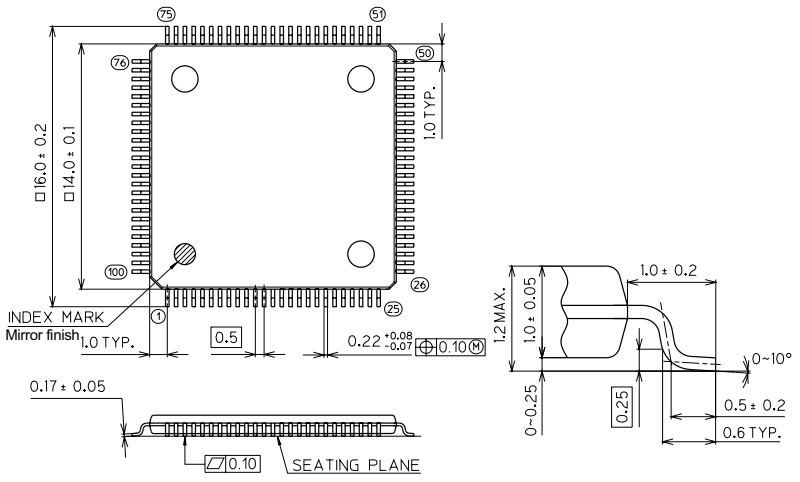
Mode setting: Open
Slave address: 1011100
Input format: ITU-R BT656 (Register setting: DISEL = 0, R656I = 1, DOSEL = 1)



PACKAGE DIMENSIONS

(Unit: mm)

TQFP100-P-1414-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.55 TYP.
Rev. No./Last Revised	4/Oct. 28, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL87V21071-01	Nov. 15, 2005	–	–	Preliminary edition 1

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