OKI Semiconductor

PEDL87V2105-02
Issue Date: Dec. 20, 2003

ML87V2105 Preliminary

Video Signal Noise Reduction IC with a Built-in 5.6 Mbit Frame Memory

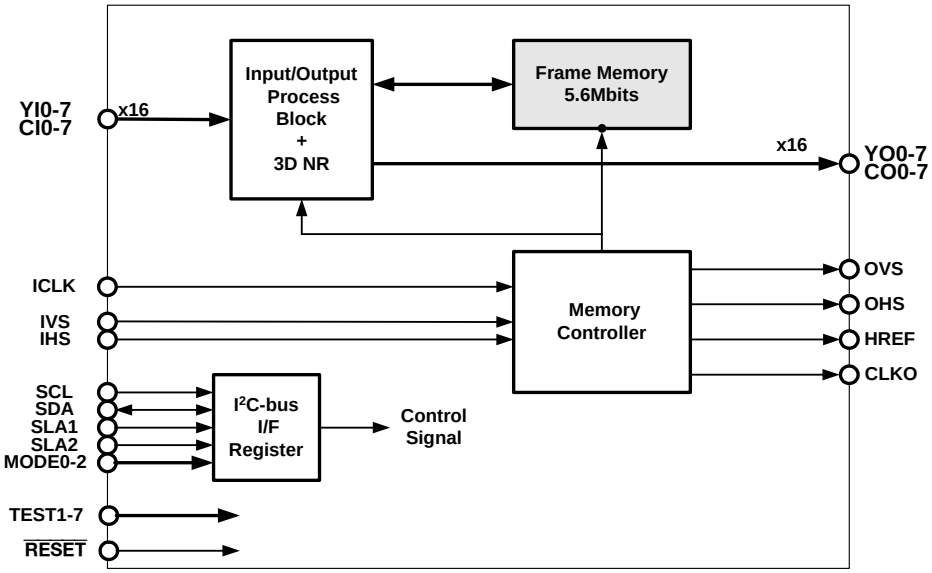
GENERAL DESCRIPTION

The ML87V2105 comprises a 5.6 Mbit frame memory, a noise reduction filter, and a memory controller to reduce frame-recursive 3D noise in video signals.
The motion adaptive noise reduction is performed between frames, between fields, or between lines, to reduce the afterimage particular to 3D noise reduction as far as possible, while achieving effective noise reduction.
The ML87V2105 also features an automatic noise reduction mode that automatically detects the noise level in the input video data to set the optimum noise reduction.
Because it is possible to select the same format for output as for input, the ML87V2105 can be introduced into an existing system, making it easy to achieve noise reduction.

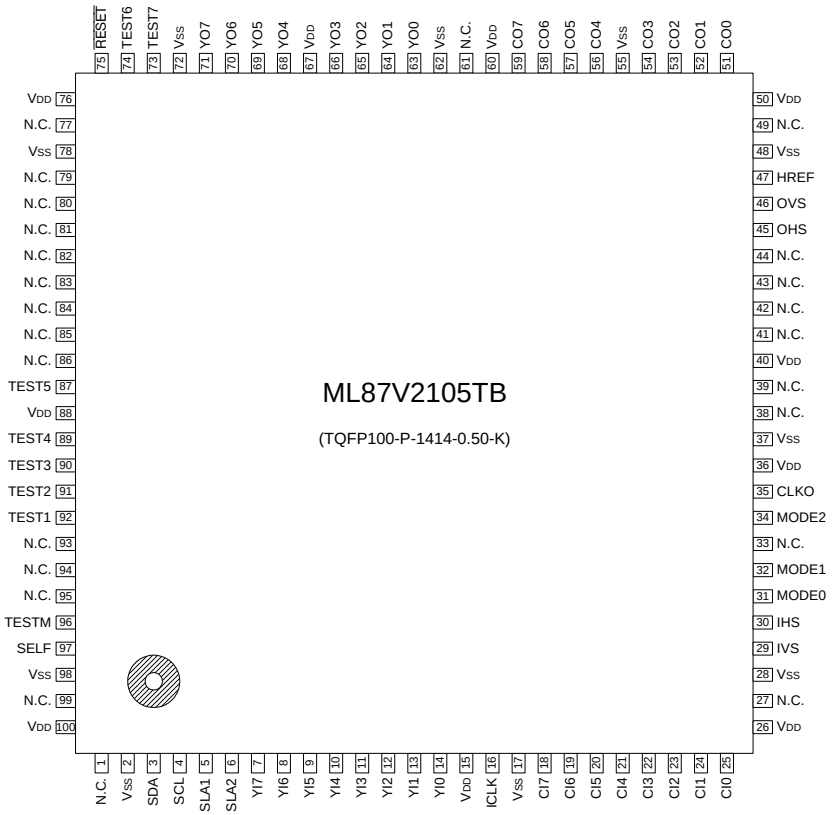
FEATURES

- Built-in memory:
  Frame memory (4:1:1 data equivalent) × 1 unit
- Maximum input and output operating frequencies (16 bits/8 bits, ITU-R BT.656):
  14.75/29.5 MHz
- Power supply voltage:
  3.3 V ± 0.3 V
- Input pin:
  LVCMOS (3.3 V)
- Output pin:
  LVCMOS (3.3 V)
- Input data format:
  YCbCr (8 bits (Y) + 8 bits (CbCr) (4:2:2) + Sync.): 16-bit mode
  YCbCr (8 bits (YCbCr) (4:2:2) + Sync.): 8-bit mode
  ITU-R BT.656 (8 bits (YCbCr)): ITU-R BT.656 mode
- Output data format:
  YCbCr (8 bits (Y) + 8 bits (CbCr) (4:2:2) + Sync.): 16-bit mode
  YCbCr (8 bits (YCbCr) (4:2:2) + Sync.): 8-bit mode (Selectable in 8-bit input mode)
  ITU-R BT.656 (8 bits (YCbCr)): ITU-R BT.656 mode (Selectable in input ITU-R BT.656)
- Serial bus:
  I^2C-bus interface: (Standard mode: 100 kbps/Fast mode: 400 kbps)
- Internal memory controller:
  Compatible with 625/50 Hz 2:1, 525/60 Hz 2:1
  Compatible horizontal effective pixels: 640 (525 line mode only), 720, 768
- Frame-recursive noise reduction:
  Frame-recursive noise detection and subtraction
  Auto mode noise reduction
- Still image output
  Selectable field still image, frame still image, or frame median still image.
  It is necessary to input the input sync signals as normal.
- Package:
  100 pin TQFP (TQFP100-P-1414-0.50-K)(ML87V2105TB)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



PIN DESCRIPTIONS

No.	Symbol	I/O	Pad Remarks	Pin Description
1	N.C.	—		Unused pin
2	V_{SS}	—		Ground
3	SDA	I/O	Schmitt(IN)/ OpenDrain(OUT)	I^2C-bus data pin
4	SCL	I	Schmitt	I^2C-bus clock pin
5	SLA1	I	Internal pull-down 50k	Slave address setting pin
6	SLA2	I	Internal pull-down 50k	Slave address setting pin
7	YI7	I		Luminance signal input pin bit 7 (MSB)
8	YI6	I		Luminance signal input pin bit 6
9	YI5	I		Luminance signal input pin bit 5
10	YI4	I		Luminance signal input pin bit 4
11	YI3	I		Luminance signal input pin bit 3
12	YI2	I		Luminance signal input pin bit 2
13	YI1	I		Luminance signal input pin bit 1
14	YI0	I		Luminance signal input pin bit 0 (LSB)
15	V_{DD}	—		Power supply 3.3 V
16	ICLK	I		Input system clock pin
17	V_{SS}	—		Ground
18	CI7	I	Internal pull-down 50k	Color difference signal input pin bit 7 (MSB)
19	CI6	I	Internal pull-down 50k	Color difference signal input pin bit 6
20	CI5	I	Internal pull-down 50k	Color difference signal input pin bit 5
21	CI4	I	Internal pull-down 50k	Color difference signal input pin bit 4
22	CI3	I	Internal pull-down 50k	Color difference signal input pin bit 3
23	CI2	I	Internal pull-down 50k	Color difference signal input pin bit 2
24	CI1	I	Internal pull-down 50k	Color difference signal input pin bit 1
25	CI0	I	Internal pull-down 50k	Color difference signal input pin bit 0 (LSB)
26	V_{DD}	—		Power supply 3.3 V
27	N.C.	—		Unused pin
28	V_{SS}	—		Ground
29	IVS	I	Schmitt pull-down 50k	Input system vertical sync signal input pin
30	IHS	I	Schmitt internal pull-down 50k	Input system horizontal sync signal input pin
31	MODE0	I	Internal pull-down 50k	Mode setting pin – bit 0
32	MODE1	I	Internal pull-down 50k	Mode setting pin – bit 1
33	N.C.	—		Unused pin
34	MODE2	I	Internal pull-down 50k	Mode setting pin – bit 2
35	CLKO	O/(I)	Internal pull-down 50k	Clock output (I^2C-bus control possible)
36	V_{DD}	—		Power supply 3.3 V
37	V_{SS}	—		Ground
38	N.C.	—		Unused pin
39	N.C.	—		Unused pin

No.	Symbol	I/O	Pad Remarks	Pin Description
40	V_{DD}	—		Power supply 3.3 V
41	N.C.	—		Unused pin
42	N.C.	—		Unused pin
43	N.C.	—		Unused pin
44	N.C.	—		Unused pin
45	OHS	O		Horizontal sync signal output pin
46	OVS	O		Vertical sync signal output pin
47	HREF	O		Data output horizontal reference signal output pin
48	V_{SS}	—		Ground
49	N.C.	—		Unused pin
50	V_{DD}	—		Power supply 3.3 V
51	CO0	O/(I)	Internal pull-down 50k	Color difference signal output pin – bit 0 (LSB)
52	CO1	O/(I)	Internal pull-down 50k	Color difference signal output pin – bit 1
53	CO2	O/(I)	Internal pull-down 50k	Color difference signal output pin – bit 2
54	CO3	O/(I)	Internal pull-down 50k	Color difference signal output pin – bit 3
55	V_{SS}	—		Ground
56	CO4	O/(I)	Internal pull-down 50k	Color difference signal output pin – bit 4
57	CO5	O/(I)	Internal pull-down 50k	Color difference signal output pin – bit 5
58	CO6	O/(I)	Internal pull-down 50k	Color difference signal output pin – bit 6
59	CO7	O/(I)	Internal pull-down 50k	Color difference signal output pin – bit 7(MSB)
60	V_{DD}	—		Power supply 3.3 V
61	N.C.	—		Unused pin
62	V_{SS}	—		Ground
63	YO0	O		Luminance signal output pin – bit 0 (LSB)
64	YO1	O		Luminance signal output pin – bit 1
65	YO2	O		Luminance signal output pin – bit 2
66	YO3	O		Luminance signal output pin – bit 3
67	V_{DD}	—		Power supply 3.3 V
68	YO4	O		Luminance signal output pin – bit 4
69	YO5	O		Luminance signal output pin – bit 5
70	YO6	O		Luminance signal output pin – bit 6
71	YO7	O		Luminance signal output pin – bit 7 (MSB)
72	V_{SS}	—		Ground
73	TEST7	I		Test input pin – bit 7 (1: test mode)
74	TEST6	I		Test input pin – bit 6 (1: test mode)
75	$\overline{\text{RESET}}$	I	Schmitt	System reset/input pin 0: System reset 1: Operation

No.	Symbol	I/O	Pad Remarks	Pin Description
76	V_{DD}	—		Power supply 3.3 V
77	N.C.	—		Unused pin
78	V_{SS}	—		Ground
79	N.C.	—		Unused pin
80	N.C.	—		Unused pin
81	N.C.	—		Unused pin
82	N.C.	—		Unused pin
83	N.C.	—		Unused pin
84	N.C.	—		Unused pin
85	N.C.	—		Unused pin
86	N.C.	—		Unused pin
87	TEST5	I	Internal pull-down 50k	Test input pin – bit 5 (1: test mode)
88	V_{DD}	—		Power supply 3.3 V
89	TEST4	I	Internal pull-down 50k	Test input pin – bit 4 (1: test mode)
90	TEST3	I	Internal pull-down 50k	Test input pin – bit 3 (1: test mode)
91	TEST2	I	Internal pull-down 50k	Test input pin – bit 2 (1: test mode)
92	TEST1	I	Internal pull-down 50k	Test input pin – bit 1 (1: test mode)
93	N.C.	—		Unused pin
94	N.C.	—		Unused pin
95	N.C.	—		Unused pin
96	TESTM	I	Internal pull-down 50k	Memory test input pin (1: test mode)
97	SELF	I	Internal pull-down 50k	Self refresh setting pin (0: Self refresh stopped, 1: Self refresh operated)
98	V_{SS}	—		Ground

Notes: Keep the test mode pins fixed to 0 or leave them open.
CL0 to CL7 and CLK0 are configured as inputs only in the test mode.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta = 25°C	–0.5 to + 4.6	V
Input pin voltage	V_I	Ta = 25°C	–0.5 to V_{DD}+0.5≦4.6	V
Output pin short-circuit current	I_{OS}	Ta = 25°C	50	mA
Power dissipation	P_D	Ta = 25°C	1	W
Operating temperature	T_{opr}	—	0 to 70	°C
Storage temperature	T_{stg}	—	–50 to + 150	°C

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	3.0	3.3	3.6	V
Power supply voltage	V_{SS}	0	0	0	V
Operating temperature	Ta	0	—	70	°C

Pin Capacitance

(V_{CC} = 3.3 V ± 0.3 V, f = 1 MHz, Ta = 25°C)

Parameter	Symbol	Min.	Max.	Unit
Input capacitance	C_i	—	5	pF
Input/output capacitance (CO0 to CO7, CLK0)	C_{io1}	—	10	pF
Input/output capacitance (SDA)	C_{io2}	—	10	pF
Output capacitance (YO0 to YO7, OVS, OHS, HREF)	C_o	—	10	pF

DC Characteristics

(Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
H level input voltage	V_{IH}	—	V_{DD} x 0.7	V_{DD}+0.3	V
L level input voltage	V_{IL}	—	–0.3	V_{DD} x 0.3	V
Schmitt trigger threshold voltage (SDA, SCL, IVS, IHS, $\overline{RESET}$)	V_{t+}	—	V_{DD} x 0.25	V_{DD} x 0.75	V
Schmitt trigger threshold voltage (SDA, SCL, IVS, IHS, $\overline{RESET}$)	V_{t-}	—	V_{DD} x 0.1	—	V
Hysteresis voltage width	V_h	—	0.1	—	V
H level input current (pull-down)	I_{IH}	50 kΩ Pull Down	20	200	µA
Input leakage current	I_{IL}	TTL	–10	10	µA
H level output voltage (other than SDA)	V_{OH}	I_{OH} = –4 mA	2.4	V_{DD}	V
L level output voltage (other than SDA)	V_{OL}	I_{OL} = 4 mA	0	0.4	V
L level output voltage (N-Ch.OD) (SDA)	V_{OOL}	I_{OL} = 4 mA	0	0.4	V
Output leakage current	I_{OL}	$0 \le V_{out} \le V_{DD}$ Output disabled	–10	10	µA
Supply current (during operation)	I_{DD1}	ICLK: 29.5 MHz Output disabled	—	80	mA
Supply current (during standby)	I_{DD2}	Input pin = V_{IL}	—	5	mA

AC Characteristics

(Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
ICLK clock cycle time	t_{ICLK}	16-bit input mode	66	—	ns
ICLK clock cycle time	t_{ICLK}	8-bit input mode ITU-R BT.656 mode	33	—	ns
ICLK clock duty ratio	dt_{ICLK}	—	40	60	%
ICLK input set-up time	t_{IISU}	—	5	—	ns
ICLK input hold time	t_{IIH}	—	3	—	ns
ICLK output delay time	t_{IOD}	C_L = 30 pF	5	25	ns
CLKO delay time	t_{CKD}	C_L = 30 pF (IICLK output)	2	25	ns
		C_L = 30 pF (ICLK output)	2	20	ns
Data through time	t_{DIDO}	C_L = 30 pF	5	20	ns

*1: ( ) indicates the input internal system clock cycle.

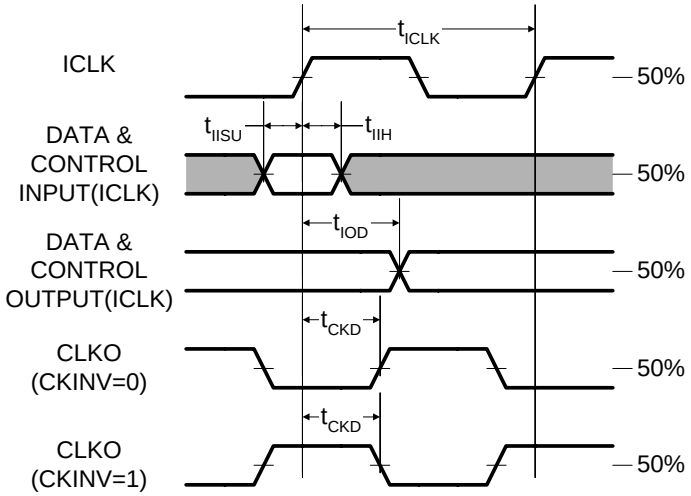
Note 1: Measurement conditions
Output comparison level: $V_{OH} = V_{DD}/2$, $V_{OL} = V_{DD}/2$
Input voltage level: V_{IH} = 3.0 V, V_{IL} = 0.0 V

Note 2: .When writing input data to the memory, compensation is applied from the second input system vertical synchronization signal when V_{DD} reaches 3.0 V after the power is turned on, and when $\overline{RESET}$ = 1. (Due to memory initialization, the first data for the first field is not compensated.)

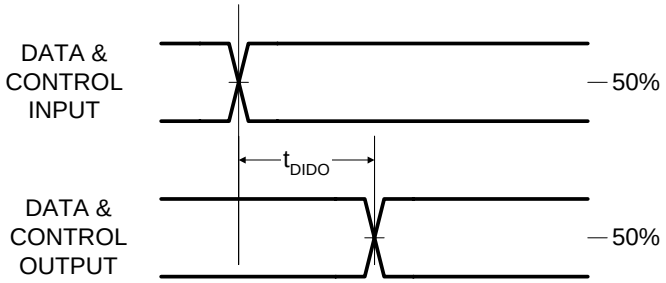
Note 3: .When reading output data from the memory, compensation is applied from the second output system vertical synchronization signal when V_{DD} reaches 3.0 V after the power is turned on, and when $\overline{RESET}$ = 1. (Due to memory initialization, the first data for the first field is not compensated.)

INPUT/OUTPUT TIMING

1. ICLK input/output timing



2. Data through mode input/output timing



FUNCTIONAL DESCRIPTION

1 Signal Processing

The ML87V2105 generates memory control signals from the input vertical and horizontal sync signals (IVS and IHS or SAV and EAV), reads and writes the frame memory data, and performs noise reduction processing on input and memory data to achieve 3D noise reduction.

1.1 Memory Control

From the IVS and IHS or SAV and EAV sync signals, this IC creates memory control signals for video signals that meet the conditions set forth in Table F1-1. It then writes input data to the frame memory and reduces frame-recursive noise.

Table F1-1 Compatible Input Modes

Vertical mode	Valid lines per field	Input data sampling frequency (MHz)	Standard pixels per line	Valid horizontal pixels
625/50Hz 2:1	288	13.5	864	720
		14.75	944	768
525/60Hz 2:1	243	13.5	858	720
		12.272727	780	640
		14.31818	910	768

1.1.1 Input Control Mode Settings

This IC offers a choice of six input control modes, shown below, which can be selected by setting either the external setting pin mode (IRMON = 0 (SUB:40h–bit [7]) or internal register mode (IRMON = 1).

Table F1-1-1 (1) Input/Output Control Mode Setting Allocation

IRMON	VMD		HMD	
	[0]	[1]	[0]	[1]
0	MODE 0 (External pin)	SUB:40h-bit[1]	MODE 1 (External pin)	SUB:40h-bit[3]
1	SUB:40h-bit[0]	SUB:40h-bit[1]	SUB:40h-bit[2]	SUB:40h-bit[3]

Table F1-1-1 (2) Input Control Mode Settings

VMD		HMD		Vertical mode	Number of valid lines	Standard clock frequency f_{ICLK} * [MHz]	Standard pixels per line	Valid horizontal pixels
[0]	[1]	[0]	[1]					
0	0	0	0	625/50 Hz 2:1	288	13.5/27	864	720
1	0	0	0	525/60 Hz 2:1	243	13.5/27	858	720
0	0	1	0	625/50 Hz 2:1	288	14.75/29.5	944	768
1	0	1	0	525/60 Hz 2:1	243	12.272727/ 24.545454	780	640
0	0	0	1	625/50 Hz 2:1	288	14.75/29.5	944	768
1	0	0	1	525/60 Hz 2:1	243	14.31818/ 28.63636	910	768
Other than above				Test modes (Not settable)				

The input system internal clock frequency f_{IICLK} is as follows:
Input 16-bit mode: $f_{IICLK} = f_{ICLK}$
Input 8-bit mode/ITU-R BT.656 mode: $f_{IICLK} = f_{ICLK}/2$

1.1.2 Input System Field Detection

The IC input data field is detected from the phase of IVS and IHS to generate the input field pulse (IF) which controls the internal frame memory.
The field detection pulse can be selected from the IHS (IFLS = 0) or from 0.5H pulse IHALF (IFLS = 1) by setting the I^2C-bus setting register IFLS (SUB:42h-bit[3]).
In the rear edge of judgment area, since the field judgment uncertainty area contains 10 clocks of IICLK (internal input system clock), external phase adjustment will be necessary if the phase of IVS lies in this area. (However, there is no problem if the change of IVS and IHS is in the same phase.)

The device also has the function to automatically generate a field pulse by judging a single field sync signal input (continuous for more than 8 fields) with the setting of FCON (SUB:42h-bit[7]) = 1. For example, if there is only field A input, the pulse toggled by IVS is regarded as the field pulse.

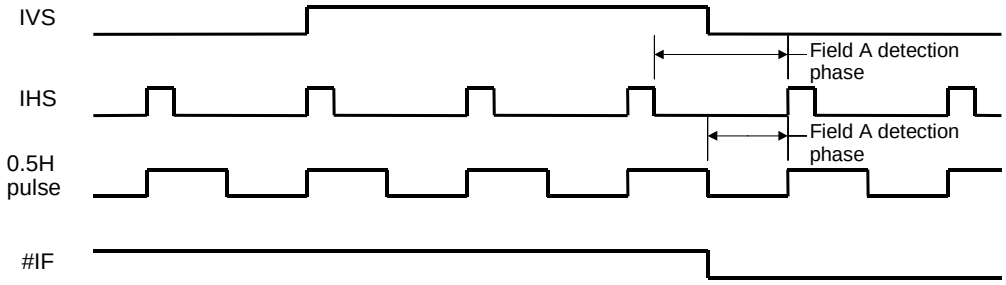


Figure F1-1-2 (1) Input System Field A Detection Timing

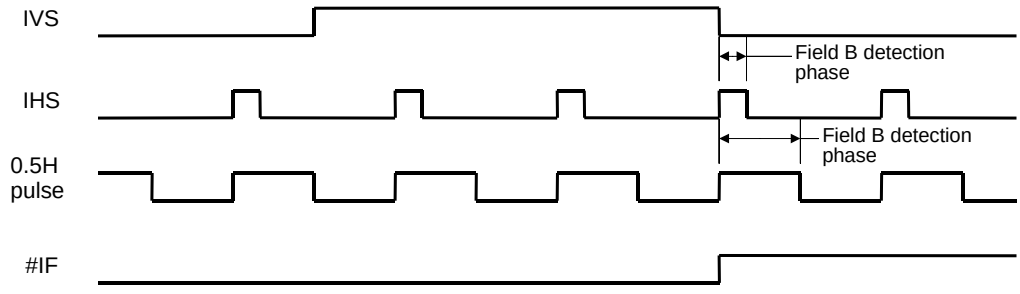


Figure F1-1-2 (2) Input System Field B Detection Timing

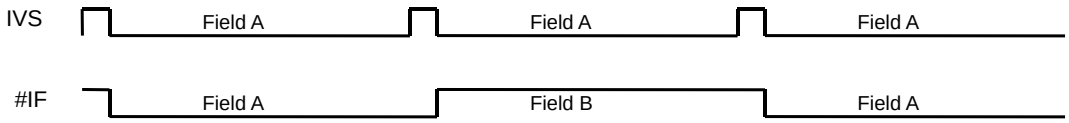


Figure F1-1-2 (3) Field Detection during Continuous Same Field Input (FCON = 1)

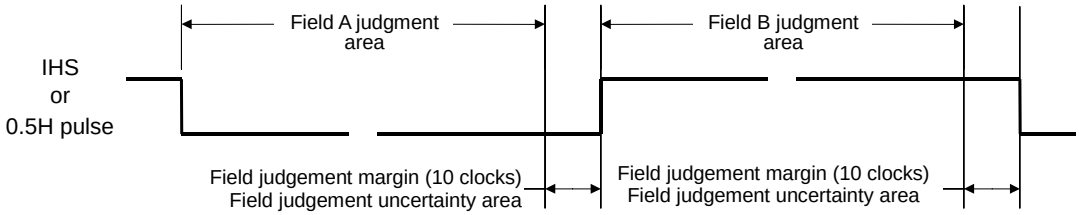


Figure F1-1-2 (4) Field Judgment Uncertainty Area

1.1.3 Setting Input System Write Enable and Read Enable

This IC generates the write enable signals (IWE) for writing data from the valid area made up of the valid vertical lines and the valid horizontal pixels defined by the input control mode settings to the write port of the field memory. Recursive noise reduction is performed for the written data.
With the write enable, it is possible to set the starting point in the vertical and horizontal directions. This setting makes it possible to line up the areas of valid lines and valid pixels with non-standard phase sync signals.

Table F1-1-3(1) Valid Input Data Area

VMD[1:0]	HMD[1:0]	Valid lines	Valid pixels
0h	0h	288	720
1h	0h	243	720
0h	1h	288	768
1h	1h	243	640
0h	2h	288	768
1h	2h	243	768
Other		Cannot be set in test mode.	

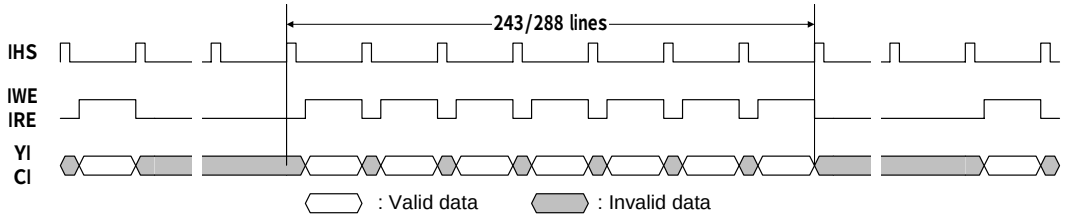


Figure F1-1-3(1) Input Vertical Valid Lines

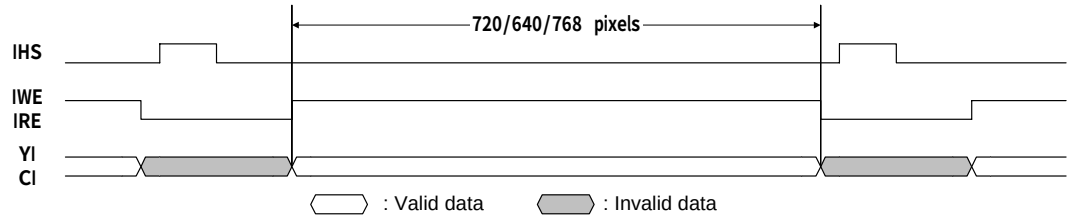


Figure F1-1-3(2) Input Horizontal Valid Pixels

- Setting of Input System Vertical Valid Line Start Position (IVPS)
  The input system vertical valid line start position (IVPS) is set in line unit with reference to the input system vertical reset (IVR: internal signal), generated from IVS, by setting NPVWE[3:0] (SUB:44h-bit[3:0]). The input data from IVPS onward is written in the memory as the valid data and held for the duration of a frame. This value can be set in ±7 lines (15 levels) with regard to the initial value (NPVWE[3:0] = 8h).

Table F1-1-3 (2) Input System Vertical Valid Line Start Position

R656	VMD [1:0]	IVPS position (number of IHS's from IVR)				
		NPVWE = 1h	·····	NPVWE = 8h	·····	NPVWE = Fh
0	0h	13 (–7 lines)	·····	20 (default)	·····	27 (+7 lines)
0	1h	7 (–7 lines)	·····	14 (default)	·····	21 (+7 lines)
1	0h	17 (–7 lines) *	·····	24 (default) *	·····	31 (+7 lines) *
1	1h	12 (–7 lines) *	·····	19 (default) *	·····	26 (+7 lines) *
Other than above		Test modes (Not settable)				

*: In the case of field B, it is +1.

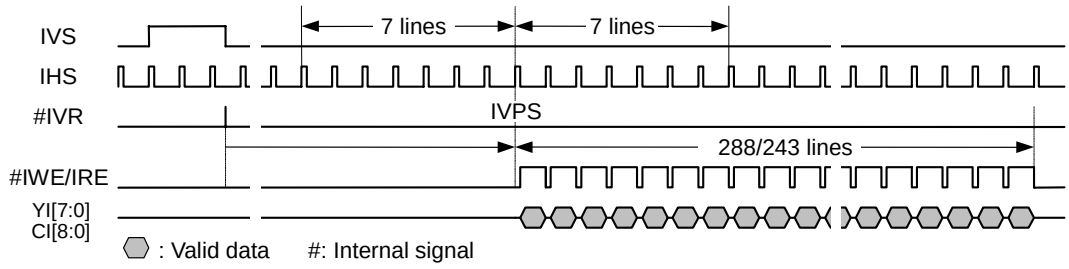


Figure F1-1-3 (3) Input System Vertical Valid Line Start Timing

- Setting of Input Sytem Horizontal Valid Pixel Start Position (IHPS)
  The input system horizontal valid pixel start position (IHPS) is set in pixel unit with reference to the input system horizontal reset (IHR: internal signal), generated from IHS, by setting NPHWE[7:0] (SUB:45h-bit[7:0]).
  The data from IHPS onward is written in the data memory of valid pixels as the valid data and held for the duration of a frame.
  This value can be set in 255 levels of ±127 pixels with regard to the initial value (NPHWE[7:0] = 80h).
  In the ITU-R BT.656 mode, the value cannot be set. Write enable with regard to valid data is generated on the basis of detected SAV, EAV.

Table F1-1-3 (3) Input System Horizontal Valid Pixel Start Position

HMD [1:0]	VMD[0]	IHPS position (number of pixels from IHS)				
		NPHWE = 01h	·····	NPHWE = 80h	·····	NHPWE = FFh
0h	0	17 (–127 pixels)	·····	144 (default)	·····	271 (+127 pixels)
0h	1	11 (–127 pixels)	·····	138 (default)	·····	265 (+127 pixels)
1h	0	49 (–127 pixels)	·····	176 (default)	·····	303 (+127 pixels)
1h	1	13 (–127 pixels)	·····	140 (default)	·····	267 (+127 pixels)
2h	0	49 (–127 pixels)	·····	176 (default)	·····	303 (+127 pixels)
2h	1	15 (–127 pixels)	·····	142 (default)	·····	269 (+127 pixels)
Other than above		Test modes (Not settable)				

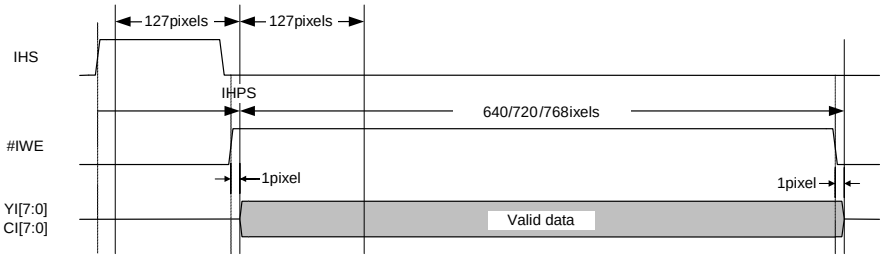


Figure F1-1-3 (4) Input Ststem Horizontal Valid Pixel Start Timing

1.1.4 Input System Sync Signal Polarity Inversion Setting

Negative polarity IVS can also be supported by setting the I^2C-bus setting register IVSINV (SUB:42h-bit[0]). Moreover, with regard to field detection, setting is possible even when setting the internal IVR generation edge.

Table F1-1-4 (1) IVINV Setting

IVSINV	Recommended input IVS polarity	IVR generation edge
0	Positive (default)	Rising edge
1	Negative	Falling edge

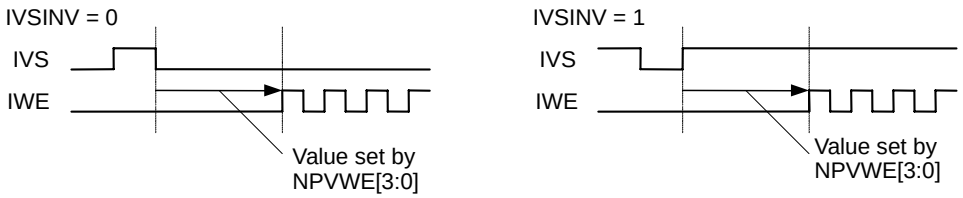


Figure F1-1-4 (1) Support of Input System Vertical Sync Signal Polarity Inversion

Negative polarity IHS can also be supported by setting the I^2C-bus setting register IHSINV (SUB:42h-bit[1]).

Table F1-1-4 (2) IHSINV Setting

IHSINV	Input IHS polarity
	Positive (default)
	Negative

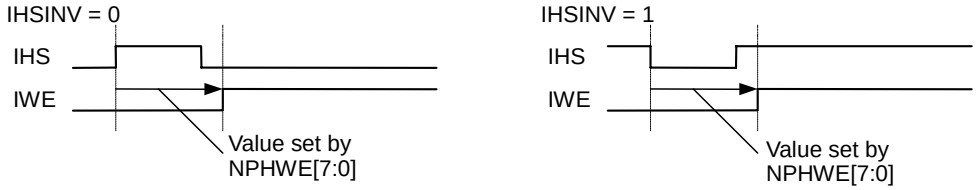


Figure F1-1-4 (2) Support of Input System Horizontal Sync Signal Polarity Inversion

1.1.5 Input System Detection Field Inversion Setting

Inversion of input system internal field detection is possible by setting IFINV (SUB:42h-bit[2]) by I^2C-bus interface. However, setting is not necessary if there is no problem in normal detection.

Table F1-1-5 IFIND Setting

IFINV	Input field	
	Field A	Field B
0	0	1
1	1	0

* PAL : Field A = 1st, 3rd, 5th, 7th color field
Field B = 2nd, 4th, 6th, 8th color field
* NTSC : Field A = 2nd, 4th color field
Field B = 1st, 3rd color field

1.1.6 Input System Vertical Reset Compensation Mode Setting

In this IC, the rear edge (in the case of standard signal, 625 lines; A-3 line, 0.5H position, in between B-315 and B-316 lines, 525 lines; A-6 line, 0.5H position, in between B-6 and B-7 lines) of normally standard vertical sync signal (IVS) is regarded as the reference position (IVR generating position) to perform field detection and memory control.
If a sync signal with unspecified phase of the IVS rear edge and horizontal sync signal (IHS) is input, the front edge can be used with the setting IVSINV = 1. But if the front edge is used in standard 626-line mode, the detection filed reverses in normal operation and field B gets written in the memory with one line earlier phase. Therefore, by setting the I^2C-bus setting register IVEM (SUB:42h-bit[4]), the detection field is inverted (A→B, B→A) and the vertical phase with regard to field B of the inverted result is delayed by 1H.
This allows compensation for field detection and IVR which is the typical front edge phase of IVS of 625-line mode.
In practice, this allows compliance with the sync signal examples shown in Table F1-1-6 and Figure F1-1-6.

Note: Use it in case the phase of field-detecting IVS and IHS reverses in the IC standard setting.

Table F1-1-6 Input System Vertical Reset Compensation by IVEM Setting

Condition	Vertical reference	Input data field	Internal decision field	IVEM setting	Field after compensation	Valid data start position
Phase 1	Rear edge IVSINV = 0	A	A	0	No compensation	n
		B	B			n
Phase 2	Rear edge IVSINV = 0	A	B	1	A	n
		B	A		B	n + 1
Phase 3	Front edge IVSINV = 1	A	A	0	No compensation	n
		B	B			n
Phase 4	Front edge IVSINV = 1	A	B	1	A	n
		B	A		B	n + 1

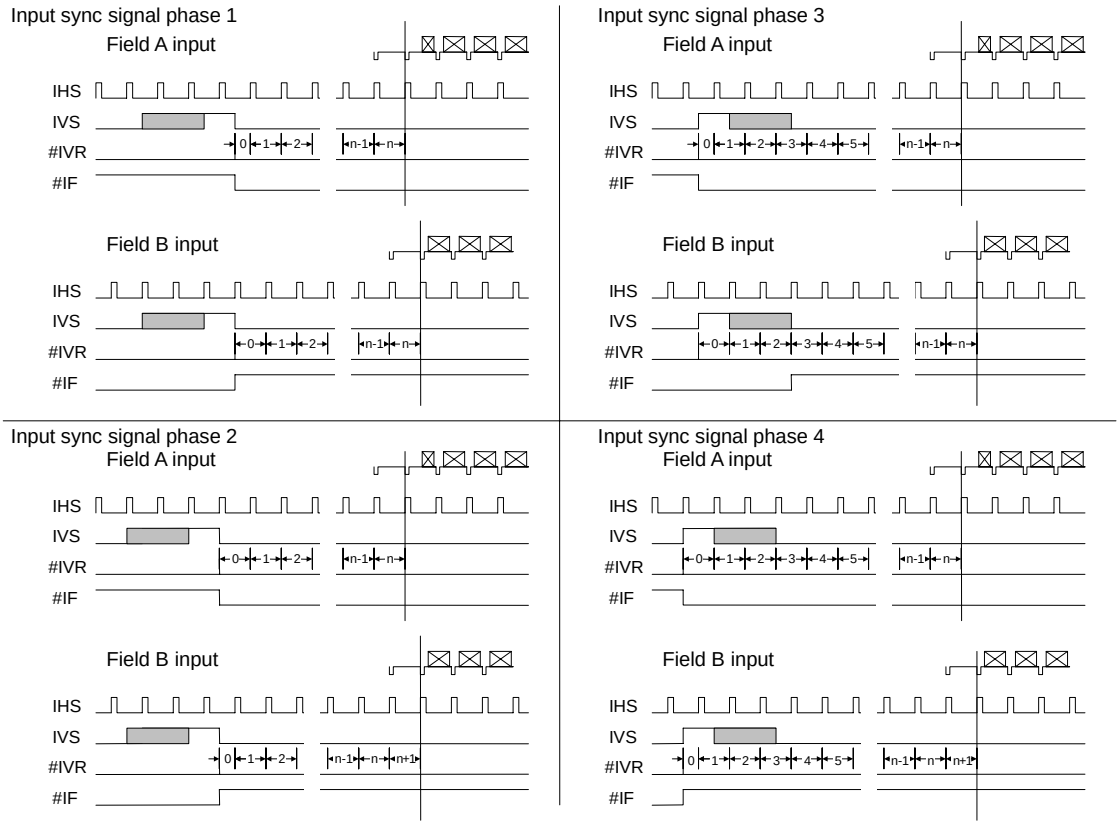


Figure F1-1-6 Input System Vertical Reset Compensation by IVEM Setting

1.1.7 Stop Memory Write Setting

By setting the I^2C-bus settings register STL[2:0] (SUB:43h-bit[2:0]), you can stop the generation of IWE and stop writing data to the memory. When you do this, the noise reduction feature stops, and until you set the start of writing, the data retained in the memory is output as a still image.
Further, by setting STLM[1:0](SUB:43h-bit[4:3]), you can select the output mode for the still image from among the following: field still image, frame still image, or frame median still image.
The still image data output is achieved by rewriting only the signals read from the memory for the valid data period selected by the IBLK signal, which indicates the valid data. Therefore, it is necessary to input the input sync signals as normal.
The data output as a field or frame (median) still image is based on the most recent data written to the memory (before the writing was stopped).
The timing of the writing stop and restoration can be set in one of thee modes: selected field A/B, field A output, and field B output.
In the timing for field A output, after the field A writing is completed, writing is stopped from the next field B vertical sync signal. Writing is restored with the field B vertical sync signal.
In the timing for field B output, after the field B writing is completed, writing is stopped from the next field A vertical sync signal. Writing is restored with the field A vertical sync signal.

Table F1-1-7(1) Writing Stop Settings

STL			Input data writing status
[0]	[1]	[2]	
0	0	0	Possible (field A restoration)
0	1	0	Possible (field B restoration)
0	X	1	Possible (either field restoration)
1	0	0	Stopped (field A maintained, still image output)
1	1	0	Stopped (field B maintained, still image output)
1	X	1	Stopped (either field output maintained, still image output)

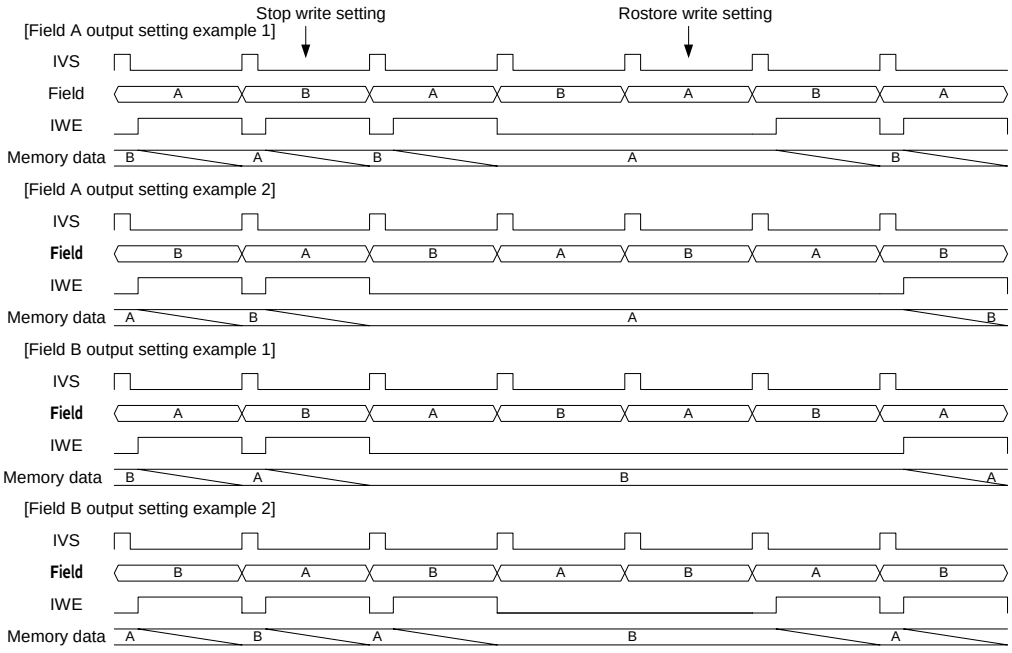


Figure F1-1-7 (1) Writing Stop/Restoration Timing

Table F1-1-7 (2) Still Image Output Mode Settings

STLM		Output Still Image Mode
[1]	[0]	
0	X	Field still image
1	0	Frame still image
1	1	Frame median still image

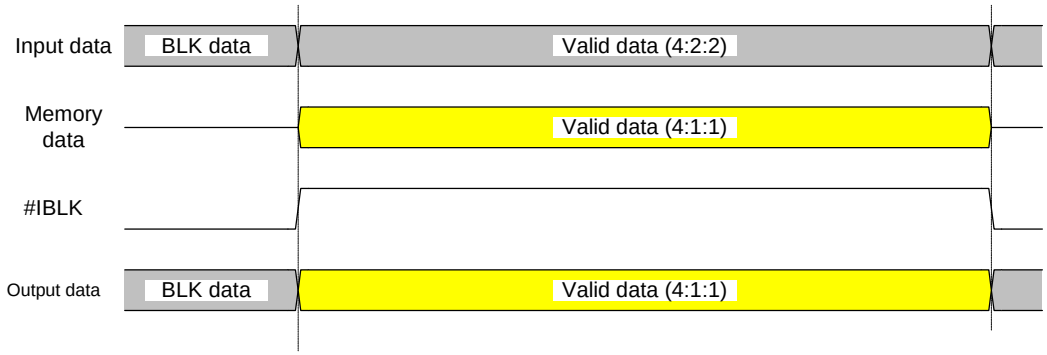


Figure F1-1-7(2) Output Data in Still Image Mode

* The data output from the memory is in 4:1:1 format, so it is converted to 4:2:2 format by interpolating linearly color difference data. Therefore, the color difference data has a lower band than normal data.

1.2 Input/Output Format

1.2.1 Input Data Format

The input of this IC complies with 16-bit 4:2:2 (YI[7:0] = Y-8bit, CI[7:0] = CbCr-8bit 4:2:2) format (input 16-bit mode), 8-bit 4:2:2 (YI[7:0] = YCbCr-8bit 4:2:2, without SAV, EVA) format (input 8-bit mode) and ITU-R BT.656 conforming (YI[7:0] = YCbCr-8bit 4:2:2, with SAV, EAV) format (ITU-R BT.656 mode).
The input format mode is set by an external pin MODE 2, I^2C-bus setting register DISEL (SUB:41h-bit[0]), or R656 (SUB:41h-bit[1]).
Switching of an external pin and a register is accomplished by setting the I^2C-bus setting register IRMON (SUB:40h-bit[7]).

Table F1-2-1 (1) Input Data Format Mode

IRMON	MODE2	DISEL	R656	Mode
0	0	X	0	Input 16-bit mode
1	X	0	0	
0	1	X	0	Input 8-bit mode
1	X	1	0	
X	X	X	1	ITU-R BT.656 mode

Table F1-2-1(2) Input Data Format

Input pin	Input 16-bit mode		Input 8-bit mode ITU-R BT.656 mode			
YI7	Y07	Y17	Cb07	Y07	Cr07	Y17
YI6	Y06	Y16	Cb06	Y06	Cr06	Y16
YI5	Y05	Y15	Cb05	Y05	Cr05	Y15
YI4	Y04	Y14	Cb04	Y04	Cr04	Y14
YI3	Y03	Y13	Cb03	Y03	Cr03	Y13
YI2	Y02	Y12	Cb02	Y02	Cr02	Y12
YI1	Y01	Y11	Cb01	Y01	Cr01	Y11
YI0	Y00	Y10	Cb00	Y00	Cr00	Y10
CI7	Cb07	Cr07	—	—	—	—
CI6	Cb06	Cr06	—	—	—	—
CI5	Cb05	Cr05	—	—	—	—
CI4	Cb04	Cr04	—	—	—	—
CI3	Cb03	Cr03	—	—	—	—
CI2	Cb02	Cr02	—	—	—	—
CI1	Cb01	Cr01	—	—	—	—
CI0	Cb00	Cr00	—	—	—	—
Y point	0	1	0		1	
C point	0		0			

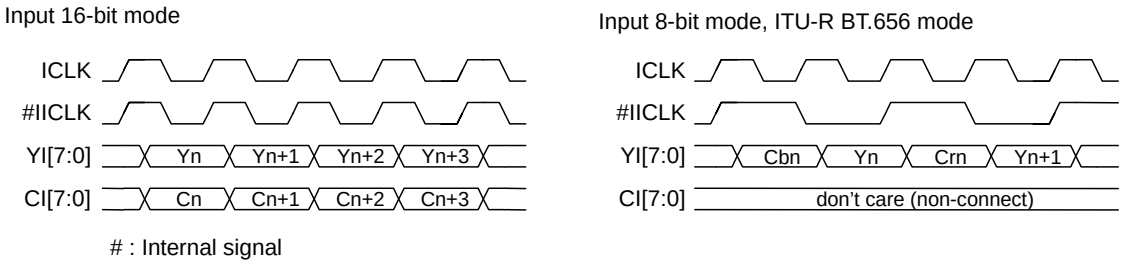


Figure F1-2-1 (1) Input Data Timing

The data and control signal interfaces according to input system modes are as follows.

- Input 16-bit mode
  Vertical sync signal: IVS
  Horizontal sync signal: IHS
  Data input pin: YI[7:0], CI[7:0] (YCbCr-4:2:2)
  Input system clock frequency: f_{ICLK} = 13.5/16/18 MHz
  Clip level: None

- Input 8-bit mode
  Vertical sync signal: IVS
  Horizontal sync signal: IHS
  Data input pin: YI[7:0], (YCbCr-4:2:2)
  Input system clock frequency: f_{ICLK} = 27/32/36 MHz
  Clip level: None

- ITU-R BT.656 mode
  Vertical sync signal: SAV, EAV split
  Horizontal sync signal: SAV, EAV split
  Data input pin: YI[7:0] (YCbCr-4:2:2)
  Input system clock frequency: f_{ICLK} = 27/32/36 MHz2
  Clip level: 00h → 01h, FFh → FEh

* By setting POFF (SUB:41h-bit[6]) = 1, SAV and EAV parity bits can be invalidated.

• Internal Input System Clock (IICLK)
The IICLK is IICLK = ICLK in 16-bit 4:2:2 mode whereas in 8-bit 4:2:2 mode and ITU-R BT.656 mode it is the clock pulse obtained by internally frequency-dividing ICLK to 1/2.
In 8-bit 4:2:2 mode, the position which is two ICLK clocks delayed from the rise of IHS is used for resetting and IICLK is generated by frequency-dividing ICLK to 1/2.
Normally reset of IICLK presumes the rise position of positive polarity IHS (IHSINV = 0), but by setting IHES (SUB:41h-bit[5]) and IHSINV, selection of compliance with negative polarity IHS and fall position is also possible.
In ITU-R BT 656 mode, ICLK is frequency-divided to 1/2 based on SAV.
In 8-bit 4:2:2 mode, if the phase of IHS for luminance and color difference data reverses (number of ICLKs from IICLK reset to initial color difference data is odd), it is possible to avoid the reversal by setting ICINV (SUB:41h-bit[4]).

Table F1-2-1 (3) IICLK Reset Position

IHES	IHSINV	Reset position
0	0	Positive polarity IHS rise (horizontal sync front edge)
1	0	Positive polarity IHS fall (horizontal sync rear edge)
0	1	Negative polarity IHS fall (horizontal sync front edge)
1	1	Negative polarity IHS rise (horizontal sync rear edge)

Table F1-2-1 (4) Compliance with Luminance-Color Difference Phase Reversal

ICINV	Usage conditions (8-bit 4:2:2 mode)
0	Number of ICLKs from IICLK reset to initial color difference data is even.
1	Number of ICLKs from IICLK reset to initial color difference data is odd.

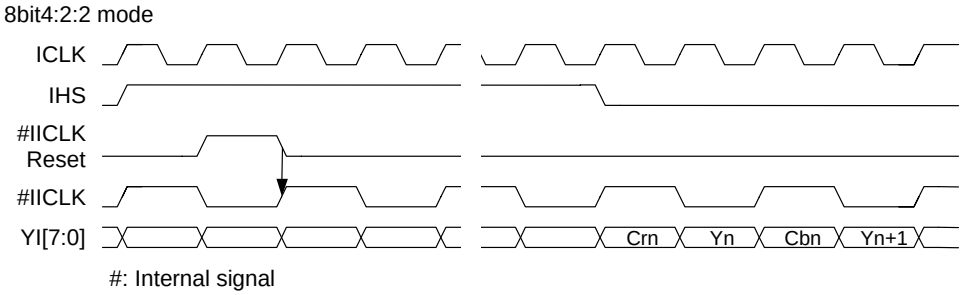


Figure F1-2-1 (2) IICLK Phase Timing Example

1.2.2 Output Data Format

The output data format for this IC is basically YCbCr 16-bit 4:2:2 because the internal signal processing is performed independently on luminance and color difference.
However, in the YCbCr 8-bit 4:2:2 mode and the ITU-R BT.656 mode, you can set DOSEL(SUB:60h-bit[1])=1 to select YCbCr 8-bit 4:2:2 (the same format as the input). When you make this setting, the unused CO[7:0] is in Hi-Z.

Table F2-2 Output Data Format

Output	Normal mode		8-bit input – 8-bit output mode (DOSEL =1)			
YO7	Y07	Y07	Cr07	Y17	Cb07	Y17
YO6	Y06	Y06	Cr06	Y16	Cb06	Y16
YO5	Y05	Y05	Cr05	Y15	Cb05	Y15
YO4	Y04	Y04	Cr04	Y14	Cb04	Y14
YO3	Y03	Y03	Cr03	Y13	Cb03	Y13
YO2	Y02	Y02	Cr02	Y12	Cb02	Y12
YD1	Y01	Y01	Cr01	Y11	Cb01	Y11
YD0	Y00	Y00	Cr00	Y10	Cb00	Y10
CO7	Cb07	Cr07	—	—	—	—
CO6	Cb06	Cr06	—	—	—	—
CO5	Cb05	Cr05	—	—	—	—
CO4	Cb04	Cr04	—	—	—	—
CO3	Cb03	Cr03	—	—	—	—
CO2	Cb02	Cr02	—	—	—	—
CO1	Cb01	Cr01	—	—	—	—
CO0	Cb00	Cr00	—	—	—	—

Table F1-2-2(2) I/O Data Format Combinations

DISEL	R656	DOSEL	Input	Output	I/O Delay
0	0	X	16 bits+Sync(H,V)	16 bits + Sync(H,V)	23(ICLK)
1	0	0	8 bits+Sync(H,V)	8 bits + Sync(H,V)	46(ICLK)
1	0	1	8 bits+Sync(H,V)	8 bits + Sync(H,V)	48(ICLK)
X	1	0	ITU-R BT.656	16 bits + Sync(H,V)	46(ICLK)
X	1	1	ITU-R BT.656	ITU-R BT.656 + Sync(H,V)	48(ICLK)

* Where input is ITU-R BT.656, the sync signals (H, V) of the output side are output as sync signals separated from SAV and EAV to OVS and OHS.

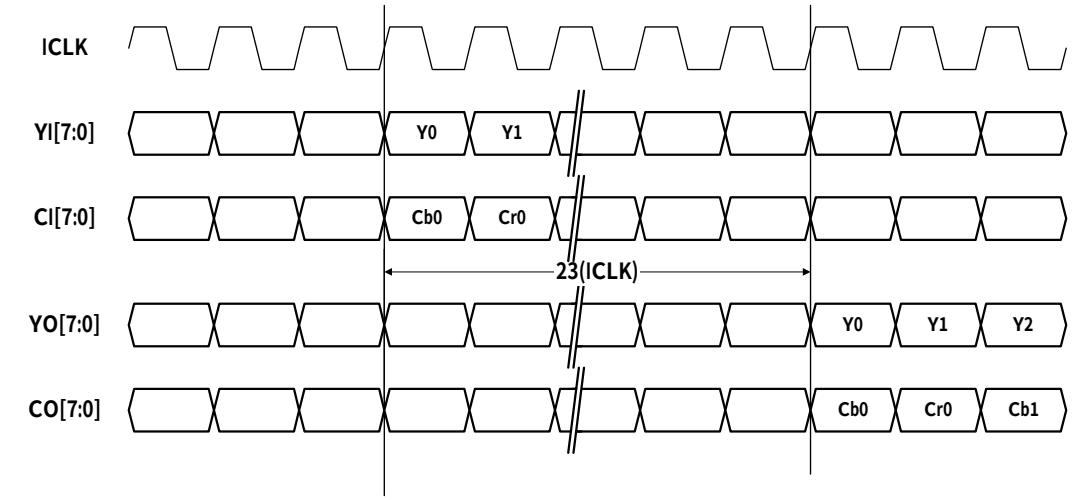


Figure F1-2-2(1) I/O Delay in the Input 16-bit Mode

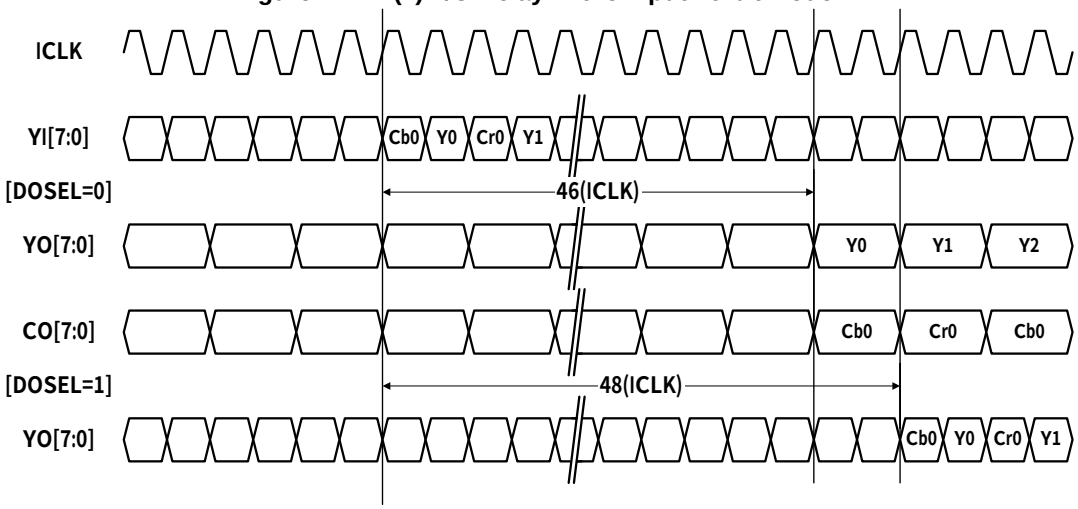


Figure F1-2-2(2) I/O Delay in the Input 8-bit Mode

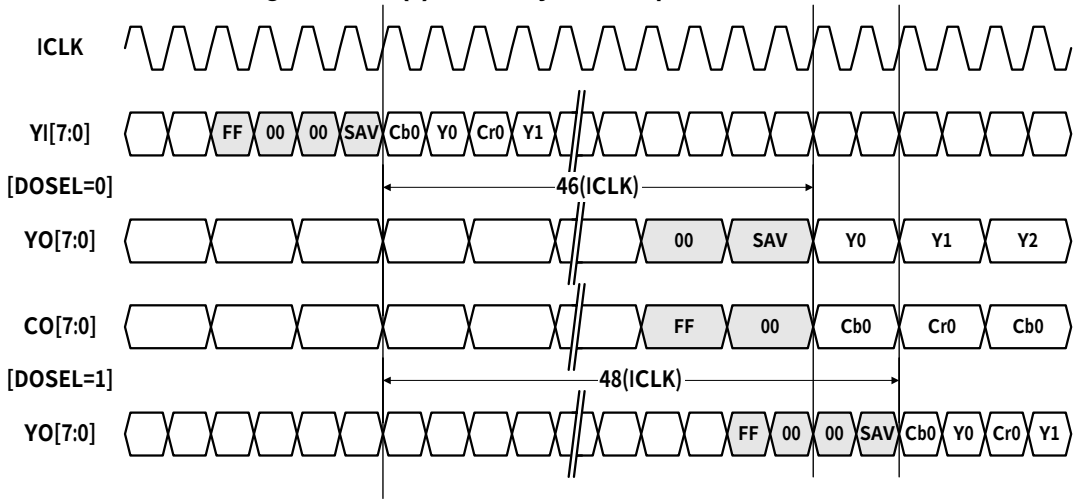


Figure F1-2-2(3) I/O Delay in the ITU-R BT.656 Mode

1.3 Noise Reduction Processing Function

The noise reduction provided by this IC detects noise and predicts motion for the input data and the data stored in the internal memory, for three correlations (between frames, between fields, and between lines). It performs motion compensation for the detected noise while reducing noise using the three correlations.

- Principle of Noise Reduction

  Difference between the current field data and the filed data preceding one frame, one field, or one line is extracted as time motion and noise independently for luminance and color difference signals.
  The low gain portion of this data is judged to be noise and the high gain portion to be motion and is extracted as motion level detection noise.
  The noise component extracted here is subjected to motion estimation by adjacent motion level and adjacent code, then further subjected to compensation based on motion and is regarded as the final noise component.
  Finally, noise reduction is carried out by subtracting this final noise data from the current field data.

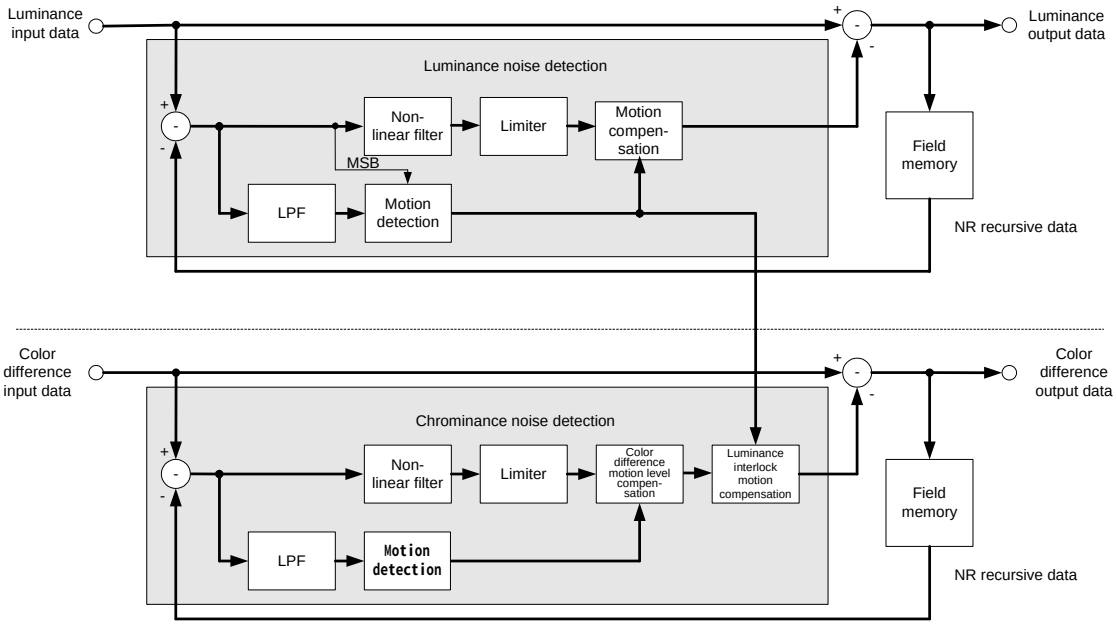


Figure F1-3 (1) Noise Detection Type Noise Reduction Configuration

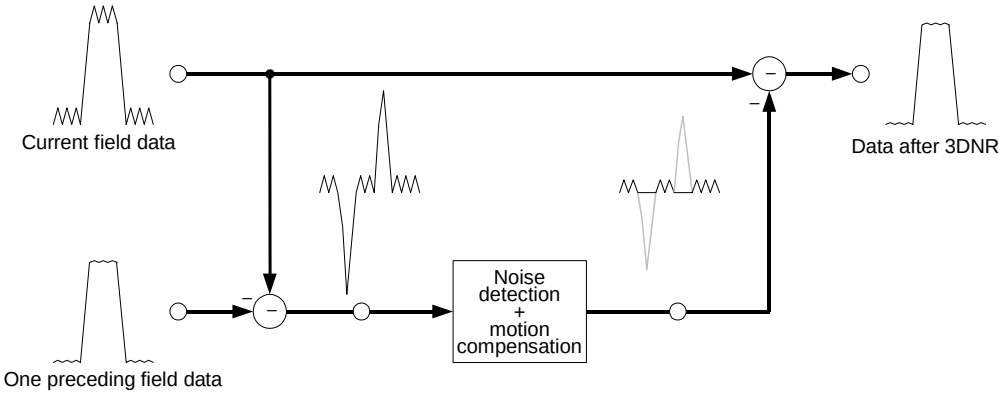


Figure F1-3 (2) Noise Reduction by Noise Detection

- Principles of Adaptive Noise Reduction

Adaptive noise reduction is achieved through the selection of noise data that utilizes the correlative relationships between frames, fields, and lines for the pixels for which the noise reduction is to be performed, as shown in Figure F1-3 (3).

The distinguishing characteristics of each correlation are as shown below.

Between frames : Same position (most effective), time difference 2V (less effective)
→Effective for still images (good NR, substantial afterimage)

Between fields : Position 0.5H different (effective), time difference 1V(effective)
→More effective for moving images than frames, more effective for still images than lines (medium NR, medium afterimage)

Between lines : Position 1H different (less effective), time difference 0 (most effective)
→Effective for moving images, but not effective for edges (medium NR, no afterimage, no NR for edges)

This IC detects motions and edges between lines, frames, and fields, based on the features described above, to select data after better correlated noise reduction and achieve effective noise reduction.

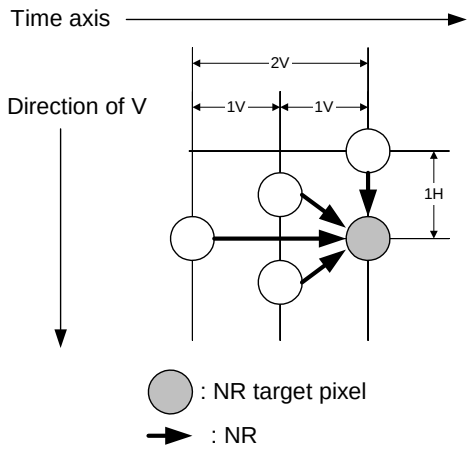


Figure F1-3 (3) Noise Reduction Correlative Relationships

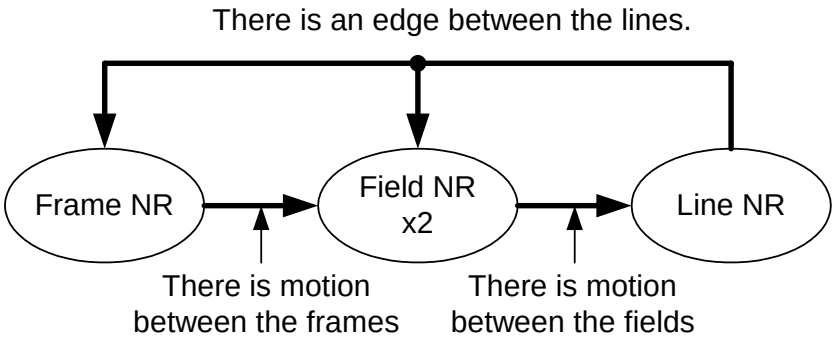


Figure F1-3 (4) Adaptive Noise Reduction Principles

1.3.1 Noise Reduction Mode

The noise reduction mode is set by NR2OFF(SUB:48h-bit[4]), FNRM[1:0] (SUB:48h-bit[6:5]), and you can select the noise reduction modes shown in Table F1-3-1.
By setting the adaptive margin that is set by YFAM(SUB:4Ah-bit[1]), CFAM(SUB:4Bh-bit[1]),weighting factor is applied to frames to improve noise reduction effect (However, afterimage will be more likely to occur).

Table F1-3-1 (1) Noise Reduction Modes

FNRM		NR2OFF	Noise Reduction Mode
[1]	[0]		
0	0	0	Fully adaptive frame-recursive NR (uses frames, fields, and lines)
0	0	1	3D adaptive frame-recursive NR (uses frames and fields)
0	1	0	2D adaptive frame-recursive NR (uses frames and lines)
0	1	1	Frame-recursive NR
1	X	0	2D adaptive field-recursive NR (uses fields and lines)
1	X	1	Field-recursive NR

Table F1-3-1 (2) Luminance Adaptive Margin Settings

YFAM	Luminance adaptive margin	Remarks
0	No	
1	Yes	Frame NR performance emphasized (greater NR, increased afterimage)

F1-3-1 (3) Color Difference Adaptive Margin Settings

CFAM	Color difference adaptive Margin	Remarks
0	No	
1	Yes	Frame NR performance emphasized (greater NR, increased afterimage)

1.3.2 Detected Noise Between Frames, Fields and Lines

Correlations are made between data in the current field and data in one preceding frame, data on one preceding and succeeding lines in one preceding frame, and data on one preceding line in the same field. Then, the smallest correlation data of absolute value of the correlation is selected as correlations between frames and fields.

From the differential values between frames and between fields (ΔY, ΔC), the signal with a low level of absolute value for the differential values (|ΔY|, |ΔC|) is judged to be the noise component and the signal with a high level is judged to be the motion component. The data judged to be the noise is extracted as the motion level detection noise.

The detected noise is output after being filtered by the area covered by the input noise detection line, the noise convergence line, and the noise upper limit line. The inclination of the input noise detection line is set by YSLT[1:0](SUB:4Ah-bit[5:4]) and CSLT[1:0](SUB:4Bh-bit[5:4]), the inclination and offset of the noise convergence line are set by YSLT[3:2](SUB:4Ah-bit[7:6]), YNS[5:0](SUB:4Ch-bit[5:0]), CSLT[3:2](SUB:4Bh-bit[7:6]) and CNS[5:0] (SUB:4Dh-bit[5:0]), and the offset of the noise upper limit line, which has 0 inclination, is set by YLM[4:0] (SUB:4Eh-bit[4:0]) and CLM[4:0] (SUB:4Fh-bit[4:0]). (Figure F1-3-1)

Table F1-3-2 Non-Linear Filter Noise Detection Area Settings

YSLT/CSLT				Noise detection line		Noise convergence line		Noise upper limit line	
[0]	[1]	[2]	[3]	Inclination	Offset	Inclination	Offset	Inclination	Offset
0	0	0	0	1	0	-1	YNS[5:0] CNS[5:0]	0	YLM[4:0] CLM[4:0]
1	0	0	0	7/8					
0	1	0	0	3/4					
1	1	0	0	1/2					
0	0	1	0	1		-3/4			
1	0	1	0	7/8					
0	1	1	0	3/4					
1	1	1	0	1/2					
0	0	0	1	1		-1/2			
1	0	0	1	7/8					
0	1	0	1	3/4					
1	1	0	1	1/2					
0	0	1	1	1		-3/2			
1	0	1	1	7/8					
0	1	1	1	3/4					
1	1	1	1	1/2					

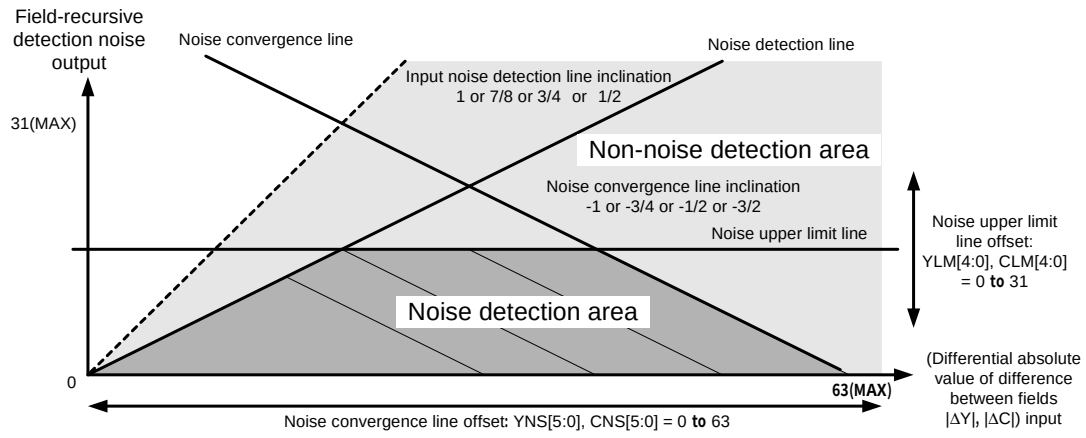


Figure F1-3-2 Field-Recursive Noise Motion Level Detection Noise Characteristics

1.3.3 Detection of Motion between Frames, Fields, and Lines

There are two types of luminance signal motion detection: level motion detection and continuous code motion detection.
Color difference signal motion detection includes level motion detection.

① Luminance Level Motion Detection
From the differential data between fields, including luminance signal motion and noise, the high frequency component (ΔHY) is filtered with the LPF, extracting only the low frequency differential data (ΔLY).

Luminance LPF: $F(z) = (1/8)z^{-2} + (1/8)z^{-1} + (1/2)z^{0} + (1/8)z^{1} + (1/8)z^{2}$

The low frequency differential data is assumed to have a large proportion of the motion component, so the absolute value of that data (|ΔLY|) is compared with the luminance noise convergence level set in YNS[5:0] to determine the amount of motion.
If the result shows that the differential absolute value is greater than the noise convergence level, it is determined that there is a lot of motion in the data, and the motion flag (YMT) = 1 is set.
If the differential absolute value is less than the noise convergence level, it is determined that there is not much motion in the data, and the motion flag (YMT) = 0 is set.

Table F1-3-3 (1) Luminance Level Motion Detection

Motion Detection Conditions	Motion Flag (YMT)
|ΔLY| > 64	1
|ΔLY| > YNS[5:0]	1
|ΔLY| ≤ YNS[5:0]	0

② Luminance Continuous Code Motion Detection
This feature detects sequences of 3, 4, and 5 continuous codes in the differential data that includes the pixels for which noise detection is being performed. Where continuity is detected, the absolute value of the low frequency differential data and the continuous code motion YMS[3:0](SUB:50h-bit[3:0]) are compared to determine the amount of motion.

- 3 Continuous Code Detection

If 3 continuous codes are detected to be the same and their low frequency differential data absolute values are equal to or greater than the continuous code motion detection level (YMS[3:0]), the data is judged to have much motion, and the 3 continuous code motion flag (YMT3) = 1 is set.
If the absolute value is less than the continuous motion detection level, the data is judged to have little motion, and the 3 continuous code motion flag (YMT3) = 0 is set.

Table F1-3-3 (2) Luminance 3 Continuous Code Motion Detection

Motion detection condition	Motion flag (YMT3)
|ΔLY| > 16	1
|ΔLY| ≥ YMS[3:0]	1
|ΔLY| < YMS[3:0]	0

• 4 Continuous Code Detection

If 4 continuous codes are detected to be the same and their low frequency differential data absolute values are equal to or greater than the continuous code motion detection level 1/2(YMS[3:1]), the data is judged to have much motion, and the 4 continuous code motion flag (YMT4) = 1 is set.
If the absolute value is less than the continuous motion detection level, the data is judged to have little motion, and the 4 continuous code motion flag (YMT4) = 0 is set.

Table F1-3-3 (3) Luminance 4 Continuous Code Motion Detection

Motion detection condition	Motion flag (YMT4)
$\|\Delta LY\| > 8$	1
$\|\Delta LY\| \geq$ YMS[3:1]	1
$\|\Delta LY\| <$ YMS[3:1]	0

• 5 Continuous Code Detection

If 5 continuous codes are detected to be the same and their low frequency differential data absolute values are equal to or greater than the continuous code motion detection level 1/4 (YMS[3:2]), the data is judged to have much motion, and the 5 continuous code motion flag (YMT5) = 1 is set.
If the absolute value is less than the continuous motion detection level, the data is judged to have little motion, and the 5 continuous code motion flag (YMT5)=0 is raised.

Table F1-3-3 (4) Luminance 5 Continuous Code Motion Detection

Motion detection condition	Motion flag (YMT5)
$\|\Delta LY\| > 4$	1
$\|\Delta LY\| \geq$ YMS[3:2]	1
$\|\Delta LY\| <$ YMS[3:2]	0

③ Color Difference Level Motion Detection

From the differential data between fields, including color difference signal motion and noise, the high frequency component (ΔHC) is filtered with the LPF, extracting only the low frequency differential data (ΔLC).

Color difference LPF: $F(z) = (1/4)z^{-2} + (1/2)z^{0} + (1/4)z^{2}$

The low frequency differential data is assumed to have a large proportion of the motion component, so the absolute value of that data ($|\Delta LC|$) is compared with the color difference noise convergence level set in CNS[5:0] to determine the amount of motion.
If the result shows that the differential absolute value is greater than the noise convergence level, the data is judged to have a lot of motion, and the color difference motion flag (CMT) = 1 is set.
If the differential absolute value is less than the noise convergence level, it is determined that there is not much motion in the data, and the motion flag (CMT) = 0 is set.
This motion flag is used in adjacent pixel motion compensation.

Table F1-3-3 (5) Color Difference Level Motion Detection

Motion detection condition	Motion flag (CMT)
$\|\Delta LC\| > 64$	1
$\|\Delta LC\| >$ CNS[5:0]	1
$\|\Delta LC\| \leq$ CNS[5:0]	0

1.3.4 Motion Compensation

This IC performs the motion compensation described below in ① and ② for the noise detected in Section 1.3.2 It does this by creating the motion compensation flags YMA[3:0] and CMA[4:0] from the motion flags (YMT, YMT3, YMT4, YMT5, and CMT) detected in Section 1.3.3, the motion compensation stop settings YMOFF[3:0] (SUB:51h-bit[3:0]) and CMOFF[4:0](SUB:52h-bit[4:0]), and the luminance linked color difference motion compensation setting CMY (SUB:52h-bit[7]).

Table F1-3-4 (1) Motion Compensation Flags

Motion compensation flag	Composite signal	Remarks
YMA[0]	YMT&YMOFF[0]	Luminance adjacent pixel level luminance motion compensation
YMA[1]	YMT&YMOFF[1]	Luminance 3 continuous codes luminance motion compensation
YMA[2]	YMT&YMOFF[2]	Luminance 4 continuous codes luminance motion compensation
YMA[3]	YMT&YMOFF[3]	Luminance 5 continuous codes luminance motion compensation
CMA[0]	CMT&CMOFF[0]	Color difference adjacent pixel level color difference motion compensation
CMA[1]	YMT&CMOFF[1]&CMY	Luminance adjacent pixel level color difference motion compensation
CMA[2]	YMT3&CMOFF[2]&CMY	Luminance 3 continuous codes color difference motion compensation
CMA[3]	YMT4&CMOFF[3]&CMY	Luminance 4 continuous codes color difference motion compensation
CMA[4]	YMT5&CMOFF[4]&CMY	Luminance 5 continuous codes color difference motion compensation

① Luminance Signal Noise Motion Compensation

This feature performs motion compensation for the detected noise using the motion compensation flag YMA[3:0].

As the method of motion compensation , you can select the reduction mode (YNRM = 0) or the noise 0 mode with YNRM(SUB:4Ah-bit[0]).

In the reduction mode, you can choose the normal reduction mode (YABN = 0) or the absolute noise reduction mode (YABN = 1) in register YABN(SUB:4Ah-bit[2]).

Table F1-3-4 (2) Luminance Motion Compensation Modes

YNRM	YABN	Motion compensation mode	Remarks
X	X	None	Detected noise as is
0	0	Normal reduction	(Detected noise) x (Reduction coefficient)
0	1	Absolute noise reduction	(Detected noise) x (Reduction coefficient)
1	X	Noise 0	Noise 0 judgment (NROFF)

Table F1-3-4 (3) Noise Reduction Coefficients

YMA				Reduction coefficient	
[3]	[2]	[1]	[0]	YABN = 0	YABN = 1
0	0	0	0	1	1
0	0	0	1	1/2	3/4
0	0	1	0	1/2	3/4
0	0	1	1	1/4	5/8
0	1	1	0	1/4	5/8
0	1	1	1	1/8	9/16
1	1	1	0	1/8	9/16
1	1	1	1	1/16	17/32

② Color Difference Signal Noise Motion Compensation

This feature performs motion compensation for the detected noise using the motion compensation flag CMA[4:0].

As the method of motion compensation , the reduction mode (CNRM = 0) or the noise 0 mode (CNRM = 1) can be selected by CNRM (SUB:4Bh-bit[0]).

In the reduction mode, the normal reduction mode (CABN = 0) or the absolute noise reduction mode (CABN = 1) can be selected by CABN (SUB:4Bh-bit[2]).

Table F1-3-4 (4) Color Difference Motion Compensation Mode

CNRM	CABN	Motion compensation mode	Remarks
X	X	None	Detected noise as is
0	0	Normal reduction	(Detected noise) x (Reduction coefficient)
0	1	Absolute noise reduction	(Detected noise) x (Reduction coefficient)
1	X	Noise 0	Noise 0 judgment (NROFF)

Table F1-3-4 (5) Color Difference Normal Reduction Mode Noise Reduction Coefficients

CMA					Reduction coefficient	
[4]	[3]	[2]	[1]	[0]	CABN=0	CABN=1
0	0	0	0	0	1	1
0	0	0	0	1	1/2	3/4
0	0	0	1	0	1/2	3/4
0	0	0	1	1	1/4	5/8
0	0	1	0	0	1/2	3/4
0	0	1	0	1	1/4	5/8
0	0	1	1	0	1/4	5/8
0	0	1	1	1	1/8	9/16
0	1	1	0	0	1/4	5/8
0	1	1	0	1	1/8	9/16
0	1	1	1	0	1/8	9/16
0	1	1	1	1	1/16	17/32
1	1	1	0	0	1/8	9/16
1	1	1	0	1	1/16	17/32
1	1	1	1	0	1/16	17/32
1	1	1	1	1	0	1/2

1.3.5 Noise Reduction Stop Setting

Noise reduction can be forcibly stopped by setting NROFF (SUB:48h-bit[0]) on the I^2C-bus interface.
However, data can be written into the memory even while noise reduction is stopped.

Table F1-3-5 NROFF Setting

NROFF	Noise Reduction
0	Operated
1	Stopped

1.3.6 Noise Reduction Demo Mode Setting

By setting NRDEMO[2:0] (SUB:48h-bit[2:0]), a screen can be split as shown in Figure F1-3-6 and noise reduction function can be confirmed as demo mode or the I^2C-bus interface.
However, the demo mode does not work when noise reduction is stopped by setting NROFF = 1.

Table F1-3-6 NRDEMO Setting

NROFF	NRDEMO			Left side of screen	Right side of screen
	[0]	[1]	[2]		
0	0	0	0	NR setting value	NR setting value
1	X	X	X	Stop NR	Stop NR
0	1	X	X	Stop NR	NR setting value
0	0	1	X	NR Setting value	Adaptive NR
0	0	0	1	NR Setting value	Adaptive 2DNR

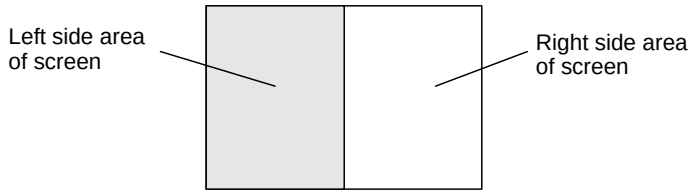


Figure F1-3-6 Noise Reduction Demo Screen

1.3.7 Noise Status Detection

In order to automatically optimize noise reduction setting, this IC has a function for detecting the overall video sample noise status during the motionless vertical blanking period.

- Detection of noise level (average and maximum values)
  Set NRDTON (SUB:49h-bit[1]) = 1 to detect the blanking period noise level for one line (NDTC = 0) of a vertical blanking period set by NRDTP[3:0](SUB:57h-bit[5:2]) and DTPSL (SUB:57h-bit[7]). Alternatively, you can set the same register to detect the blanking noise for **one line (NDTC = 1)** of the maximum noise level of multiple lines (maximum 16 lines not including valid lines) ending with line NRDTP[3:0]. The blanking period noise (average and maximum values) detection can be performed frame by frame.
  Set PNON (SUB:49h-bit[7]) = 1 to detect the amount of noise in the valid data period.
  The detection starting position is set in DTPSL. When DTPSL = 0, the starting position is immediately after the end of the valid lines; when DTPSL = 1, the starting position is one line after the end of the valid lines.
  When NRDTON = 0, the final status data for NRDTON = 1 is preserved. Initially, the average and maximum noise values are set at 0.
  The fields for which detection is to be performed are set in NRDTF (SUB:49h-bit[5]). When NRDTF = 0, field A vertical blanking period is set; when NRDTF = 1, field B vertical blanking period is set.
  By setting YNAMS (SUB:57-bit[0]) and CNAMS (SUB:57h-bit[1]), it is possible to select either an 8-frame average of the detected noise (YNMAS = 0, CNAMS = 0) or the level of detected noise in a single frame (YNMAS = 1, CNAMS = 1).

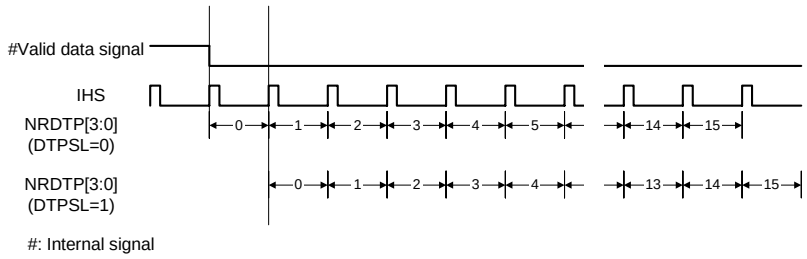


Figure F1-3-7 (1) Vertical Blanking Noise Status Detection timing (NDTC = 0)

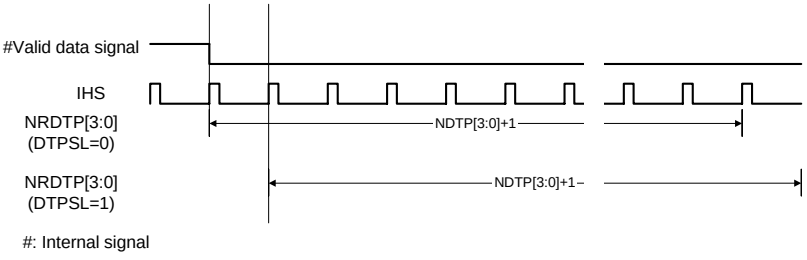


Figure F1-3-7 (2) Vertical Blanking Noise Status Detection timing (NDTC = 1)

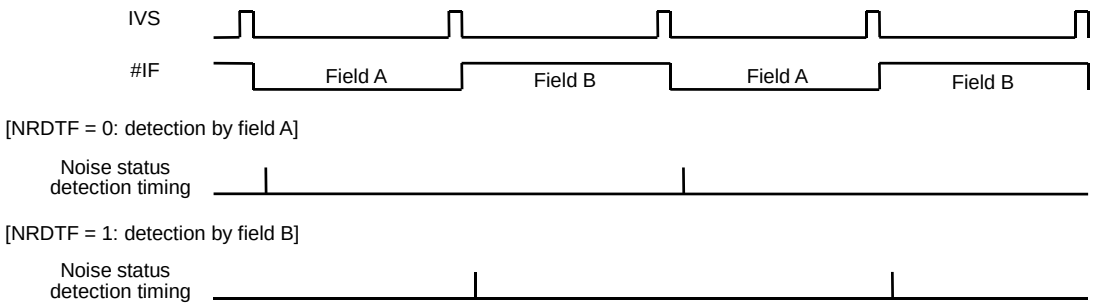


Figure F1-3-7 (3) Detection Field Based on NRDTF

Table F1-3-7 (1) Vertical Blanking Sample Noise Detection Settings

NRDTON	Noise detection
0	Stopped (previously detected data is maintained)
1	Operating

Table F1-3-7 (2) Noise Detection Field Settings

NRDTF	Noise detection field
0	Field A
1	Field B

Table F1-3-7 (3) Blanking Period Noise Detection Line Settings

NDTC	Noise detection line
0	1 line set at the NRDTP[3:0] position
1	Multiple lines from the line after the last valid line to NRDTP[3:0]

Table F1-3-7 (4) Noise Detection Value Select Settings

YNAMS CNAMS	Noise detection value
0	8-frames average
1	Single frame

Table F1-3-7 (5) Noise Detection Area

PNON	Noise detection area
0	Vertical blanking period
1	Vertical blanking period + valid data period

① Detection of Basic Noise Status Signals

Detection of the basic noise status signal (YBDTO, CBDTO) involves comparing the average noise value (YBAVRO[6:0], CBAVRO[6:0]) and the noise status comparison value (YAVR1[5:0] (SUB:53h-bit[5:0]), CAVR1[5:0] (SUB:54h-bit[5:0])) of the blanking period. The noise status is switched when the new status has continued for four frames or more.

The detection of the noise status signal has the hysteresis characteristic shown in Figure F1-3-6(4). You can select the characteristic with YAH1(SUB:53h-bit[7]) and CAH1 (SUB:54h-bit[7]).

Table F1-3-7 (6) Luminance Blanking Period Noise Status Detection

Before transition YBDTO	Condition	After transition YBDTO
0	YBAVRO[6:0] ≤ YAVR1[5:0]	0
0	YBAVRO[6:0] > YAVR1[5:0]	1
1	YBAVRO[6:0] ≤ YAVR1[5:0] x (hysteresis coefficient)	0
1	YBAVRO[6:0] > YAVR1[5:0] x (hysteresis coefficient)	1

Table F1-3-7 (7) Color Difference Blanking Period Noise Status Detection

Before transition CBDTO	Condition	After transition CBDTO
0	CBAVRO[6:0] ≤ CAVR1[5:0]	0
0	CBAVRO[6:0] > CAVR1[5:0]	1
1	CBAVRO[6:0] ≤ CAVR1[5:0] x (hysteresis coefficient)	0
1	CBAVRO[6:0] > CAVR1[5:0] x (hysteresis coefficient)	1

Table F1-3-7 (8) Noise Status Reduction Direction Detection Hysteresis Settings

YAH1 CAH1	Noise reduction direction switching coefficient
0	3/4
1	7/8

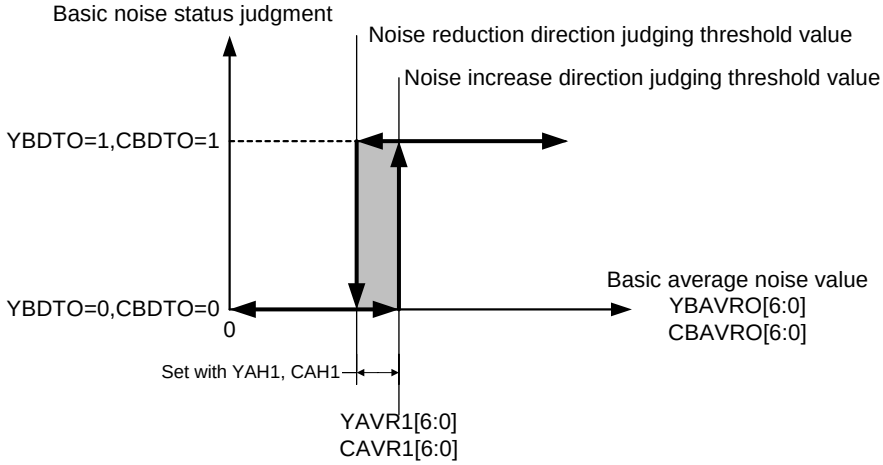


Figure F1-3-7 (4) Basic Noise Status Judgment Transition Diagram

② Judgment Noise Level Selection

Select the judgment noise level based on the procedure for basic noise level detection described above.
When PNON (SUB:49h-bit[7]) = 0, the blanking period noise level is referenced for the judgment noise level.
When PNON = 1, the overall noise status is referenced on the noise level of the valid data period when the noise status of the blanking period is judged to be low noise (YBDTO1 = 0, CBDTO1 = 0). When the noise status of the blanking period is judged to be high (YBDTO1 = 1, CBDTO1 = 1), the average noise level of the blanking period and the average noise level of the valid period are compared and the smaller value is referenced for the overall noise status.
Switching between the blanking period and the valid data period occurs when the noise average value condition has continued for four frames or more.

Table F1-3-7 (9) Luminance Judgment Noise Level Selection

PNON	YBDTO1	Luminance noise average value condition	Luminance judgment noise level
0	X	—	Blanking period noise level
1	0	—	Valid data period noise level
1	1	Blanking period noise level ≤ Valid data period noise level	Blanking period noise level
1	1	Blanking period noise level > Valid data period noise level	Valid data period noise level

Table F1-3-7 (10) Color Difference Judgment Noise Level Selection

PNON	CBDTO1	Color difference noise average condition	Color difference judgment noise level
0	X	—	Blanking period noise level
1	0	—	Valid data period noise level
1	1	Blanking period noise level ≤ Valid data period noise level	Blanking period noise level
1	1	Blanking period noise level > Valid data period noise level	Valid data period noise level

③ Judging noise status detection

Judgment of the noise status is achieved by comparing the average noise value (YAVRO[6:0], CAVRO[6:0]), the noise status comparison value (I^2C-bus setting registers YAVR1[5:0] (SUB:53h-bit[5:0]), CAVR1[5:0] (SUB:54h-bit[5:0]), YAVR2 [6:0] (SUB:55h-bit[6:0]), CAVR2[6:0] (SUB:56h-bit[6:0])). Based on this judgment, the noise status signals (YDTO1, CDTO1, YDTO2, CDTO2) are generated.

The detection of noise status signal has a hysteresis characteristic as shown in Figure F1-3-6 (5). Select the characteristic with YAH1 (SUB:53h-bit[7]), CAH1 (SUB:54h-bit[7]), YAH2 (SUB:55h-bit[7]), and CAH2 (SUB:56h-bit[7]).

It is also possible to mask the luminance detection in order to enable color difference detection by setting ACY (SUB:49h-bit[2]. The color difference detection is enabled when YDTO1 = 1 for CDTO1 and YDTO2 = 1 for CDTO2.

Table F1-3-7 (11) Luminance Judgment Noise Status Detection 1

Before transition YDTO1	Condition	After transition YDTO1
0	YAVRO[6:0] ≤ YAVR1[5:0]	0
0	YAVRO[6:0] > YAVR1[5:0]	1
1	YAVRO[6:0] ≤ YAVR1[5:0] x (hysteresis coefficient)	0
1	YAVRO[6:0] > YAVR1[5:0] x (hysteresis coefficient)	1

Table F1-3-7 (12) Color Difference Judgment Noise Status Detection 1

Before transition CDTO1	Condition	After transition CDTO1
0	CAVRO[6:0] ≤ CAVR1[5:0]	0
0	CAVRO[6:0] > CAVR1[5:0]	1
1	CAVRO[6:0] ≤ CAVR1[5:0] x (hysteresis coefficient)	0
1	CAVRO[6:0] > CAVR1[5:0] x (hysteresis coefficient)	1

Table F1-3-7 (13) Luminance Judgment Noise Level Detection 2

Before transition YDTO2	Condition	After transition YDTO2
0	YAVRO[6:0] ≤ YAVR2[6:0]	0
0	YAVRO[6:0] > YAVR2[6:0]	1
1	YAVRO[6:0] ≤ YAVR2[6:0] x (hysteresis coefficient)	0
1	YAVRO[6:0] > YAVR2[6:0] x (hysteresis coefficient)	1

Table F1-3-7 (14) Color Difference Judgment Noise Status Detection 2

Before transition CDTO2	Condition	After transition CDTO2
0	CAVRO[6:0] ≤ CAVR2[6:0]	0
0	CAVRO[6:0] > CAVR2[6:0]	1
1	CAVRO[6:0] ≤ CAVR2[6:0] x (hysteresis coefficient)	0
1	CAVRO[6:0] > CAVR2[6:0] x (hysteresis coefficient)	1

Table F1-3-7 (15) Color Difference Noise Status Detection Mask Setting

ACY	Color difference noise status detection
0	Color difference independent detection
1	Luminance detection mask detection

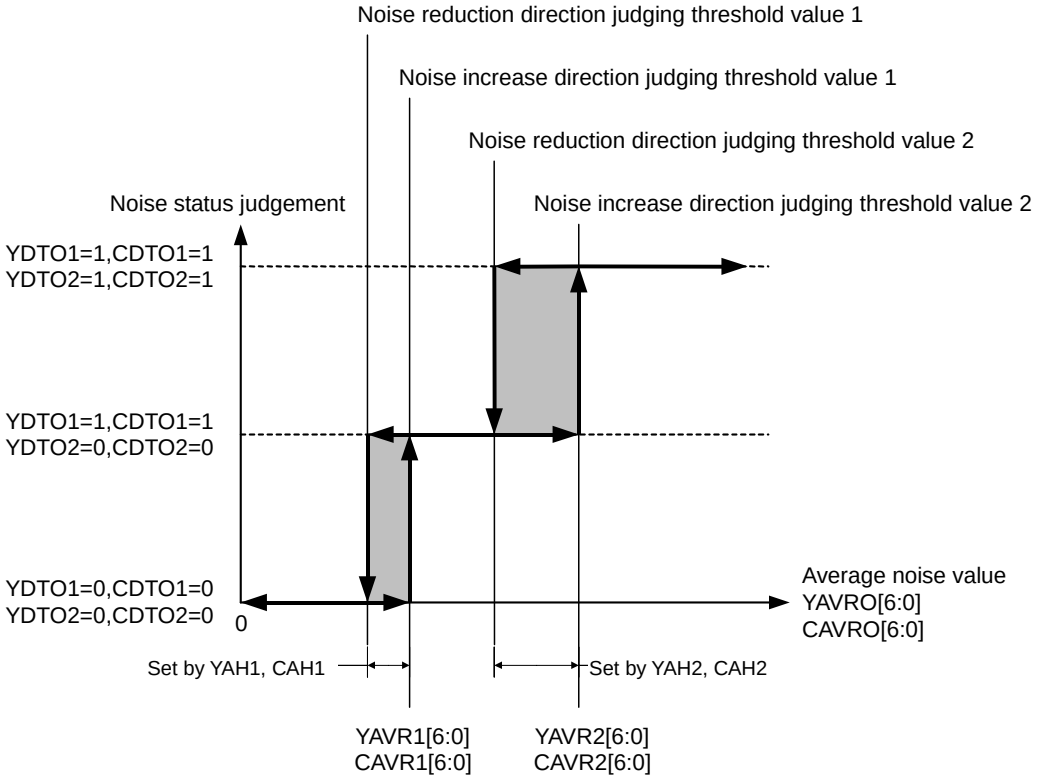


Figure F1-3-7 (5) Noise Status Judgment Transition Diagram

- I^2C-bus interface read of detected noise

  The detected judgment, the average and maximum detected noise values and the noise status signal in the blanking period can be read using the I^2C-bus interface.

Table F1-3-7 (16) I^2C-bus Interface Read of Detected Noise Data

Read data	Sub-address data bit	Data content
YAVRO[6:0]	SUB:58h-bit[6:0]	Luminance judgment average noise value
YDTO1	SUB:58h-bit[7]	Luminance judgment noise status 1 (noise low/medium judgment)
CAVRO[6:0]	SUB:59h-bit[6:0]	Color difference judgment average noise value
CDTO1	SUB:59h-bit[7]	Color difference judgment status 1 (noise low/medium judgment)
YMAXO[4:0]	SUB:5Ah-bit[4:0]	Luminance judgment maximum noise value
YDTO2	SUB:5Ah-bit[7]	Luminance judgment noise status 2 (noise medium/high judgment)
CMAXO[4:0]	SUB:5Bh-bit[4:0]	Color difference judgment maximum noise value
CDTO2	SUB:5Bh-bit[7]	Color difference judgment noise status 2 (noise medium/high judgment)
YBAVRO[6:0]	SUB:5Ch-bit[6:0]	Luminance blanking average noise value
YBDTO	SUB:5Ch-bit[7]	Luminance blanking noise status (basic noise judgment)
CBAVRO[6:0]	SUB:5Dh-bit[6:0]	Color difference blanking average noise value
CBDTO	SUB:5Dh-bit[7]	Color difference blanking noise status (basic noise judgment)

1.3.8 Noise Reduction Auto Mode

The noise reduction setting value of this IC is normally register fixed mode, but considering that the noise level may considerably exceed the set value or the noise level is almost zero, this IC is equipped with an auto mode to automatically perform setting of noise reduction by setting NRAUTO (SUB:49h-bit[0]) and using the maximum noise values (YMAXO[5:0], CMAXO[5:0]) and noise status signals (YDTO1, YDTO2, CDTO1, CDTO2) detected in section 1.3.7.

When NRAUTO = 1, the auto mode of 3-status transition shown in Tables F1-3-8 (1), (2) operates. In auto mode, any of status transition modes (auto mode 1, auto mode 2) can be selected by AMM (SUB:49h-bit[3]) and overall follow-up mode by YANRM (SUB:4Ah-bit[1]), CANRM (SUB:4Bh-bit[1]) can be selected.

The noise reduction setting value in auto mode can be precisely set by AYABN (SUB:4Ah-bit[3]), ACABN (SUB:4Bh-bit[3]), AYNS[1:0] (SUB:4Ch-bit[7:6]), ACNS[1:0] (SUB:4Dh-bit[7:6]), AYLM [1:0] (SUB:4Eh-bit[7:6]), ACLM[1:0] (SUB:4Fh-bit[7:6]), AYMS [1:0] (SUB:50h-bit[7:6]), and AYMOFF[3:1] (SUB:51h-bit[7:5]).

Table F1-3-8 (1) Auto Mode (AMM = 0)

NRAUTO	YBDTO CBDTO	YDTO1 CDTO1	YDTO2 CDTO2	Noise reduction mode (Noise status)	Remarks
0	X	X	X	Register fixed value mode	
1	0	0	X	Auto mode (NROFF status)	Same as NROFF = 1
1	0	1	X	Auto mode (Noise low follow-up status) With upper limit Maximum motion compensation	AYNS [1:0], YCNA [1:0], AYLM [1:0], YCLM [1:0], and AYMS [1:0] are valid. YNRM, CNRM, YABN and CABN settings are ignored; operation is equivalent to YNRM = 1, CNRM = 1, YABN = 0 and CABN = 0.
1	1	X	0	Auto mode (Fixed register status)	All registers other than YMS [4:0] are the same as for the register fixed value mode. AYMS [1:0] is valid.
1	1	X	1	Auto mode (Noise high follow-up status) With lower limit	AYABN, ACABN, AYNS[1:0], YCNS[1:0], AYLM[1:0], YCLM[1:0], AYMS[1:0], and AYMOFF[3:1] are valid.

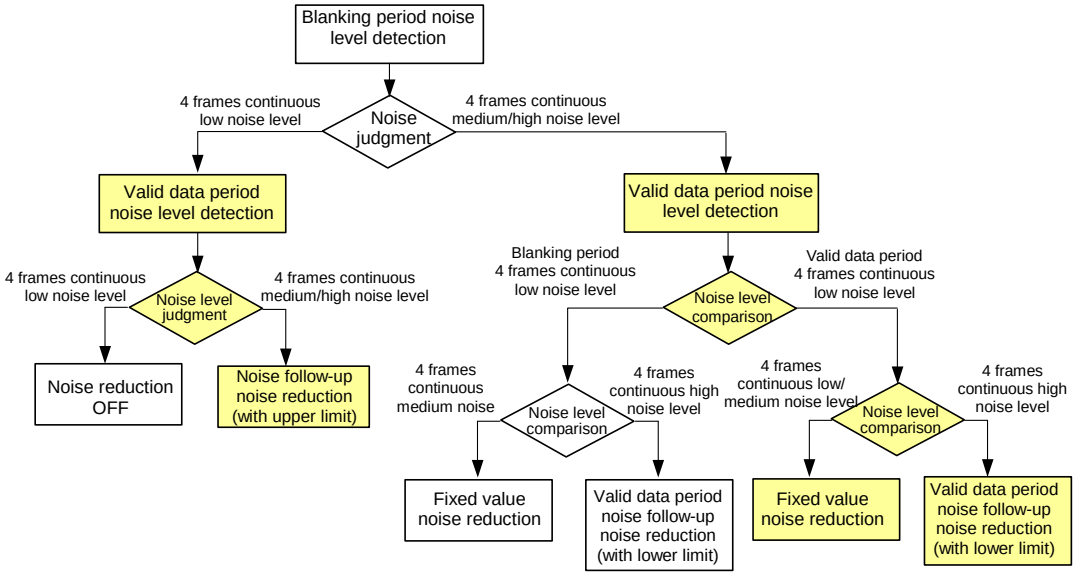


Figure F1-3-8 (1) Auto Mode Judgment Flow (AMM = 0)

Table F1-3-8 (2) Auto Mode 2 (AMM = 1)

NRAUTO	YBDTO CBDTO	YDTO1 CDTO1	YDTO2 CDTO2	Noise reduction mode	Remarks
0	X	X	X	Register fixed value mode	
1	0	0	X	Auto mode (Noise low follow-up status) With upper limit motion compensation maximum	AYNS [1:0], YCNA [1:0], AYLM [1:0], YCLM [1:0], and AYMS [1:0] are valid. YNRM, CNRM, YABN and CABN settings are ignored; operation is equivalent to YNRM = 1, CNRM = 1, YABN = 0 and CABN = 0.
1	0	1	X	Auto mode (Noise low follow-up status) With upper limit	AYNS[1:0], YCNA[1:0], AYLM[1:0], YCLM[1:0], and AYMS[1:0] are valid.
1	1	X	0	Auto mode (Fixed register status)	AYMS[1:0] and AYOFF[3:1] are valid same as register fixed value mode other than YMS[4:0] and YMOFF[3:1].
1	1	X	1	Auto mode (Noise high follow-up status) With lower limit	AYABN, ACABN, AYNS[1:0], YCNA[1:0], AYLM[1:0], YCLM[1:0], and AYMOFF[3:1] are valid.

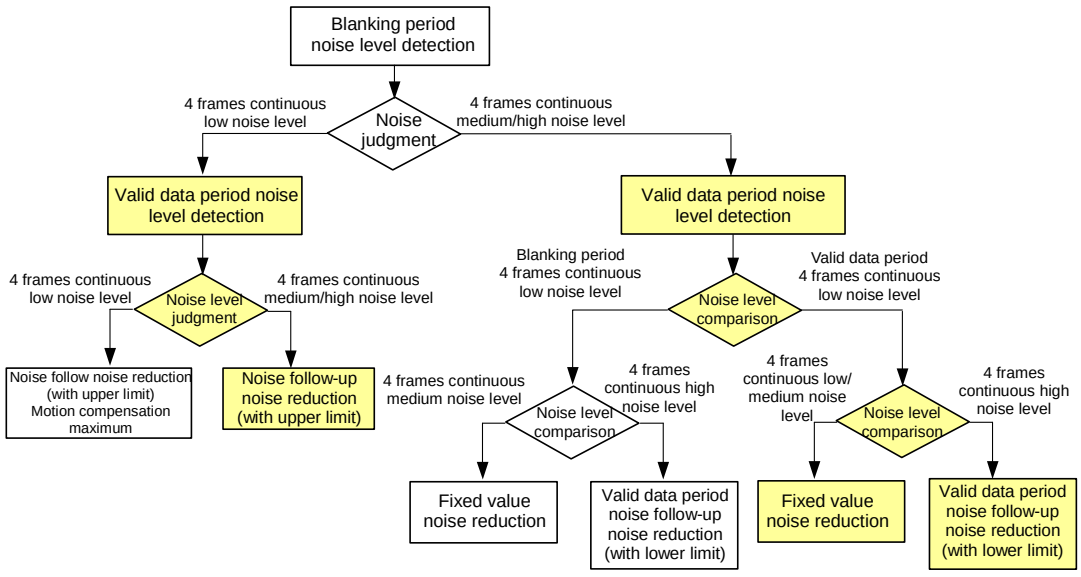


Figure F1-3-8 (2) Auto Mode Judgment Flow (AMM = 1)

(1) Auto Mode Luminance Noise Reduction Mode Settings (AYABN)
Sets whether or not to use the luminance absolute noise reduction mode in the auto mode luminance noise follow-up status (YDTO2 = 1).

Table F1-3-8 (3) Auto Mode Luminance Noise Reduction Mode Settings (YABN = 0)

YDTO2	AYABN	Luminance noise reduction mode
0	X	YABN dependent
1	0	YABN dependent
1	1	Absolute noise reduction mode (equivalent to YABN = 1 operation)

(2) Auto Mode Color Difference Noise Reduction Mode Settings (ACABN)
Sets whether or not to use the color difference absolute noise reduction mode in the auto mode color difference noise follow-up status (CDTO2 = 1).

Table F1-3-8 (4) Auto Mode Color Difference Noise Reduction Mode Settings (CABN = 0)

CDTO2	ACABN	Color Difference Noise Reduction Mode
0	X	CABN dependent
1	0	CABN dependent
1	1	Absolute noise reduction mode (equivalent to CABN = 1 operation)

(3) Auto Mode Luminance Noise Convergence Level Settings (AYNS[1:0])
Sets whether or not to use the luminance noise convergence level automatic setting in the auto mode luminance noise follow-up status (YDTO2 = 1).
When AMM = 0, noise reduction stops with YDTO1 = 0, so the luminance noise convergence level is ignored.

Table F1-3-8 (5) Auto Mode Luminance Noise Convergence Level Settings

YBDTO	YDTO1	YDTO2	AYNS [1]	AYNS [0]	Luminance noise convergence level
0	X	X	0	X	YNS[5:0]
			1	0	YNS[5:0] + YMAXO[4:0](max:3Fh)
			1	1	Smaller of YMAXO[4:0] x 3(max:3Fh) and YNS[5:0]
1	X	0	X	X	YNS[5:0]
1	X	1	0	X	YNS[5:0]
			1	0	YNS[5:0] + YMAXO[4:0](max:3Fh)
			1	1	Larger of YMAXO[4:0] x 3(max:3Fh) and YNS[5:0]

(4) Auto Mode Color Difference Noise Convergence Level Settings (ACNS[1:0])
Sets whether or not to use the color difference noise convergence level automatic setting in the auto mode noise follow-up status (CDTO2 = 1).
When AMM = 0, noise reduction stops with CDTO1 = 0, so the color difference noise convergence level is ignored.

Table F1-3-8 (6) Auto Mode Color Difference Noise Convergence Level Settings

CBDTO	CDTO1	CDTO2	ACNS		Color Difference Noise Convergence Level
			[1]	[0]	
0	X	0	0	X	CNS[5:0]
			1	0	CNS[5:0] + CMAXO[4:0](max:3Fh)
			1	1	Smaller of CMAXO[4:0] x 3(max:3Fh) and CNS[5:0]
1	X	0	X	X	CNS[5:0]
1	X	1	0	X	CNS[5:0]
			1	0	CNS[5:0] + CMAXO[4:0](max:3Fh)
			1	1	Larger of CMAXO[4:0] x 3(max:3Fh) and CNS[5:0]

(5) Auto Mode Luminance Noise Upper Limit Level Settings (AYLM[1:0])
Sets whether or not to use the luminance noise upper limit level automatic setting in the auto mode luminance noise follow-up status (YDTO2 = 1).
When AMM = 0, noise reduction stops with YDTO1 = 0, so the luminance noise upper limit level is ignored.

Table F1-3-8 (7) Auto Mode Luminance Noise Upper Limit Level Settings

YBDTO	YDTO1	YDTO2	AYLM		Luminance noise upper limit level
			[1]	[0]	
0	X	0	0	X	YLM[4:0]
			1	0	Smaller of YMAXO[4:0] x 0.75(max:1Fh) and YLM[4:0]
			1	1	Smaller of YMAXO[4:0](mx:1Fh) and YLM[4:0]
1	X	0	X	X	YLM[4:0]
1	X	1	0	X	YLM[4:0]
			1	0	Larger of YMAXO[4:0] x 0.75(max:1Fh) and YLM[4:0]
			1	1	Larger of YMAXO[4:0](max:1Fh) and YLM[4:0]

(6) Auto Mode Color Difference Noise Upper Limit Level Settings (ACLM[1:0])
Sets whether or not to use the color difference noise upper limit level automatic setting in the auto mode color difference noise follow-up status (CDTO2 = 1).
When AMM = 0, noise reduction stops with CDTO1 = 0, so the color difference noise upper limit level is ignored.

Table F1-3-8 (8) Auto Mode Color Difference Noise Upper Limit Level Settings

CBDTO	CDTO1	CDTO2	ACLM		Color Difference noise upper limit level
			[1]	[0]	
0	X	0	0	X	CLM[4:0]
			1	0	Smaller of CMAXO[4:0] x 0.75 (max:1Fh) and CLM[4:0]
			1	1	Smaller of CMAXO[4:0](max:1Fh) and CLM[4:0]
1	X	0	X	X	CLM[4:0]
1	X	1	0	X	CLM[4:0]
			1	0	Larger of CMAXO[4:0] x 0.75(max:1Fh) and CLM[4:0]
			1	1	Larger of CMAXO[4:0](max:1Fh) and CLM[4:0]

(7) Auto Mode Luminance Continuous Code Motion Detection Level Settings (AYMS[1:0])
Sets whether or not to use the luminance continuous code motion detection level automatic setting except in the auto mode luminance noise follow-up status (YDTO2 = 0).
When AMM = 0, noise reduction stops with YDTO1 = 0, so the luminance continuous code motion detection level is ignored.

Table F1-3-8 (9) Luminance Continuous Code Motion Detection Level Settings

YDTO2	AYMS		Luminance continuous code motion detection level
	[1]	[0]	
0	0	X	YMS[4:0]
0	1	0	Smaller of YMAXO[4:0]/2(max:1Fh) and YMS[3:0]
0	1	1	Smaller of YMAXO[4:0](max:1Fh) and YMS[3:0]
1	X	X	YMS[4:0]

(8) Auto Mode Luminance Motion Compensation Stop Settings (AYMOFF[3:1])
Sets whether or not to use the luminance motion compensation stop automatic setting in the auto mode 1 luminance noise follow-up status (YDTO2 = 1) and the auto mode 2 (AMM = 1) luminance fixed register 2 status (YDTO = 1).

Table F1-3-8 (10) Auto Mode 1 Luminance Motion Compensation Stop Settings (AMM = 0)

YDTO2	AYMOFF[a]	Luminance motion compensation
0	X	Motion compensation YMOFF[a] dependent
1	0	Motion compensation YMOFF[a] dependent
1	1	Motion compensation stopped (equivalent to YMOFF[a] = 1)

Table F1-3-8 (11) Auto Mode 2 Luminance Motion Compensation Stop Settings (AMM = 1)

YDTO1	AYMOFF[a]	Luminance motion compensation
0	X	Motion compensation YMOFF[a] dependent
1	0	Motion compensation YMOFF[a] dependent
1	1	Motion compensation stopped (equivalent to YMOFF[a] = 1)

Table F1-3-8 (12) All Follow-up Mode (YANRM = 1,CANRM = 1)

NRAUTO	YBDTO CBDTO	YDTO1 CDTO1	YDTO2 CDTO2	Noise reduction modes (Noise status)	Remarks
0	X	X	X	Register fixed value mode	
1	0	0	X	Auto mode (Large noise follow-up motion compensation)	Equivalent to YMOFF[3:0] = 0h AYABN, ACABN, AYNS[1:0], YCNS[1:0], AYLM[1:0], YCLM[1:0], and AYMS[1:0] are effective. 1/4 of the NR parameter fixed value is the maximum.
1	0	1	X	Auto mode (Large noise follow-up motion compensation)	Equivalent to YMOFF[3:0] = 2h AYABN, ACABN, AYNS[1:0], YCNS[1:0], AYLM[1:0], YCLM[1:0], AYMS[1:0], and AYMOFF[3:1] are effective. 1/2 of NR parameter fixed value is the maximum.
1	1	X	0	Auto mode (Medium noise follow-up motion compensation)	Equivalent to YMOFF[3:0] = 2h AYABN, ACABN, AYNS[1:0], YCNS[1:0], AYLM[1:0], YCLM[1:0], AYMS[1:0], and AYMOFF[3:1] are effective. 1/2 of NR parameter fixed value is the maximum.
1	1	X	1	Auto mode (Small noise follow-up motion compensation)	Equivalent to YMOFF[3:0] = 6h AYABN, ACABN, AYNS[1:0], YCNS[1:0], AYLM[1:0], YCLM[1:0], AYMS[1:0], and AYMOFF[3:1] are effective. The NR parameter fixed value is the maximum.

(9) Auto Mode Luminance Adaptive Margin Settings
In the auto mode, the luminance adaptive margin is set independently of YFAM.

Table F1-3-8 (13) Luminance Adaptive Margin Settings

YDTO2	Luminance adaptive margin setting
0	YFAM dependent
1	Equivalent to YFAM = 1 operation

(10) Auto Mode Color Difference Adaptive Margin Settings
In the auto mode, the color difference adaptive margin is set independently of CFAM.

Table F1-3-8 (14) Color difference Adaptive Margin Settings

CDTO2	Color Difference adaptive margin setting
0	CFAM dependent
1	Equivalent to CFAM = 1 operation

(11) Auto Mode Adaptive 2DNROFF Settings
When A2OFF = 1 is set, the noise status of the blanking period is the noise follow-up level and where YDTO1 or CDTO1 is 1, the adaptive 2DNR is set to be OFF.

Table F1-3-8 (15) Adaptive 2DOFF Settings

Blanking period noise	YDTO1 or CDTO1	Adaptive 2DNR setting
0	X	NR2OFF dependent
1	0	NR2OFF dependent
1	1	Adaptive 2DNROFF

[Notes on Using Noise State Detection and Auto Mode Noise Reduction]

Using the noise state detection and auto mode noise reduction functions of this IC can degrade picture quality because of the possibility of wrong detection of noise state due to persistence of vision . Therefore, check the following points beforehand and then use these functions:

1. Noise state detection is performed once in vertical blanking in one frame. Since it is not possible to correctly determine the noise detection position by factors such as TV system, area, input source (VTR, DVD), pre-stage tuner and video decoder, accurate detection of the noise state is disabled. Therefore, confirm the operation prior to using these functions.

2. Where the input source has been recorded by a home VTR, the data of the blanking period in particular is uncertain. Do not use noise reduction in the noise follow-up status (YDTO2 = 1, CDTO2 = 1) unless you have determined that there is no problem.
   (There are some cases where the VTR is input as RF input, so take appropriate measures such as preventing the noise follow-up status from operating on the RF channel for external input.)

3. Since VTR input is assumed for an external input source, do not use the noise follow up status.

4. In composite video input signal, if only that position is selectable in which data can be in the position of noise state detection, enable the luminance link mode for color difference by setting ACY=1 considering that luminance data can enter the color difference data or do not use the color difference auto mode.

5. There are cases of no noise in the vertical blanking period, or a part of the vertical blanking period, by a pre-stage tuner or video decoder. Perform NRDTP[3:0] setting and make sure to select a position at which noise level is the same as the valid data.
   If noise is not detectable within the settable vertical blanking period at NRDTP[3:0] setting, then it is not possible to use the noise state detection and the auto mode noise reduction.

6. Regarding the video signals added later of devices such as DVD, cameras, and digital recording, the noise level of the added sync signals is detected as the noise state because the noise state detection is performed in the vertical blanking period.

7. Noise state detection is not performed at all times if the hysteresis characteristic of noise state detection is not valid (frequent occurrence of state switching). The noise detection is performed by NRDTON = 1 (8 frames or more) at the time of RF channels or input source switching only. Thereafter, settings to hold the noise state etc., at NRDTON = 0 up to the next switching become necessary.

2. OTHER FUNCTIONS

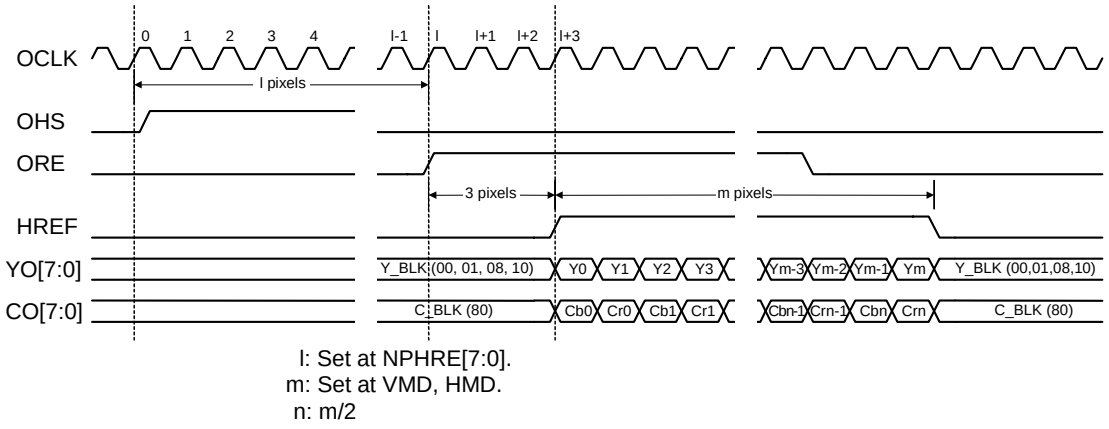
2.1 REF Pin Output

Set the I2C-bus setting register REFSL[1:0] (SUB:60h-bit[4:3]) to select a horizontal reference signal, color difference select signal, or effective area signal for output from the HREF pin.

Table F2-1 REF Pin Output Selection

REFSL		REF pin output
[0]	[1]	
0	0	Horizontal reference signal
0	1	Color difference select signal
1	0	Effective area signal (horizontal reference signal + vertical blanking signal)
1	1	Output system filed pulse signal

- Horizontal reference signal
  This signal is a signal for default valid data period 1 and blanking period 0. This signal can be used as the reference for separating Cb, Cr, etc.



l: Set at NPHRE[7:0].
m: Set at VMD, HMD.
n: m/2

Figure F2-1 (1) Horizontal Reference Signal

- Color difference select signal
  The color difference select signal is a signal that toggles between 0 (at valid period start) and ICLK. It can be used as a signal for separating Cb and Cr.

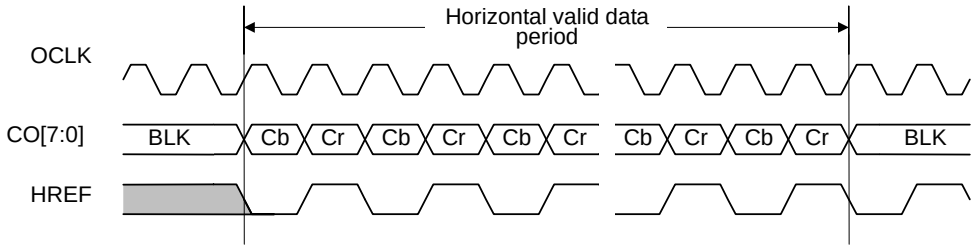


Figure F2-1 (2) Color Difference Select Signal Timing

- Effective area signal
  The effective area signal is created from a synthesis of the vertical valid blanking signal (vertical valid data period: 1, vertical blanking period: 0) and the horizontal reference signal (horizontal valid data period: 1, horizontal blanking period: 0). It is output as a signal with valid data period: 1, blanking period: 0.

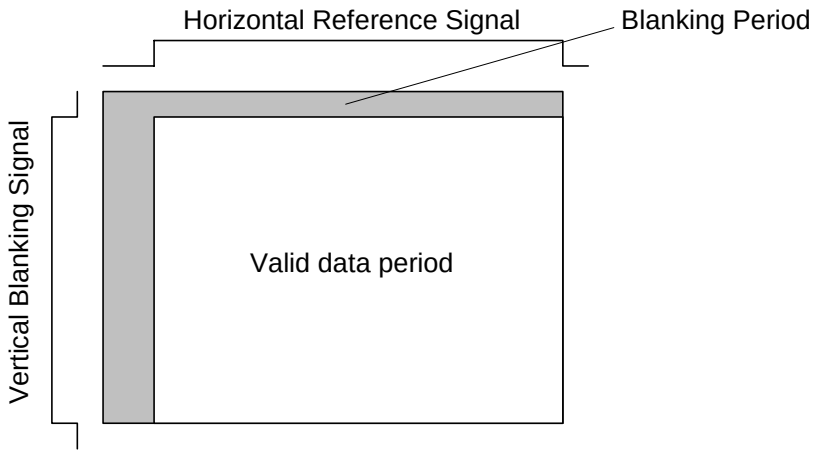


Figure F2-1 (3) Effective Area

- Field pulse signal
  Normally, the field pulse signal detected from the IVS and IHS phases is output.
  In the ITU-R BT.656 mode, an F signal separated from SAV, EAV is output.

2.2 Output Polarity Settings for the OVS, OHS and HREF Pins

You can reverse the polarity of the sync signals output by the OVS, OHS, and HREF pins by setting the I^2C-bus settings registers OVSINV(SUB:61h-bit[0]), OHSINV(SUB:61h-bit[1]), and HREFINV(SUB:61h-bit[2]).

Table F2-2 (1) OVS Pin Polarity

OVSINV	OVS output
0	Same polarity as input
1	Reverse polarity of input

Table F2-2 (2) OVS Pin Polarity

OHSINV	OHS output
0	Same polarity as input
1	Reverse polarity of input

Table F2-2 (3) HREF Pin Polarity

HREFINV	HREF output
0	Same polarity as internally generated
1	Reverse polarity of internally generated

2.3 Output Signal Level Range Settings

ITU-R601 compliance is specified for the input signal level range for this IC. Output is normally the same as input, but where 00h and FFh are input for the valid data period, you can set the output signal level range to be 01h to FEh by setting the I^2C-bussettings register R601(SUB:40h-bit[6]) = 1. In such cases, even if YBLS[1:0] is used to set the invalid data mask signal level for luminance signals to 00h, a signal level of 01h will be output as the output lowest signal level.

Table F2-3 Output Signal Level Range

R601	Output signal level range
0	00h to FFh
1	01h to FEh

2.4 CLKO Output Setting

As a data latch for post-stage ICs of this IC, the CLKO pin can output a clock synchronized with data. Enable control of the CLKO pin is possible with CKEN (SUB:60h-bit[7]).
Further, by setting CKINV (SUB:60h-bit[5]) as necessary, the polarity of the CLKO output clock can be inverted.

Table F2-4 CLKO Output

CKEN	CKSL	CKINV	CLKO output
0	**X**	**X**	**Hi-Z(Pulldown50kΩ)**
1	0	0	IICLK
1	0	1	IICLK inversion
1	1	0	ICLK
1	1	1	ICLK inversion

* In the 16-bit input mode, IICLK = ICLK.

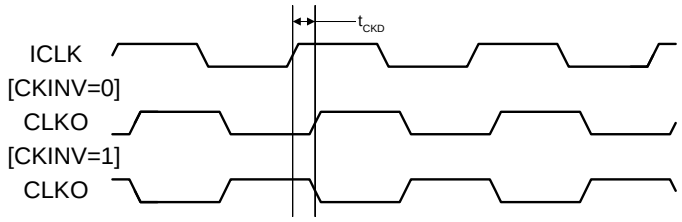


Figure F2-4 (1) CLKO Output Timing (16-bit mode)

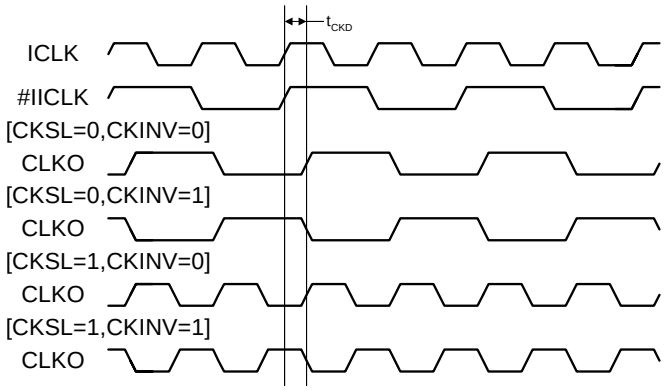


Figure F2-4 (2) CLKO Output Timing (Input 8-bit/ ITU-R BT.656 mode)

2.5 Input Through Mode

By setting the register setting PASS(SUB:72h-bit[0]) = 1, the data (YI[7:0], CI[7:0]) and sync signals (IVS, IHS) that are input to the input system pins are directly output from the output system data (YO[7:0], CO[7:0]) and sync signal (OVS, OHS) pins. IHS is output from HREF pin at this time.

Table F2-5 Input Through Mode

Input pin	Output pin
YI[7:0]	YO[7:0]
CI[7:0]	CO[7:0]
IVS	OVS
IHS	OHS HREF

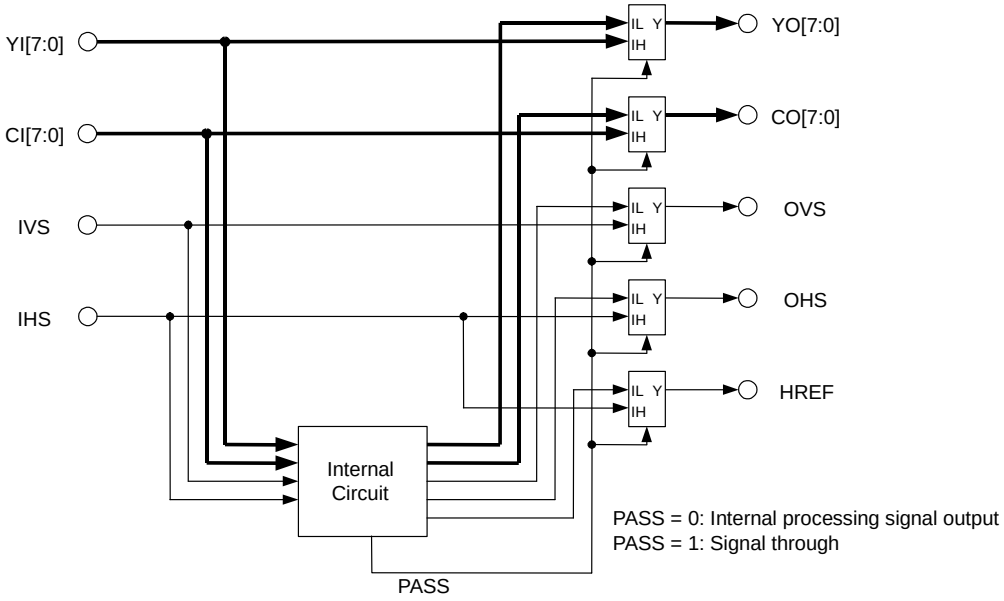


Figure F2-5 Input Through Mode

2.6 Output Disable

By setting the OUTDS(SUB:72h-bit[1]) = 1, the output pins (YO[7:0], CO[7:0], OVS, OHS, HREF, CLKO) are set in the Hi-Z state. Note that CO[7:0] and CLKO pins are internally pulled down with 50 kΩ.

3. I²C-BUS INTERFACE

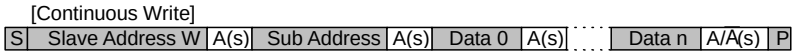
The IC incorporates an interface that conforms to the I²C-bus interface standards of Philips. This allows setting a filter selection etc., by an external micro-computer etc.
The slave address is set to 10111XX0 to write to and 10111XX1 to read from the IC.
Here, XX is set by the user with external setting pins. Namely, the slave address 10111, SLA2, SLA1, W/R is obtained by using SLA2 and SLA1.

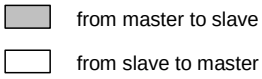
Table F3 (1) Slave Address

SLA2	SLA1	Slave Address (Write)	Slave Address (Read)
0	0	B8h	B9h
0	1	BAh	BBh
1	0	BCh	BDh
1	1	BEh	BFh

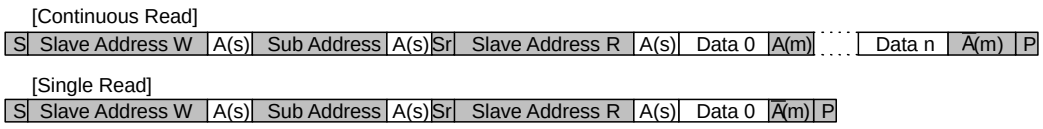
- I²C-bus format
  Input format of the I²C-bus interface is shown below.

Write Format





Read Format



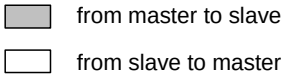


Table F3 (2) Description of the I²C-bus Format

Symbol	Description
S	Start condition
Sr	Restart condition
Slave Address W	Slave address 1011_1XX0 (XX is set externally.)
Slave Address R	Slave address 1011_1XX1 (XX is set externally.)
A(s)	Acknowledge (Slave side generates.)
A(m)	Acknowledge (Master side generates.)
Sub Address	Sub-address byte
Data n	Data byte
P	Stop condition

As mentioned above, it is possible to read/write data at successive sub-addresses starting from a certain sub-address (continuous read/write). Read/write to a non-contiguous sub-address is performed by repeating the acknowledge and stop conditions of input format (single read/write) of the above-mentioned data 0.
The IC does not return acknowledge in the following cases:

Slave-address does not match.
Non-existing sub-address is specified.

The input timing diagram is shown below.

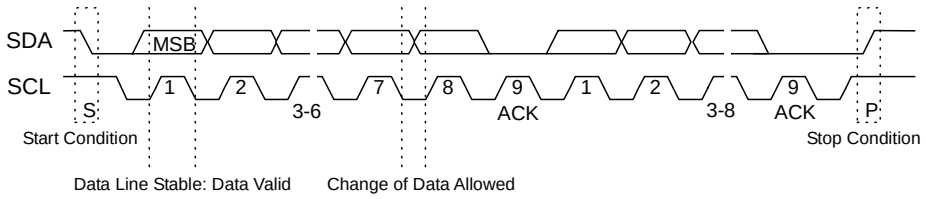


Figure F3 I²C-bus Interface Basic Timing

- Setting internal reflect timing
  Input System: IVS fall position (IVSINV = 0) or IVS rise position (IVSINV = 1).

* Settings by I²C-bus interface should be made by avoiding the position of above-mentioned setting internal reflect timing. If the setting is performed at a position that contains the above timing, the setting may not finish inside the same field.

DESCRIPTION OF THE REGISTERS

The IC is equipped with 54 bytes (sub-address 40h to 7Fh) of sub-address registers (8-bit unit) that can access by the I^2C-bus interface.
Write cycle of the I^2C-bus interface returns acknowledge by sub-addresses from 40h to 7Fh.
Regarding the read-only sub-addresses, acknowledge is returned but data write is not performed.
Settings such as mode setting, noise reduction function, memory control function, sync signals generation become possible by accessing these registers.
All writable registers become readable also.

Note: Blank (reserved) registers must be set to 0.

1. Map of the Registers

Table R1 (1) Map of the Registers (40h to 47h)

SA	DATA								Initial value	Sync
	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0		
40h	IRMON	R601	—	—	HMD		VMD		00h	IVS
					1	0	1	0		
41h	—	POFF	IHES	ICINV	—	—	R656	DISEL	00h	—
42h	FCON	—	—	IVEM	IFLS	IFINV	IHSINV	IVSINV	00h	IVS
43h	—	—	—	STLM		STL			00h	IVS
				1	0	2	1	0		
44h	—	—	—	—	NPVWE				08h	IVS
					3	2	1	0		
45h	NPHWE								80h	IVS
	7	6	5	4	3	2	1	0		

* (—): Reserved register

Table R1 (2) Map of the Registers (48h to 5Fh)

SA	DATA								Initial value	Sync
	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0		
48h	—	FNRM		NR2OFF	NRDEMO			NROFF	01h	IVS
		1	0		2	1	0			
49h	PNON	NDTC	NRDTF	—	AMM	ACY	NRDTON	NRAUTO	00h	IVS
4Ah	YSLT				AYABN	YABN	YFAM	YNRM	10h	IVS
	3	2	1	0						
4Bh	CSLT				ACABN	CABN	CFAM	CNRM	10h	IVS
	3	2	1	0						
4Ch	AYNS		YNS						18h	IVS
	1	0	5	4	3	2	1	0		
4Dh	ACNS		CNS						0Fh	IVS
	1	0	5	4	3	2	1	0		
4Eh	AYLM		AYNDL	YLM					06h	IVS
	1	0		4	3	2	1	0		
4Fh	ACLM		ACNDL	CLM					03h	IVS
	1	0		4	3	2	1	0		
50h	AYMS		A2OFF	—	YMS				04h	IVS
	1	0			3	2	1	0		
51h	AYMOFF			—	YMOFF				06h	IVS
	3	2	1		3	2	1	0		
52h	CMY	—	—	CMOFF					80h	IVS
				4	3	2	1	0		
53h	YAH1	—	YAVR1						00h	IVS
			5	4	3	2	1	0		
54h	CAH1	—	CAVR1						00h	IVS
			5	4	3	2	1	0		
55h	YAH2	YAVR2							7Fh	IVS
		6	5	4	3	2	1	0		
56h	CAH2	CAVR2							7Fh	IVS
		6	5	4	3	2	1	0		
57h	DTPSL	—	NRDTP				CNAMS	YNAMS	00h	IVS
			3	2	1	0				
58h	YDTO1	YAVRO							00h	IVS (R)
		6	5	4	3	2	1	0		
59h	CDTO1	CAVRO							00h	IVS (R)
		6	5	4	3	2	1	0		
5Ah	YDTO2	—	—	YMAXO					00h	IVS (R)
				4	3	2	1	0		
5Bh	CDTO2	—	—	CMAXO					00h	IVS (R)
				4	3	2	1	0		
5Ch	YBDTO	YBAVRO							00h	IVS (R)
		6	5	4	3	2	1	0		
5Dh	CBDTO	CBAVRO							00h	IVS (R)
		6	5	4	3	2	1	0		

* (—): Reserved register
* Sub-addresses 58h to 5Dh are read-only registers.
* Sub-addresses 5Eh and 5Fh are reserved registers.

Table R1 (3) Map of the Registers (60h to 6Fh)

SA	DATA								Initial value	Sync
	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0		
60h	CKEN	CKSL	CKINV	REFSL		—	DOSEL	—	00h	—
				1	0					
61h	—	—	—	—	—	HREFINV	OHSINV	OVSINV	00h	—

* (—): Reserved register
* Sub-addresses 62h to 6Fh are reserved registers.

Table R1 (4) Map of the Registers (70h to 7Fh)

SA	DATA								Initial value	Sync
	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0		
70h	TST1								00h	—
	7	6	5	4	3	2	1	0		
71h	TST1								00h	—
	15	14	13	12	11	10	9	8		
72h	RLTG	—	—	—	—	—	OUTDS	PASS	00h	—
73h	—	—	RYNS						00h	IVS (R)
			5	4	3	2	1	0		
74h	—	—	RCNS						00h	IVS (R)
			5	4	3	2	1	0		
75h	RYABN	RYNRM	RYNR OFF	RYLM					00h	IVS (R)
				4	3	2	1	0		
76h	RCABN	RCNRM	RCNR OFF	RCLM					00h	IVS (R)
				4	3	2	1	0		
77h	RYMOFF			RNR2 OFF	RYMS				00h	IVS (R)
	3	2	1		3	2	1	0		
78h	—	—	—	—	—	—	HSSEL	ISYNC	00h	—
79h	SHSDL								00h	—
	7	6	5	4	3	2	1	0		

* (—): Reserved register
* Sub-addresses 7Ah to 7Fh are reserved registers.

2. Description of the Registers

2.1 Mode Setting

SUB_ADDRESS = 40h (W/R): Write/read common mode setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	IRMON	R601	(Reserved)	(Reserved)	HMD		VMD	
					1	0	1	0

VMD[1:0] Initial value: 00; Setting range: 00 to 11
Sets vertical lines operation mode.
In normal operation, 2 and 3 are not set.
VMD[0] is validated when IRMON = 1.

Table R2-1 (1) Vertical Line Operation Mode Setting

VMD		Vertical line operation mode setting
[1]	[0]	
0	**0**	**625-line mode**
0	1	525-line mode
1	0	(Not settable)
1	1	

HMD[1:0] Initial value: 00; Setting range: 00 to 11
Sets horizontal effective pixels (sampling frequency) mode.
In normal operation, 3 is not set.
HMD[0] is validated at IRMON = 1.

Table R2-1 (2) Horizontal Valid Pixel Mode Setting

HMD		Horizontal valid pixels mode setting	Sampling frequency
[1]	[0]		
0	**0**	**720-pixel mode**	13.5 MHz
0	1	Square (768/640) pixel mode	14.75/12.272727 MHz
1	0	768-pixel mode	14.75/14.31818 MHz
1	1	Test mode	—

R601 Initial value: 0; Setting range: 0 to 1
Sets input/output valid data signal level.
This setting is necessary if the input signal level conforms to ITU-R BT.601.

Table R2-1 (3) Input/Output Valid Data Signal Level Range

R601	Input signal level range
0h	**00h to FFh**
1h	ITU-R BT.601 (01h to FEh)

IRMON Initial value: 0; Setting range: 0 to 1
Sets external pin/internal registers switching for memory control mode setting

Table R2-1 (4) External Pin Setting Switching Setting

IRMON	Register set mode setting
0	**External pin (MODE[2:0])**
1	Internal registers (VMD[0], HMD[0], DISEL)

2.2 Input System Settings

2.2.1 Input data setting

SUB_ADDRESS = 41h(W/R): Input data setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	(Reserved)	POFF	IHES	ICINV	(Reserved)	(Reserved)	R656	DISEL

DISEL Initial value: 0; Setting range: 0 to 1

Sets input data format.

When R656 = 0, the input data format of 16-bit YCbCr 4:2:2 or 8-bit YCbCr 4:2:2 is selectable.

This register is valid when IRMON = 1. When IRMON = 0, the MODE2 external pin performs the similar operation.

R656 Initial value: 0; Setting range: 0 to 1

Sets input data format.

When R656 = 1, the input data format supports the ITU-R BT.656 standards regardless of DISEL and MODE2 settings.

Table R2-2-1 (1) Input Data Format Setting

IRMON	MODE2	DISEL	R656	Input data format
0	0	X	0	16-bit 4:2:2 YCbCr
1	X	0	0	
0	1	X	0	8-bit 4:2:2 YCbCr
1	X	1	0	
X	X	X	1	ITU-R BT.656 mode

ICINV Initial value: 0; Setting range: 0 to 1

Sets internal input system clock (IICLK) polarity.

Sets the polarity of IICLK (ICLK frequency-divided by 2) generated in the input 8-bit mode and ITU-R BT.656 mode.

This setting is not in synchronization with IVS.

Table R2-2-1 (2) IICLK Polarity Setting

ICINV	IICLK polarity
0	At IHS rise reset: 1
1	At IHS rise reset: 0

IHES Initial value: 0; Setting range: 0 to 1

Sets IHS edge for internal input system clock (IICLK) reset

Selects the reset timing of IICLK generated in 1H period at the fall or rise of IHS.

Table R2-2-1 (3) IHS Edge Setting for IICLK Reset

IHES	IHS edge for H reset
0	**Rise**
1	Fall

POFF Initial value: 0; Setting range: 0 to 1

Sets ITU-R BT.656 mode parity check.

Table R2-2-1 (4) ITU-R BT.656 Mode Parity Check Setting

POFF	Parity check
0	**ON**
1	OFF

2.2.2 Input system memory control mode setting

SUB_ADDRESS = 42h(W/R): Input system memory control mode setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	FCON	(Reserved)	(Reserved)	IVEM	IFLS	IFINV	IHSINV	IVSINV

IVSINV Initial value: 0; Setting range: 0 to 1

Sets input polarity (timing edge) of input system vertical synchronization signal (IVS).
The IC operates with the fall of IVS positive polarity as a reference. However, in case the IVS input is of negative polarity, it is possible to match the polarity reference such as the rise of positive polarity.

Table R2-2-2 (1) IVS Input Polarity (Edge) Setting

IVSINV	IVS input polarity 1	IVS input polarity 2
0	**Positive polarity (Fall)**	**Negative polarity (Fall)**
1	Negative polarity (Rise)	Positive polarity (Rise)

IHSINV Initial value: 0; Setting range: 0 to 1

Sets input polarity (timing edge) of input system horizontal synchronization signal (IHS).
The IC operates with the rise of IHS positive polarity as a reference. However, if the IHS input is of negative polarity, it is possible to match the polarity reference such as making the fall of positive polarity.

Table R2-2-2 (2) IHS Input Polarity (Edge) Setting

IHSINV	IHS input polarity 1	IHS input polarity 2
0	**Positive polarity (Rise)**	**Negative polarity (Rise)**
1	Negative polarity (Fall)	Positive polarity (Fall)

IFINV Initial value: 0; Setting range: 0 to 1

Sets the polarity of input system detection field pulse.

Table R2-2-2 (3) Polarity Setting of Input System Detection Field Pulse

IFINV	Detection field pulse
0	**Decision result**
1	Decision result inversion

IFLS Initial value: 0; Setting range: 0 to 1

Sets input system field decision mode selection.

Table R2-2-2 (4) Input System Field Decision Mode Selection Setting

IFLS	Detection field pulse
0	**IHS decision**
1	0.5H pulse decision

IVEM Initial value: 0; Setting range: 0 to 1

Sets input system vertical reset compensation mode.

When IVEM = 1, inverts the detection field and performs 1 line delay reset for field B.

Table R2-2-2 (5) Input System Vertical Reset Compensation Mode Setting

IVEM	IVS reset compensation
0	**No compensation**
1	Compensation (Field inversion, field B 1 line delay vertical reset)

FCON Initial value: 0; Setting range: 0 to 1

Sets successive same field input countermeasure.

Automatically generates both fields by detecting 8 or more successive same fields.

Table R2-2-2 (6) Detection Field Pulse Polarity Setting

FCON	Detection field pulse
0	**Decision result mode**
1	Automatic field generation mode

2.2.3 Memory control setting 1 (write stop)

SUB_ADDRESS = 43h(W/R): Memory write stop setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	(Reserved)	(Reserved)	(Reserved)	(Reserved)	(Reserved)	STL		
						2	1	0

STL[2:0] Initial value: 000; Setting range: Refer to Table R2-2-3.
Sets input data write stop control.
When data write stops, holds the field data just before the data write stops.

Table R2-2-3 (1) Input Data Write Stop Setting

STL			Input data write
[2]	[1]	[0]	
0	0	0	Possible (field B recovery)
0	1	0	Possible (field A recovery)
1	X	0	Possible (arbitrary field recovery)
0	0	1	Stop (field A data hold)
0	1	1	Stop (field B data hold)
1	X	1	Stop (arbitrary field data hold)

STLM[1:0] Initial value: 0; Setting range: 0 to 1
Sets output when input data writing stop is controlled.

Table R2-2-3 (2) Output Mode Settings when Input Data Writing is Stopped

STLM		Output mode
[1]	[0]	
X	**0**	**Field output mode**
0	1	Frame output mode (normal)
1	1	Frame output mode (median)

2.2.4 Memory control setting 2 (phase adjustment)

SUB_ADDRESS = 44h(W/R): Input system memory control vertical phase adjustment setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	(Reserved)	(Reserved)	(Reserved)	(Reserved)	NPVWE			
					3	2	1	0
SUB_ADDRESS = 45h(W/R): Input system memory control horizontal phase adjustment setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	NPHWE							
	7	6	5	4	3	2	1	0

NPVWE[3:0] Initial value: 1000; Setting range: 0001 to 1111
When INSINV = 0, sets the number of lines (IHS input count) from the IVS fall position up to the vertical standard write start position.
When IVSINV = 1, the number of lines is set from the IVS rise position.

NPHWE[7:0] Initial value: 1000_0000; Setting range: 0000_0001 to 1111_1111

When IHSINV = 0, sets the number of pixels from the IHS rise position up to the horizontal standard write start position.

When IHSINV = 1, sets the number of pixels from the IHS fall position.

2.3 Noise Reduction Settings

2.3.1 Noise reduction stop/demo mode setting

SUB_ADDRESS = 48h(W/R): Noise reduction stop/demo mode setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	(Reserved)	FNRM		NR2OFF	NRDEMO			NROFF
		1	0		2	1	0	

NROFF Initial value: 1; Setting Range: 0 to 1
Sets On/Off of field-recursive (3-dimension) noise reduction function.
Although data is written to the memory when the setting is off, all the noise reduction functions are stopped.

NRDEMO[2:0] Initial value: 000; Setting range: Refer to Table R2-3-1(1).
Sets On/Off of noise reduction function demo mode.
Motion compensation stop is the same as YMOFF[3:0] = Fh, CMOFF[4:0] = 1Fh.

Table R2-3-1 (1) Noise Reduction Stop/Demo Mode On/Off Setting

NROFF	NRDEMO			Left side screen	Right side screen
	[0]	[1]	[2]		
0	0	0	0	NR setting value	NR setting value
1	**X**	**X**	**X**	**Stop NR.**	**Stop NR.**
0	1	X	X	Stop NR.	NR setting value
0	0	1	X	NR setting value	Adaptive NR forced ON
0	0	0	1	NR setting value	Adaptive 2DNR forced ON

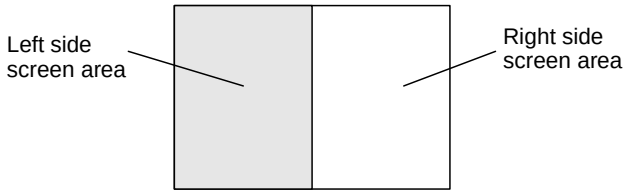


Figure R2-3-1 Noise Reduction Demo Screen

NR2OFF Initial value: 0; Setting range: 0 to 1
Sets the ON/OFF of the 2D (between lines) noise reduction feature.

Table R2-3-1 (2) 2D Noise Reduction Settings

NR2OFF	2D noise reduction
0	**ON (adaptive)**
1	OFF

FNRM[1:0] Initial value:0; Setting range: 00 to 11
Sets the noise reduction recursive mode.

Table R2-3-1 (3) Recursive Mode Settings

FNRM		Mode
[1]	[0]	
0	**0**	**Frame / field adaptive mode**
0	1	Frame mode
1	X	Field mode

2.3.2 Noise reduction auto mode setting

SUB_ADDRESS = 49h(W/R): Noise reduction auto mode setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	PNON	NDTC	NRDTF	(Reserved)	AMM	ACY	NRDTON	NRAUTO

NRAUTO Initial value: 0; Setting range: 0 to 1

Sets noise reduction auto mode.

When NRAUTO = 1, the noise reduction setting can be performed based on the noise state detected at NRDTON = 1.

Table R2-3-2 (1) Auto Level Setting Mode Setting

NRAUTO	Noise reduction mode
0	**Register fixed mode**
1	Auto mode

NRDTON Initial value: 0; Setting range: 0 to 1

Sets On/Off of noise detection.

When NRDTON = 1, performs noise detection on areas set by NRDTF, NRDTP[3:0], NDTC and PNON. The average and maximum detected noise values are updated every frame.

In memory read mode (DNR = 0) with NRDTON = 1, the data of the noise detection top or the last valid lines on which noise is detected will be output.

Table R2-3-2 (2) Noise Detection On/Off Setting

NRDTON	Noise detection
0	**Stop (Hold)**
1	Updated every frame

ACY Initial value: 0; Setting range: 0 to 1

Sets color difference noise detection flag mode.

When ACY = 1, masking for the color difference noise detection flags (CDTO1, CDTO2) is performed by luminance noise detection flags (YDTO1, YDTO2). Holds the noise detection flag to “0” even if the color difference noise detection value has exceeded the setting level as far as the luminance noise detection value does not exceed the setting value.

Table R2-3-2(3) Color Difference Noise Detection Flag Mode Setting

ACY	Color difference noise detection flag mode
0	**Color difference independent**
1	Luminance linked

AMM Initial value: 0; Setting range: 0 to 1

Sets noise reduction auto mode transition.

Selects noise reduction transition mode at NRAUTO = 1.

Table R2-3-2 (4) Noise Reduction Auto Mode Status Transition Setting

AMM	Noise Reduction Status		
	YDTO1 = 0, YDTO2 = 0 CDTO1 = 0, CDTO2 = 0	YDTO1 = 1, YDTO2 = 0 CDTO1 = 1, CDTO2 = 0	YDTO1 = 1, YDTO2 = 1 CDTO1 = 1, CDTO2 = 1
0	**Noise reduction OFF**	**Fixed register state A (Without automatic motion compensation OFF)**	**Noise follow-up state (With automatic motion compensation OFF)**
1	Fixed register state B1 (Without automatic motion compensation OFF. Same as YNRM = 1, CNRM = 1)	Fixed register state B2 (With automatic motion compensation OFF)	Noise follow-up state (With automatic motion compensation OFF)

NRDTF Initial value: 0; Setting range: 0 to 1

Sets noise detection field.

Noise detection is performed once in one frame in the vertical blanking period of one side. Performs selection of that detection field.

Table R2-3-2 (5) Noise Detection Field Setting

NRDTF	Noise detection field
0	**Field A**
1	Field B

NDCT Initial value: 0; Setting range: 0 to 1

Sets noise detection area in the blanking period.

Selects the setting of the basic noise detection period.

Table R2-3-2 (6) Basic Noise Detection Period Setting

NDTCF	Basic noise detection period
0	**1 line set by NRDTP[3:0]**
1	Multiple lines set by NRDTP[3:0]

PNON Initial value: 0; Setting range: 0 to 1

Sets noise detection area.

Selects whether the valid data area is used or not for noise detection.

Table R2-3-2 (7) Noise Detection Mode Setting

NDTCF	Noise detection period
0	**Vertical blanking area only**
1	Vertical blanking area + valid data area

2.3.3 Noise reduction motion compensation mode/noise detection inclination setting

SUB_ADDRESS = 4Ah(W/R): Luminance noise reduction motion compensation mode/Noise detection inclination setting

DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	YSLT				AYABN	YABN	YFAM	YNRM
	3	2	1	0				

SUB_ADDRESS = 4Bh(W/R): Color difference noise reduction motion compensation mode/Noise detection inclination setting

DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	CSLT				ACABN	CABN	CFAM	CNRM
	3	2	1	0				

YNRM Initial value: 0; Setting range: Refer to Table R2-3-3 (1).
Sets luminance noise reduction motion compensation mode selection.

YFAM Initial value: 0; Setting range: Refer to Table R2-3-3 (3).
Sets luminance adaptive noise reduction mode.

YABN Initial value: 0; Setting range: Refer to Table R2-3-3 (5).
Sets luminance absolute noise mode.
It is possible not to perform 1/2 motion compensation as absolute noise with respect to the motion level detection noise of luminance signal.

AYABN Initial value: 0; Setting range: Refer to Table R2-3-3 (7).
Sets auto mode luminance absolute noise mode.
By setting to "1", the luminance absolute noise mode operates in luminance noise follow-up state (YDTO2=1) of the auto mode. (The same operation as YABN = 1.)

YSLT[3:0] Initial value: 0001; Setting range: Refer to Table R2-3-3 (9).
Sets luminance noise reduction noise detection lines/convergence lines inclination.

CNRM Initial value: 0; Setting range: Refer to Table 2-3-3 (2).
Sets color difference noise reduction motion compensation mode selection.

CFAM Initial value: 0; Setting range: Refer to Table R2-3-3 (4).
Sets color difference adaptive noise reduction mode.

CABN Initial value: 0; Setting range: Refer to Table 2-3-3 (6).
Sets color difference absolute noise mode.
It is possible not to perform 1/2 motion compensation as absolute noise with respect to the motion level detection noise of color difference signal.

ACABN Initial value: 0; Setting range: Refer to Table 2-3-3 (8).
Sets auto mode color difference absolute noise mode.
By setting to "1", the color difference absolute noise mode operates in the color difference noise follow-up state (CDTO2 = 1) of the auto mode. (The same operation as CABN = 1.)

CSLT[3:0] Initial value: 0001; Setting range: Refer to Table 2-3-3 (10).
Sets color difference noise reduction noise detection line/convergence line inclination.

Table R2-3-3 (1) Luminance Noise Reduction Motion Compensation Mode Setting

YNRM	Luminance motion decision noise processing (Motion compensation)
0	**(Non-linear filter detection noise) × (Attenuation coefficient)**
1	Fix to 0. (Decision without noise)

Table R2-3-3 (2) Color Difference Noise Reduction Motion Compensation Mode Setting

CNRM	Color difference motion decision noise processing (Motion compensation)
0	**(Non-linear filter detection noise) × (Attenuation coefficient)**
1	Fix to 0. (Decision without noise)

Table R2-3-3 (3) Luminance Adaptive Noise Reduction Mode Settings

YFAM	Luminance adaptive noise reduction mode
0	**With adaptive margin (weak NR, few afterimages)**
1	Without adaptive margin (strong NR, many afterimages)

Table R2-3-3 (4) Color Difference Adaptive Noise Reduction Mode

CFAM	Color Difference adaptive noise reduction mode
0	**With adaptive margin (weak NR, few afterimages)**
1	Without adaptive margin (strong NR, many afterimages)

Table R2-3-3 (5) Luminance Absolute Noise Mode Setting

YABN	Luminance mode	Remarks
0	**Normal noise mode**	**(Detection noise) × (Motion compensation attenuation coefficient)**
1	Absolute noise mode	(Detection noise)/2 + {(Detection noise) × (Motion compensation attenuation coefficient)}/2

Table R2-3-3 (6) Color Difference Absolute Noise Mode Setting

CABN	Color difference mode	Remarks
0	**Normal noise mode**	**(Detection noise) × (Motion compensation attenuation coefficient)**
1	Absolute noise mode	(Detection noise)/2 + {(Detection noise) × (Motion compensation attenuation coefficient)}/2

Table R2-3-3 (7) Auto Mode Luminance Absolute Noise Mode Setting (Valid when NRAUTO=1)

AYABN	Noise follow-up state luminance mode
0	**Normal noise mode**
1	Absolute noise mode

Table R2-3-3 (8) Auto mode Color Difference Absolute Noise Mode Setting (Valid when NRAUTO=1)

ACABN	Noise follow-up state color difference mode
0	**Normal noise mode**
1	Absolute noise mode

Table R2-3-3 (9) Luminance Non-linear Filter Noise Detection/Convergence Line Inclination Setting

YSLT				Noise detection line coefficient (Inclination)	Noise convergence line coefficient (Inclination)
[3]	[2]	[1]	[0]		
X	X	0	0	1	–
X	**X**	**0**	**1**	**7/8**	**–**
X	X	1	0	3/4	–
X	X	1	1	1/2	–
0	**0**	**X**	**X**	**–**	**1 (–1)**
0	1	X	X	–	3/4 (–3/4)
1	0	X	X	–	1/2 (–1/2)
1	1	X	X	–	3/2 (–3/2)

Table R2-3-3 (10) Color Difference Non-linear Filter Noise Detection/Convergence Line Inclination Setting

CSLT				Noise detection line coefficient (Inclination)	Noise convergence line coefficient (Inclination)
[3]	[2]	[1]	[0]		
X	X	0	0	1	–
X	**X**	**0**	**1**	**7/8**	**–**
X	X	1	0	3/4	–
X	X	1	1	1/2	–
0	**0**	**X**	**X**	**–**	**1 (–1)**
0	1	X	X	–	3/4 (–3/4)
1	0	X	X	–	1/2 (–1/2)
1	1	X	X	–	3/2 (–3/2)

2.3.4 Noise convergence level setting

SUB_ADDRESS = 4Ch(W/R): Luminance noise convergence level setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	AYNS		YNS					
	1	0	5	4	3	2	1	0
SUB_ADDRESS = 4Dh(W/R): Color difference noise convergence level setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	ACNS		CNS					
	1	0	5	4	3	2	1	0

YNS[5:0] Initial value: 01_1000; Setting range: 00_0000 to 11_1111
Sets luminance noise convergence level.
This setting can be used also for the adjacent motion compensation level.
The setting can be adjusted in 0 to 63 levels for differential data of luminance signal fields. The detected noise level is limited to 1Fh as a result of combining the detection and convergence lines.

AYNS[1:0] Initial value: 00; Setting range: Refer to Table R2-3-4 (1).
Sets auto mode luminance noise convergence level.
Becomes valid in the auto mode noise follow-up state.

CNS[5:0] Initial value: 00_1111; Setting range: 00_0000 to 11_1111
Sets color difference noise convergence level.
This setting can be used also for the adjacent motion compensation level.
The setting can be adjusted in 0 to 63 levels for differential data of the color difference signal field. The detected noise level is limited to 1Fh as a result of combining the detection and convergence lines.

ACNS[1:0] Initial value: 00; Setting range: Refer to Table R2-3-4 (2).

Sets auto mode color difference noise convergence level.
Becomes valid in the noise follow-up state in the auto mode.

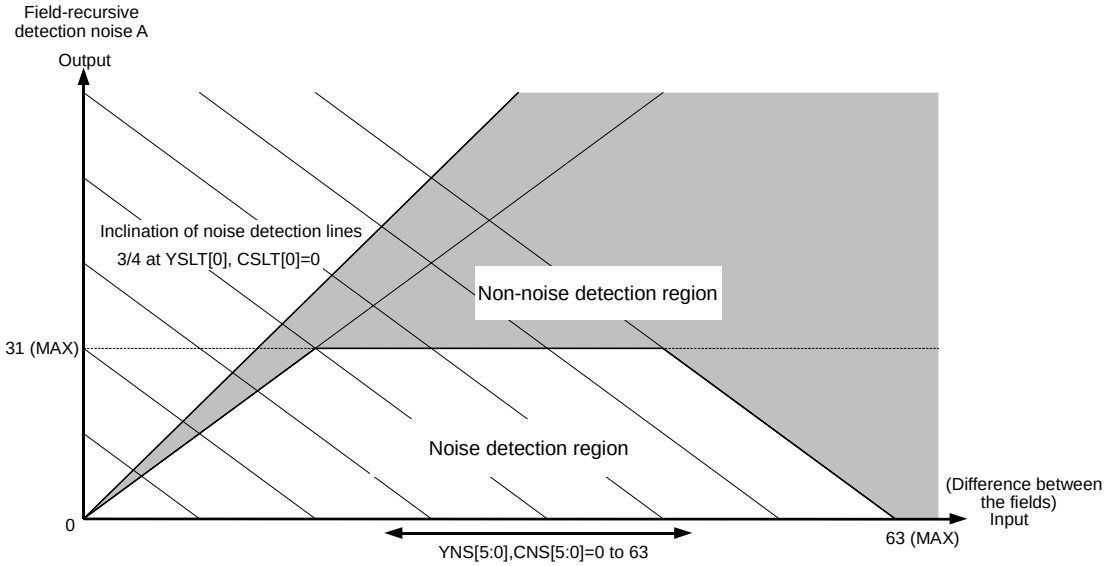


Figure R2-3-4 Example of Noise Detection by the YNS and CNS Settings

Table R2-3-4 (1) Auto Mode Luminance Noise Convergence Level Setting (Valid at NRAUTO=1)

AYNS		Noise Follow-up State Noise Convergence Level
[1]	[0]	
X	**0**	**YNS[5:0]**
0	1	YNS[5:0] + YMAXO[5:0] (Max.: 3Fh)
1	1	YMAXO[5:0] × 3 (Max.: 3Fh)

Table R2-3-4 (2) Auto Mode Color Difference Noise Convergence Level Setting (Valid at NRAUTO=1)

ACNS		Noise Follow-up State Noise Convergence Level
[1]	[0]	
X	**0**	**CNS[5:0]**
0	1	CNS[5:9] + CMAXO[5:0] (Max.: 3Fh)
1	1	CMAXO[5:0] × 3 (Max.: 3Fh)

2.3.5 Noise upper limit setting

SUB_ADDRESS = 4Eh(W/R): Luminance noise upper limit level setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	AYLM		AYNDL	YLM				
	1	0		4	3	2	1	0
SUB_ADDRESS = 4Fh(W/R): Color difference noise upper limit level setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	ACLM		ACNDL	CLM				
	1	0		4	3	2	1	0

YLM[4:0] Initial value: 0_0110; Setting range: 0_0000 to 1_1111
Sets luminance noise upper limit level.
The limit values are selected by 00h to 1Fh.

AYNDL Initial value: 0; Setting range: 0 to 1
Sets luminance noise upper limit level of noise detection.
By setting 1, unexpected noise at noise detection is restricted to control the rapid change in the noise detection amount.

AYLM[1:0] Initial value: 00; Setting range: Refer to table R2-3-5 (1).
Sets auto mode luminance noise upper limit level.
Becomes valid in noise follow-up state in the auto mode.

CLM[4:0] Initial value: 0_0011; Setting range: 0_0000 to 1_1111
Sets color difference noise upper limit level.
The limit values are selected by 00h to 1Fh.

ACNDL Initial value: 0; Setting range: 0 to 1
Sets color difference noise upper limit level of noise detection.
By setting 1, unexpected noise at noise detection is restricted to control the rapid change in the noise detection amount is controlled.

ACLM[1:0] Initial value: 00; Setting range: Refer to table R2-3-5 (2).
Sets auto mode color difference noise upper limit level.
Becomes valid in the auto mode noise follow-up state.

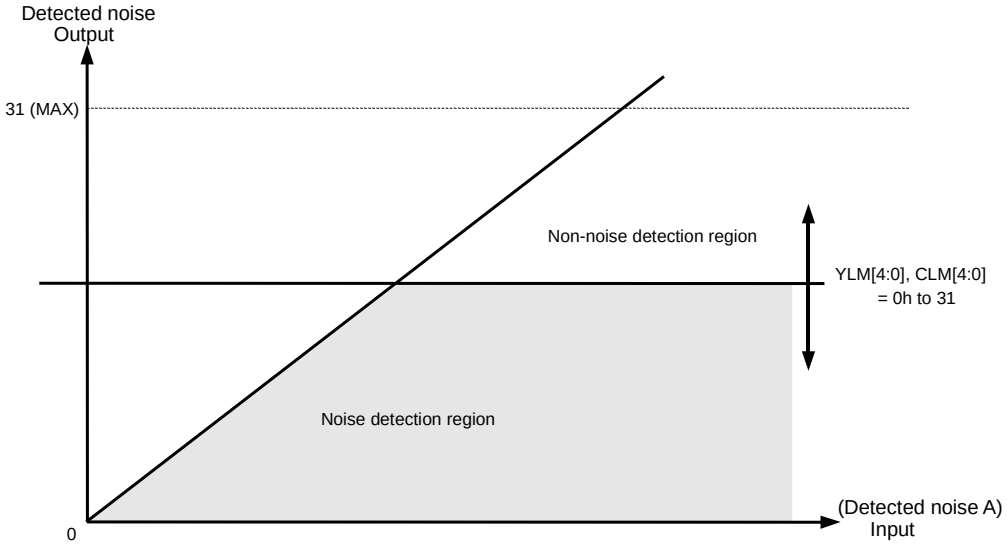


Figure R2-3-5 Noise Detection Limits by YLM and CLM Settings

Table R2-3-5 (1) Auto Mode Luminance Noise Upper Limit Level Setting (Valid at NRAUTO = 1)

AYLM		Noise Follow-up State Luminance Noise Upper Limit Level
[1]	[0]	
X	**0**	**YLM[4:0]**
0	1	YMAXO[4:0] × 0.75 (Max.: 1Fh)
1	1	YMAXO[4:0] (Max.: 1Fh)

Table R2-3-5 (2) Auto Mode Color Difference Noise Upper Limit Level Setting (Valid at NRAUTO = 1)

ACLM		Noise Follow-up State Color Difference Noise Upper Limit Level
[1]	[0]	
X	**0**	**CLM[4:0]**
0	1	CMAXO[4:0] × 0.75 (Max.: 1Fh)
1	1	CMAXO[4:0] (Max.: 1Fh)

2.3.6 Luminance continuous code motion compensation level setting

SUB_ADDRESS = 50h(W): Luminance Continuous Code Motion Compensation Level Setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	AYMS		(Reserved)	YMS				
	1	0		4	3	2	1	0

YMS[3:0] Initial value: 0100; Setting range: 0000 to 1111

Sets luminance signal continuous code motion compensation level.
Settable in 0 to 30 levels for the luminance signal field differential absolute value data.
Assigns respective setting values to the 3-continuous codes, 4-continuous codes and 5-continuous codes motion detection, decides data having large motion components for |ΔLY| exceeding the setting, and performs the noise attenuation compensation (YNRM = 0) or NROFF compensation (YNRM = 1).

Table R2-3-6 (1) 3-Continuous Code Motion Compensation Decision

Motion detection condition	Motion decision
|ΔLY| > 16	Large (Compensation operation)
|ΔLY| > YMS[3:0]	Large (Compensation operation)
|ΔLY| ≤ YMS[3:0]	Small (No compensation)

Table R2-3-6 (2) 4-Continuous Code Motion Compensation Decision

Motion detection condition	Motion decision
|ΔLY| > 8	Large (Compensation operation)
|ΔLY| > YMS[3:1]	Large (Compensation operation)
|ΔLY| ≤ YMS[3:1]	Small (No compensation)

Table R2-3-6 (3) 5-Continuous Code Motion Compensation Decision

Motion detection condition	Motion decision
|ΔLY| > 4	Large (Compensation operation)
|ΔLY| > YMS[3:2]	Large (Compensation operation)
|ΔLY| ≤ YMS[3:2]	Small (No compensation)

AYMS[1:0] Initial value: 00; Setting range: Refer to table R2-3-5 (4).

Sets auto mode luminance motion compensation level.
Valid in the auto mode noise follow-up state.

Table R2-3-6 (4) Auto Mode Motion Compensation Level Setting (Valid at NRAUTO = 1)

AYMS		Noise follow-up state motion compensation level
[1]	[0]	
X	**0**	**YMS[3:0]**
0	1	YMAXO[4:0]/2 (Max.: Fh)
1	1	YMAXO[4:0] (Max.: Fh)

A2OFF Initial value: 0; Setting range: 0 to 1

Sets the auto mode 2D noise reduction OFF.

If there is a lot of noise in the auto mode, the adaptive 2D noise reduction is turned OFF.

Table R2-3-6 (5) Auto Mode 2D Noise Reduction OFF Setting

A2OFF	2D noise reduction
0	**Depends on NR2OFF setting**
1	Adaptive 2DNR OFF in noise status 2

2.3.7 Noise reduction motion compensation ON/OFF setting

SUB_ADDRESS = 51h(W/R): Luminance Noise Reduction Motion Compensation ON/OFF Setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	AYMOFF			(Reserved)	YMOFF			
	3	2	1		3	2	1	0
SUB_ADDRESS=52h(W/R): Color Difference Noise Reduction Motion Compensation ON/OFF Setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	CMY	(Reserved)	(Reserved)	CMOFF				
				4	3	2	1	0

YMOFF[3:0] Initial value: 0000; Setting range: Refer to Table R2-3-7 (1).
Sets motion compensation ON/OFF of luminance signal field-recursive noise reduction detection noise.

Table R2-3-7 (1) Luminance Motion Compensation ON/OFF Setting 1

YMOFF				Luminance motion level detection noise motion compensation
[0]	[1]	[2]	[3]	
0	X	X	X	**Luminance horizontal contiguous motion level compensation - ON**
1	X	X	X	Luminance horizontal contiguous motion level compensation - OFF
X	**0**	X	X	**Luminance horizontal contiguous 3-continuous code motion compensation - ON**
X	1	X	X	Luminance horizontal contiguous 3-continuous code motion compensation - OFF
X	X	**0**	X	**Luminance horizontal contiguous 4-continuous code motion compensation - ON**
X	X	1	X	Luminance horizontal contiguous 4-continuous code motion compensation - OFF
X	X	X	**0**	**Luminance horizontal contiguous 5-continuous code motion compensation - ON**
X	X	X	1	Luminance horizontal contiguous 5-continuous code motion compensation – OFF

AYMOFF[3:1] Initial value: 000; Setting range: Refer to Tables R2-3-7 (2), (3).
Sets auto mode motion compensation ON/OFF of luminance signal field recursive noise reduction detection noise.
Validates in auto mode 1 (AMM = 0) noise follow-up state or in auto mode 2 (AMM = 1) fixed register state B2/ noise follow-up state. (The same operation as of YMOFF[3:1].)

Table R2-3-7 (2) Auto Mode 1 Motion Compensation Setting (Valid at NRAUTO = 1)

AYMOFF[*]	Noise follow-up state motion compensation
0	**Motion compensation ON**
1	Motion compensation OFF

* is 1 to 3.

Table R2-3-7 (3) Auto Mode 2 Motion Compensation Setting (Valid at NRAUTO = 1)

AYMOFF[*]	Fixed register state B2/Noise follow-up state luminance mode
0	**Motion compensation ON**
1	Motion compensation OFF

* is 1 to 3.

CMOFF[4:0] Initial value: 0_0000; Setting range: Refer to Table R2-3-7 (4).
Sets motion compensation ON/OFF of color difference signal field recursive noise reduction detection noise.

CMY Initial value: 0; Setting range: Refer to Table R2-3-7 (4).
Sets color difference motion compensation mode.
Allows to use motion compensation for the color difference signal also for the luminance signal.

Table R2-3-7 (4) Color Difference Motion Compensation ON/OFF Setting

CMOFF					CMY	Color difference motion level detection noise motion compensation
[0]	[1]	[2]	[3]	[4]		
0	X	X	X	X	X	**Color difference horizontal contiguous motion level compensation - ON**
1	X	X	X	X	X	Color difference horizontal contiguous motion level compensation - OFF
X	**0**	X	X	X	**0**	**Luminance horizontal contiguous motion level compensation - OFF**
					1	Luminance horizontal contiguous motion level compensation - ON
X	1	X	X	X	X	Luminance horizontal contiguous motion level compensation - OFF
X	X	**0**	X	X	**0**	**Luminance horizontal contiguous 3-continuous code motion compensation - OFF**
					1	Luminance horizontal contiguous 3-continuous code motion compensation - ON
X	X	1	X	X	X	Luminance horizontal contiguous 3-continuous code motion compensation - OFF
X	X	X	**0**	X	**0**	**Luminance horizontal contiguous 4-continuous code motion compensation - OFF**
					1	Luminance horizontal contiguous 4-continuous code motion compensation - ON
X	X	X	1	X	X	Luminance horizontal contiguous 4-continuous code motion compensation - OFF
X	X	X	X	**0**	**0**	**Luminance horizontal contiguous 5-continuous code motion compensation - OFF**
					1	Luminance horizontal contiguous 5-continuous code motion compensation - ON
X	X	X	X	1	X	Luminance horizontal contiguous 5-continuous code motion compensation - OFF

2.3.8 Noise state detection setting

SUB_ADDRESS = 53h(W/R): Luminance noise state 1 detection setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	YAH1	(Reserved)	YAVR1					
			5	4	3	2	1	0
SUB_ADDRESS = 54h(W/R): Color difference noise state 1 detection setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	CAH1	(Reserved)	CAVR1					
			5	4	3	2	1	0
SUB_ADDRESS = 55h(W/R): Luminance noise state 2 detection setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	YAH2	YAVR2						
		6	5	4	3	2	1	0
SUB_ADDRESS = 56h(W/R): Color difference noise state 2 detection setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	CAH2	CAVR2						
		6	5	4	3	2	1	0

YAVR1[5:0] Initial value: 00_0000; Setting range: 00_0000 to 11_1111
Sets increase direction decision average value level of luminance noise state 1.
Becomes the decision level when the noise level is in the increase direction.
YAVR1[5:4] is an integral part and YAVR1[3:0] is a decimal part.
Make sure to set a value smaller than YAVR2[6:0].

YAH1 Initial setting: 0; Setting range: 0 to 1
Sets decrease direction decision average value level hysteresis coefficient of luminance noise state 1.
The decision level of the noise level in decreasing direction is set by (YAVR1[5:0]) × (Coefficient).

CAVR1[5:0] Initial value: 00_0000; Setting range: 00_0000 to 11_1111
Sets increase direction decision average value level of color difference noise state 1.
Becomes the decision level of the noise level in increasing direction.
CAVR1[5:4] is an integral part and CAVR1[3:0] is decimal part.
Make sure to set the value smaller than CAVR2[6:0].

CAH1 Initial value: 0; Setting range: 0 to 1
Sets decrease direction decision average value level hysteresis coefficient of color difference noise state 1.
The decision level of the noise level in the decreasing direction is set by (CAVR1[5:0]) × (Coefficient)

YAVR2[6:0] Initial value: 111_1111; Setting range: 000_0000 to 111_1111
Sets increase direction decision average value level of luminance noise state 2.
Becomes the decision level of the noise level in increasing direction.
YAVR2[6:4] is an integral part and YAVR2[3:0] is a decimal part.
Make sure to set the value larger than YAVR1[5:0].

YAH2 Initial value: 0; Setting range: 0 to 1
Sets decrease direction decision average value level hysteresis coefficient of luminance noise state 2.
The decision level of the noise level in decreasing direction is set by (YAVR2[6:0]) × (Coefficient).

CAVR2[6:0] Initial value: 111_1111; Setting range: 000_0000 to 111_1111
Sets increase direction decision average value level of color difference noise state 2.
Becomes the decision level of the noise level in increasing direction.
CAVR2[6:4] is an integral part and CAVR2[3:0] is a decimal part.
Make sure to set the value larger than CAVR1[5:0].

CAH2 Initial value: 0; Setting range: 0 to 1
Sets decrease direction decision average value level hysteresis coefficient of color difference noise state 2.
The decision level of the noise level in decreasing direction is set by (CAVR2[6:0]) × (Coefficient)

Table R2-3-8 (1) Luminance Noise State 1 Decision Level Conditions

Level condition	State
YAVRO[6:0] > YAVR1[5:0]	YDTO1 = 0 → 1
YAVRO[6:0] ≤ (YAVR1[5:0] × Coefficient)	YDTO1 = 1 → 0

Table R2-3-8 (2) Color Difference Noise State 1 Decision Level Conditions

Level condition	State
CAVRO[6:0] > CAVR1[5:0]	CDTO1 = 0 → 1
CAVRO[6:0] ≤ (CAVR1[5:0] × Coefficient)	CDTO1 = 1 → 0

Table R2-3-8 (3) Luminance Noise State 2 Decision Level Conditions

Level condition	State
YAVRO[6:0] > YAVR2[6:0]	YDTO2 = 0 → 1
YAVRO[6:0] ≤ (YAVR2[6:0] × Coefficient)	YDTO2 = 1 → 0

Table R2-3-8 (4) Color Difference Noise State 2 Decision Level Conditions

Level condition	State
CAVRO[6:0] > CAVR2[6:0]	CDTO2 = 0 → 1
CAVRO[6:0] ≤ (CAVR2[6:0] × Coefficient)	CDTO2 = 1 → 0

Table R2-3-8 (5) Luminance Noise State 1 Hystersis Coefficient

YAH1	Noise decrease direction switching coefficient
0	3/4
1	7/8

Table R2-3-8 (6) Color Difference Noise State 1 Hystersis Coefficient

CAH1	Noise decrease direction switching coefficient
0	3/4
1	7/8

Table R2-3-8 (7) Luminance Noise State 2 Hystersis Coefficient

YAH2	Noise decrease direction switching coefficient
0	3/4
1	7/8

Table R2-3-8 (8) Color Difference Noise State 2 Hystersis Coefficient

CAH2	Noise decrease direction switching coefficient
0	3/4
1	7/8

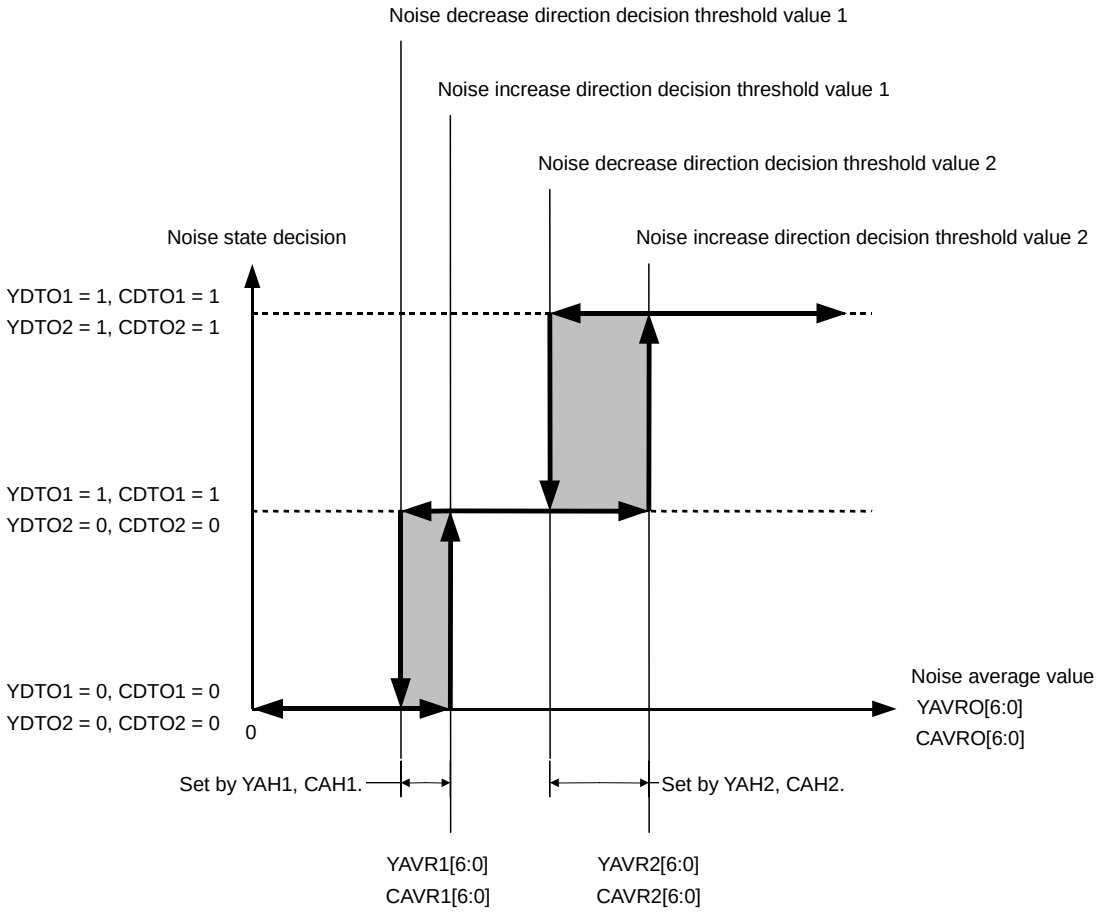


Figure R2-3-8 Noise State Decision Transition Diagram

2.3.9 Noise read data select setting

SUB_ADDRESS=57h(W/R): Noise read data select setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	DTPSL	(Reserved)	NRDTP				CNAMS	YNAMS
			3	2	1	0		

YNAMS Initial value: 0; Setting range: 0 to 1
Sets luminance signal noise data read selection.
Selects a value that is reflected on YAVRO[6:0] and YMAXO[5:0].

Table R2-3-9 (1) Luminance Signal Noise Data Read Select Setting

YNAMS	YAVRO [6:0], YMAXO[5:0]
0	**8 frames average**
1	1 frame detection

CNAMS Initial value: 0; Setting range: 0 to 1
Sets color difference signal noise data read selection.
Selects a value that is reflected on CAVRO[6:0] and CMAXO[5:0].

Table R2-3-9 (2) Color Difference Signal Noise Data Read Select Setting

CNAMS	CAVRO [6:0], CMAXO[5:0]
0	**8 frames average**
1	1 frame detection

NRDTP[3:0] Initial value: 0000; Setting range: 0001 to 1111
Sets auto mode noise detection position.

DTPSL Initial value: 0; Setting range: 0 to 1
Sets noise detection reference position.

Table R2-3-9 (3) Noise Detection Reference Position Setting

DTPSL	Noise detection reference position
0	**1st line after valid data end line**
1	2nd line after valid data end line

2.3.10 Noise level read registers (read only)

SUB_ADDRESS = 58h(R): Luminance noise average value level read register								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	YDTO1	YAVRO						
		6	5	4	3	2	1	0
SUB_ADDRESS = 59h(R): Color difference noise average value level read register								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	CDTO1	CAVRO						
		6	5	4	3	2	1	0
SUB_ADDRESS = 5Ah(R): Luminance noise maximum value level read register								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	YDTO2	0	0	YMAXO				
				4	3	2	1	0
SUB_ADDRESS = 5Bh(R): Color difference noise maximum value level read register								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	CDTO2	0	0	CMAXO				
				4	3	2	1	0
SUB_ADDRESS = 5Ch(R): Luminance blanking period noise average value level read register								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	YBDTO	YBAVRO						
		6	5	4	3	2	1	0
SUB_ADDRESS = 5Dh(R): Color difference blanking period noise average value level read register								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	CBDTO	CBAVRO						
		6	5	4	3	2	1	0

YAVRO[6:0] Read value range: 000_0000 to 111_1111
Luminance noise level of 8 frames average (YNAMS = 0), or of 1 frame (YNAMS = 1), of noise absolute value average of lines detected at NRDTON = 1
Updated every frame. 7Fh is read out if the noise level exceeds 7Fh.
YAVRO[6:4] is an integral part and YAVRO[3:0] is a decimal part.

CAVRO[6:0] Read value range: 000_0000 to 111_1111
Color difference noise level of 8 frames average (CNAMS = 0), or of 1 frame (CNAMS = 1), of noise absolute value average of lines detected at NRDTON = 1
Updated every frame. 7Fh is read out if the noise level exceeds 7Fh.
CAVRO[6:4] is an integral part and CAVRO[3:0] is a decimal part.

YDTO1 Read value range: 0 to 1
Luminance Noise Detection Flag
At NRDTON = 1, YDTO1 is set to “1” if YAVRO[6:0] > YAVR1[5:0] state continues in 4 frames.

CDTO1 Read value range: 0 to 1
Color difference noise detection flag 1.
At NRDTON = 1, CDTO1 is set to “1” if CAVRO[6:0] > CAVR1[5:0] state continues in 4 frames.

YDTO2 Read value range: 0 to 1
Luminance noise detection flag 2.
At NRDTON = 1, YDTO2 is set to "1" if YAVRO[6:0] > YAVR2[6:0] state continues in 4 frames.
YDTO2 is fixed to "0" in the case of YAVR2[6:0] = 7Fh.

CDTO2 Read value range: 0 to 1
Color difference noise detection flag 2.
At NRDTON = 1, CDTO2 is set to "1" if CAVRO[6:0] > CAVR2[6:0] state continues in 4 frames.
CDTO2 is fixed to "0" in the case of CAVR2[6:0] = 7Fh.

YMAXO[4:0] Read value range: 0_0000 to 1_1111
Luminance noise level of 8 frames average (YNAMS = 0), or of 1 frame (YNAMS = 1), of the noise maximum value of lines detected at NRDTON = 1.
Updated every frame. 3Fh is read out if the noise level exceeds 3Fh.

CMAXO[4:0] Read value range: 0_0000 to 1_1111
Color difference noise level of 8 frames average (CNAMS = 0), or of 1 frame (CNAMS = 1), of the noise maximum value of lines detected at NRDTON = 1.
Updated every frame. 3Fh is read out if the noise level exceeds 3Fh.

YBAVRO[6:0] Read value range: 000_0000 to 111_1111
Luminance noise level of 8 frames average (YNAMS = 0), or of 1 frame (YNAMS = 1), of luminance blanking noise absolute value average of lines detected at NRDTON = 1
Updated every frame. 7Fh is read out if the noise level exceeds 7Fh.
YBAVRO[6:4] is an integral part and YBAVRO[3:0] is a decimal part.

CBAVRO[6:0] Read value range: 000_0000 to 111_1111
Color difference noise level of 8 frames average (CNAMS = 0), or of 1 frame (CNAMS = 1), of color difference blanking noise absolute value average of lines detected at NRDTON = 1
Updated every frame. 7Fh is read out if the noise level exceeds 7Fh.
CBAVRO[6:4] is an integral part and CBAVRO[3:0] is a decimal part.

YBDTO Read value range: 0 to 1
Luminance vertical blanking period noise detection flag.
At NRDTON = 1, YBDTO is set to "1" if YBAVRO[6:0] > YAVR1[5:0] state continues in 4 frames.

CBDTO Read value range: 0 to 1
Color difference vertical blanking period noise detection flag.
At NRDTON = 1, CBDTO is set to "1" if CBAVRO[6:0] > CAVR1[5:0] state continues in 4 frames.

* When PNON = 0, noise detection is not performed for the valid data period, so the data in YAVRO1[6:0] = YBAVRO[6:0], CAVRO1[6:0] = CBAVRO[6:0], YDTO1 = YBDTO, CDTO1 = CBDTO is read.

2.4 Output System Settings

2.4.1 Output data setting

SUB_ADDRESS=60h(W/R): Output data setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	CKEN	CKSL	CKINV	REFSL		(Reserved)	DOSEL	(Reserved)
				1	0			

DOSEL Initial value: 0; Setting range: 0 to 1
Sets the output format.

Table R2-4-1 (1) Output Format Mode Setting

DOSEL	Output format mode
0	**16-bit output**
1	I/O same format

REFSL Initial value: 00; Setting range: 00 to 11
Sets HREF pin output.
Selects and outputs any one of the horizontal reference signal, color difference select signal, effective area signal, and field pulse signal.

Table R2-4-1 (3) HREF Pin Output Selection

REFSL		HREF pin output
[0]	[1]	
0	**0**	**Horizontal reference signal**
0	1	Color difference select signal
1	0	Effective area signal
1	1	Field pulse signal

CKINV Initial value: 0; Setting range: Refer to Table R2-4-1 (4).
Sets CLKO output polarity.

CKSL Initial value: 0; Setting range: Refer to Table 2-4-1 (4)
Sets CLKO output selection.

CKEN Initial value: 0; Setting range: Refer to Table R2-4-1 (4).
Sets CLKO output enable.

Table R2-4-1 (4) CLKO Output Setting

CKEN	CKSL	CKINV	CLKO output
0	**X**	**X**	**Hi-Z**
1	0	0	IICLK
1	0	1	Inverted IICLK
1	1	0	ICLK
1	1	1	Inverted ICLK

* During input 16-bit mode, IICLK = ICLK.

2.4.2 Output synchronization signal setting

SUB_ADDRESS=61h(W/R): Output sync signal setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	(Reserved)	(Reserved)	(Reserved)	(Reserved)	(Reserved)	HREF INV	OVSINV	OHSINV

OVSINV Initial value: 0; Setting range: 0 to 1
Sets output polarity.

Table R2-4-2 (1) OVS Polarity Setting

OVSINV	OVS polarity
0	**Positive polarity**
1	Negative polarity

OHSINV Initial value: 0; Setting range: 0 to 1
Sets output polarity.

Table R2-4-2 (2) OHS Polarity Setting

OHSINV	OHS polarity
0	**Positive polarity**
1	Negative polarity

HREF Initial value: 0; Setting range: 0 to 1
Sets HREF output polarity.

Table R2-4-2 (3) HREF Polarity Setting

HREFINV	HREF polarity
0	**Positive polarity**
1	Negative polarity

2.4.3 Sync Signal Generation Adjustment Settings (for demonstration)

*** The registers in this section are published as settings for generating the necessary sync signals for monitor display in evaluation boards. Because only standard signals are assumed, the operation of final products is not guaranteed. Use these settings only when using an evaluation board.**

SUB_ADDRESS=78h (W/R): Output system memory control mode settings								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	(Reserved)	(Reserved)	(Reserved)	(Reserved)	(Reserved)	(Reserved)	HSSEL	ISYNC
SUB_ADDRESS=79h(W/R): OHS generation start position settings								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	SHSDL							
	7	6	5	4	3	2	1	0

ISYNC Initial value: 0; Setting range: 0 to 1
OVS and OHS internal sync signal generation settings.

Table R2-4-3 (1) Internal Sync Signal Generation Settings

ISYNC	OVS and OHS output
0	**Input delay output**
1	Internally generated output

HSSEL Initial value: 0; Setting range: 0 to 1
OHS pin output signal settings

Table R2-4-3 (2) Internally Generated OVS, OHS Field Settings

HSSEL	OHS phase
0	**Horizontal sync signal**
1	Composite sync

SHSDL[7:0] Initial value: 0011_1111; Setting range: 0000_0001 to 1111_1111
Internal sync generator OHS generation start position settings.

2.5 Test Settings

2.5.1 Test mode settings

SUB_ADDRESS = 70h(W/R): Test mode setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	TST1							
	7	6	5	4	3	2	1	0
SUB_ADDRESS = 71h(W/R): Test mode setting								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	TST1							
	15	14	13	12	11	10	9	8

TST1[7:0] Initial value: 0000_0000; Setting range: 0000_0000 to 1111_1111
TST1[15:8] Initial value: 0000_0000; Setting range: 0000_0000 to 1111_1111
Sets test mode: Normally fixed to 0000_0000.

2.5.2 Other mode settings

SUB_ADDRESS = 72h(W/R): Other settings								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	RLTG	(Reserved)	(Reserved)	(Reserved)	(Reserved)	(Reserved)	OUTDS	PASS

PASS Initial value: 0; Setting range: 0 to 1

Sets data through mode.

The input pin is directly connected to the output pin. At this time, there is a delay generated equal to the time it takes for the output data to pass through the internal circuitry.

Table R2-5-2 (1) Data Through Mode Setting

PASS	Mode
0	**Normal operation**
1	Data through

OUTDS Initial value: 0; Setting range: 0 to 1

Sets to disable forcibly all outputs (YO[7:0], CO[7:0], OVS, OHS, HREF, CLKO).

Table R2-5-2 (2) All Outputs Disable Setting

OUTDS	All output pins
0	**Dependent on other settings (R656, DISEL, DOSEL)**
1	Disable

RLTG Initial value: 0; Setting range: 0 to 1

Sets the register setting synchronous mode. Normally 0, used only for tests.

Table R2-5-2 (3) Register Set Mode Setting

RLTG	Data reflection
0	**IVS, OVS synchronous**
1	When I^2C-bus is set

2.5.3 Read NR setting values

SUB_ADDRESS = 73h(R): Luminance noise convergence level read register								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	0	0	RYNS					
			5	4	3	2	1	0
SUB_ADDRESS = 74h(R): Color difference noise convergence level read register								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	0	0	RCNS					
			5	4	3	2	1	0
SUB_ADDRESS = 75h(R): Luminance noise upper limit level read register								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	RYABN	RYNRM	RYNR OFF	RYLM				
				4	3	2	1	0
SUB_ADDRESS = 76h(R): Color difference noise upper limit level read register								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	RCABN	RCNRM	RCNR OFF	RCLM				
				4	3	2	1	0
SUB_ADDRESS = 77h(R): Luminance motion compensation level read register								
DATA_BIT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Register name	RYMOF			RNR2 OFF	RYMS			
	3	2	1		3	2	1	0

RYNS[5:0] Read value range: 00_0000 to 11_1111
Reads luminance noise convergence level of internal operation state.
RYNS[5:0] = YNS[5:0] in case either the auto mode is not set (NRAUTO = 0) or the follow-up is not set in the auto mode (AYNS[0] = 0).

RCNS[5:0] Read value range: 00_0000 to 11_1111
Reads color difference noise convergence level of internal operation state.
RCNS[5:0] = CNS[5:0] in case either the auto mode is not set (NRAUTO = 0) or the follow-up is not set in the auto mode (ACNS[0] = 0).

RYLM[5:0] Read value range: 0_0000 to 1_1111
Reads luminance noise upper limit level of internal operation state.
RYLM[4:0] = YLM[4:0] in case either the auto mode is not set (NRAUTO = 0) or the follow-up is not set in the auto mode (AYLM[0] = 0).

RYNROF Read value range: 0 to 1
Reads luminance NR On/Off switching signal of internal operation state.
In case the auto mode is not set (NRAUTO = 0): RYNROFF = NROFF

RYNRM Read value range: 0 to 1
Reads luminance motion detection noise mode 0 switching signal of internal operation state.
In case the auto mode is not set (NRAUTO = 0): RYNRM = YNRM

RYABN Read value range: 0 to 1
Reads luminance absolute noise mode switching signal of internal operation state.
RYABN = YABN in case either the auto mode is not set (NRAUTO = 0) or the follow-up setting is not set in the auto mode (AYABN = 0).

RCLM[4:0] Read value range: 0_0000 to 1_1111
Reads color difference noise upper limit level of internal operation state.
RCLM[4:0] = YCM[4:0] in case either the auto mode is not set (NRAUTO = 0) or the follow-up is not set in the auto mode (ACLM[0] = 0).

RCNROFF Read value range: 0 to 1
Reads color difference NR ON/OFF switching signal of internal operation state.
In case the auto mode is not set (NRAUTO = 0): RCNROFF = NROFF

RCNRM Read value range: 0 to 1
Reads color difference motion detection noise mode 0 switching signal of internal operation state.
In case the auto mode is not set (NRAUTO = 0): RCNRM = CNRM

RCABN Read value range: 0 to 1
Reads color difference absolute noise mode switching signal of internal operation state.
RCABN = CABN in case either the auto mode is not set (NRAUTO = 0) or the follow-up is not set in the auto mode (ACABN = 0).

RYMS[3:0] Read value range: 0_0000 to 1_1111
Reads luminance motion compensation level of internal operation state.
RYMS[4:0] = YMS[4:0] in case either the auto mode is not set (NRAUTO = 0) or the follow-up is not set in the auto mode (AYMS[0] = 0).

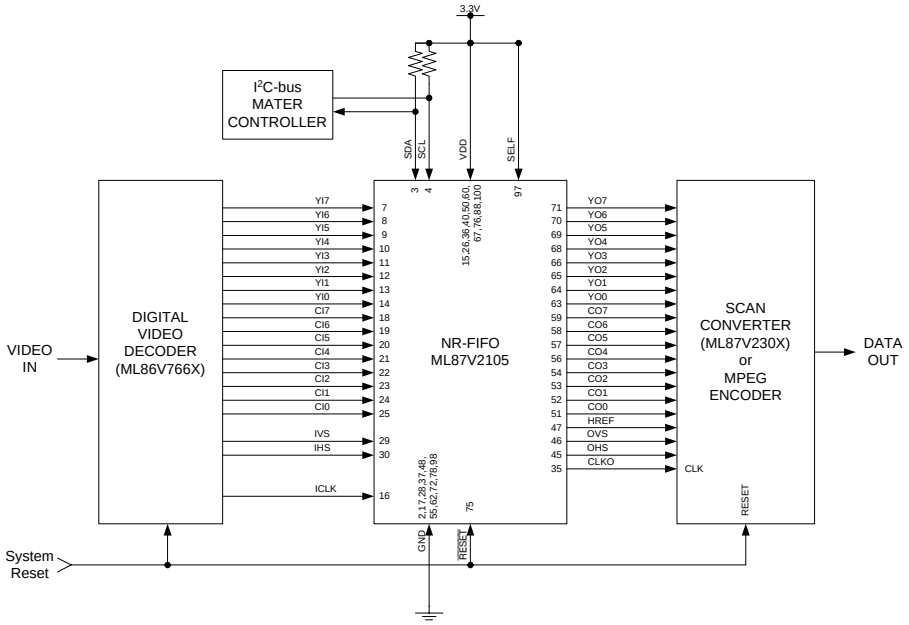
RNR2OFF Read value range: 0 to 1
Adaptive 2D noise reduction ON/OFF signal of internal operation status.
If the auto mode is not set (NRAUTO = 0) or if A2OFF = 1 is not set in the auto mode, RNR2OFF = NR2OFF is set.

RYMOF[3:1] Read value range: 000 to 111
Reads luminance motion compensation On/Off switching signal of internal operation state
RYMOF[*] = YMOFF[*] in case either the auto mode is not set (NRAUTO = 0) or the follow-up is not set in the auto mode (AYMOFF[*] = 0). (Here, * is 1 to 3.)

CIRCUIT APPLICATION EXAMPLES

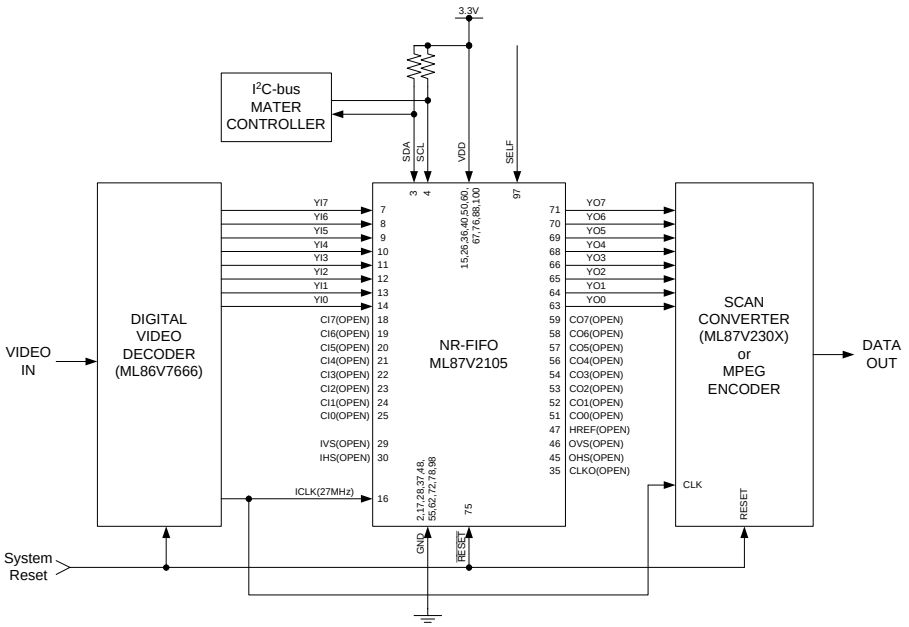
Application Example 1

Mode setting: Open
Slave address: 1011100
Input format: 16-bit YCbCr (Register setting: DISEL = 0, R656 = 0)



Application Example 2

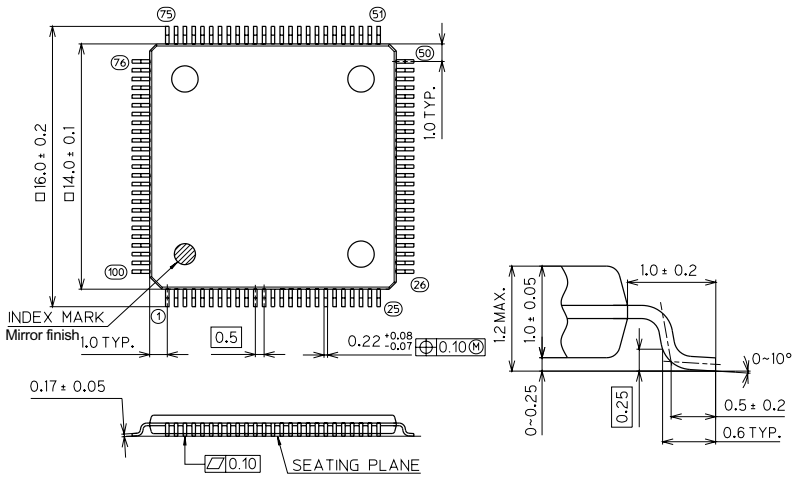
Mode setting: Open
Slave address: 1011100
Input format: ITU-R BT656 (Register setting: DISEL = 0, R656 = 1)



PACKAGE DIMENSIONS

(Unit: mm)

TQFP100-P-1414-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.55 TYP.
Rev. No./Last Revised	4/Oct. 28, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL87V2105-01	Nov. 14, 2003	–	103	Preliminary edition 1
PEDL87V2105-02	Dec. 20, 2003	103	103	Internal pull down, application schematic

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