LOW POWER SCHOTTKY INTEGRATED CIRCUITS

T54LS640/641/645
T74LS640/641/645

67C 16526 D T-52-31

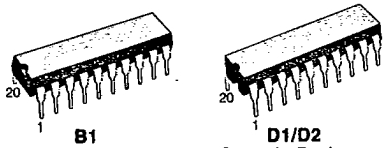
PRELIMINARY DATA

OCTAL BUS TRANSCEIVERS

DESCRIPTION

The T54LS/T74LS640/641/645 are octal bus transceivers designed for asynchronous two-way communication between data buses. Control function implementation reduces to a minimum external timing requirements. This circuit permits transmission of data from the A bus to B or from the B bus to A bus depending upon the logic level of the direction control (DIR) input. The device can be disabled by the Enable input ($\overline{G}$) causing the buses to be effectively isolated.

DEVICE	OUTPUT	LOGIC
LS640	3-State	Inverting
LS641	Open-Collector	True
LS645	3-State	True



B1
Plastic Package

D1/D2
Ceramic Package

M1
Micro Package

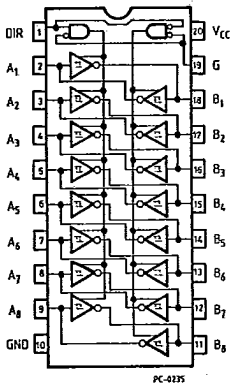
C1
Plastic Chip Carrier

ORDERING NUMBERS:

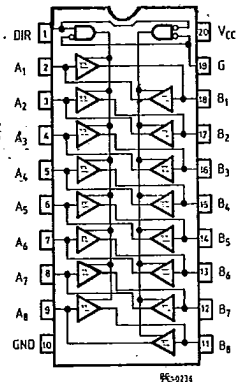
T54LSXXX D2
T74LSXXX D1
T74LSXXX B1
T74LSXXX C1
T74LSXXX M1

LOGIC AND CONNECTION DIAGRAMS DIP (top view)

LS640

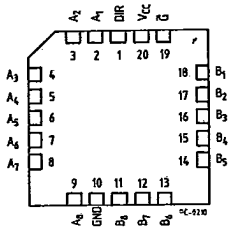


LS641/LS645

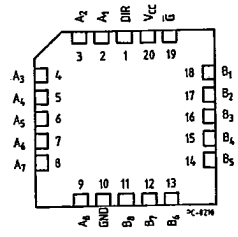


CHIP CARRIER

LS640



LS641/LS645



T54LS640/641/645
T74LS640/641/645

TRUTH TABLE

CONTROL INPUTS		OPERATION	
		LS640	LS641 LS645
$\overline{G}$	DIR		
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus
H	X	Isolation	Isolation

L = LOW Voltage Level,
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 15	V
V_O	Output Voltage, Applied to Output	0 to 10	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS640/641/645D2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS640/641/645XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

T54LS640/641/645
T74LS640/641/645

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (T54LS/T74LS640/645)

Symbol	Parameter		Limits Min.	Typ.	Max.	Test Conditions (Note 1)	Units
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs	V
V_{IL}	Input LOW Voltage	54			0.5	Guaranteed input LOW Voltage for all Inputs	V
		74			0.6		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA	V
V_{OH}	Output HIGH Voltage	54,74	2.4	3.4		V_{CC} = MIN, I_{OH} = −3.0mA	V
		54	2.0			I_{OH} = −12mA, V_{CC} = MIN	V
		74	2.0			I_{OH} = −15mA, V_{CC} = MIN	V
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 12mA, V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table	V
		74		0.35	0.5	I_{OL} = 24mA, V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table	V
I_{OZH}	Output Off Current HIGH				20	V_{CC} = MAX, V_{OUT} = 2.4V	μA
I_{OZL}	Output Off Current LOW				−400	V_{CC} = MAX, V_{OUT} = 0.4V	μA
I_{IH}	Input HIGH Current A or B				20	V_{CC} = MAX, V_{IN} = 2.7V	μA
	DIR or $\overline{G}$				0.1	V_{CC} = MAX, V_{IN} = 7.0V	mA
	DIR or $\overline{G}$				0.1	V_{CC} = MAX, V_{IN} = 5.5V	mA
	A or B						
I_{IL}	Input LOW Current				−0.4	V_{CC} = MAX, V_{IN} = 0.4V	mA
I_{OS}	Output Short Circuit Current (Note 2)		−40		−225	V_{CC} = MAX	mA
I_{CC}	Power Supply Current Total, Output HIGH				70	V_{CC} = MAX	mA
	Total, Output LOW				90		
	Total at HIGH Z				95		

AC CHARACTERISTICS: T_A = 25°C (T54LS/T74LS640/645)

Symbol	Parameter	Limits LS640 Min.	LS640 Typ.	LS640 Max.	LS645 Min.	LS645 Typ.	LS645 Max.	Test Conditions	Units
t_{PLH}	Propagation Delay, A to B		6.0	10		8.0	15	C_L = 45pF, R_L = 667Ω	ns
t_{PHL}			8.0	15		11	15		
t_{PLH}	Propagation Delay, B to A		6.0	10		8.0	15		ns
t_{PHL}			8.0	15		11	15		
t_{PZL}	Output Enable Time,		31	40		31	40		ns
t_{PZH}	$\overline{G}$ DIR to A		23	40		26	40		
t_{PZL}	Output Enable Time,		31	40		31	40		ns
t_{PZH}	$\overline{G}$ DIR to B		23	40		26	40		
t_{PLZ}	Output Disable Time,		15	25		15	25	C_L = 5.0pF	ns
t_{PHZ}	$\overline{G}$ DIR to A		15	25		15	25		
t_{PLZ}	Output Disable Time,		15	25		15	25		ns
t_{PHZ}	$\overline{G}$ DIR to B		15	25		15	25		

Notes:
1) For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

T54LS640/641/645
T74LS640/641/645

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (T54LS/T74LS641)

Symbol	Parameter		Limits Min.	Typ.	Max.	Test Conditions (Note 1)	Units
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs	V
V_{IL}	Input LOW Voltage	54			0.5	Guaranteed input LOW Voltage for all Inputs	V
		74			0.6		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA	V
I_{OH}	Output HIGH Current				100	V_{CC} = MIN, V_{OH} = 5.5V	μA
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 12mA; V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table	V
		74		0.35	0.5	I_{OL} = 24mA	
I_{IH}	Input HIGH Current				20 0.1	V_{CC} = MAX, V_{IN} = 2.7V V_{CC} = MAX, V_{IN} = 7.0V	μA mA
I_{IL}	Input LOW Current				−0.4	V_{CC} = MAX, V_{IN} = 0.4V	mA
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW Total at HIGH Z				 70 90 95	V_{CC} = MAX	mA

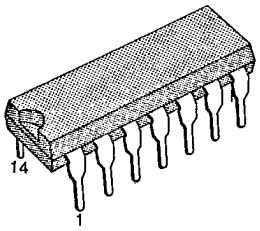
AC CHARACTERISTICS: T_A = 25°C (T54LS/T74LS641)

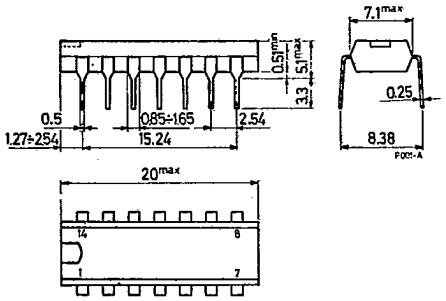
Symbol	Parameter	Limits Min.	Typ.	Max.	Test Conditions	Units
t_{PLH} t_{PHL}	Propagation Delay, A to B		17 16	25 25	V_{CC} = 5.0V C_L = 45pF R_L = 667Ω	ns
t_{PLH} t_{PHL}	Propagation Delay, B to A		17 16	25 25		ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{G}$, DIR to A		23 34	40 50		ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{G}$, DIR to B		25 37	40 50		ns

Notes:
1) For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2) Typical values are at V_{CC} = 5.0V, T_A = 25°C

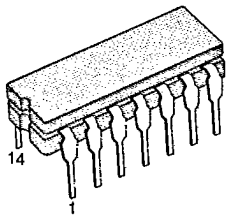
Packages

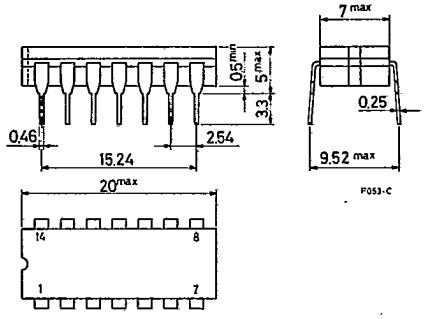
14-LEAD PLASTIC DIP





14-LEAD CERAMIC DIP





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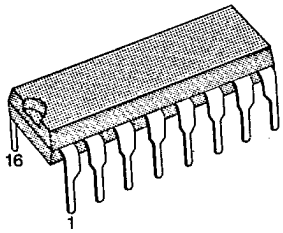
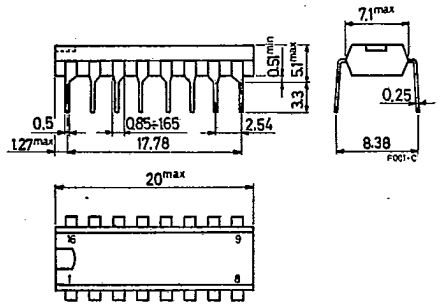
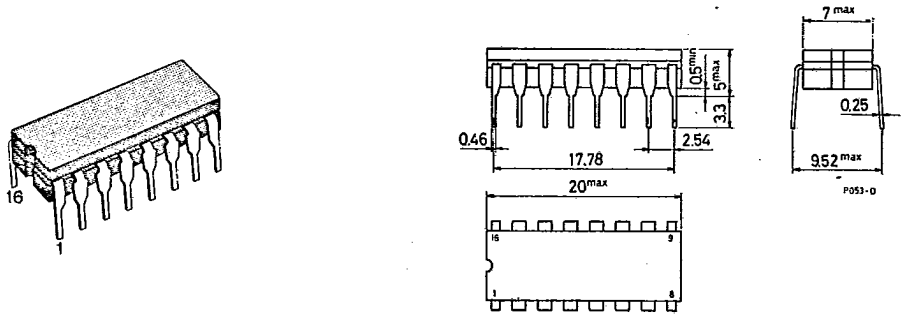




Packages

16-LEAD CERAMIC DIP



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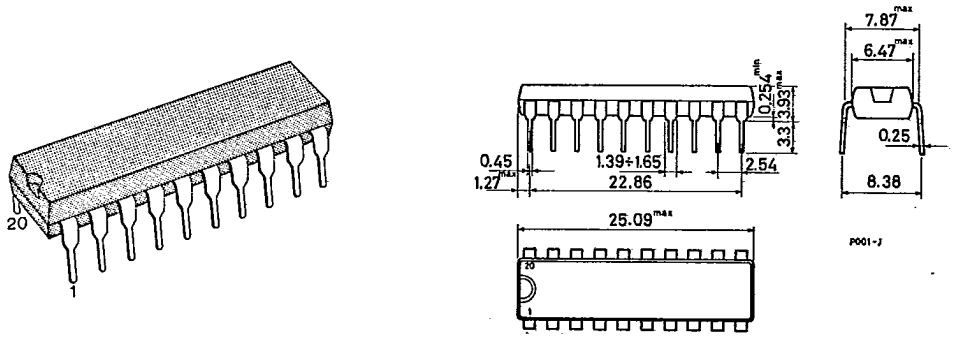

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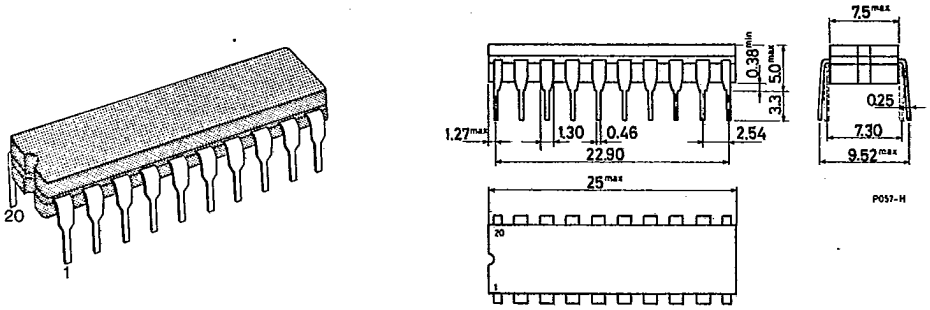
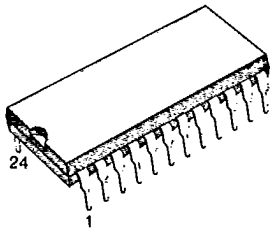
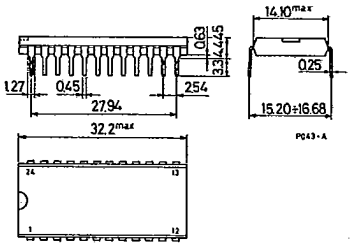


Packages

24-LEAD PLASTIC DIP





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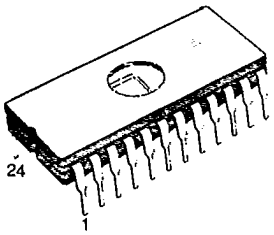
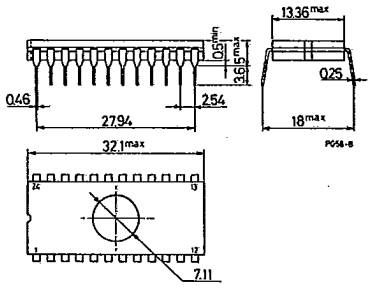
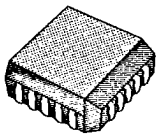
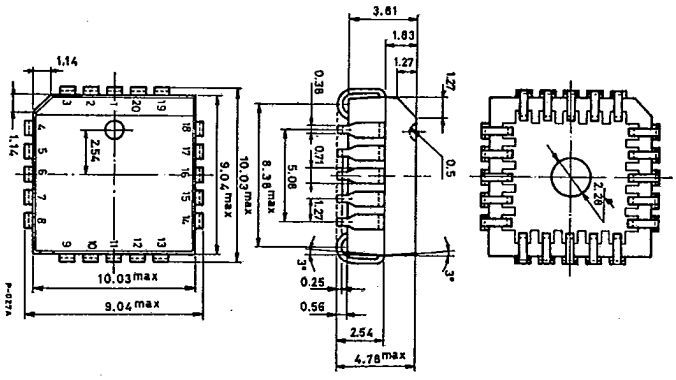




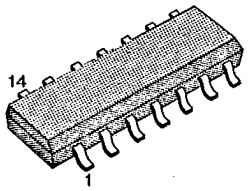
CHIP CARRIER 20 LEAD PLASTIC

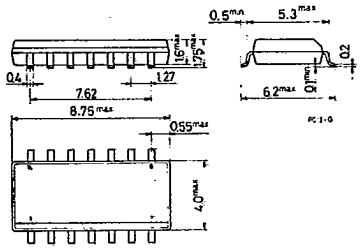




Packages

14-LEAD PLASTIC DIP MICROPACKAGE





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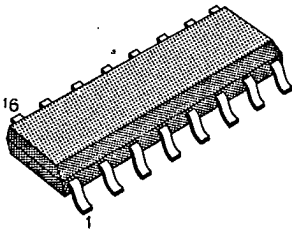

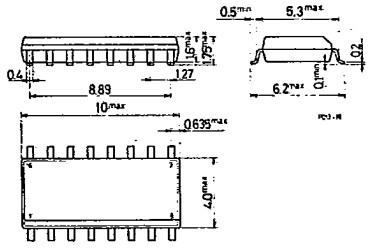

NOTE: FOR 20-LEAD PLASTIC DIP MICROPACKAGE CONTACT SGS

Surface Mounted

One possible solution to the important problem of PWB minimization, is that of using surface mounted components. Integrated circuits in SO (Small Outline) packages are made up of standard chips mounted in very small plastic packages.
The advantages given by using these devices are:

PWB Reduction

This is by far the most important advantage since the reduction of PWB size varies from 40 to 60% in comparison with standard board types. (See page 584 for package dimensions.)

Assembly Cost Reduction

SO Devices require no preliminary operation prior to mounting and can therefore be easily utilized in fully automatic equipment.

Increasing Reliability

The following characteristics lead to a higher level of reliability with respect to their standard packaged counter parts:

- The mounting system is fully automatic
- PWB number and the interconnections between them are reduced when the same number of devices are used.
- The high density of components on the board makes it thermally much more stable.

Noise Reduction and Improved Frequency Response

The reduction of the length of the connecting wires between the leads and the silicon guarantees a more homogeneous propogation delay between the external pins, with respect to the standard type.

Assembly Without Board Holes

The devices are placed on the board and soldered. This technology permits a higher level of tolerance in the positioning (automatic) of the device. For the standard DIP types this must be done with great accuracy due to the insertion of the leads into their holes.