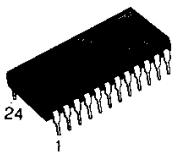
T54LS181
T74LS181

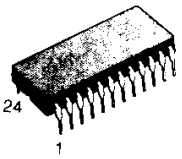
4-BIT ARITHMETIC LOGIC UNIT

DESCRIPTION

The T54LS181/T74LS181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all possible 16 logic, operations on two variables and a variety of arithmetic operations.



B1
Plastic Package



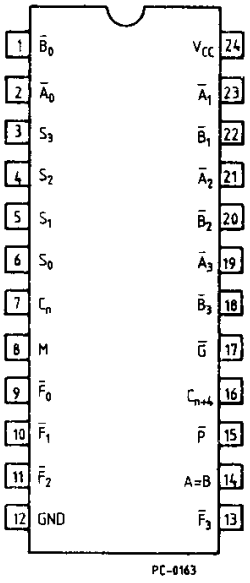
D1/D2
Ceramic Package

ORDERING NUMBERS:
T54LS181 D2
T74LS181 D1
T74LS181 B1

- PROVIDES 16 ARITHMETIC OPERATIONS ADD, SUBTRACT, COMPARE, DOUBLE, PLUS TWELVE OTHER ARITHMETIC OPERATIONS
- PROVIDES ALL 16 LOGIC OPERATIONS OF TWO VARIABLES:
  — EXCLUSIVE-OR, COMPARE, AND, NAND, OR, NOR, PLUS TEN OTHER LOGIC OPERATIONS
- FULL LOOKAHEAD FOR HIGH SPEED ARITHMETIC OPERATION ON LONG WORDS
- INPUT CLAMP DIODES

PIN CONNECTION
(top view)

DUAL IN LINE

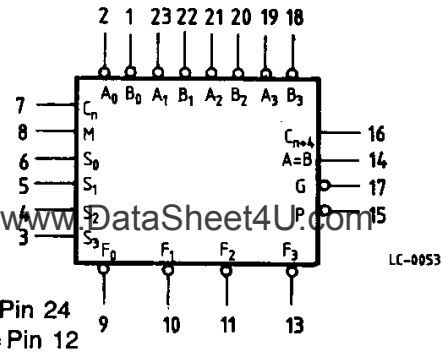


PC-0163

PIN NAMES

$\bar{A}_0$-$\bar{A}_3$,$\bar{B}_0$-$\bar{B}_3$	Operand (Active LOW) Inputs
S_0-S_3	Function-Select Inputs
M	Mode Control Input
C_n	Carry Input
$\bar{F}_0$-$\bar{F}_3$	Function (Active LOW) Outputs
A = B	Comparator Output
$\bar{G}$	Carry Generate (Active LOW) Output
$\bar{P}$	Carry Propagate (Active LOW) Output
C_{n+4}	Carry Output

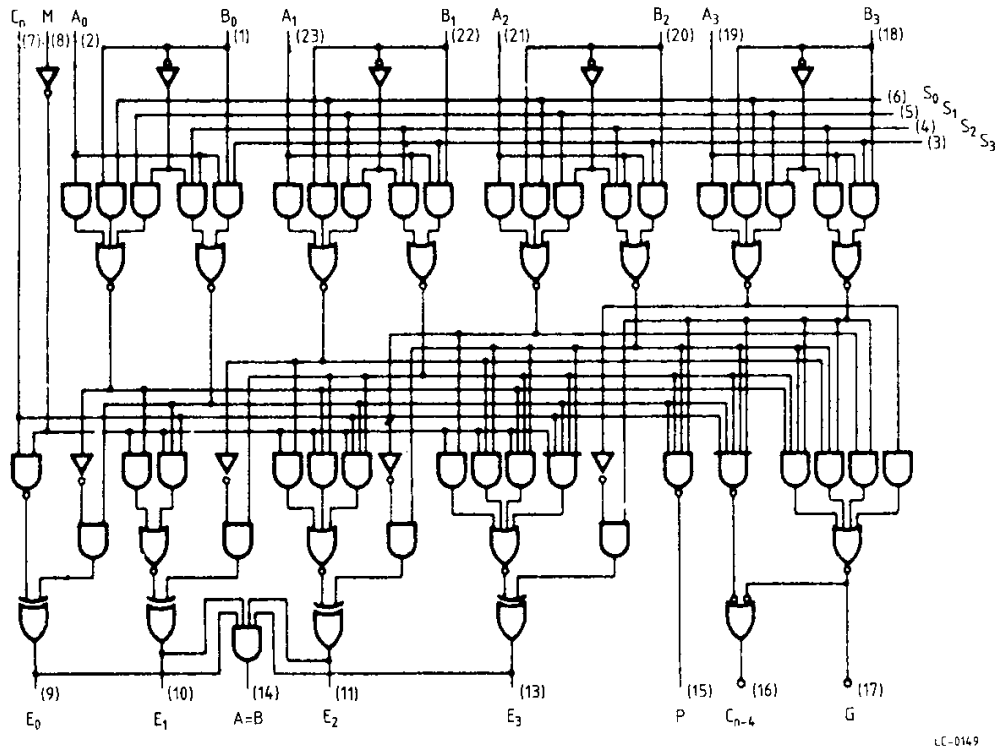
LOGIC SYMBOL



LC-0053

V_{CC} = Pin 24
GND = Pin 12

LOGIC DIAGRAM



V_{CC} = Pin 24
GND = Pin 12
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 15	V
V_O	Output Voltage, Applied to Output	−0.5 to 10	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS181D2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS181XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

T54LS181
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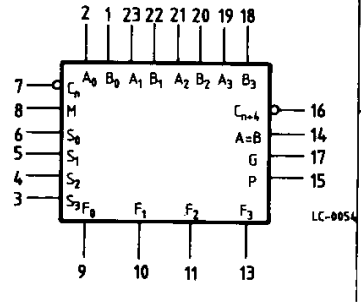
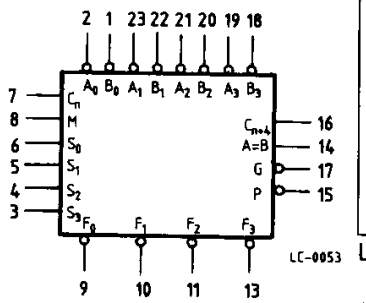
TRUTH TABLE

ACTIVE HIGH



ACTIVE LOW



MODE SELECT INPUTS				ACTIVE LOW INPUTS & OUTPUTS		ACTIVE HIGH INPUTS & OUTPUTS	
S_3	S_2	S_1	S_0	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = L)	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	AB minus 1	$\overline{A+B}$	A + B
L	L	H	L	$\overline{A+B}$	A$\overline{B}$ minus 1	$\overline{AB}$	A + $\overline{B}$
L	L	H	H	Logical 1	minus 1	Logical 0	minus 1
L	H	L	L	$\overline{A+B}$	A plus (A + $\overline{B}$)	$\overline{A\overline{B}}$	A plus A$\overline{B}$
L	H	L	H	$\overline{B}$	AB plus (A + $\overline{B}$)	$\overline{B}$	(A + B) plus A$\overline{B}$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1	A $\oplus$ B	A minus B minus 1
L	H	H	H	A + $\overline{B}$	A + $\overline{B}$	A$\overline{B}$	AB minus 1
H	L	L	L	$\overline{AB}$	A plus (A + B)	$\overline{A+B}$	A plus AB
H	L	L	H	A $\oplus$ B	A plus B	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	A$\overline{B}$ plus (A + B)	B	(A + $\overline{B}$) plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logical 0	A plus A*	Logical 1	A plus A*
H	H	L	H	A$\overline{B}$	AB plus A	A + $\overline{B}$	(A + B) plus A
H	H	H	L	AB	A$\overline{B}$ plus A	A + B	(A + $\overline{B}$) plus A
H	H	H	H	A	A	A	A minus 1

L = LOW Voltage Level, H = HIGH Voltage Level.
*Each bit is shifted to the next more significant position.
**Arithmetic operations expressed in 2s complement notation.

FUNCTIONAL DESCRIPTION

The T54LS181/T74LS181 is a 4-bit high speed Arithmetical Logic Unit (ALU). Controlled by the four Function Select Inputs (S_0...S_3) and the Mode Control Input (M), it can perform all the possible 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations.

When the Mode Control Input (M) is HIGH, all internal carriers are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control Input is LOW, the carriers are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the singal $\overline{P}$ (carry Proptage) and $\overline{G}$ (Carry Generate). $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, the LS181 can be used in a simple ripple carry mode by connecting the Carry Output (C_{n+4}) signal to the Carry Input (C_n) of the next unit. For high speed operation the LS181 is used in conjunction with other carry lookahead circuits. One carry lookahead package is required for each group of four LS181 devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the LS181 goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The A = B output is open collector and can be wired - AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A and B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated, the LS181 can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Test Conditions (Note 1)		Units
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs		V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Voltage for all Inputs		V
		74			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA		V
V_{OH}	Output HIGH Voltage Any Output except A = B	54	2.5	3.4		V_{CC} = MIN, I_{OH} = −400μA, V_{IN} = V_{IH} or V_{IL} per Truth Table		V
		74	2.7	3.4				
I_{OH}	Output HIGH Current A = B Output Only				100	V_{CC} = MIN, V_{OH} = 5.5V		
V_{OL}	Output LOW Voltage Except $\overline{G}$ and $\overline{P}$	54,74		0.25	0.4	I_{OL} = 4.0mA	V_{IL} per Truth Table	V
		74		0.35	0.5	I_{OL} = 8.0mA		V
	Output LOW Voltage Output $\overline{G}$			0.47	0.7	I_{OL} = 16mA		V
	Output LOW Voltage Output $\overline{P}$	54		0.35	0.6	I_{OL} = 8.0mA		V
		74		0.35	0.7			
I_{IH}	Input HIGH Current Mode Input				20	V_{CC} = MAX, V_{IN} = 2.7V		μA
	$\overline{A}$ and $\overline{B}$ Inputs				60			
	S Input				80			
	Carry Inputs				100			
	Mode Input				0.1	V_{CC} = MAX, V_{IN} = 7.0V		mA
	$\overline{A}$ and $\overline{B}$ Inputs				0.3			
	S Input				0.4			
	Carry Inputs				0.5			
I_{IL}	Input LOW Current Mode Input				−0.36	V_{CC} = MAX, V_{IN} = 0.4V		mA
	$\overline{A}$ and $\overline{B}$ Inputs				−1.08			
	S Input				−1.44			
	Carry Inputs				−2.0			
I_{OS}	Output Short Circuit Current (Note 2)		−20		−100	V_{CC} = MAX, V_{OUT} = 0V		mA
I_{CC}	Power Supply Current Condition A (Note 3)	54		20	32	V_{CC} = MAX		mA
		74		20	34			
	Power Supply Current Condition B (Note 3)	54		21	35			
		74		21	37			

Notes:

1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2) Not more than one output should be shorted at a time.
3) With output open, I_{CC} is measured for the following conditions:
   A. S_0 through S_3, M and A inputs are at 4.5V, all other inputs are grounded.
   B. S_0 through S_3 and M are at 4.5V, all other inputs are grounded.
4) Typical values are at V_{CC} = 5.0V, T_A = 25°C

AC CHARACTERISTICS: $T_A = 25°C$

Symbol	Parameter	Limits		Test Conditions	Units
		Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay, (C_n to C_{n+4})	18 13	27 20	M = 0V, (Sum or Diff Mode) See Fig. 1 and Tables I and II	ns
t_{PLH} t_{PHL}	(C_n to $\overline{F}$ outputs)	17 13	26 20	M = 0V, (Sum Mode) See Fig. 1 and Table I	ns
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to $\overline{G}$ Outputs)	19 15	29 23	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$ (Sum Mode) See Fig. 1 and Table I	ns
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to $\overline{G}$ Outputs)	21 21	32 32	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$ (Diff Mode) See Fig. 2 and Table II	ns
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to $\overline{P}$ Outputs)	20 20	30 30	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$ (Sum Mode) See Fig. 1 and Table I	ns
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to $\overline{P}$ Outputs)	20 22	30 33	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$ (Diff Mode) See Fig. 2 and Table II	ns
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to any $\overline{F}$ Outputs)	21 13	32 20	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$ (Sum Mode) See Fig. 1 and Table I	ns
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to any $\overline{F}$ Outputs)	21 21	32 32	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$ (Diff Mode) See Fig. 2 and Table II	ns
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to any $\overline{F}$ Outputs)	22 26	32 38	M = 4.5V (Logic Mode) See Fig. 1 and Table III	ns
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to C_{n+4} Output)	25 25	38 38	$M = 0V$, $S_0 = S_3 = 4.5V$, $S_1 = S_2 = 0V$ (Sum Mode) See Fig. 3 and Table I	ns
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to C_{n+4} Output)	27 27	41 41	$M = 0V$, $S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$ (Diff Mode)	ns
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to A = B Output)	33 41	50 62	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$ $R_L = 2k\Omega$ (Diff Mode) See Fig. 2 and Table II	ns

AC WAVEFORMS

Fig. 1

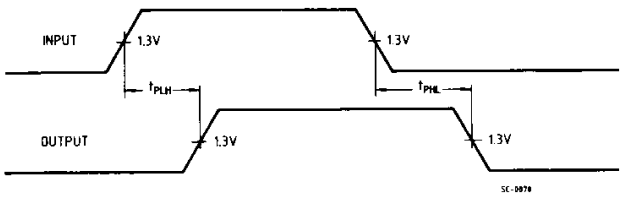


Fig. 2

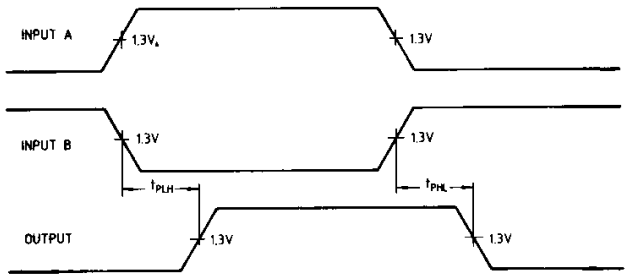
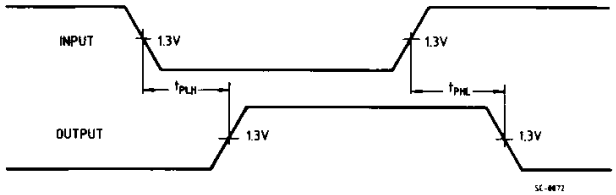


Fig. 3



SUM MODE TEST TABLE I

FUNCTION INPUTS: $S_0 = S_3 = 4.5V$, $S_1 = S_2 = M = 0V$

Parameter	Input Under Test	OTHER INPUT SAME BIT		OTHER DATA INPUTS		Output Under Test
		APPLY 4.5V	APPLY GND	APPLY 4.5V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}_I$	$\overline{B}_I$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_I$
t_{PLH} t_{PHL}	$\overline{B}_I$	$\overline{A}_I$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_I$
t_{PLH} t_{PHL}	$\overline{A}_I$	$\overline{B}_I$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_{I+1}$
t_{PLH} t_{PHL}	$\overline{B}_I$	$\overline{A}_I$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_{I+1}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

DIFF MODE TEST TABLE II

FUNCTION INPUTS: $S_1 = S_2 = 4.5V$, $S_0 = S_3 = M = 0V$

Parameter	Input Under Test	OTHER INPUT SAME BIT		OTHER DATA INPUTS		Output Under Test
		APPLY 4.5V	APPLY GND	APPLY 4.5V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_I$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_I$
t_{PLH} t_{PHL}	$\overline{A}_I$	None	$\overline{B}_I$	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_{I+1}$
t_{PLH} t_{PHL}	$\overline{B}_I$	$\overline{A}_I$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_{I+1}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4}

LOGIC TEST TABLE III

Parameter	Input Under Test	OTHER INPUT SAME BIT		OTHER DATA INPUTS		Output Under Test	Function Inputs
		APPLY 4.5V	APPLY GND	APPLY 4.5V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$	$S_1 = S_2 = M = 4.5V$ $S_0 = S_3 = 0V$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$	$S_1 = S_2 = M = 4.5V$ $S_0 = S_3 = 0V$