OKI Open up your dreams

OKI Semiconductor

FEDL2216FULL-03
Issue Date: Sep. 20, 2007

ML2216-XXX/ML22P16

Oki ADPCM2 Algorithm-Based Speech Synthesis LSI

GENERAL DESCRIPTION

The ML2216-XXX is speech synthesis device with a 8Mbit P2ROM built-in.
The ML2216-XXX incorporates ADPCM2 decoder, 12-bit D/A converter, and low-pass filter. Moreover, the monophonic speaker amplifier for driving a direct speaker is built in.
The ML2216-XXX carried out all functions required for a voice response circuit to one chip. For this reason, inclusion to small and pocket equipment became still easier.

ML2216-xxx serves as write-in shipment.
ML22P16 is speech synthesis device with 8M bit OTP memory built-in. User is able to program a device one time by using exclusive tool.

FEATURES

- Built-in memory capacity and the Maximum playback time length (please refer to the following table)

Type	ROM capacity	Maximum playback time length (sec) (In 4-bit ADPCM2)		
		F_{SAM} = 4.0 kHz	F_{SAM} = 8.0 kHz	F_{SAM} = 16 kHz
ML2216/ML22P16	8 Mbit	524	262	131

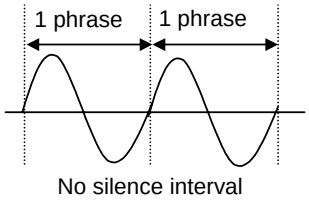
- Non-linear 8-bit PCM, 8-bit PCM, 16-bit PCM, and 4-bit ADPCM2 algorithms
- Sampling frequency: 4.0 kHz, 5.3 kHz, 6.4 kHz, 8.0 kHz, 10.7 kHz, 12.8 kHz, 16.0 kHz
- 12-bit D/A converter built in
- Built-in low-pass filter: Digital filter
- Amplifier built-in for a speaker drive: 0.3W 8Ω(At VDD=5.0V)
- CPU interface: 3 line type serial clock synchronization
- Maximum number of phrases: 256 phrases
- Volume control function: VOLUME command (16 step / OFF)
- Repeat function: LOOP command
- Master clock frequency: 4.096 MHz
- Power supply voltage: 2.7V to 3.6V or 4.5V to 5.5V
- Operating temperature: -20°C to +85°C
- Package: 44-pin plastic QFP (QFP44-P-910-0.80-2K)
  (ML2216-XXXGA, ML22P16GA)

Downloaded from Elcodis.com electronic components distributor

Table below summarizes the points of difference between the ML2250 family and the ML2216/ML22P16.

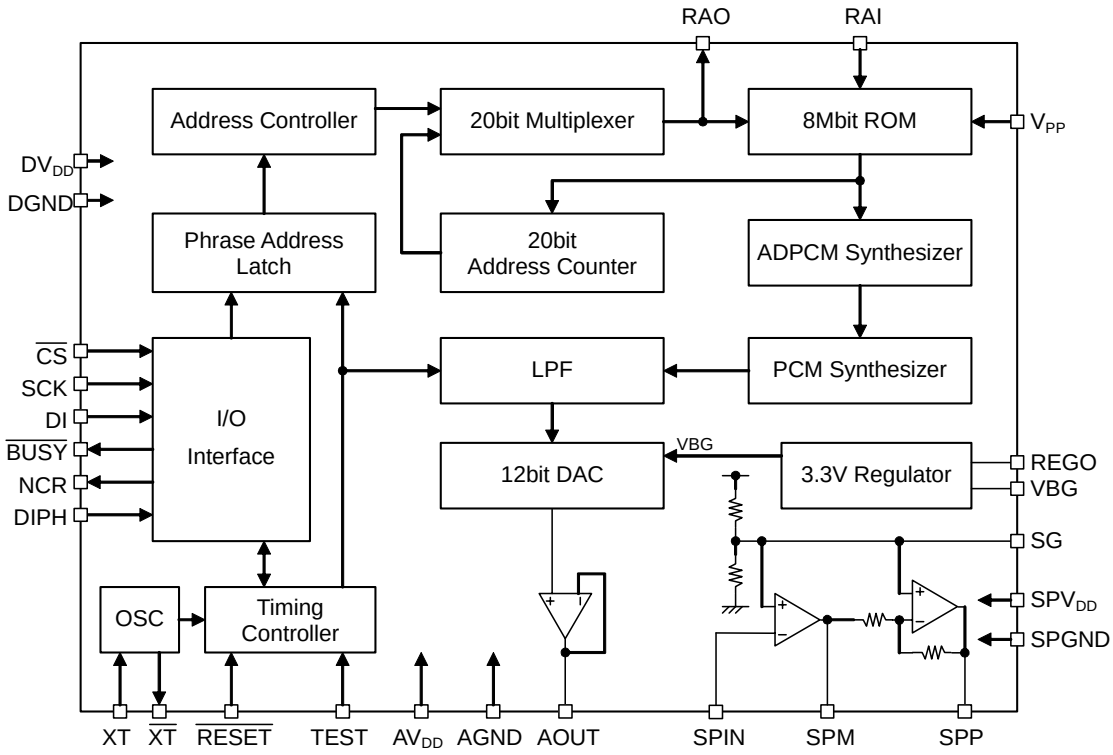
	ML2250 family	ML2216/ML22P16
Interface	Parallel or serial	Serial
Playback method	2-bit ADPCM2 4-bit ADPCM2 8-bit PCM 8-bit non-linear PCM 16-bit PCM	4-bit ADPCM2 8-bit PCM 8-bit non-linear PCM 16-bit PCM
Max. number of phrases	256	256
Sampling frequency (kHz)	4.0/5.3/6.4/8.0/10.7/12.8/16.0/21.3/25.6/32.0/42.7/48.0	4.0/5.3/6.4/8.0/10.7/12.8/16.0
Clock frequency	4.096 MHz	4.096 MHz
D/A converter	Voltage type: 14 bits	Current type: 12 bits
Low-pass filter	FIR type interpolation filter	Secondary comb filter
Amplifier for a speaker drive	None	built-in
Number of channels	2 channels	1 channel
Phrase control table	Both 2 channels without user definable phrase restrictions	1 channel without user definable phrase restrictions
Volume adjustment	29 steps (–2 dB/–5 dB steps)	16 steps
Silent insertion function	built-in(4ms to 1024ms)	built-in(20ms to 1024ms)
Repeat function	No limit	No limit
Seam silence interval in continuous playback	0 (Note)	0 (Note)
Others	External data input possible	—
Package	44-pin plastic QFP	44-pin plastic QFP

Note: Continuous playback shown in the figure below is possible.



Downloaded from Elcodis.com electronic components distributor

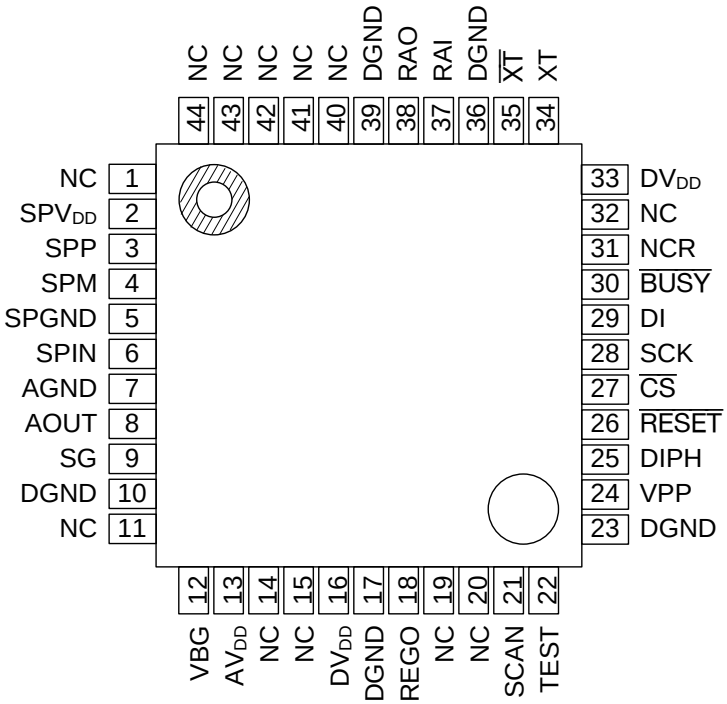
BLOCK DIAGRAM



Downloaded from Elcodis.com electronic components distributor

PIN CONFIGURATION (TOP VIEW)

44-pin plastic QFP



NC: No Connection

Downloaded from Elcodis.com electronic components distributor

PIN DESCRIPTIONS

Pin	Symbol	Type	Description
26	$\overline{\text{RESET}}$	I	reset input pin. At “L” level input, the device enters the initial state. During reset input, operation of all circuits stops and it will be in a power down state. Input the "L" level at the time of a power supply injection. After power supply voltage is stabilized, please make it "H" level.
27	$\overline{\text{CS}}$	I	CPU interface chip select pin. A serial interface becomes effective on the "L" level.
28	SCK	I	serial clock input pin.
29	DI	I	serial data input pin.
25	DIPH	I	A DIPH pin chooses the timing which takes in serial data inside LSI. When a DIPH pin is the "L" level, DI input data is taken in inside LSI by the rising edge of a SCK clock. When a DIPH pin is "H" level, DI input data is taken in inside LSI by the falling edge of a SCK clock.
30	$\overline{\text{BUSY}}$	O	A $\overline{\text{BUSY}}$ pin outputs the signal which shows a phrase reproduction state. The "L" level is outputted during reproduction.
31	NCR	O	A NCR pin outputs the signal which shows the input permission state of a command. When the NCR pin is "H" level ,a command input is possible. When the NCR pin is the "L" level ,a command input cannot be performed.
34	XT	I	Wired to a crystal or ceramic oscillator. A feedback resistor of around 1 MΩ is built in between this XT pin and $\overline{\text{XT}}$ pin (pin 35). When using an external clock, input the clock from this pin. When you use a crystal or ceramic oscillator, please connect with the latest of LSI as much as possible.
35	$\overline{\text{XT}}$	O	Wired to a ceramic or crystal oscillator. When using an external clock, keep this pin open. When you use a crystal or ceramic oscillator, please connect with the latest of LSI as much as possible.
18	REGO	O	Regulator output pin. It becomes the power supply of Built-in P2ROM. Insert a 10 μF or larger capacitor between this pin and DGND pin.
12	VBG	O	Standard voltage output pin for 3.3V regulators. Insert a 0.1 μF capacitor between this pin and DGND pin.
9	SG	O	Standard voltage output pin of built-in speaker amplifier. Insert a 0.1 μF or larger capacitor between this pin and AGND pin.
8	AOUT	O	Analog output pin. When you input into built-in speaker amplifier, insert a 10 μF capacitor between this pin and SPIN pin.

Downloaded from Elcodis.com electronic components distributor

Pin	Symbol	Type	Description
6	SPIN	I	Analog input pin of built-in speaker amplifier. A reversal amplifier consists of connecting external resistance between AOUT pin and SPM pin.
4	SPM	O	Analog output pin of built-in speaker amplifier. A speaker is connected between SPM pin and SPP pin. External resistance is connected between SPIN pin and this pin.
3	SPP	O	Analog output pin of built-in speaker amplifier. A speaker is connected between SPM pin and SPP pin.
38	RAO	O	Address output pin of Built-in P2ROM. It connects with RAI pin directly.
37	RAI	I	Address input pin of Built-in P2ROM. RAO pin is connected directly.
24	VPP	I	Program power supply pin at the time of the data writing to P2ROM. Input “L” level to this pin.
22	TEST	I	Test pin for the device. Input “L” level to this pin. This pin has a pull-down resistor built in.
21	SCAN	I	Test pin for the device. Input “L” level to this pin. This pin has a pull-down resistor built in.
16, 33	DV_{DD}	—	Digital power supply pin. Insert a 0.1 μF or larger bypass capacitor between this pin and DGND pin.
10, 17, 23, 36, 39	DGND	—	Digital ground pin.
13	AV_{DD}	—	Analog power supply pin. Insert a 0.1 μF or larger bypass capacitor between this pin and AGND pin.
7	AGND	—	Digital ground pin.
2	SPV_{DD}	—	Speaker amplifier ower supply pin. Insert a 10 μF or larger bypass capacitor between this pin and SPGND pin.
5	SPGND	—	Speaker amplifier Ground pin.

Downloaded from Elcodis.com electronic components distributor

ABSOLUTE MAXIMUM RATINGS

(DGND = AGND = SPGND = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Digital power supply voltage	DV_{DD}	Ta = 25°C	–0.3 to +7.0	V
Analog power supply voltage	AV_{DD}		–0.3 to +7.0	V
Speaker amplifier power supply voltage	SPV_{DD}		–0.3 to +7.0	V
Input voltage	V_{IN}	Ta = 25°C	–0.3 to DV_{DD} +0.3	V
Permissible loss	P_D		1.66	W
Output short-circuit current	I_{SC}	Except SPM and SPP and REGO pin	10	mA
		SPM and SPP pin	540	mA
		REGO pin	40	mA
Storage temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(DGND = AGND = SPGND = 0 V)

Parameter	Symbol	Condition	Range			Unit
Digital power supply voltage	DV_{DD}	When not using a regulator	2.7 to 3.6			V
		When using a regulator	4.5 to 5.5			V
Analog power supply voltage	AV_{DD}	When not using a regulator	2.7 to 3.6			V
		When using a regulator	4.5 to 5.5			V
Speaker amplifier power supply voltage	SPV_{DD}	When not using a regulator	2.7 to 3.6			V
		When using a regulator	4.5 to 5.5			V
Operating temperature	T_{OP}	—	-20 to +85			°C
Master clock frequency	f_{OSC}	—	Min.	Typ.	Max.	MHz
			3.5	4.096	4.5	
Crystal oscillation external capacity	Cd,Cg	—	15	30	45	pF

Downloaded from Elcodis.com electronic components distributor

ELECTRICAL CHARACTERISTICS

DC Characteristics (3 V)

DV_{DD} = AV_{DD} = SPV_{DD} = 2.7 to 3.6 V, DGND = AGND = SPGND = 0 V, Ta = -20 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	0.86×V_{DD}	—		V
"L" input voltage	V_{IL}	—	—	—	0.14× V_{DD}	V
"H" output voltage1	V_{OH1}	I_{OH} = –1mA	V_{DD} –0.4	—	—	V
"H" output voltage2 (Note 1)	V_{OH2}	I_{OH} = –100µA	V_{DD} –0.4	—	—	V
"L" output voltage1	V_{OL1}	I_{OL} = 4 mA	—	—	0.4	V
"L" output voltage2 (Note 1)	V_{OL2}	I_{OL} = 100 µA	—	—	0.4	V
"H" input current 1	I_{IH1}	V_{IH} = DV_{DD}	—	—	10	µA
"H" input current 2 (Note 2)	I_{IH2}	V_{IH} = DV_{DD}	0.3	2.0	15	µA
"H" input current 3 (Note 3)	I_{IH3}	V_{IH} = DV_{DD}	5	40	130	µA
"L" input current 1	I_{IL1}	V_{IL} = DGND	–10	—	—	µA
"L" input current 2 (Note 2)	I_{IL2}	V_{IL} = DGND	–15	–2.0	–0.3	µA
"L" input current3 (Note 3)	I_{IL3}	V_{IL} = DGND	–10	—	—	µA
Playback Operating current consumption 1	I_{DD}	f_{OSC} = 4.096 MHz at no load Read Operation	—	—	10	mA
Standby current consumption	I_{DDS}	Ta = -20 to +85°C	—	1	20	µA

Notes: 1.Applies to $\overline{XT}$pin.
2.Applies to XT pin.
3.Applies to TEST and SCAN pins.

Downloaded from Elcodis.com electronic components distributor

DC Characteristics (5 V)

DV_{DD} = AV_{DD} = SPV_{DD} = 4.5 to 5.5 V, DGND = AGND = SPGND = 0 V, Ta = -20 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	0.8×V_{DD}	—		V
"L" input voltage	V_{IL}	—	—	—	0.2× V_{DD}	V
"H" output voltage1	V_{OH1}	I_{OH} = –1mA	V_{DD} –0.4	—	—	V
"H" output voltage2 (Note 1)	V_{OH2}	I_{OH} = –100µA	V_{DD} –0.4	—	—	V
"L" output voltage1	V_{OL1}	I_{OL} = 4 mA	—	—	0.4	V
"L" output voltage2 (Note 1)	V_{OL2}	I_{OL} = 100 µA	—	—	0.4	V
"H" input current 1	I_{IH1}	V_{IH} = DV_{DD}	—	—	10	µA
"H" input current 2 (Note 2)	I_{IH2}	V_{IH} = DV_{DD}	0.8	5.0	20	µA
"H" input current 3 (Note 3)	I_{IH3}	V_{IH} = DV_{DD}	30	140	350	µA
"L" input current 1	I_{IL1}	V_{IL} = DGND	–10	—	—	µA
"L" input current 2 (Note 2)	I_{IL2}	V_{IL} = DGND	–20	–5.0	–0.8	µA
"L" input current3 (Note 3)	I_{IL3}	V_{IL} = DGND	–10	—	—	µA
Playback Operating current consumption 1	I_{DD}	f_{OSC} = 4.096 MHz at no load Read Operation	—	—	10	mA
Standby current consumption	I_{DDS}	Ta =-20 to +85°C	—	1	30	µA

Notes: 1.Applies to $\overline{XT}$pin.
2.Applies to XT pin.
3.Applies to TEST and SCAN pins.

Downloaded from Elcodis.com electronic components distributor

Analog Section Characteristics (3 V)

DV_{DD} = AV_{DD} = SPV_{DD} = 2.7 to 3.6 V, DGND = AGND = SPGND = 0 V, Ta = -20 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AOUT output load resistance	R_{LA}	When 1 / 2AV_{DD} output	5	—	—	kΩ
AOUT output voltage range	V_{AO}	No output load	0.1	—	2.0	V
SPIN Input resistance	R_{SPI}	—	1	—	—	MΩ
SPP pull-down resistor	R_{SPP}	When power-down state	15	—	65	kΩ
SPM pull-down resistor	R_{SPM}	When power-down state	1	—	20	kΩ
SPM, SPP output load resistance	R_{LSP}	—	8	—	—	Ω
Speaker amplifier output electric power	P_{SPO}	SPV_{DD} = 3.3V,fin = 1kHz, R_{SPO} = 8Ω,THD≥10%	80	100	—	mW
SPM-SPP output offset voltage at non-signal	V_{OF}	SPIN – SPM profit = 0dB When 8Ω load	-50	—	50	mV
SG output voltage	V_{SG}	—	0.48×AV_{DD}	0.5×AV_{DD}	0.52×AV_{DD}	V
SG output resistance	R_{SG}	—	12	20	28	kΩ

Downloaded from Elcodis.com electronic components distributor

Analog Section Characteristics (5 V)

DV_{DD} = AV_{DD} = SPV_{DD} = 4.5 to 5.5 V, DGND = AGND = SPGND = 0 V, Ta = -20 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AOUT output load resistance	R_{LA}	When 1 / 2AV_{DD} output	50	—	—	kΩ
AOUT output voltage range	V_{AO}	No output load	0.1	—	2.0	V
SPIN Input resistance	R_{SPI}	—	1	—	—	MΩ
SPP pull-down resistor	R_{SPP}	When power-down state	15	—	65	kΩ
SPM pull-down resistor	R_{SPM}	When power-down state	1	—	20	kΩ
SPM, SPP output load resistance	R_{LSP}	—	8	—	—	Ω
Speaker amplifier output electric power	P_{SPO}	SPV_{DD} = 5.0V,fin = 1kHz, R_{SPO} = 8Ω,THD≥10%	250	300	—	mW
SPM-SPP output offset voltage at non-signal	V_{OF}	SPIN – SPM profit = 0dB When 8Ω load	-50	—	50	mV
SG output voltage	V_{SG}	—	0.48×AV_{DD}	0.5×AV_{DD}	0.52×AV_{DD}	V
SG output resistance	R_{SG}	—	12	20	28	kΩ

Downloaded from Elcodis.com electronic components distributor

AC Characteristics (3 V)

DV_{DD} = AV_{DD} = SPV_{DD} = 2.7 to 3.6 V, DGND = AGND = SPGND = 0 V, Ta = -20 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Master clock duty cycle	f_{duty}	—	40	50	60	%
$\overline{\text{RESET}}$ input pulse width	t_{RST}	—	1	—	—	µs
$\overline{\text{SCK}}$ setup time for falling edge of $\overline{\text{CS}}$	t_{CKS}	—	200	—	—	ns
$\overline{\text{SCK}}$ hold time for rising edge of $\overline{\text{CS}}$	t_{CKH}	—	200	—	—	ns
Data setup time for rising edge of SCK	t_{DIS1}	DIPH pin = "L"	50	—	—	ns
Data hold time for rising edge of SCK	t_{DIH1}	DIPH pin = "L"	50	—	—	ns
Data setup time for falling edge of SCK	t_{DIS2}	DIPH pin = "H"	50	—	—	ns
Data hold time for falling edge of SCK	t_{DIH2}	DIPH pin = "H"	50	—	—	ns
SCK "H" level pulse width	t_{SCKH}	—	200	—	—	ns
SCK "L" level pulse width	t_{SCKL}	—	200	—	—	ns
NCR output delay time for rising edge of SCK	t_{DN1}	DIPH pin = "L"	—	—	150	ns
NCR output delay time for falling edge of SCK	t_{DN2}	DIPH pin = "H"	—	—	150	ns
$\overline{\text{BUSY}}$ output delay time for rising edge of SCK	t_{DB1}	DIPH pin = "L"	—	—	150	ns
$\overline{\text{BUSY}}$ output delay time for falling edge of SCK	t_{DOH1}	DIPH pin = "L"	—	—	150	ns
Command input interval time	t_{INT}	f_{OSC} = 4.096 MHz, at command input(STOP,SLOOP, CLOOP,VOL)	6	—	—	µs
Command input permission time	t_{CM}	f_{OSC} = 4.096 MHz, at continuous playback, at SLOOP command input	—	—	10	ms
"L" level output time of NCR and $\overline{\text{BUSY}}$ at PUP1 command input	t_{PUP1}	f_{OSC} = 4.096 MHz, at external clock input	1.9	2	2.1	ms
"L" level output time of NCR and $\overline{\text{BUSY}}$ at PUP2 command input	t_{PUP2}		65	66	67	ms
"L" level output time of NCR and $\overline{\text{BUSY}}$ at PDWN1 command input	t_{PD1}	f_{OSC} = 4.096 MHz	—	—	6	µs
"L" level output time of NCR and $\overline{\text{BUSY}}$ at PDWN2 command input	t_{PD2}		63	64	65	ms
"L" level output time1 of NCR(Note 1)	t_{NCR1}	f_{OSC} = 4.096 MHz	—	—	6	µs
"L" level output time2 of NCR(Note 2)	t_{NCR2}	f_{OSC} = 4.096 MHz after the phrase data of the PLAY command was inputted	—	4.125	4.38	ms
"L" level output time of $\overline{\text{BUSY}}$(Note 3)	t_{BSY}	f_{OSC} = 4.096 MHz	—	—	6	µs

Notes: 1.Applies to command input. It removes, after the command (PUP1, PUP2 ,PDWN1, PDWN2, SLOOP, CLOOP) was inputted. And It removes, after the phrase data of the PLAY command was inputted.
2.At the time after playback (fs=4.0kHz). In the case of other sampling frequencies, the time of this item is proportional to the sampling frequency. After reset release is set as 4kHz of sampling frequencies.
3.Applies to command input. It removes, after the command (PUP1, PUP2, PDWN1, PDWN2, SLOOP, CLOOP) was inputted, when not playback. And It removes, after the phrase data of the PLAY command was inputted.

Downloaded from Elcodis.com electronic components distributor

AC Characteristics (5 V)

DV_{DD} = AV_{DD} = SPV_{DD} = 4.5 to 5.5 V, DGND = AGND = SPGND = 0 V, Ta = -20 to +85°C

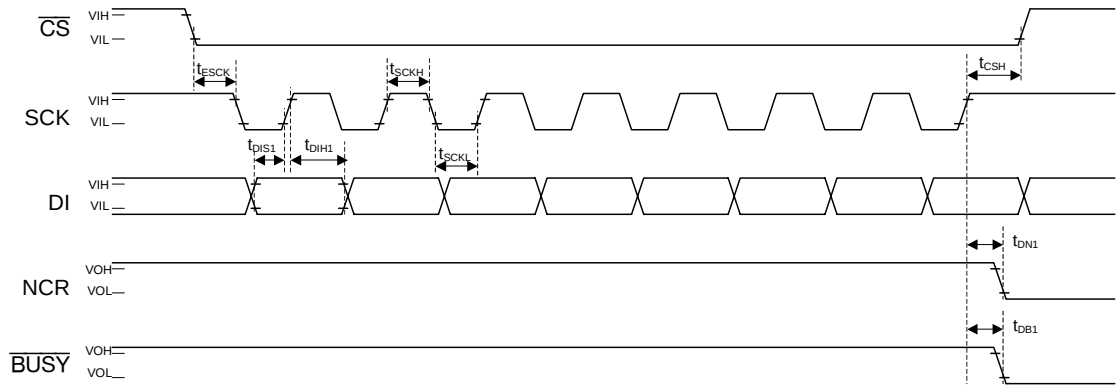
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Master clock duty cycle	f_{duty}	—	40	50	60	%
$\overline{\text{RESET}}$ input pulse width	t_{RST}	—	1	—	—	µs
$\overline{\text{SCK}}$ setup time for falling edge of $\overline{\text{CS}}$	t_{CKS}	—	200	—	—	ns
$\overline{\text{SCK}}$ hold time for rising edge of $\overline{\text{CS}}$	t_{CKH}	—	200	—	—	ns
Data setup time for rising edge of SCK	t_{DIS1}	DIPH pin = "L"	50	—	—	ns
Data hold time for rising edge of SCK	t_{DIH1}	DIPH pin = "L"	50	—	—	ns
Data setup time for falling edge of SCK	t_{DIS2}	DIPH pin = "H"	50	—	—	ns
Data hold time for falling edge of SCK	t_{DIH2}	DIPH pin = "H"	50	—	—	ns
SCK "H" level pulse width	t_{SCKH}	—	200	—	—	ns
SCK "L" level pulse width	t_{SCKL}	—	200	—	—	ns
NCR output delay time for rising edge of SCK	t_{DN1}	DIPH pin = "L"	—	—	150	ns
NCR output delay time for falling edge of SCK	t_{DN2}	DIPH pin = "H"	—	—	150	ns
$\overline{\text{BUSY}}$ output delay time for rising edge of SCK	t_{DB1}	DIPH pin = "L"	—	—	150	ns
$\overline{\text{BUSY}}$ output delay time for falling edge of SCK	t_{DOH1}	DIPH pin = "L"	—	—	150	ns
Command input interval time	t_{INT}	f_{OSC} = 4.096 MHz, at command input(STOP,SLOOP, CLOOP,VOL)	6	—	—	µs
Command input permission time	t_{CM}	f_{OSC} = 4.096 MHz, at continuous playback, at SLOOP command input	—	—	10	ms
"L" level output time of NCR and $\overline{\text{BUSY}}$ at PUP1 command input	t_{PUP1}	f_{OSC} = 4.096 MHz, at external clock input	1.9	2	2.1	ms
"L" level output time of NCR and $\overline{\text{BUSY}}$ at PUP2 command input	t_{PUP2}		65	66	67	ms
"L" level output time of NCR and $\overline{\text{BUSY}}$ at PDWN1 command input	t_{PD1}	f_{OSC} = 4.096 MHz	—	—	6	µs
"L" level output time of NCR and $\overline{\text{BUSY}}$ at PDWN2 command input	t_{PD2}		63	64	65	ms
"L" level output time1 of NCR(Note 1)	t_{NCR1}	f_{OSC} = 4.096 MHz	—	—	6	µs
"L" level output time2 of NCR(Note 2)	t_{NCR2}	f_{OSC} = 4.096 MHz after the phrase data of the PLAY command was inputted	—	4.125	4.38	ms
"L" level output time of $\overline{\text{BUSY}}$(Note 3)	t_{BSY}	f_{OSC} = 4.096 MHz	—	—	6	µs

Notes:
1. Applies to command input. It removes, after the command (PUP1,PUP2,PDWN1,PDWN2,SLOOP, CLOOP) was inputted. And It removes, after the phrase data of the PLAY command was inputted.
2. At the time after playback(fs=4.0kHz). In the case of other sampling frequencies, the time of this item is proportional to the sampling frequency. After reset release is set as 4kHz of sampling frequencies.
3. Applies to command input. It removes, after the command (PUP1,PUP2,PDWN1,PDWN2,SLOOP, CLOOP) was inputted, when not playback. And It removes, after the phrase data of the PLAY command was inputted.

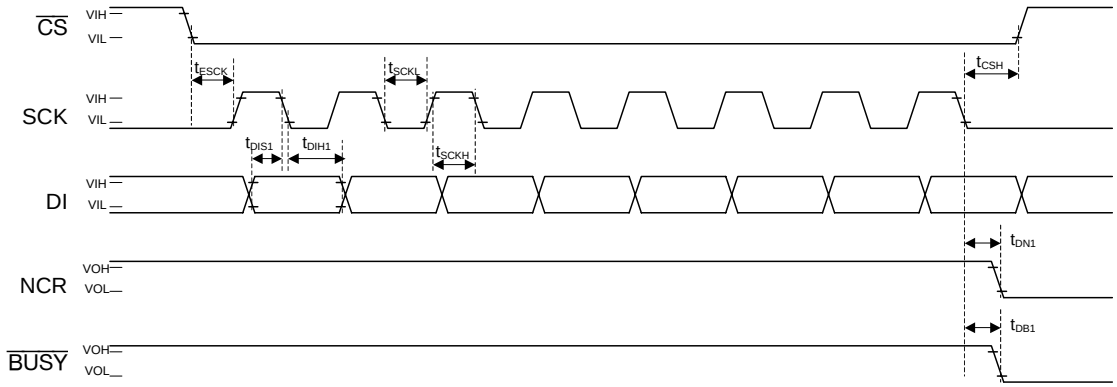
Downloaded from Elcodis.com electronic components distributor

TIMING DIAGRAMS

Serial CPU Interface Timing (at DIPH pin = “L”)

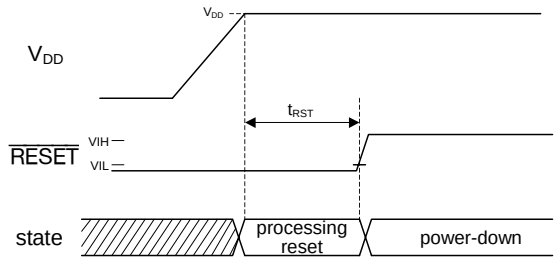


Serial CPU Interface Timing(at DIPH pin = “H”)



Downloaded from Elcodis.com electronic components distributor

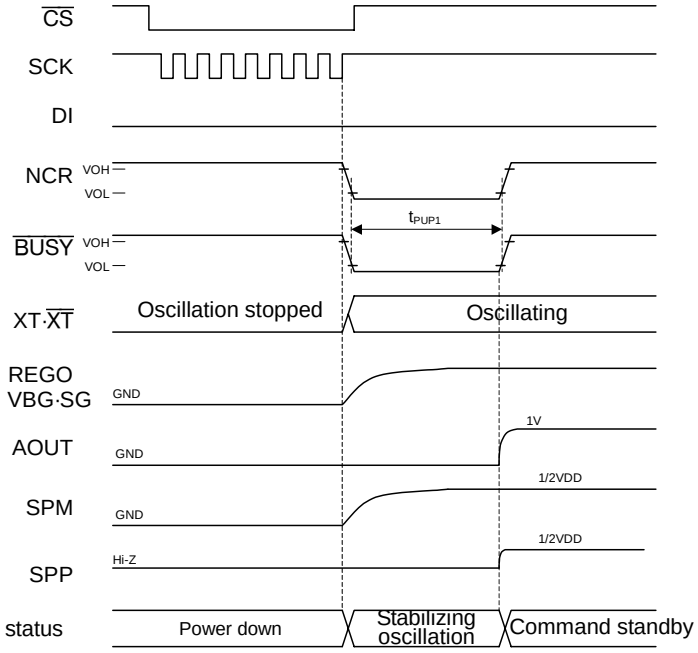
Power-On Timing



After a power supply injection will be in an oscillation stop.

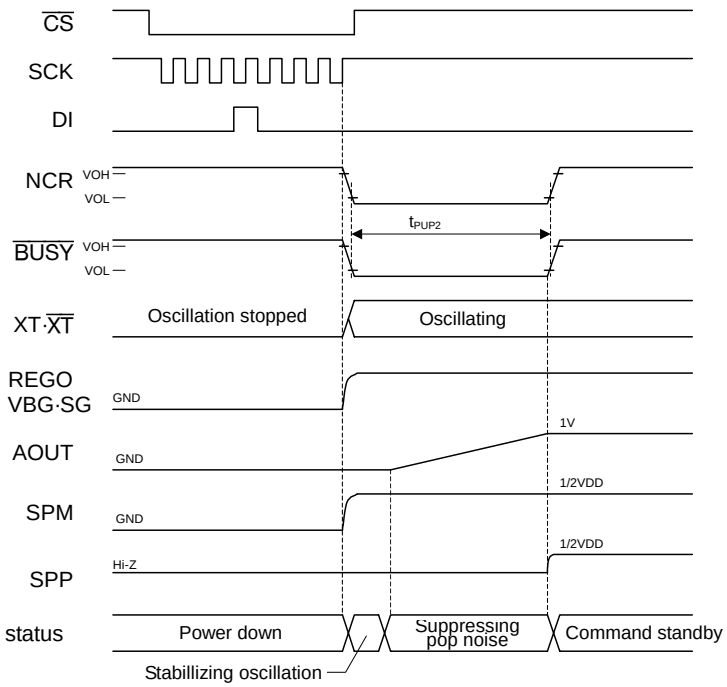
Power-Up Timing

- PUP1 command input



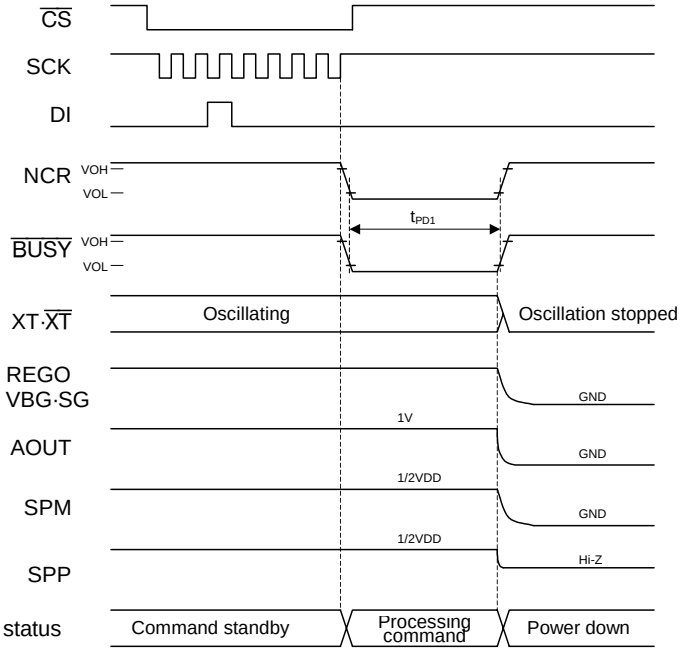
Downloaded from Elcodis.com electronic components distributor

• PUP2 command input



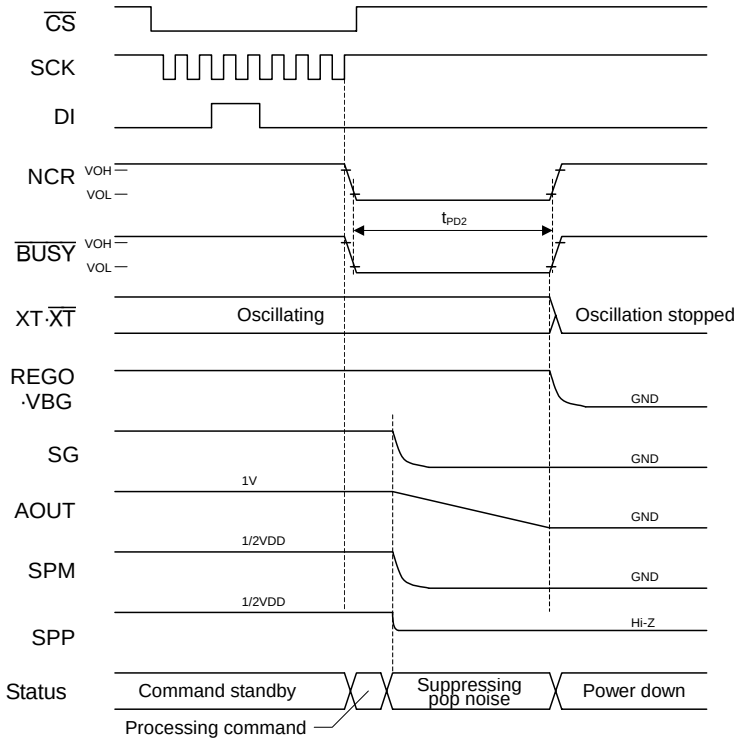
Power-Down Timing

• PDWN1 command input

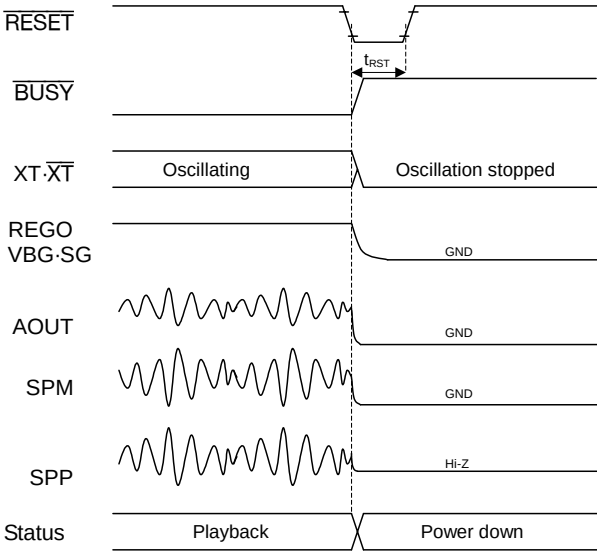


Downloaded from Elcodis.com electronic components distributor

• PDWN2 command input



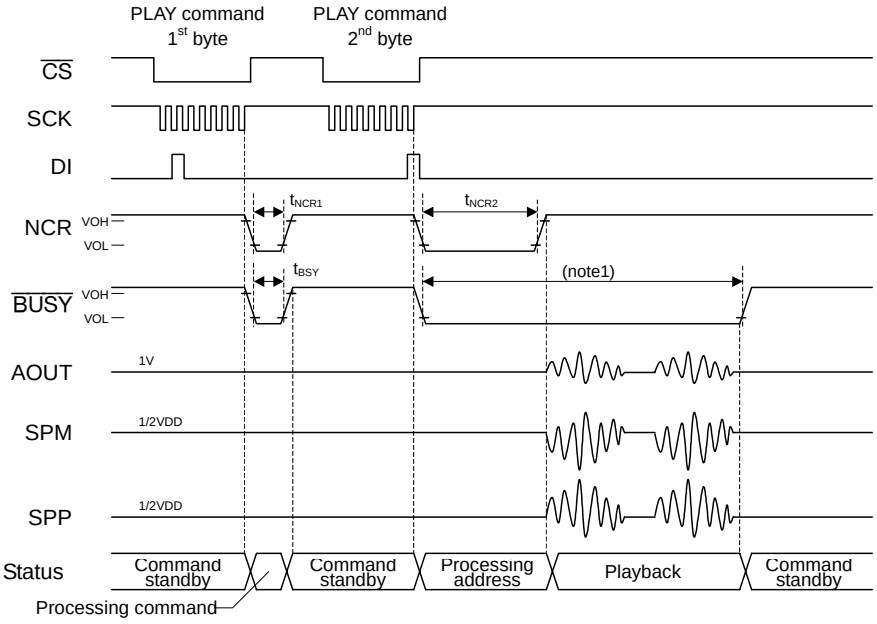
• $\overline{\text{RESET}}$ input



Note: The same timing even when $\overline{\text{RESET}}$ is input while waiting for command.

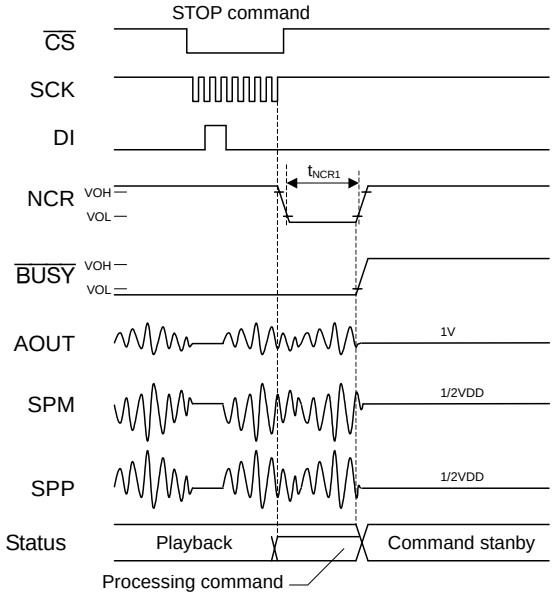
Downloaded from Elcodis.com electronic components distributor

Playback Timing by PLAY command



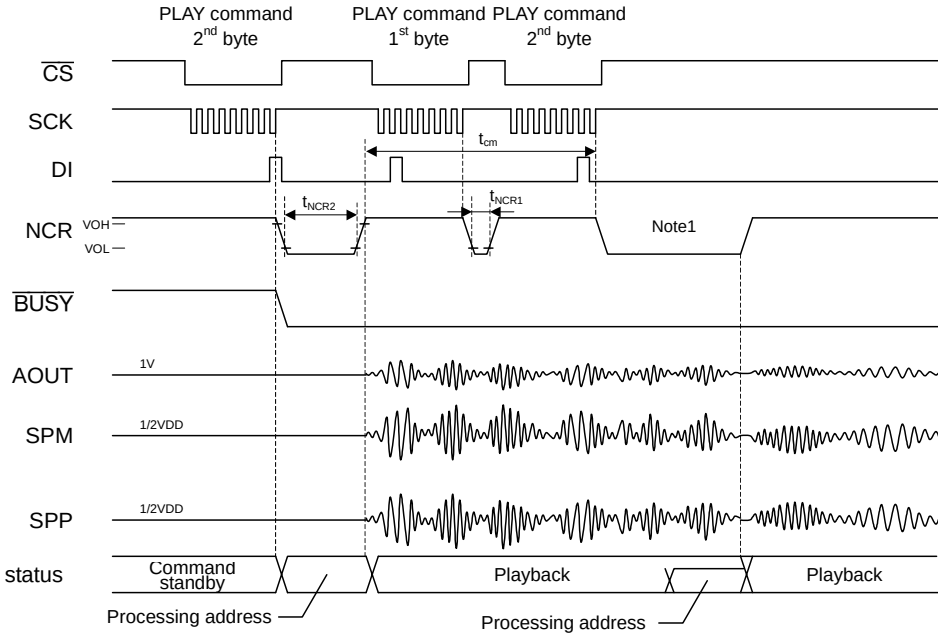
Note 1: Length of "L" interval of $\overline{BUSY1}$ is = t_{NCR2} + playback time length.

Playback Stop Timing



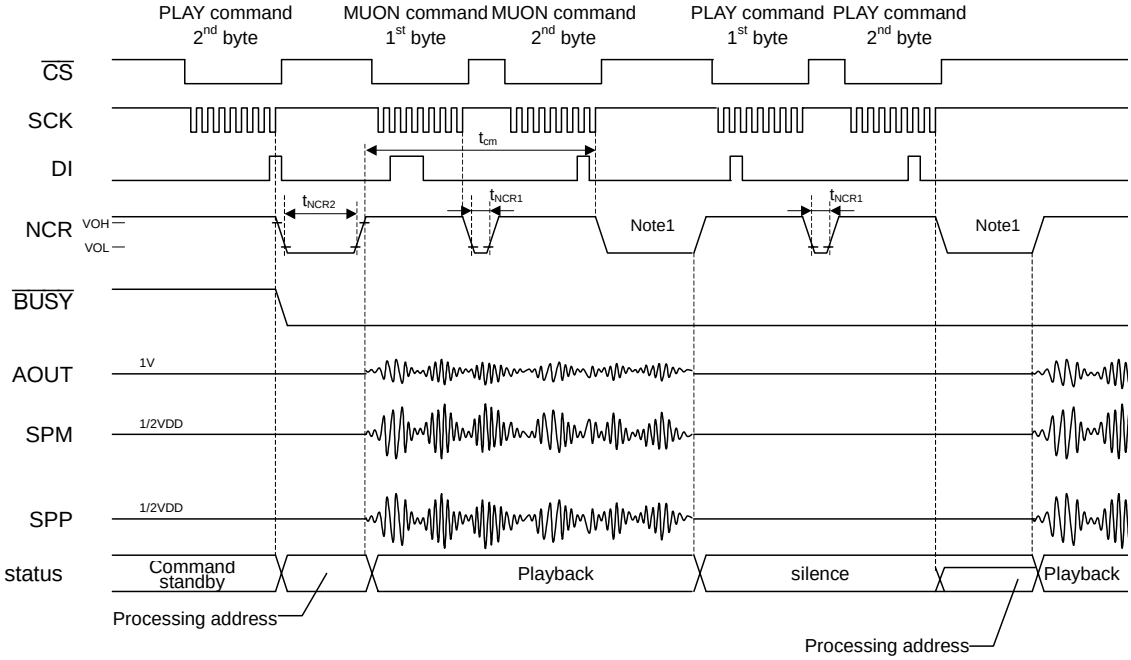
Downloaded from Elcodis.com electronic components distributor

Continuation Playback Timing by PLAY command



Note 1 "L" level time width of NCR pin changes with the timing which inputs PLAY command, while playback is going on.

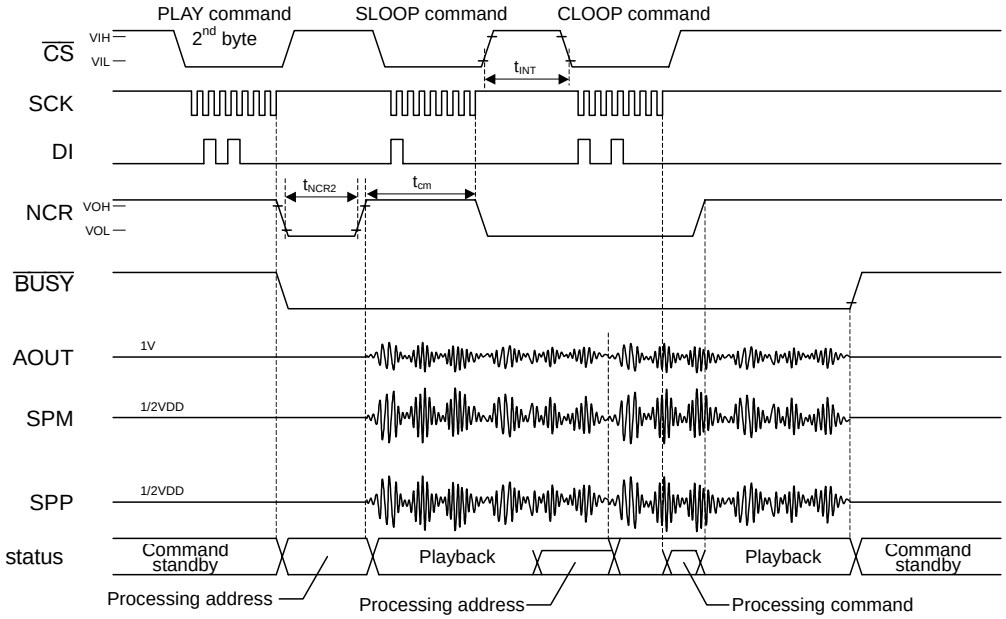
Silence Insertion Timing (MUON command is input during channel 1 playback)



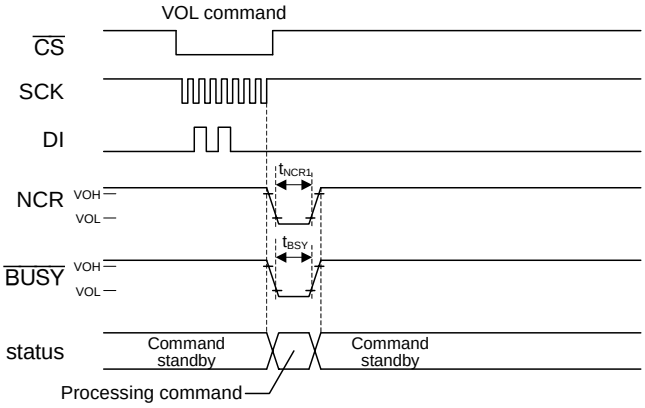
Note 1: "L" level time width of NCR pin changes with the timing which inputs MUON command, while silence is going on.

Downloaded from Elcodis.com electronic components distributor

LOOP Playback Set/Release Timing (LOOP playback setting/releasing of channel 1 playback)



VOL Command Input Timing



Downloaded from Elcodis.com electronic components distributor

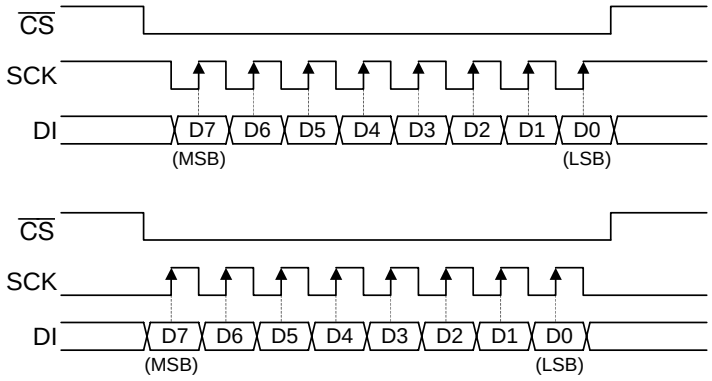
FUNCTIONAL DESCRIPTION

Serial Interface

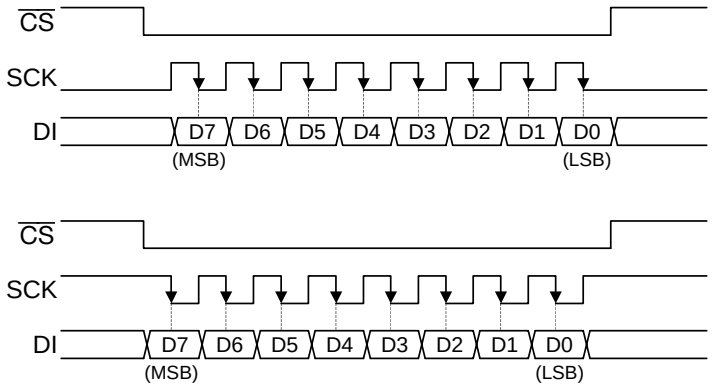
The serial interface inputs various commands and data by CS, SCK, and DI pin.
The micro-computer interface becomes effective when CS pin is set to “L” level.
To input the commands and data, “L” level is input to CS pins followed by, from MSB, to DI pin in synchronization with the input clock signal at SCK pin. Data at DI pin is captured inside the device on the rising or falling edge of the clock at SCK pin. And the command is executed on the rising or falling edge of eight clocks of a SCK pin.
The selection of rising/falling edge of SCK clock is determined by the DIPH pin. If the DIPH pin is at “L” level, the DI pin data is captured inside the device on the rising edge of SCK clock. Conversely, if DIPH pin is at “H” level, then the DI pin data is captured on the falling edge of SCK clock.
Even if it makes CS pin “L” level fixation, the input of command data is possible. However, when pulses other than specification are inputted into a SCK pin, LSI does not operate normally. The count of the number of clocks of a SCK pin returns to an initial state by making CS pin into “H” level.

Command and Data Input Timings

- SCK Rising Edge Operation (DIPH pin is at “L” level)



- SCK falling Edge Operation (DIPH pin is at “H” level)



Downloaded from Elcodis.com electronic components distributor

Commands List

Each command is 1-byte (8 bits) input. PLAY and MUON only are 2 bytes input.

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
PUP1	0	0	0	0	–	–	–	–	Instantly shifts the power down device to the command standby state.
PUP2	0	0	0	1	–	–	–	–	Suppresses pop noise and shifts the power down device to the command standby state.
PDWN1	0	0	1	0	–	–	–	–	Instantly shifts the device from the command standby state to the power down state.
PDWN2	0	0	1	1	–	–	–	–	Suppresses pop noise and shifts the device from the command standby state to power down state.
PLAY	0	1	0	0	–	–	–	–	Inputs the phrase, and then starts the playback.
	F7	F6	F5	F4	F3	F2	F1	F0	
STOP	0	1	1	0	–	–	–	–	ends the voice.
MUON	0	1	1	1	–	–	–	–	Inserts silence time and then inserts silence.
	M7	M6	M5	M4	M3	M2	M1	M0	
SLOOP	1	0	0	0	–	–	–	–	Repeats the playback mode setting command. Effective only for the channel being used for playback.
CLOOP	1	0	0	1	–	–	–	–	Repeat playback mode releasing command. Inputting the STOP command releases repeat playback mode automatically.
VOL	1	0	1	0	V3	V2	V1	V0	Sets the volume of playback.
SPKR	1	0	1	1	–	–	OP	PD	Power down control commands of speaker amplifier.

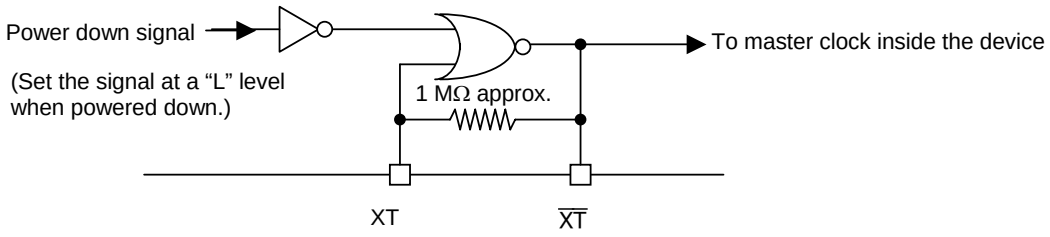
F7 to F0: Phrase address
M7 to M0:Silence time length
V3 to V0: Sound volume
PD power down control of speaker amplifier
OP pop noise control of speaker amplifier

Downloaded from Elcodis.com electronic components distributor

Power Down Function

In power down state, the power down function in the device stops the internal operation and oscillation, and minimizes the static Idd.
When an external clock is in use, input "L" level to the XT pin, so that current does not flow into the oscillation circuit.

Figure below shows the equivalent circuit of $\overline{XT}$ and XT pins.



Initial state at the time of reset input and power down state

Each output pin state is shown.

Digital output pin	state	Analog output pin	state
NCR	"H" level	REGO	DGND level
$\overline{BUSY}$	"H" level	VBG	AGND level
RAO	"L" level	SG	AGND level
		AOUT	AGND level
		SPM	SPGND level
		SPP	SPGND level

Voice Synthesis Algorithm

The ML2250 family contains 5 algorithm types to match the characteristic of playback voice: 4-bit ADPCM 2 algorithm, 8-bit PCM algorithm, 8-bit non-linear PCM algorithm, and 16-bit PCM algorithm.
Key feature of each algorithm is described in the table below.

Voice synthesis algorithm	Applied waveform	Feature
Oki 4-bit ADPCM2	Normal voice waveform	Oki's specific speech synthesis algorithm of improved waveform follow-up with improved 4-bit ADPCM.
Oki 8-bit Nonlinear PCM	High-frequency components inclusive sound effect etc.	Algorithm which plays back mid-range of waveform as 10-bit equivalent voice quality.
8-bit PCM	High-frequency components inclusive sound effect etc.	Normal 8-bit PCM algorithm
16-bit PCM	High-frequency components inclusive sound effect etc.	Normal 16-bit PCM algorithm

Downloaded from Elcodis.com electronic components distributor

Memory Allocation and Creating Voice Data

The ROM is partitioned into 4 data areas: voice (i.e., phrase) control area, test area, voice area, and phrase control table area.
The voice control area manages the ROM's voice data. It controls the start/end addresses of voice data, usage/not usage of the phrase control table function and so on. The voice control area stores voice control data for 256 phrases.
The test area stores the data for testing.
The voice area stores the actual waveform data.
The phrase control table area stores data for effective use of voice data. As for the details, please refer to the Phrase Control Table Function.
There is no phrase control table area if the phrase control table is not used.

The ROM data is created using a development tool.

ROM Addresses (ML2216)

0x00000 0x007FF	Voice control area (16 Kbit Fixed)
0x00800 0x00807	Test area
0x00808 max: 0xFFFFF	Voice area
max: 0xFFFFF	Phrase Control Table area Depends on creation of ROM data.

Playback Time and Memory Capacity

The playback time depends upon the memory capacity, sampling frequency, and playback method.
The equation showing the relationship is given below.

$$\text{Playback time [sec]} = \frac{1{,}024 \times (\text{Memory capacity} - 16)\ \text{(bit)}}{\text{Sampling frequency (kHz)} \times \text{Bit length}}$$

(Bit length is ADPCM, ADPCM 2 = 4 bits; PCM = 8 bits.)

Example: Let the sampling frequency be 16 kHz and 4-bit ADPCM algorithm. If one 8 Mbits ROM is used, then the playback time is obtained as follows:

$$\text{Playback time} = \frac{1{,}024 \times (8 \times 1{,}024 - 16)\ \text{(bit)}}{16\ \text{(kHz)} \times 4\ \text{(bit)}} \cong 131\ \text{(sec)}$$

The above equation gives the playback time when the phrase control table function is not used.

Downloaded from Elcodis.com electronic components distributor

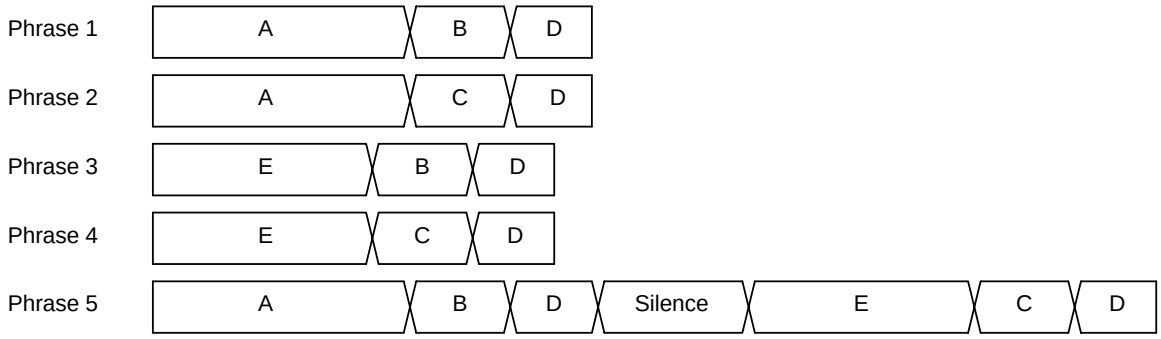
Phrase Control Table Function

The phrase control table function makes it possible to play back multiple phrases in succession. The following functions are set using the phrase control table function:

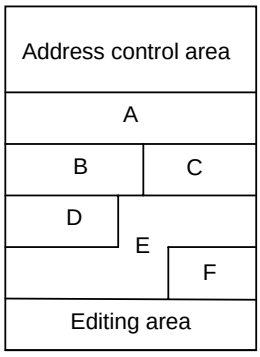
- Continuous playback: There is no limit to the number of times a continuous playback can be specified. It depends on the memory capacity only.
- Silence insertion function: 20 to 1024 ms

Using the phrase control table function enables to effectively use the memory capacity of voice ROM.
Below is an example of the ROM configuration in the case of using the phrase control table function.

Example 1: Phrases Using the Phrase Control Table Function



Example 2: Example of ROM Data in case Example 1 Converted to ROM



Downloaded from Elcodis.com electronic components distributor

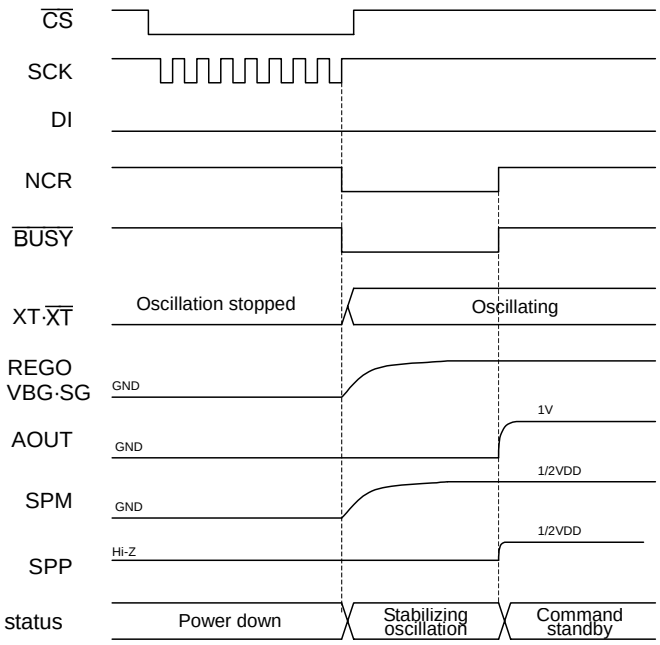
Command Function Descriptions

1. PUP1 Command

• command	0	0	0	0	–	–	–	–

PUP1 command is used to shift the ML2216 from power down state to the command standby state.
In the power down state, since the ML2216 can receive either PUP1 or PUP2 command only, the device will ignore any other input command.
The ML2216 enters into the power down state in any of the following 3 conditions:

1) When the power is inserted.
2) At $\overline{\text{RESET}}$ input
3) When NCR and $\overline{\text{BUSY}}$ go “H” level after inputting the power down command.



The oscillation starts operation after PUP1 command input and, after an elapse of about 2 ms oscillation stabilization time, the AOUT output abruptly changes from GND level to 1V level. Therefore, this abrupt change in AOUT output will cause to generate the pop noise if the AOUT output is not processed outside. To suppress the pop noise, input the PUP2 command.
Regulator and speaker amplifier output start operation after PUP1 command input. However, SPP pin changes from GND level to $1/2V_{DD}$ level after an elapse of about 2 ms oscillation stabilization time.
All commands that will be input during oscillation stabilization are ignored,
However, if $\overline{\text{RESET}}$ is input, ML2216 soon enters the power down state.

Downloaded from Elcodis.com electronic components distributor

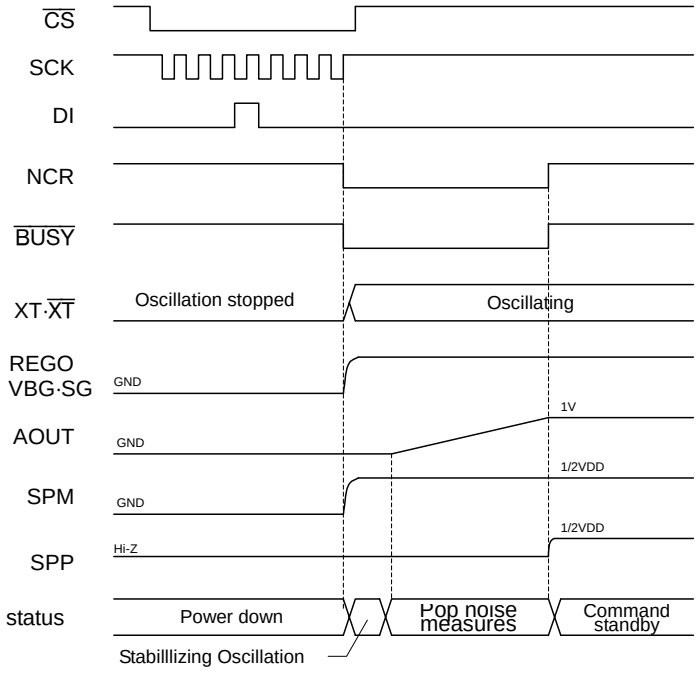
2. PUP2 Command

• command

0	0	0	1	–	–	–	–

PUP2 command is used to take measures for the pop noise from the power down state and to shift the ML2216 to the command standby state.
Since ML2216 receives either PUP1 or PUP2 command only in the power down state, it will ignore any other command input.
The ML2216 enters into the power down state in any of the following 3 conditions:

1) When the power is inserted.
2) At $\overline{\text{RESET}}$ input
3) When NCR and $\overline{\text{BUSY}}$ go "H" level after the power down command is input.



The oscillation starts operation after PUP2 command input and, after an elapse of about 2 ms oscillation stabilization time, the AOUT output gradually changes from GND level to 1V level in about 64 ms.
Regulator and speaker amplifier output start operation after PUP2 command input. However, SPP pin changes from GND level to $1/2V_{DD}$ level after reaching the level whose AOUT output is about 1V.
All commands that will be input during oscillation stabilization or while pop noise is being suppressed, are ignored. However, if $\overline{\text{RESET}}$ is input, the ML2216 soon enters the power down state.

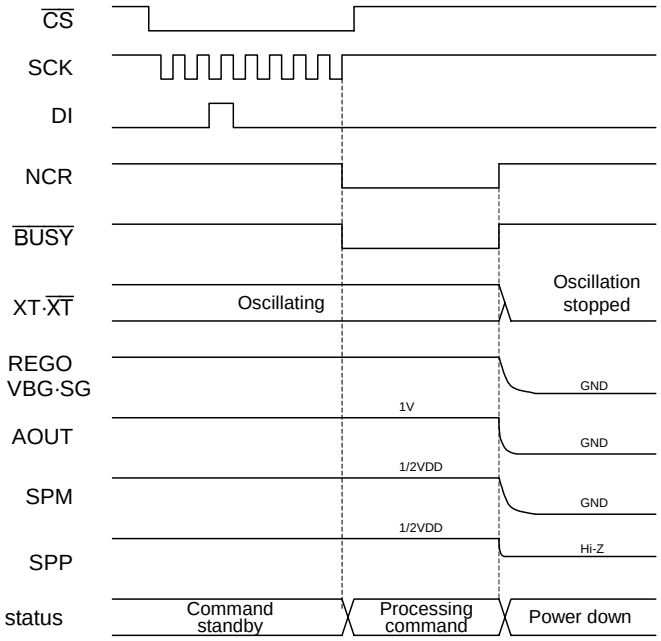
Downloaded from Elcodis.com electronic components distributor

3. PDWN1 Command

• command

0	0	1	0	–	–	–	–

The PDWN1 command is used to shift the ML2216 from command standby state (both NCR and $\overline{BUSY}$ are “H”) to the power down state.
To resume speech synthesis processing after the ML2216 has shifted to the power down state, first input the PUP1 or PUP2 command and then input the PLAY command.



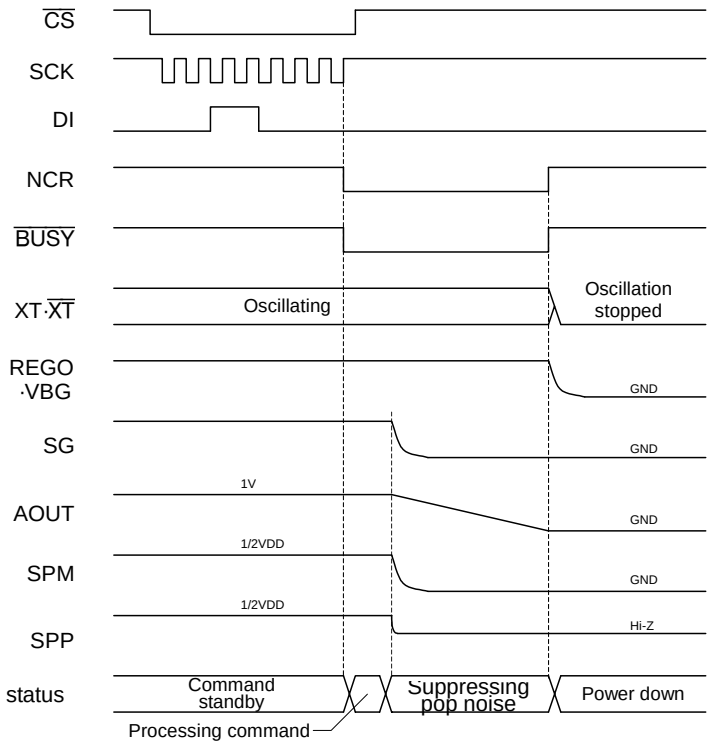
After PDWN1 command input and after an elapse of the PDWN1command processing time, the oscillation stops and the AOUT output abruptly changes from 1V level to GND level. This abrupt change in the AOUT output will cause to generate pop noise if the AOUT output is not processed outside. To suppress pop noise, input the PDWN2 command.
Regulator and speaker amplifier output stop operation After PDWN1 command input and after an elapse of the PDWN1command processing time. At this time, SPP output will be in a “Hi-Z” state in order to prevent a pop noise.

Downloaded from Elcodis.com electronic components distributor

4. PDWN2 Command

• command	0	0	1	1	–	–	–	–

PDWN2 command is used to take measures for the pop-noise from the command standby state (both NCR and $\overline{BUSY}$ are “H”) and to shift the ML2216 to the power down state.
To resume speech synthesis processing after the ML2216 has shifted to the power down state, first input the PUP1, or PUP2, command followed by the PLAY command.



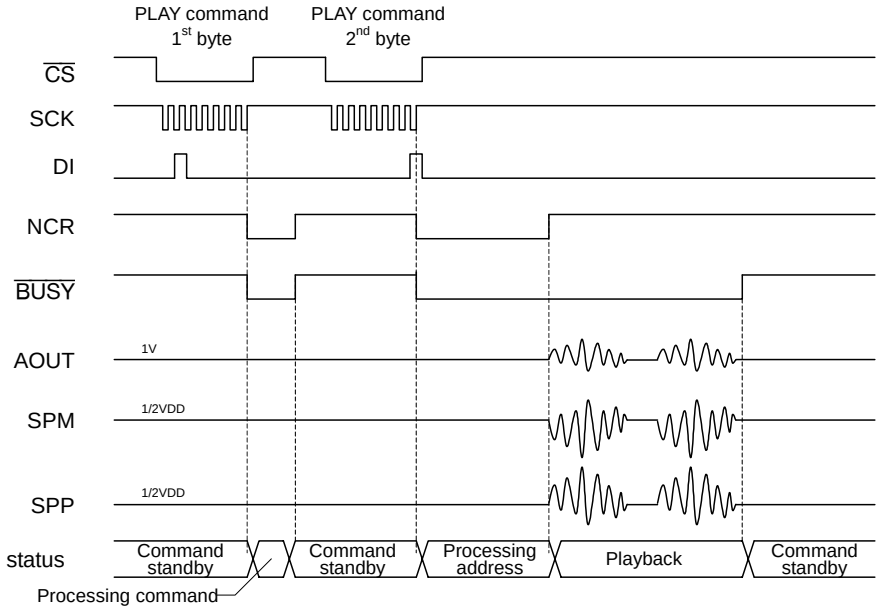
After PDWN2 command input and the elapse of PDWN2 command processing time, the AOUT output changes gradually in 64 ms from 1V level to GND level.
Speaker amplifier output stop operation After PDWN2 command input and after an elapse of the PDWN2command processing time. At this time, SPP output will be in a “Hi-Z” state in order to prevent a pop noise.
All commands that will be input while the pop noise is being suppressed, are ignored. However, if $\overline{RESET}$ is input, the ML2216 soon enters the power down state.

Downloaded from Elcodis.com electronic components distributor

5. PLAY Command

• command									
	0	1	0	0	–	–	–	–	1 byte
	F7	F6	F5	F4	F3	F2	F1	F0	2 bytes

PLAY command is a 2-byte command. The command first sets the playback command, and next sets the playback phrase. PLAY command should be input during the NCR signal of the playback is on the "H" level.
Since it is possible to specify the playback phrase (F7 to F0) at the time of creating the ROM that stores voice data, please set the phrase that was set when the ROM was created.
Figure below shows the timing of phrase (F7 to F0 = 01H) playback.



When the 1st byte of the PLAY command is input, the device enters a state in which it waits for the 2nd byte to input after the elapse of the command processing time. When the 2nd byte of PLAY command is input then, after an elapse of the command processing time, the device starts reading from the address information ROM of phrase for playback. Thereafter, the playback operation starts, the playback is performed up to the specified ROM address, and then the playback ends automatically.
NCR signal remains "L" level during the address control, and returns to "H" level when the address control is finished and the playback starts. When this NCR signal goes "H" level, then it is possible to input the PLAY command of the next playback phrase.
$\overline{\text{BUSY}}$ signal remains "L" level during the address control and while playback is going on, and returns to "H" level when the playback is finished. Whether the playback is going on can be known by the $\overline{\text{BUSY}}$ signal.

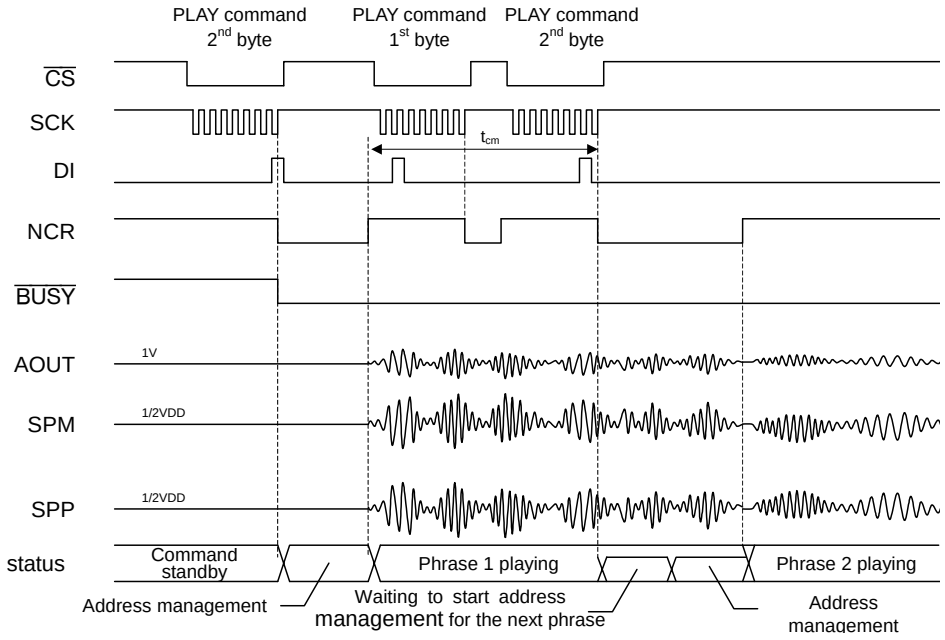
Address Management Time

The time required for managing the address of the playback phrase after the PLAY command is input depends on the lowest sampling frequency that was used to playback the previous phrase. It is the time of 16 or 17 cycle of a sampling frequency. After power is turned on or after $\overline{\text{RESET}}$ is input, a sampling frequency of 4 kHz is used.

Downloaded from Elcodis.com electronic components distributor

PLAY Command Input Timing for Continuous Play

The diagram below shows the input timing for the PLAY command when a phrase is played in continuation of the phrase that preceded it.



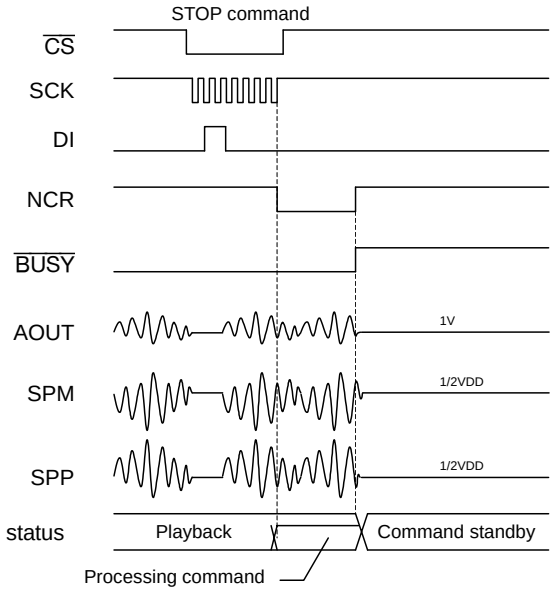
As shown in the above figure, When continuing playback, input the PLAY command of the following phrase within 10 ms (tcm) after NCR is set to “H” level. Then, silence is not inserted between phrases.

Downloaded from Elcodis.com electronic components distributor

6. STOP Command

• command	0	1	1	0	–	–	–	–

STOP command is used to stop playback. When the speech synthesis processing stops, the AOUT output of that channel becomes $1/4V_{DD}$ and the NCR and $\overline{BUSY}$ signals go "H".
Although it is possible to input the STOP command regardless of the status of playing back NCR, a prescribed command interval time is necessary.
Note that STOP command input during power down, shifting to power up, and shifting to power down will be ignored.



If the STOP command input is carried out, an AOUT output will change to the level of about 1 V. For this reason, a pop noise may be generated. Input the STOP command to prevent a pop noise after making volume small gradually using the VOL command.

Downloaded from Elcodis.com electronic components distributor

7. MUON Command

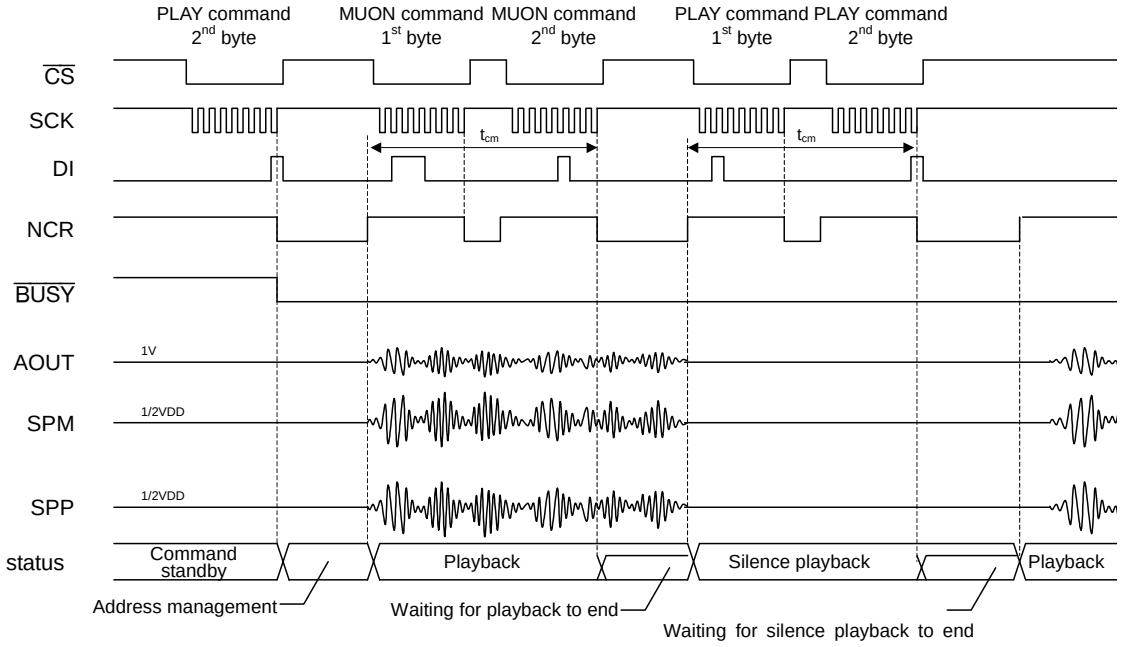
• command

0	1	1	1	–	–	–	–	1 byte
M7	M6	M5	M4	M3	M2	M1	M0	2 bytes

MUON command is a 2-byte command. This command is used to insert silence between the 2 playback phrases. The command first sets the MUON command, and next sets the silence time length. MUON command should be input during the NCR signal of the playback is on the "H" level.
The silence length (M7 to M0) can be set in 252 steps between 20 ms and 1024 ms in 4 ms intervals.
Following is the equation to set the silence time length:
However, please set silent length (M7 to M0) as 04h or more.

$$T_{mu} = (2^7 \times (M7) + 2^6 \times (M6) + 2^5 \times (M5) + 2^4 \times (M4) + 2^3 \times (M3) + 2^2 \times (M2) + 2^1 \times (M1) + 2^0 \times (M0) + 1) \times 4 \text{ ms}$$

The timing diagram shown below is a case of inserting a silence of 20 ms between the 2 phrases of address (F7 to F0 = 01H) and address (F7 to F0 = 01H).



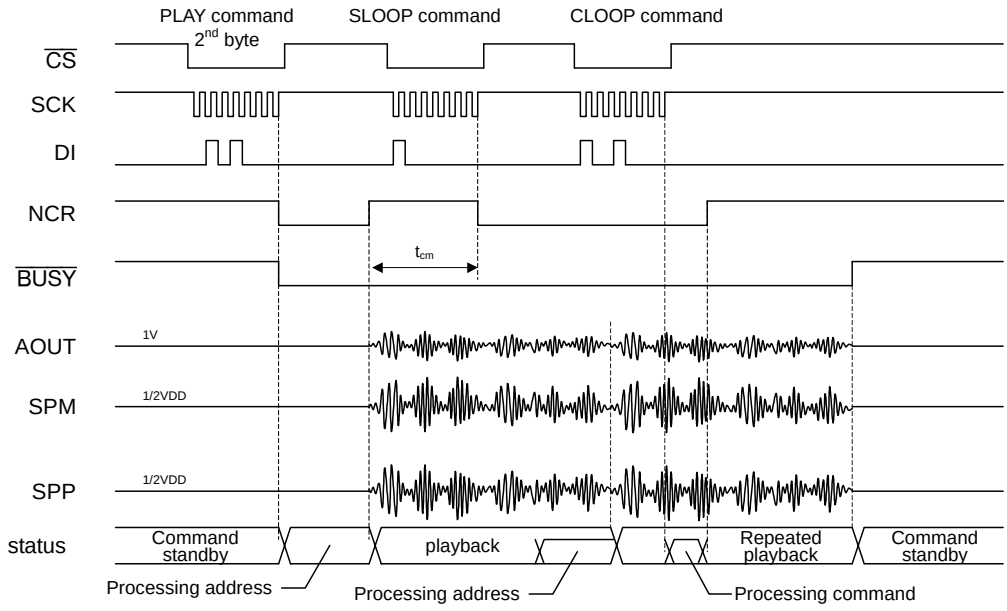
When the PLAY command is input, the address control of phrase 1 ends, the phrase playback starts, and the NCR signal goes "H" level. The MUON command is input after this NCR signal changes to the "H" level. After the MUON command input, the NCR signal remains at "L" level up to the end of phrase 1 playback, and the device enters into a state waiting for the phrase 1 playback to end.
When the phrase 1 playback finishes, the silence playback starts, and NCR signal goes "H" level. The PLAY command that specified the next playback phrase 1 is input after this NCR signal has changed to the "H" level. After the PLAY command input, the NCR signal once again returns to "L" level and the device enters the state waiting for phrase 1 address control and the end of silence playback.
When the silence playback finishes, the phrase 1 playback starts, the NCR signal goes "H" level, and the device enters a state in which it is possible to input the next PLAY or MUON command.
$\overline{\text{BUSY}}$ signal remains "L" level from input of the phrase 1 PLAY command up to the end of phrase 1 playback.

Downloaded from Elcodis.com electronic components distributor

8. SLOOP Command

• command	1	0	0	0	–	–	–	–

The SLOOP command is used to repeatedly playback. The CLOOP command is used to release the repeated playback setting.
Since the SLOOP command is valid only during the playback is going on, make sure to input the SLOOP command after the PLAY command input. And Input SLOOP command when NCRn = “H”. NCRn is “L” level while the LOOP playback is being set.
Once “the LOOP playback is being set., the voice is repeatedly played back until the repeated playback setting is released by CLOOP command, or stop playback by the STOP command. In the case of a phrase using the edit function, the edited phrase is repeatedly played back.
Since the repeated playback is released when the STOP command is input, input the SLOOP command once again if desired to repeat the playback.
Figure below shows the timing diagram to repeat the playback.



SLOOP Command Input Scope

Input the SLOOP command of the following phrase within 10 ms (tcm) after NCR is set to “H” level. If the SLOOP command is input in this interval, it is effective and repetitive play is performed.

Downloaded from Elcodis.com electronic components distributor

9. CLOOP Command

• command	1	0	0	1	–	–	–	–

The CLOOP command releases the repetitive playback.
When the repetitive playback mode is released, the NCR goes to the "H" level.
It is possible to input the CLOOP command regardless of the status of the NCR of that is playing back, but the prescribed command interval is required.

CLOOP Command Input Timing

Depending on the timing of the CLOOP command input during repetitive playback, the repetitive playback will end either at the end of the currently playing back phrase or after one more repetition of the phrase.

The difference is due to the same process that is required for repetitive playback and normal continuous playback. If the CLOOP command is input at a point in the phrase where the remaining voice data is less than the number of sampling periods required for address management, the address management of the next phrase to be played back (in this case, the same phrase) will have already begun. As the conclusion of address management automatically starts the next phrase playback, the CLOOP command will not take effect until that repetition is complete.

The input timing of the CLOOP command that is necessary to release repetitive playback without the final repetition is the same as the input timing for the PLAY command in which no silence is inserted between the phrases at the time of continuous playback, as shown in the table below.

Playback method	After PLAY command input
4 bit Oki ADPCM2	35th sample or before
8 bit nonlinear / 8 bit PCM	18th sample or before
16 bit PCM	18th sample or before

If the CLOOP command for the second phrase is input before the number of samples indicated in the table is reached, repetitive playback ends at the end of the currently playing back phrase.

Downloaded from Elcodis.com electronic components distributor

10. VOL Command

- command

1	0	1	0	V3	V2	V1	V0

VOL command is used to adjust the volume. It is possible to input the VOL command regardless of the status of the NCR of that is playing back, but the prescribed command interval is required.
Note that VOL command input during power down, shifting to power up, and shifting to power down will be ignored.
The volume can be set in 16 steps. The initial value after reset release is set to 0dB. The setting value of the VOL command is held at the time of power down and STOP command input.

Following are the volume settings (V3 to V0):

V3	V2	V1	V0	Volume
0	0	0	0	0 dB
0	0	0	1	–0.63 dB
0	0	1	0	–1.31 dB
0	0	1	1	–2.05 dB
0	1	0	0	–2.85 dB
0	1	0	1	–3.74 dB
0	1	1	0	–4.73 dB
0	1	1	1	–5.85 dB
1	0	0	0	–7.13 dB
1	0	0	1	–8.64 dB
1	0	1	0	–10.45 dB
1	0	1	1	–12.76 dB
1	1	0	0	–15.92 dB
1	1	0	1	–20.90 dB
1	1	1	0	–33.98 dB
1	1	1	1	OFF

Downloaded from Elcodis.com electronic components distributor

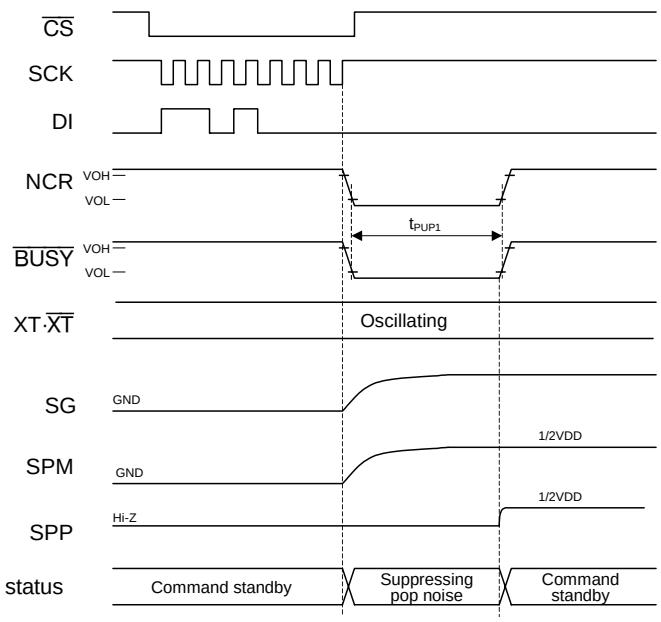
11. SPKR Command

• command	1	0	1	1	–	–	OP	PD

SPKR command is used to power down control of speaker amplifier.
When PD bit is the “L” level, speaker amplifier is in a power up state.
When OP bit is the “L” level, it will be in a power up state through the stable time for about 2ms.
When OP bit is the “H” level, it will be in a power up state through the stable time for about 66ms.
However, when the ML2216 is changed into a power down state with PDWN1 and PDWN2 command, speaker amplifier will also be in a power down state.
When PD bit is the “H” level, speaker amplifier is in a power down state. Speaker amplifier holds a power down state until it changes PD bit into the “L” level with the SPKR command again, even if it will be in a power up state with PUP1 and PUP2 command.
After reset release, PD bit and OP bit are set as the state of the “L” level.
Irrespective of OP bit, when PD bit is the “L” level, it will be in a power down state through command processing time.
The SPKR command can input only NCR=”H” and BUSY=” H”. Note that SPKR command input during power down, shifting to power up, and shifting to power down will be ignored.

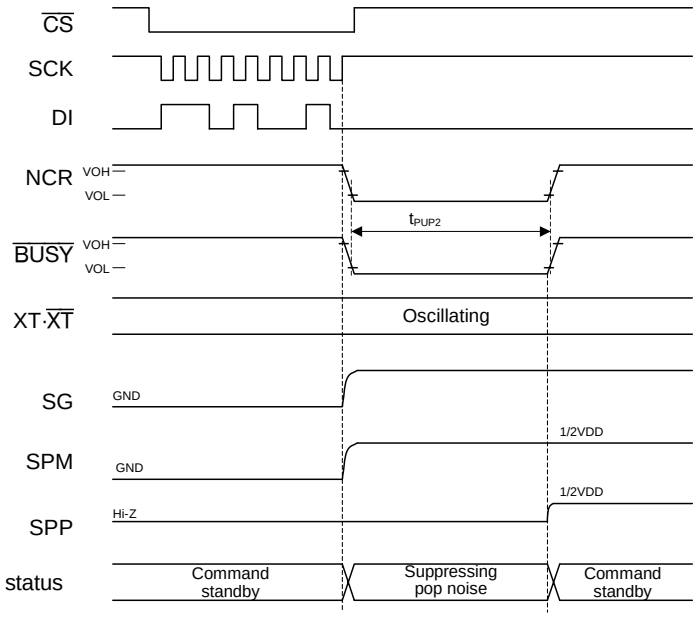
Speaker amplifier power up timing (at PD bit = “0”)

At OP bit = “0”



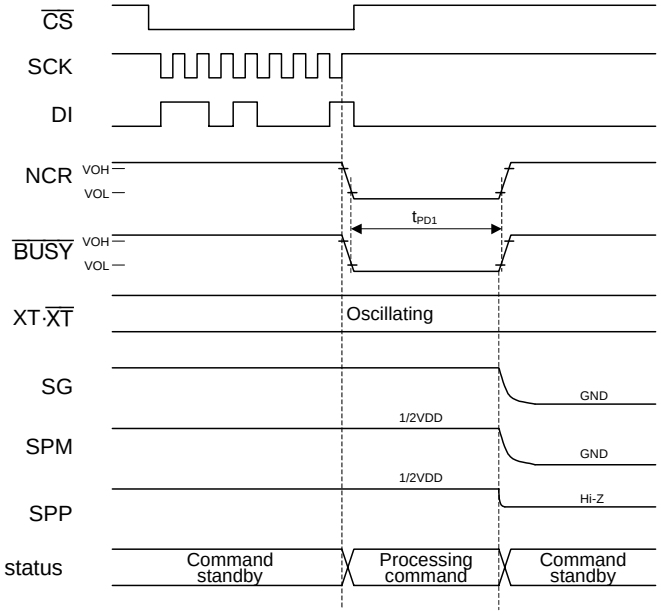
Downloaded from Elcodis.com electronic components distributor

At OP bit = “1”



Speaker amplifier power up timing (at PD bit = “1”)

At OP bit = “0” or OP bit = “1”



Downloaded from Elcodis.com electronic components distributor

• States of speaker amplifier

PD bit	PDWN1,2 command input	PUP1,2 command input	SPKR command
0	Power down	Power up	Power up
1	Power down	Power down	Power down

It is possible to input the SPKR command during command standby.

Disposal of VBG and SG pin

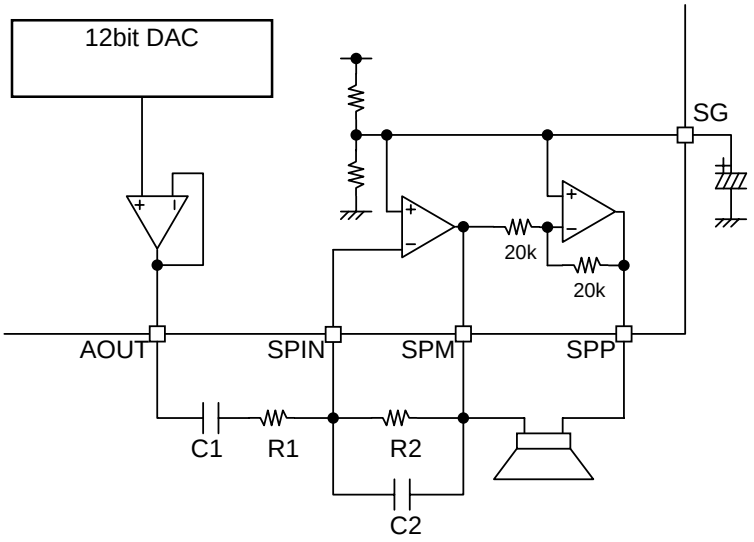
VBG pin is standard voltage of built-in regulator and D/A converter. SG pin is the signal ground of built-in speaker amplifier. Connect a capacitor between AGND pin so that a noise does not take these pins.
A capacity value recommends the following value. However, determine a capacity value after checking with the system.
In addition, after each output voltage is stabilized, start playback operation.

Pin	Recommendation capacity value	Note
VBG	0.1μF ± 10%	The stable time of regulator output REGO pin voltage and AOUT pin output voltage becomes long, so that connection capacity becomes large.
SG	4.7μF ± 20%	The stable time of the speaker amplifier output SPM and SPP pin voltage becomes long, so that connection capacity becomes large.

Downloaded from Elcodis.com electronic components distributor

The external circuit composition method of speaker amplifier

As shown in the following figure, external resistance and a speaker are connected.



The speaker amplifier voltage gain from output pins SPM and SPP is given by the following equation.

$$AV1 = \frac{R2}{R1} \times 2 \quad [\text{Times}]$$

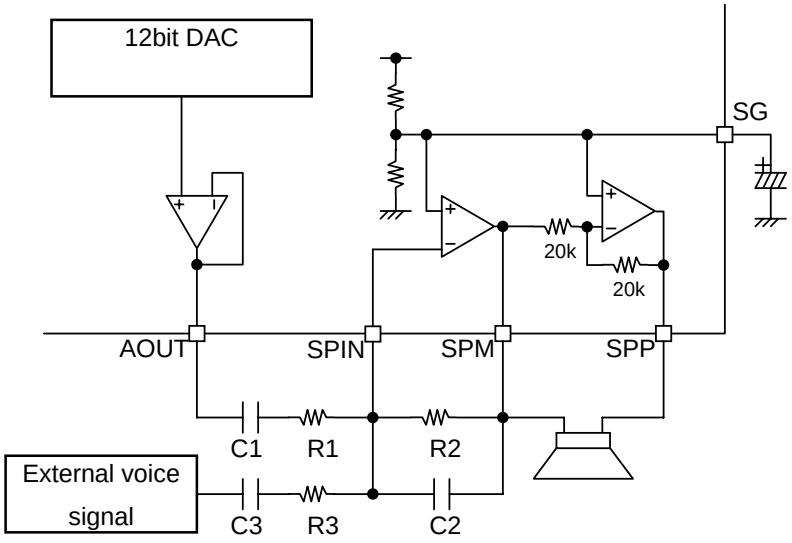
The cutoff frequency fc1 at the lower frequency is given by the following equation.

$$fc1 = \frac{1}{2 \times \pi \times C1 \times R1} \quad [\text{Hz}]$$

The cutoff frequency fc2 at the higher frequency is given by the following equation.

$$fc2 = \frac{1}{2 \times \pi \times C2 \times R2} \quad [\text{Hz}]$$

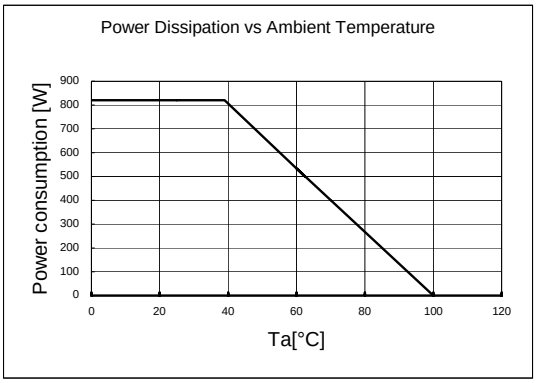
When mixing with an external voice signal, an external circuit is provided as shown in the following figure.

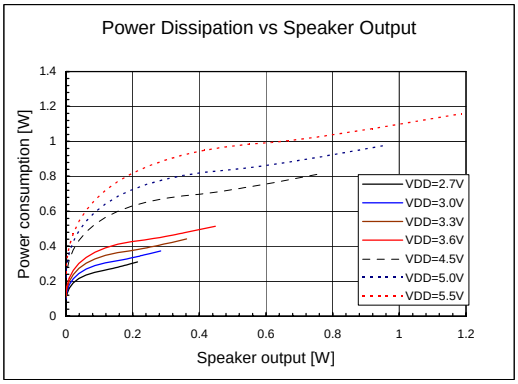


Downloaded from Elcodis.com electronic components distributor

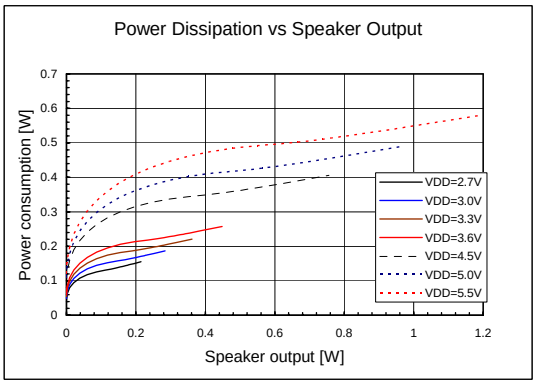
Recommended Power Dissipation

Recommended power dissipation is shown below.





When the operating DUTY is 100%, power dissipation = power consumption.
When the operating DUTY is 50%, refer to the graph below.



An example for usage :
When setting the speaker output at 0.6 W and the operating DUTY at 50%, use the ML2216 device at ambient temperatures of 62.5°C or less.

Downloaded from Elcodis.com electronic components distributor

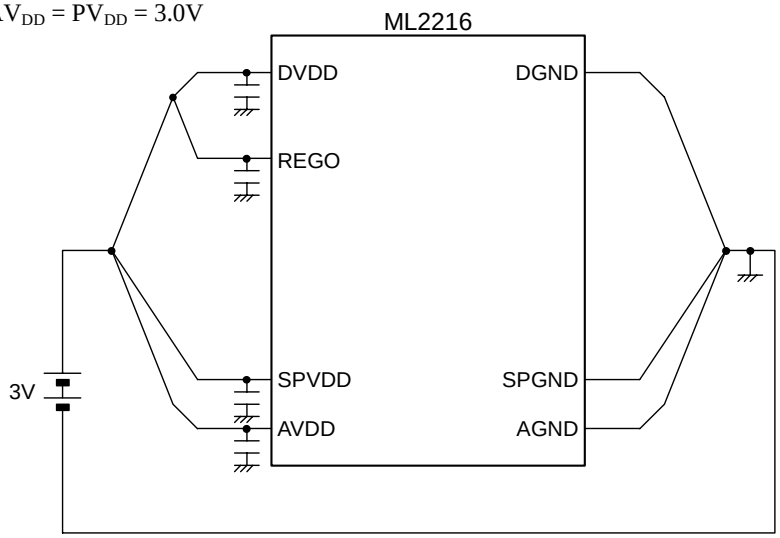
Arrangement of a power supply

The power supply of ML2216 is divided into the following three power supplies.

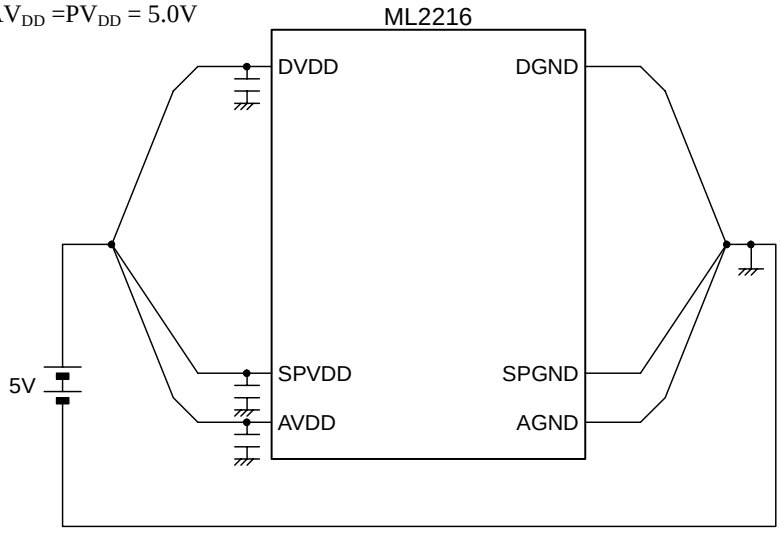
Digital power supply (DVDD)
Analog power supply (AVDD)
speaker amplifier supply (SPVDD)

To be shown in the following figure, supply DV_{DD}, SPV_{DD}, and AV_{DD} from the same power supply, and they are on wiring and divide them into an analog system power supply and a digital system.

At $DV_{DD} = AV_{DD} = PV_{DD} = 3.0V$



At $DV_{DD} = AV_{DD} = PV_{DD} = 5.0V$



Downloaded from Elcodis.com electronic components distributor

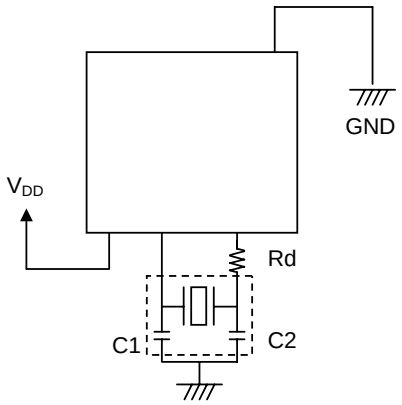
RECOMMENDED CERAMIC OSCILLATORS

Recommended ceramic oscillators and their manufacturers are listed and their connection circuits are shown below.

KYOCERA Corporation

Frequency [Hz]	Product	Operating conditions					
		C1 [pF]	C2 [pF]	Rf [Ohm]	Rd [Ohm]	Power supply voltage [V]	Temperature range [°C]
4.000M	PBRC4.00MR50X000	15 (Internal capacitance)		---	1.5k	2.7 to 3.6 4.5 to 5.5	–20 to +85
4.096M	PBRC4.096MR50X000						

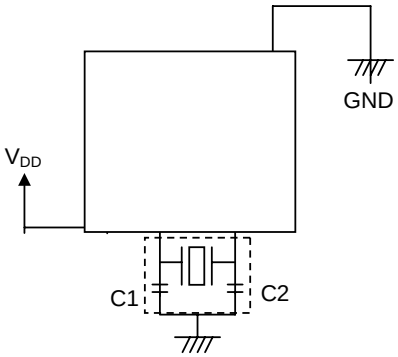
Connection circuit:



TDK Corporation

Frequency [Hz]	Product	Operating conditions					
		C1 [pF]	C2 [pF]	Rf [Ohm]	Rd [Ohm]	Power supply voltage [V]	Temperature range [°C]
4.000M	FCR4.0MXC5	30 (Internal capacitance)		---	---	2.7 to 3.6	–20 to +85
	FCR4.0MXC5					4.5 to 5.5	
4.096M	FCR4.09MXC5	30 (Internal capacitance)		---	---	2.7 to 3.6	–20 to +85
	FCR4.09MXC5					4.5 to 5.5	

Connection circuit:

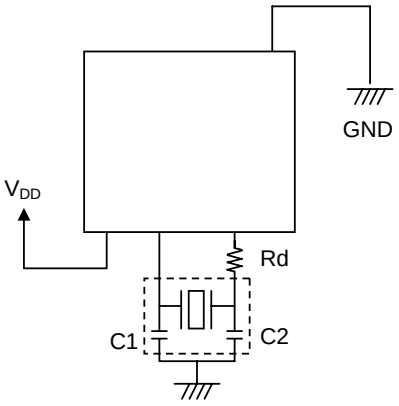


Downloaded from Elcodis.com electronic components distributor

Murata Manufacturing Co., Ltd.

Frequency [Hz]	Type	Product	Operating conditions					
			C1 [pF]	C2 [pF]	Rf [Ohm]	Rd [Ohm]	Power supply voltage [V]	Temperature range [°C]
4.000M	SMD	CSTCR4M00G55-R0	39 (Internal capacitance)		---	1.0k	2.7 to 5.5	–20 to +85
	Lead	CSTLS4M00G56-B0	47 (Internal capacitance)					
	SMD	CSTCR4M00G55-R0	39 (Internal capacitance)					
	Lead	CSTLS4M00G56-B0	47 (Internal capacitance)					
4.096M	SMD	CSTCR4M09G55-R0	39 (Internal capacitance)		---	1.0k	2.7 to 5.5	
	Lead	CSTLS4M09G56-B0	47 (Internal capacitance)					
	SMD	CSTCR4M09G55-R0	39 (Internal capacitance)					
	Lead	CSTLS 4M09G56-B0	47 (Internal capacitance)					

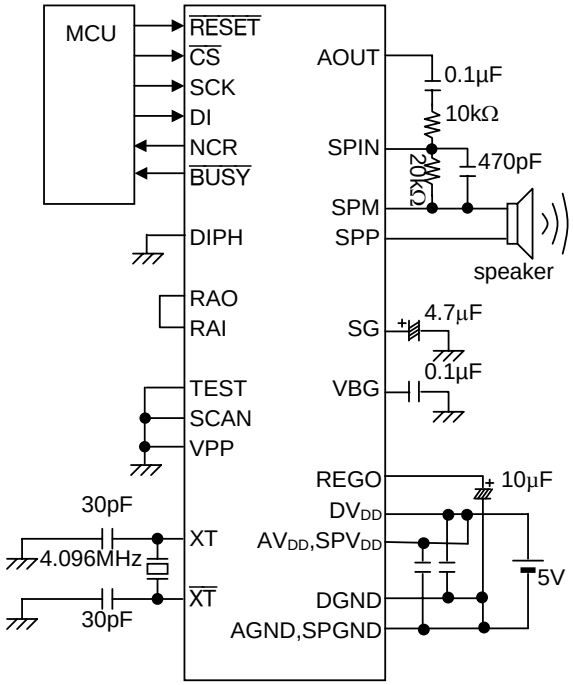
Connection circuit:



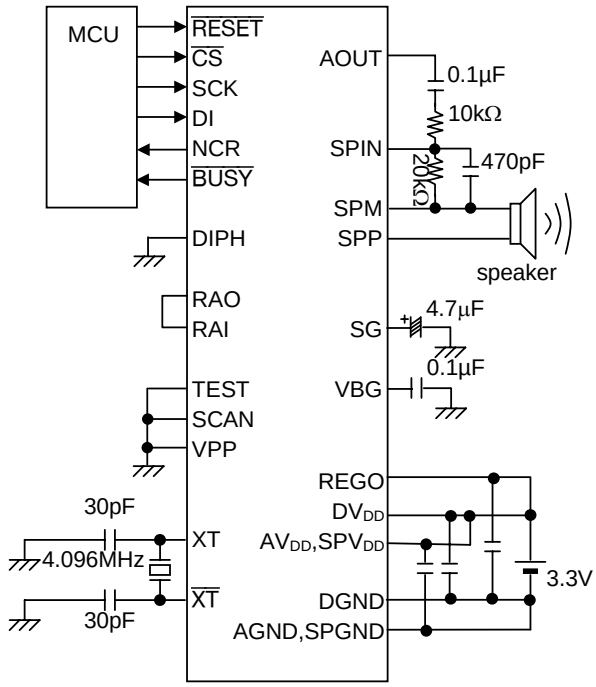
Downloaded from Elcodis.com electronic components distributor

APPLICATION CIRCUIT EXAMPLE (ML2216)

At $DV_{DD} = AV_{DD} = SPV_{DD} = 5.0V$



At $DV_{DD} = AV_{DD} = SPV_{DD} = 3.0V$

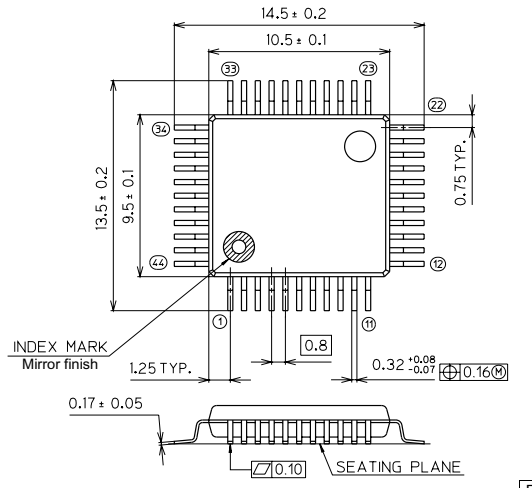


Downloaded from Elcodis.com electronic components distributor

PACKAGE DIMENSIONS

(Unit: mm)

QFP44-P-910-0.80-2K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.41 TYP.
Rev. No./Last Revised	4/Nov. 28, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Downloaded from Elcodis.com electronic components distributor

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL2216FULL-01	Jun. 14, 2006	–	–	Final edition 1
FEDL2216FULL-02	Oct. 23, 2006	5, 39, 45	5, 39, 45	Changed the VBG pin capacitance from 150 pF to 0.1 μF.
		22	22	Changed “0” in the Commands List to “—”.
		23	23	Added "(Set the signal at a "L" level when powered down)" in the figure in the "Power Down Function" Section.
		26 to 30, 32 to 35, and 37	26 to 30, 32 to 35, and 37	Modified the command configuration.
		42	42	• Replaced the two figures. • Changed SPV_{DD} to PV_{DD}.
		–	43 and 44	Added "RECOMMENDED CERAMIC OSCILLATORS" Section.
		45	45	• Changed the resistance across SPIN pin and 0.1 μF capacitor from 20 kΩ to 10 kΩ in the two figures. • Changed the capacitance across SPIN pin and the speaker from 100 pF to 470 pF in the two figures. • Changed the capacitance across VBG pin and ground from 150 pF to 0.1 pF in the two figures.
FEDL2216FULL-03	Sep. 20, 2007	–	–	• Add ML22P16 information

Downloaded from Elcodis.com electronic components distributor

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

5. Neither indemnity against nor license of a third party's industrial and intellectual property right, etc. is granted by us in connection with the use of the product and/or the information and drawings contained herein. No responsibility is assumed by us for any infringement of a third party's right which may result from the use thereof.

6. The products listed in this document are intended for use in general electronics equipment for commercial applications (e.g., office automation, communication equipment, measurement equipment, consumer electronics, etc.). These products are not authorized for use in any system or application that requires special or enhanced quality and reliability characteristics nor in any system or application where the failure of such system or application may result in the loss or damage of property, or death or injury to humans.
   Such applications include, but are not limited to, traffic and automotive equipment, safety devices, aerospace equipment, nuclear power control, medical equipment, and life-support systems.

7. Certain products in this document may need government approval before they can be exported to particular countries. The purchaser assumes the responsibility of determining the legality of export of these products and will take appropriate and necessary steps at their own expense for these.

8. No part of the contents contained herein may be reprinted or reproduced without our prior permission.

Copyright 2007 Oki Electric Industry Co., Ltd.

Downloaded from Elcodis.com electronic components distributor