ML22808/ML22804/ML22802-XXX
ML22P808/ML22P804/ML22P802

OKI ADPCM Algorithm-Based Speech Synthesis LSI

This document contains minimum specifications. For full specifications, please contact your nearest OKI office or representative.

GENERAL DESCRIPTION

The ML22808/ML22804/ML22802-xxx are speech synthesis LSI devices that have P2ROM for storing voice data. The voice output component has an ADPCM2 decoder to enable high speech quality, a D/A converter, and a low-pass filter.
It is easy to configure a speech synthesizer by connecting a power amplifier and a CPU externally.
The ML22808/ML22804/ML22802-xxx allow selection of a playback method from among the 8-bit PCM, non-linear 8-bit PCM, 16-bit PCM, and 4-bit ADPCM2 algorithms and enable volume control.
The ML22808/ML22804/ML22802-xxx, supported by the ROM codes, are the products in which written speech data is included.
The ML22P808/ML22P804/ML22P802 are OTP products in which speech data can be easily written by the user using a dedicated writer. These devices are suitable for applications in developing products, manufacturing of a wide variety of products in small quantities, and requiring quick turn around.

- Capacity of the internal memory device and the maximum vocal reproduction time (when 4-bit OKI ADPCM2 algorithm used)

Product name	ROM capacity	Maximum vocal reproduction time (sec)		
		F_{SAM} = 4.0 kHz	F_{SAM} = 8.0 kHz	F_{SAM} = 16 kHz
ML22808-XXX/ML22P808	8 Mbits	524	262	131
ML22804-XXX/ML22P804	4 Mbits	262	131	65
ML22802-XXX/ML22P802	2 Mbits	131	65	32

- Speech synthesis method: An algorithm can be specified for each phrase from among the following:
  4-bit OKI ADPCM2
  8-bit Nonlinear PCM
  8-bit PCM/16-bit PCM
- Sampling frequency: An fsam value can be specified fro each phrase.
  4.0/8.0/16.0 kHz, 5.3/10.7 kHz, 6.4/12.8 kHz
- Built-in low-pass filter and 12-bit D/A converter
- CPU command interface: 3-wired serial / clock synchronous
- Maximum number of phrases: 256 phrases, from 00h to FFh (per bank)
- Memory bank switching: Enabled between bank 1 and bank 4 using the SEL0 and SEL1 pins
- Memory bank selecting: Selectable between bank 1 and bank 4 by setting the SEL0 and SEL1 pins (Other than ML22802/ML22P802)

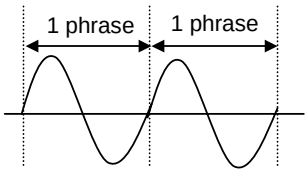
Selectable between bank1 and bank 2 (ML22802/ML22P802)

- Volume control: Can be adjusted in 16 levels or set to OFF
- Repeat function: LOOP command
- Source oscillation frequency: 4.096 MHz
- Power supply voltage: 2.7 to 3.6 V
- Operating temperature range: 20 to +85°C
- Package: 30-pin plastic SSOP (SSOP30-P-56-0.65-K)
- Product name: ML22P808MB, ML22P804MB, ML22P802MB
  ML22808-xxxMB, ML22804-xxxMB, ML22802-xxxMB
  (xxx indicates a ROM code number)

The table below summarizes the differences between the ML2216 and the ML2280X

Item	ML2216	ML2280X
CPU interface	Serial	Serial
Playback method	4-bit ADPCM2 8-bit straight PCM 8-bit non-linear PCM 16-bit straight PCM	4-bit ADPCM2 8-bit straight PCM 8-bit non-linear PCM 16-bit straight PCM
Maximum number of phrases	256	256 up to 1024 (per bank)
Sampling frequency (kHz)	4.0/5.3/6.4/ 8.0/10.7/12.8 16.0	4.0/5.3/6.4/ 8.0/10.7/12.8 16.0
Clock frequency	4.096 MHz (has a crystal oscillator circuit built-in)	4.096 MHz (has a crystal oscillator circuit built-in)
D/A converter	Current-type 12-bit	Current-type 12-bit
Low-pass filter	3D comb filter	3D comb filter
Speaker driving amplifier	Built-in type; 0.3W (at 8Ω, VDD=5V)	No
Edit ROM	Yes	Yes
Volume control	16 levels	16 levels
Silence insertion	Yes 20 to 1024 ms (4 ms steps)	Yes 20 to 1024 ms (4 ms steps)
Repeat function	Yes	Yes
Interval at which a seam is silent during continuous playback (*1)	No	No
Memory bank switching	No	Yes
Package	44-pin QFP	30-pin SSOP

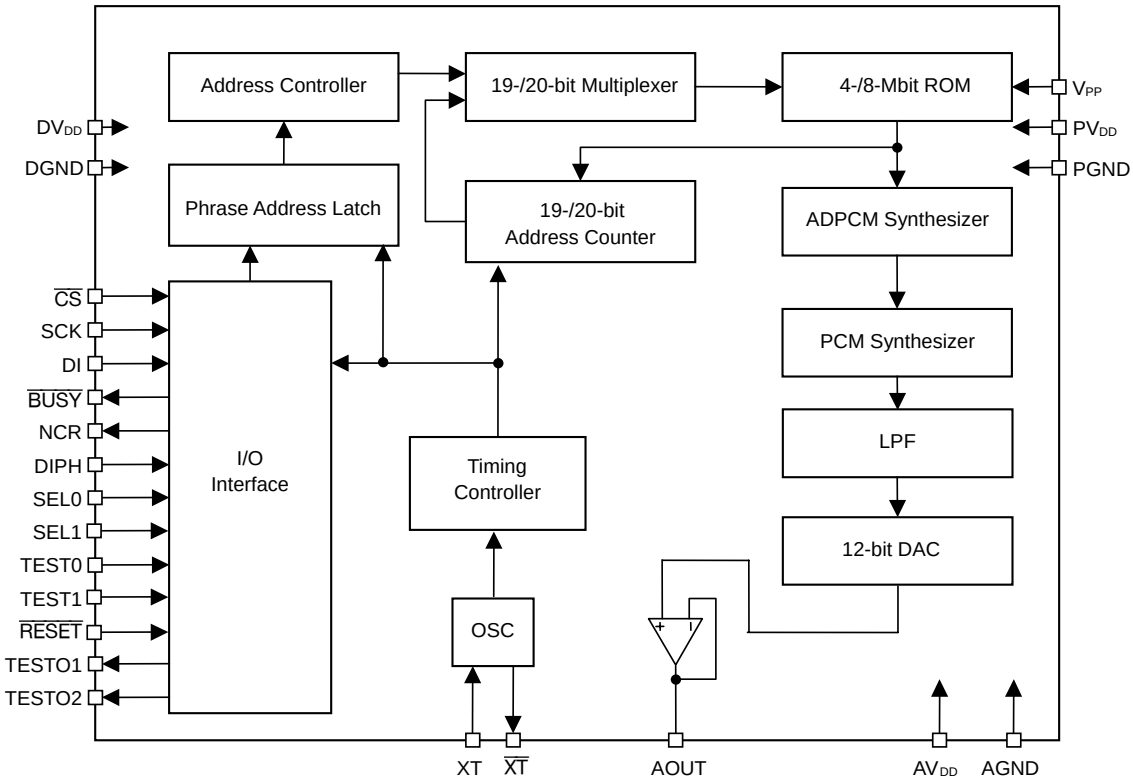
*1: Continuous playback as shown below is possible.



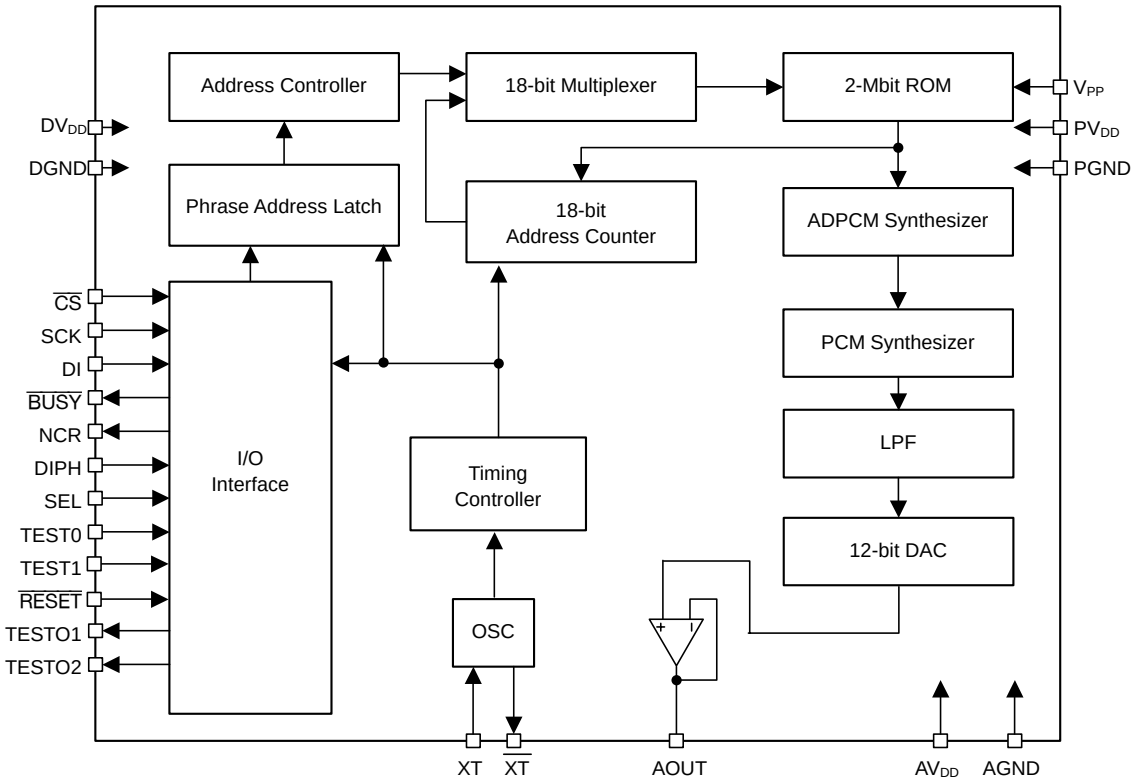
No silence interval

BLOCK DIAGRAM

ML22808/ML22804/ML22P808/ML22P804:

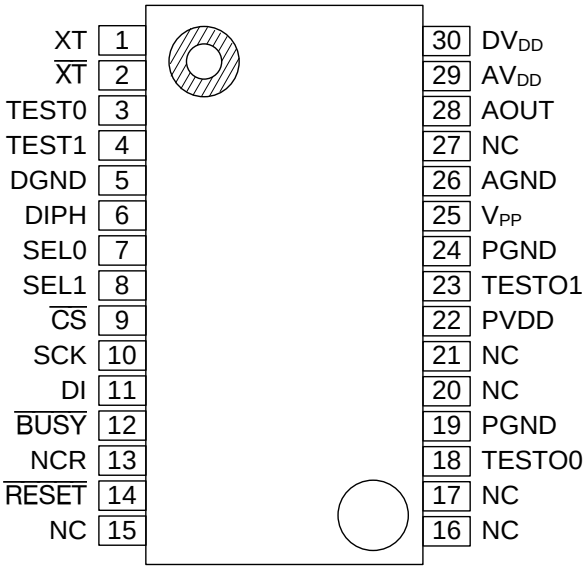


ML22802/ML22P802:



PIN CONFIGURATION (TOP VIEW)

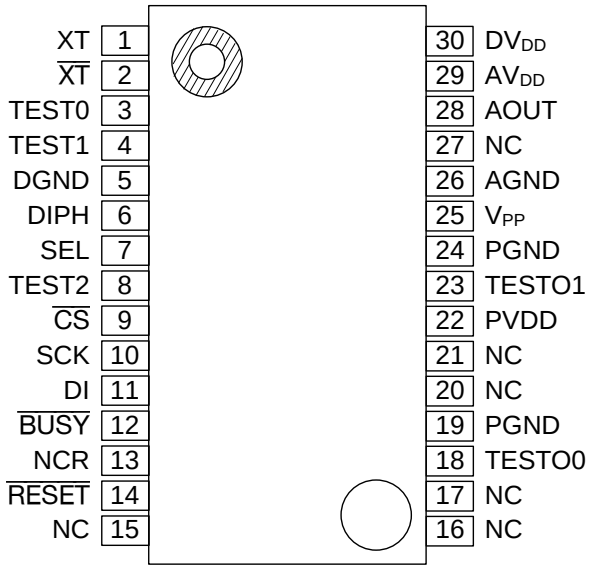
ML22808/ML22804/ML22P808/ML22P804:



NC: No Connection

30-Pin Plastic SSOP

ML22802/ML22P802:



NC: No Connection

30-Pin Plastic SSOP

PIN DESCRIPTION

Pin	Symbol	Type	Description
1	XT	I	Connects to a crystal or a ceramic resonator. A feedback resistor of around 1 MΩ is built in between this XT pin and $\overline{XT}$ pin. When using an external clock, input the clock from this pin. If a crystal or a ceramic resonator is used, connect it as close to the LSI as possible.
2	$\overline{XT}$	O	Connects to a crystal or a ceramic resonator. When using an external clock, leave this pin open. If a crystal or a ceramic resonator is used, connect it as close to the LSI as possible
3	TEST0	I	Input pin for testing. Tie this pin at a “L” level (DGND level).
4	TEST1	I	Input pin for testing. Tie this pin at a “L” level (DGND level).
5	DGND	—	Digital ground pin.
6	DIPH	I	Pin for choosing between rising edges and falling edges as to the edges of the SCK pulses used for shifting serial data input to the DI pin into the inside of the LSI. When this pin is at a “L” level, DI input data is shifted into the LSI on the rising edges of the SCK clock pulses; when this pin is at a “H” level, DI input data is shifted into the LSI on the falling edges of the SCK clock pulses.
7 (SEL)	SEL0	I	Memory bank selecting pin. Enabled when memory bank selecting is specified at the time the PUP1 or PUP2 command is input. Do not change during speech playback (when the $\overline{BUSY}$ pin is at “L”)
8 (TEST2)	SEL1	I	ML22808/ML22804/ML22P808/ML22P804: Memory bank selecting pin. Enabled when memory bank selecting is specified at the time the PUP1 or PUP2 command is input. Do not change during speech playback (when the $\overline{BUSY}$ pin is at “L”) ML22802/ML22P802: Input pin for testing. Tie this pin at “L” (DGND level).
9	$\overline{CS}$	I	Chip select input pin. A “L” level on this pin enables the serial interface.
10	SCK	I	Serial clock input pin.
11	DI	I	Serial data input pin.
12	$\overline{BUSY}$	O	Pin that outputs a signal that indicates the phrase playback status. If the LSI is playing a phrase, this pin outputs a “L” level. If the LSI is in a standby state, this pin outputs a “H” level.
13	NCR	O	Pin that outputs a signal that indicates whether command input is enabled or disabled. If command input is enabled, this pin outputs a “H” level. If command input is disabled, this pin outputs a “L” level.
14	$\overline{RESET}$	I	During a reset input, the entire circuit is stopped and enters a power down state. Upon power-on, input a “L” level to this pin. Put this pin into a “H” level after the power supply voltage is stabilized.
18	TESTO0	O	Output pin for testing. Leave this pin open.
19,24	PGND	—	Ground pin for the internal P2ROM.
22	PV_{DD}	—	Power supply pin for the internal P2ROM. Connect a capacitor of 0.1 μF or more between this pin and PGND.
23	TESTO1	O	Output pin for testing. Leave this pin open.

Pin	Symbol	Type	Description
25	V_{PP}	I	VPP power supply pin used for writing data to the internal P2ROM. Tie this pin at the DGND level.
26	AGND	—	Analog ground pin.
28	AOUT	O	Playback signal output pin.
29	AV_{DD}	—	Analog power supply pin. Connect a capacitor of 0.1 μF or more between this pin and PGND.
30	DV_{DD}	—	Digital power supply pin. Connect a capacitor of 0.1 μF or more between this pin and PGND.

Note:
The pin names in the parentheses are applied to ML22802/ML22P802.

ABSOLUTE MAXIMUM RATINGS

(DGND = PGND = AGND = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Digital power supply voltage	DV_{DD}, PV_{DD}	Ta = 25°C	–0.3 to +5.0	V
Analog power supply voltage	AV_{DD}		–0.3 to +5.0	V
Input voltage	V_{IN}	Ta = 25°C When a JEDEC2-layer board is mounted	–0.3 to DV_{DD}+0.3	V
Power dissipation	P_D		1.3	W
Output short-circuit current	I_{SC}	—	10	mA
Storage temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(DGND = PGND = AGND = 0 V)

Parameter	Symbol	Condition	Range			Unit
Digital power supply voltage	DV_{DD}, PV_{DD}	—	2.7 to 3.6			V
Analog power supply voltage	AV_{DD}	—	2.7 to 3.6			V
Operating temperature	T_{OP}	—	-20 to +85			°C
Master clock frequency	f_{OSC}	—	Min.	Typ.	Max.	MHz
			3.5	4.096	4.5	
External crystal oscillator capacitance	Cd, Cg	—	15	30	45	pF

ELECTRICAL CHARACTERISTICS

DC Characteristics

DV_{DD} = PV_{DD} = AV_{DD} = 2.7 to 3.6 V, DGND = PGND = AGND = 0 V, Ta = -20 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	0.86 × V_{DD}	—	—	V
"L" input voltage	V_{IL}	—	—	—	0.14 × V_{DD}	V
"H" output current 1	V_{OH1}	I_{OH} = –1 mA	V_{DD} – 0.4	—	—	V
"H" output current 2 (*1)	V_{OH2}	I_{OH} = –100 µA	V_{DD} – 0.4	—	—	V
"L" output current 1	V_{OL1}	I_{OL} = 2 mA	—	—	0.4	V
"L" output current 2 (*1)	V_{OL2}	I_{OL} = 100 µA	—	—	0.4	V
"H" input current 1	I_{IH1}	V_{IH} = DV_{DD}	—	—	10	µA
"H" input current 2 (*2)	I_{IH2}	V_{IH} = DV_{DD}	0.3	2.0	15	µA
"L" input current 1	I_{IL1}	V_{IL} = DGND	–10	—	—	µA
"L" input current 2 (*2)	I_{IL2}	V_{IL} = DGND	–15	–2.0	–0.3	µA
"H" output leakage current (*3)	I_{LOH}	V_{IH} = DV_{DD}	—	—	10	µA
"L" output leakage current (*3)	I_{LOL}	V_{IL} = DGND	–10	—	—	µA
Supply current during playback	I_{DD}	f_{OSC} = 4.096 MHz No output load	—	—	10	mA
Power-down supply current	I_{DDS}	Ta = -20 to +85°C	—	1	20	µA

Note: The input voltages and input currents apply to all the input pins except the XT pin.
The output voltages apply to all the output pins except the AOUT pin.

*1: Applies to the $\overline{XT}$ pin.
*2: Applies to the XT pin.
*3: Applies to the TESTO0 and TESTO1 pins.

Analog Section Characteristics

DV_{DD} = PV_{DD} = AV_{DD} = 2.7 to 3.6 V, DGND = PGND = AGND = 0 V, Ta = -20 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AOUT output load resistance	R_{LAO}	During silence playback	5	—	—	kΩ
AOUT output voltage range	V_{AOUT}	No output load	0.07 × AV_{DD}	—	0.64 × AV_{DD}	V

FUNCTIONAL DESCRIPTION

Serial CPU Interface

Command data can be input through the DI pin by signals input through the $\overline{CS}$ and SCK pins.

Setting the $\overline{CS}$ pin to a “L” level enables the serial CPU interface.

After the $\overline{CS}$ pin is set to a “L” level, the command data, which is synchronized with the SCK clock signal, is input through the DI pin from the MSB. The command data input through the DI pin is shifted into the LSI on the rising or falling edges of the SCK clock pulses and the command is executed by the rising or falling edge of the eighth pulse of the SCK clock.

Choosing between rising edges and falling edges of the clock pulses input through the SCK pin is determined by the signal input through the DIPH pin:

- When the DIPH pin is at a “L” level, the data input through the DI pin is shifted into the LSI on the rising edges of the SCK clock pulses.
- When the DIPH pin is at a “H” level, the data input through the DI pin is shifted into the LSI on the falling edges of the SCK clock pulses.

It is possible to input command data in the LSI even by holding the $\overline{CS}$ pin continuously at a “L” level. However, if unexpected pulses caused by noise are induced through the SCK pin, SCK clock pulses are incorrectly counted. As a result, command data cannot be input correctly. Setting the $\overline{CS}$ pin to a “H” level returns the count of the SCK clock pulses to the initial state.

Command List

Each command is configured in 1-byte (8-bit) units. Each of the PLAY and MUON command forms one command by two bytes each.

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
PUP1	0	0	0	0	—	—	S1	S0	Instantly shifts the device currently powered down to a command wait state.
PUP2	0	0	0	1	—	—	S1	S0	Suppresses pop noise and shifts the device currently powered down to a command wait state.
PDWN1	0	0	1	0	—	—	—	—	Instantly shifts the device from a command wait state to a power down state.
PDWN2	0	0	1	1	—	—	—	—	Suppresses pop noise and shifts the device from a command wait state to a power down state.
PLAY	0	1	0	0	—	—	—	—	Phrase-specified playback start command. Use the data of the 2nd byte to specify a phrase number.
	F7	F6	F5	F4	F3	F2	F1	F0	
STOP	0	1	1	0	—	—	—	—	Playback stop command.
MUON	0	1	1	1	—	—	—	—	Inserts silence. Use the data of the 2nd byte to specify the length of silence.
	M7	M6	M5	M4	M3	M2	M1	M0	
SLOOP	1	0	0	0	—	—	—	—	Command for setting the repeat playback mode. Enabled during playback.
CLOOP	1	0	0	1	—	—	—	—	Command for releasing the repeat playback mode. If the STOP command is input, repeat playback mode is released automatically.
VOL	1	0	1	0	V3	V2	V1	V0	Volume setting command.

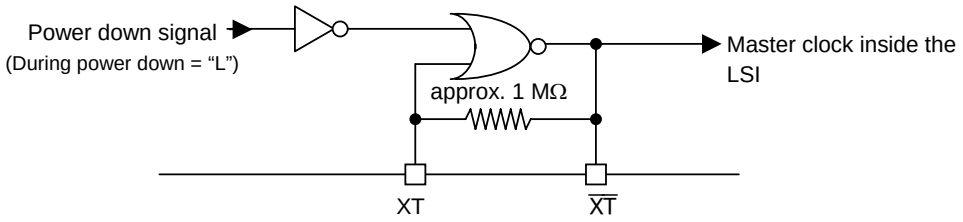
S1, S0 : Number of memory banks (*)
F7–F0 : Phrase address
M7–M0 : Length of silence period
V3–V0 : Sound volume

* S0 is fixed to “0” for ML22802/ML22P802.

Power Down Function

This LSI has the power down function. When in a power down state, all the circuits including the oscillator circuit stop operating, thus minimizing the supply current. When supplying an external clock to the XT pin, tie the pin at a "L" level during power down.

The figure below shows a equivalent circuit to an oscillator circuit.



The Initial Status at Reset Input and the Status at Power Down of Output Pins

The status of relative output pins at reset input and power down is shown below.

Digital output pin	State	Analog output pin	State
NCR	"H" level	AOUT	GND level
BUSY	"H" level		

Voice Synthesis Algorithm

The ML22804/ML22808-xxx contain four algorithm types to match the characteristic of playback voice: 4-bit ADPCM2 algorithm, 8-bit straight ADPCM2 algorithm, 8-bit non-linear PCM algorithm, and 16-bit straight PCM algorithm.
Key feature of each algorithm is described in the table below.

Voice synthesis algorithm	Applied waveform	Feature
OKI 4-bit ADPCM2	Normal voice waveform	OKI's specific speech synthesis algorithm of improved waveform follow-up with improved 4-bit ADPCM.
OKI 8-bit Nonlinear PCM	High-frequency components inclusive sound effect etc.	Algorithm, which plays back mid-range of waveform as 10-bit equivalent voice quality.
8-bit PCM		Normal 8-bit PCM algorithm
16-bit PCM		Normal 16-bit PCM algorithm

Playback Time and Memory Capacity

The playback time depends upon the memory capacity, sampling frequency, and playback method.
The equation showing the relationship is given below.
The equation below gives the playback time when the edit ROM function is not used.

(Bit length is 2 bits for 2-bit ADPCM2; 4 bits for 4-bit ADPCM2; 8 bits for PCM.)

Example:

Let the sampling frequency be 16 kHz and 4-bit ADPCM2 algorithm. Then the playback time is approx. 65 seconds, as shown below.

$$\text{Playback time} = \frac{1.024 \times (4096 - 16)\ (\text{Kbit})}{16\ (\text{kHz}) \times 4\ (\text{bit})} \cong 65\ (\text{sec})$$

Edit ROM Function

The edit ROM function makes it possible to play back multiple phrases in succession. The following functions are set using the edit ROM function:

- Continuous playback: There is no limit to the number of times a continuous playback can be specified. It depends on the memory capacity only.
- Silence insertion function: 20 to 1024 ms

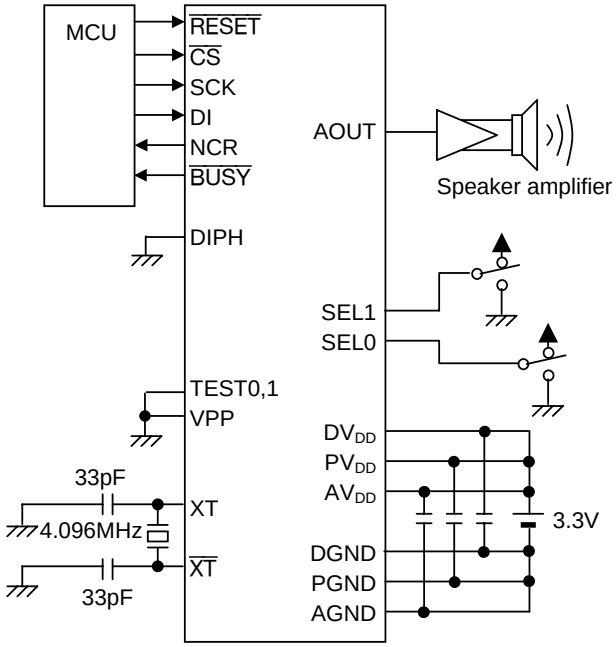
Using the edit ROM function enables an effective use of the memory capacity of voice ROM.

Memory Bank Selecting Function

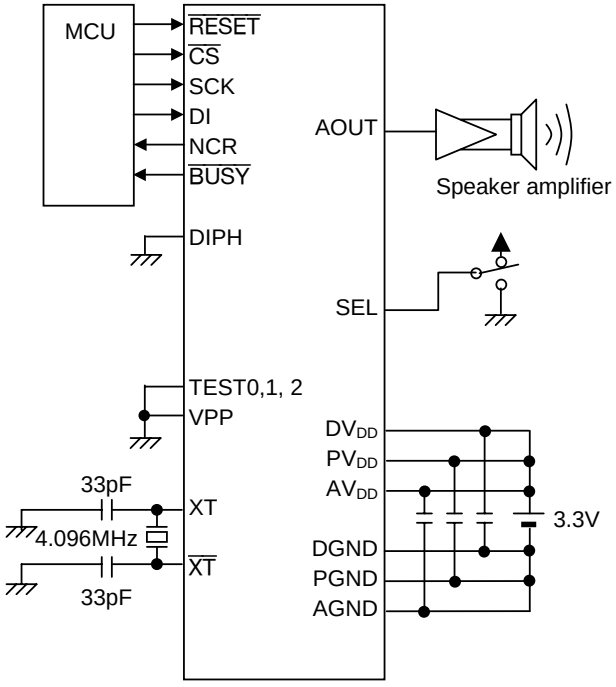
Using the memory bank selecting function, the internal ROM area in the ML22808/ML22804/ML22P808/ ML22P804 can be divided into up to four areas. If four banks are used, up to 1024 phrases can be played back since each bank is capable of up to 256 phrases. Using the memory bank selecting function, the internal ROM area in the MLl22802/ML22P802 can be divided into up to two areas. If two banks are used, up to 512 phrases can be played back because each bank is capable of up to 256 phrases. Using this function, it is possible to put together multiple ROM codes into one code.
In the case of the ML22808/ML22804/ML22P808/ML22P804, the memory is used by setting the SEL1 and SEL0 pins and in the case of the ML22802/ML22P802, the memory is used by setting the SEL pin, as shown in the tables below. In addition, when playing phrases, it is necessary to specify the number of memory banks by PUP1 or PUP2.

APPLICATION CIRCUITS

• ML22808/ML22804/ML22P808/ML22P804



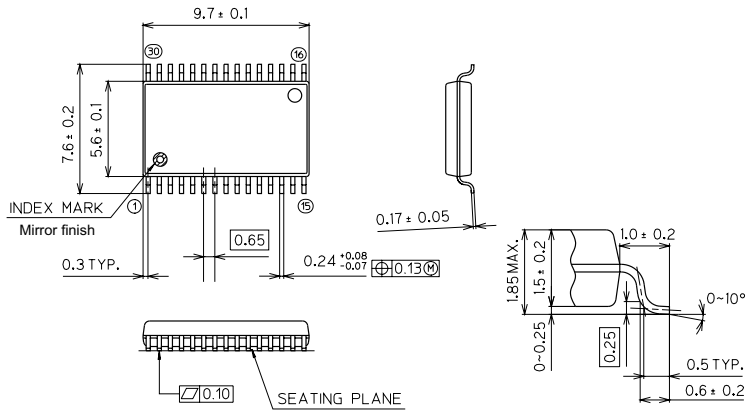
• ML22802/ML22P802



PACKAGE DIMENSIONS

(Unit: mm)

SSOP30-P-56-0.65-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.19 TYP.
Rev. No./Last Revised	5/Dec. 5, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact OKI's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No	Date	Page		Description
		Previous Edition	Current Edition	
FEDL2280XDIGEST-01	Sep. 29, 2006	–	–	Final edition 1
FEDL2280XDIGEST-02	Apr. 10, 2007	–	–	Final edition 2
		–	1 to 8, and 11	The product names (ML22802 and ML22P808 / ML22P804/ML22P802) have been added.
FEDL2280XDIGEST-03	Dec. 25, 2007	–	P13	The explanation for POWER down was modified.
		–	P1,9,10	Operating temperature was expanded..

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. OKI assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

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