OKI Semiconductor

This version: Jan. 1998
Previous version: Oct. 1997

MSM7650

NTSC/PAL Digital Encoder

GENERAL DESCRIPTION

The MSM7650 is a digital NTSC/PAL encoder. By inputting digital image data conforming to CCIR Rep624-4, it outputs analog composite video signals and analog S video signals. For the scanning system, interlaced or noninterlaced mode can be selected.
Since the MSM7650 is provided with pins dedicated to overlay function, text and graphics can be superimposed on a video signal.
In addition, this encoder has an internal 9-bit DAC. So, when compared with using a conventional analog encoder, the number of components, the board space, and points of adjustment can greatly be reduced, thereby realizing a low cost and high-accuracy system.
The host interface provided conforms to Philips's I²C specifications, which reduces interconnections between this encoder and mounting components.
The internal synchronization signal generator (SSG) allows the MSM7650 to operate in master or slave mode.

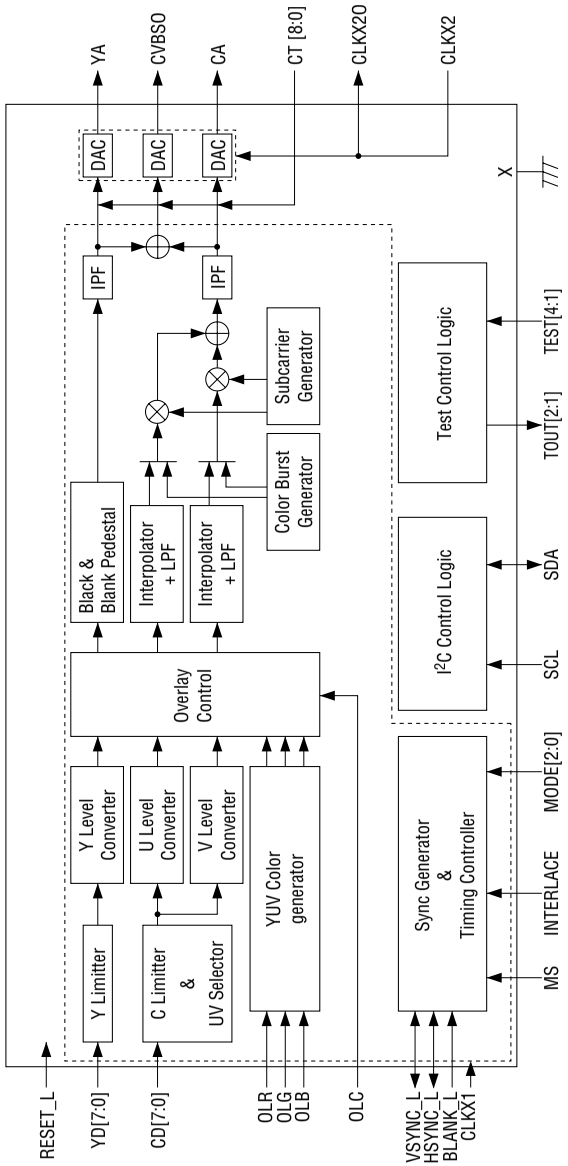
FEATURES

- Video signal system: NTSC/PAL
- Scanning system: interlaced/noninterlaced
- Input digital level: conforms to ITU-601 (CCIR601)
- Input-output timing: conforms to CCIR Rep 624-4
- Input signal (sampling ratio)
  Y:Cb:Cr (4:2:2/4:1:1)
- Supported sampling rates
  - NTSC 4Fsc (14.32 MHz)
  - NTSC ITU-R601 (13.5 MHz)
  - NTSC Square Pixel (12.27 MHz)
  - PAL ITU-R601 (13.5 MHz)
  - PAL Square Pixel (14.75 MHz)
- Internal SSG circuit (internally generates sync signals)
- Operation by external synchronization possible
- Internal 3ch 9-bit DAC (samples by double frequency)
- 3-bit title graphics can be displayed
- I²C-bus host interface function
- Package
  80-pin plastic QFP (QFP80-P-1420-0.80-BK) (Product name: MSM7650GS-BK)

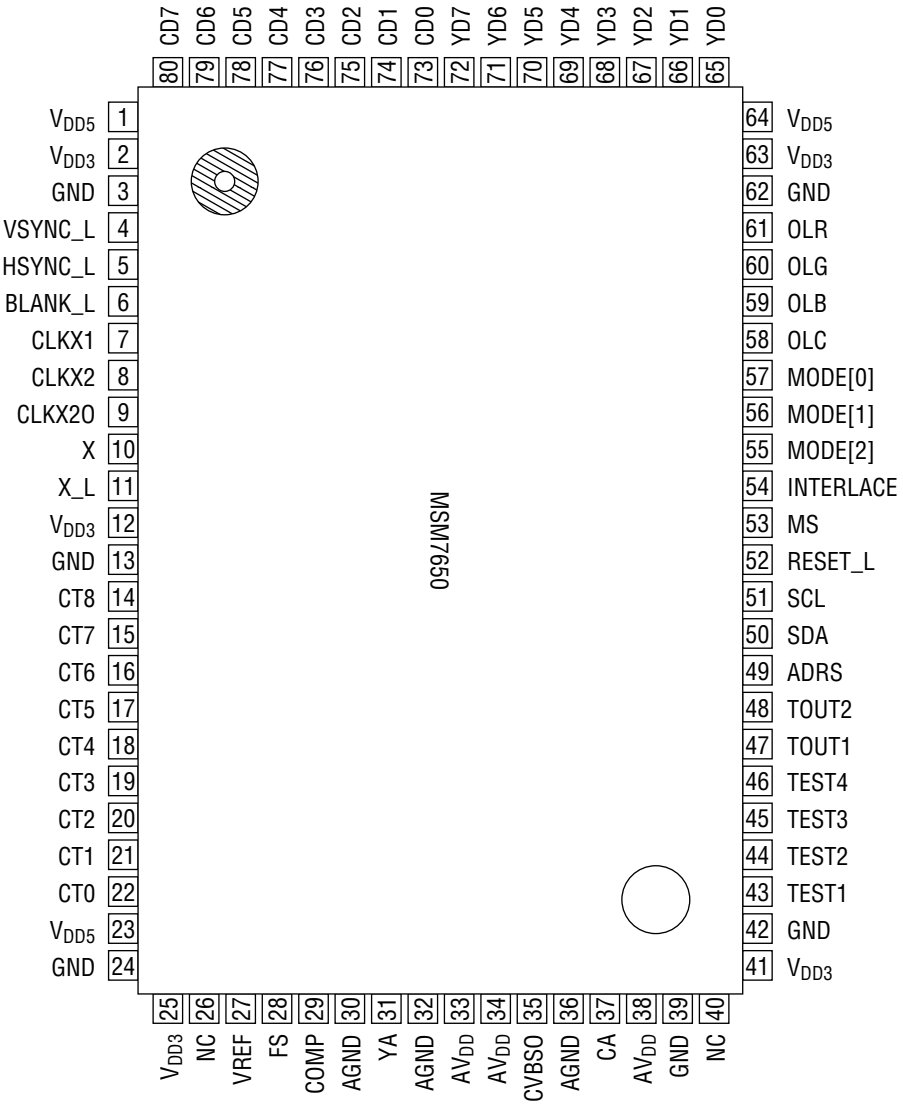
APPLICATIONS

- Video game equipment
- Electronic still camera
- Video printer
- Video camera
- Scanner
- Image file system
- CD-ROM
- Video graphics board
- Videophone
- Video conference system
- Multimedia equipment
- Digital VTR

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC : No-connection pin

80-Pin Plastic QFP

PIN DESCRIPTIONS (1/2)

Pin	I/O	Symbol	Description
1		V_{DD5}	5.0V power supply
2		V_{DD3}	3.3V power supply
3		GND	Digital GND
4	I/O	VSYNC_L	Vertical sync signal Polarity is negative. Output pin in master mode; input pin in slave mode.
5	I/O	HSYNC_L	Horizontal sync signal Polarity is negative. Output pin in master mode; input pin in slave mode.
6	I	BLANK_L	Composite blank signal. Polarity is negative.
7	I	CLKX1	Pixel clock input pin
8	I	CLKX2	Double pixel clock input pin
9	O	CLKX2O	Double pixel clock output pin
10	I	X	Test pin. Normally, fixed to "0".
11	O	X_L	Test pin
12		V_{DD3}	3.3V power supply
13		GND	Digital GND
14 to 22	I	CT8 to CT0	Input pin for testing. Normally, fixed to "0" or "1".
23		V_{DD5}	5.0V power supply
24		GND	Digital GND
25		V_{DD3}	3.3V power supply
26		NC	Not connected
27	I/O	VREF	Reference voltage for DAC
28	I	FS	DAC full scale adjustment pin
29	I	COMP	DAC phase compensation pin
30	I	AGND	Analog GND
31	O	YA	Analog luminance signal output pin
32		AGND	Analog GND
33		AV_{DD}	Analog power supply
34		AV_{DD}	Analog power supply
35	O	CVBSO	Analog composite video signal output pin
36		AGND	Analog GND
37	O	CA	Analog chrominance signal output pin
38		AV_{DD}	Analog power supply
39		GND	Digital GND
40		NC	Not connected
41		V_{DD3}	3.3V power supply
42		GND	Digital GND
43		TEST1	Input pin 1 for testing. Normally, fixed to "0".
44	I	TEST2	Input pin 2 for testing. Normally, fixed to "0".
45	I	TEST3	Input pin 3 for testing. Normally, fixed to "0".

PIN DESCRIPTIONS (2/2)

Pin	I/O	Symbol	Description
46	I	TEST4	Input pin 4 for testing. Normally, fixed to "0".
47	O	TOUT1	Output pin for testing
48	O	TOUT2	Output pin for testing
49	I	ADRS	I^2C-bus subaddress setting pin. One of two addresses switchable can be selected as subaddress. 1: 1000110/0: 1000100
50	I/O	SDA	I^2C-bus data pin
51	I	SCL	I^2C-bus clock pin
52	I	RESET_L	System reset pin. "1" at an open state by an internal pull-up resistor
53	I	MS	Operation mode select signal pin for synchronization circuit. 1: master/0: slave. "1" at an open state by an internal pull-up resistor
54	I	INTERLACE	Interlace/noninterlace select signal pin. 1: interlaced/0: noninterlaced. "1" at an open state by an internal pull-up resistor
55 to 57	I	MODE[2] to MODE[0]	Video mode select pins These pins are valid when MR[7] is "1". 000: NTSC CCIR 001: NTSC Square Pixel 010: NTSC 4Fsc 100: PAL CCIR 101: PAL Square Pixel "000" at an open state by an internal pull-down resistor
58	I	OLC	Transparent control signal Overlay signal is displayed when this pin is "H".
59	I	OLB	Overlay text color (Blue component)
60	I	OLG	Overlay text color (Green component)
61	I	OLR	Overlay text color (Red component)
62		GND	Digital GND
63	I	V_{DD3}	3.3V power supply
64		V_{DD5}	5.0V power supply
65 to 72	I	YD0 to YD7	Digital image luminance signal data input pin Level is based on ITU-601. YD7 is MSB.
73 to 80		CD0 to CD7	Digital image chrominance signal data input pin Level is based on ITU-601. CD7 is MSB.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD5}	Ta=25°C	–0.3 to +7	V
	V_{DD3}	Ta=25°C	–0.3 to +4.5	
	AV_{DD}	Ta=25°C	–0.3 to +4.5	
Input Voltage	V_I	Ta=25°C	–0.3 to V_{DD5} +0.3	V
Analog Output Current	I_O	—	40	mA
Power Consumption	P_W	—	800	mW
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD5}	Ta=25˚C	4.5	5.0	5.5	V
	V_{DD3}	Ta=25˚C	3.0	3.3	3.6	
	AV_{DD}	Ta=25˚C	3.0	3.3	3.6	
Power Supply Voltage	GND	Ta=25˚C	—	0.0	—	V
	AGND	Ta=25˚C	—	0.0	—	
High Level Input Voltage	V_{IH1}	SDA, CLKX1, Except CLKX2, Ta=25˚C	2.2	—	V_{DD5}	V
	V_{IH2}	SDA, Ta=25˚C	$0.8V_{DD5}$	—	V_{DD5}	V
	V_{IH3}	CLKX1,CLKX2, Ta=25˚C	2.4	—	V_{DD5}	V
Low Level Input Voltage	V_{IL}	—	0.0	—	0.5	V
Operating Temperature Range	Ta	—	0.0	—	70	˚C
External Reference Voltage (*1)	Vrefex	—	—	1.25	—	V
DA Current Setting Resistance (*2)	Riadj	—	—	330	—	Ω
DA Output Load Resistance	R_L	—	—	75	—	Ω

(*1) When external reference voltage is not supplied, internal reference voltage is as follows.

Internal Reference Voltage	Vrefin	—	1.15	—	1.45	V

(*2) A volume control resistor of approx. 500Ω is recommendable for adjusting the output current.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta=0 to +70°C, V_{DD3}=3.3V±0.3V, V_{DD5}=5V±10%)

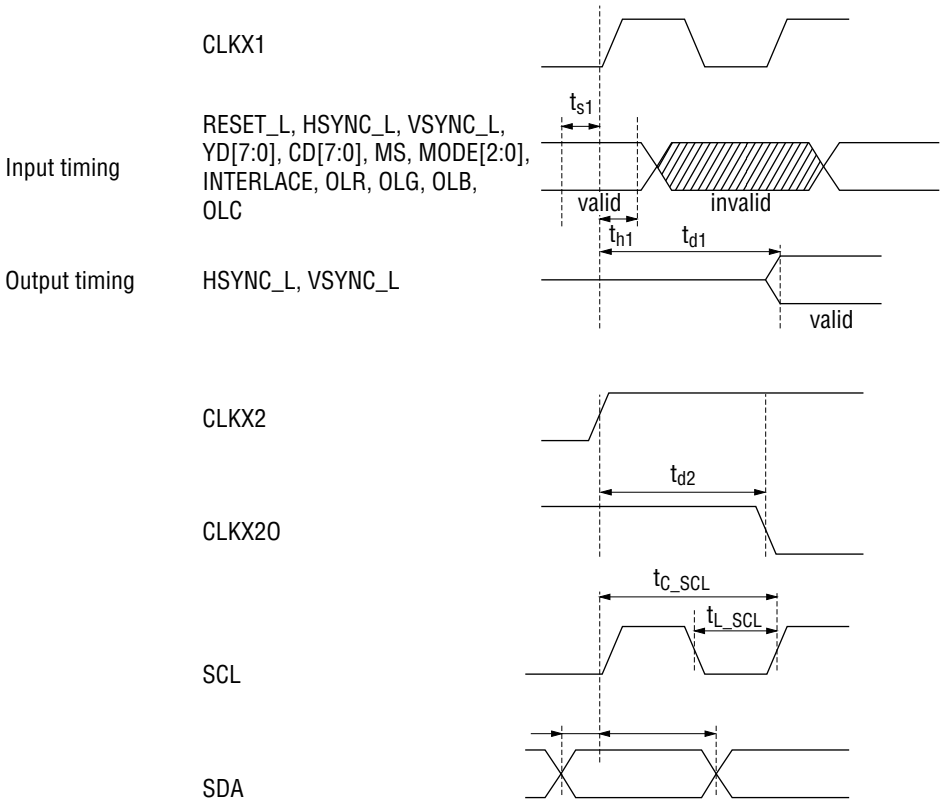
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High Level Output Voltage	V_{OH}	I_{OH}=–4mA (*1) I_{OH}=–8mA (*2)	0.8V_{DD5}	—	V_{DD5}	V
Low Level Output Voltage	V_{OL}	I_{OL}=4mA (*1) I_{OL}=8mA (*2)	0	—	0.6	V
Input Leak Current	I_I	V_I=GND to V_{DD5}	–10	—	10	µA
Output Leak Current	I_O	V_I=GND to V_{DD5} (*3)	–10	—	10	µA
Power Supply Current (operating)	I_{DDO}	CLKX1=13.5MHz CLKX2=27.0MHz	—	120	140	mA
Power Supply Current (standby)	I_{DDS}	RESET_L="L" CLKX1=CLKX2=0Hz	—	65	80	mA
I² C-bus SDA Output Voltage	$SDAV_L$	Low level, I_{OL}=3mA	0	—	0.4	V
I²C-bus SDA Output Current	$SDAI_O$	During Acknowledge	3	—	—	mA
Internal Reference Voltage	Vrefin	—	1.15	—	1.45	V
DA Output Load Resistance	R_L	—		75		Ω
Integral Linearity	SINL			±2		LSB
Differential Linearity	SDNL			±1		LSB

(*1) HSYNC_L, VSYNC_L, SDA, TO, CT[7:0]
(*2) CLKX2O
(*3) SDA

AC Characteristics

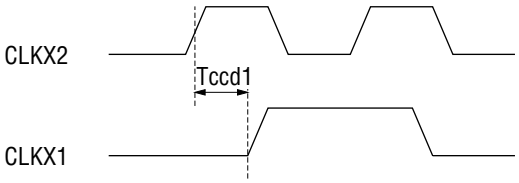
(Ta=0 to +70°C, V_{DD3}=3.3V±0.3V, V_{DD5}=5V±0.5V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CLKX Cycle Time	T_S	PAL Square Pixel	—	67.8	—	ns
		NTSC 4Fsc	—	69.8	—	ns
		NTSC Square Pixel	—	81.5	—	ns
		ITU-RS601	—	74.1	—	ns
Input Data Setup Time	t_{s1}	—	7.03	—	—	ns
Input Data Hold Time	t_{h1}	—	9.48	—	—	ns
Output Delay Time	t_{d1}	—	18.35	—	24.12	ns
CLKX2O Delay Time	t_{d2}	—	7.69	—	9.53	ns
Clock Cycle Time	t_{C_SCL}	Rpull_up=4.7kΩ	200			ns
Clock Duty Cycle	t_{D_SCL}		—	50	—	%
Low Level Cycle	t_{L_SCL}	Rpull_up=4.7kΩ	100			ns

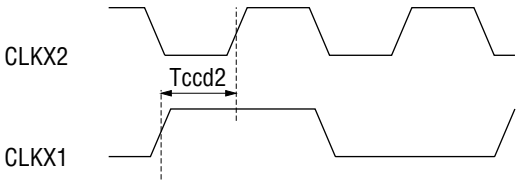


The phase relations between CLKX1 and CLKX2 are shown below.

1. When the CLKX1 pulse rises later than the CLKX2 pulse.



2. When the CLKX1 pulse rises earlier than the CLKX2 pulse.



Tccd1: 20.14 [ns]
Tccd2: 3.27 [ns]

BLOCK FUNCTIONAL DESCRIPTION

Y Limitter

This block limits the contents outside the specified range as follows for input luminance signal YD specified by the ITU-601 standard.
- Signals are limited to YD = 235 when YD_IN > 235
- Signals are limited to YD = 16 when YD_IN < 16
- In other cases, signals are fed as is to next processing

C Limitter

This block limits the contents outside the specified range as follows for input chrominance signals specified by the ITU-601 standard.
The input chrominance signal is output as a 2's complement format.
The processing procedure follows.

1) Format processing for input chrominance signals
- If MR [6] = 0, CD is in offset binary format. CD is converted to 2's complement format and is fed to next processing.
- If MR [6] = 1, CD is in 2's complement format. CD is fed as is to next processing.

2) Clipping processing
- Signals are limited to CD = 112 when CD>112
- Signals are limited to CD = -112 when CD < -112
- In other cases, signals are fed to next processing

In addition, this block separates U and V components from the input chrominance signal CD into which data of U and V components has been inserted using time sharing, and then passes signals to the next process.

- **Y Level Converter**
  Converts ITU-601 standard luminance signal level to DAC digital input level.

- **U Level Converter**
  Converts ITU-601 standard chrominance signal level to DAC digital input level.

- **V Level Converter**
  Converts ITU-601 standard chrominance signal level to DAC digital input level.

- **YUV Color Generator**
  This block generates luminance and chrominance signals from over lay color signals OLR, OLG and OLB. Control signals (CR [2:0]) control the output content (overlay or color bar) and output level (100%, 75%, 50%, 25%).

- **Overlay Control**
  This block selects input image data or YUV Color Generator output signals.
  It is determined by the level of the control signal (OLC, CR [2]), as shown below:
  CR [2] = 1, OLC = ?: Selects color bar signal (YUV Color Generator output signal).
  CR [2] = 0, OLC = 1: Selects overlay signal (YUV Color Generator output signal).
  CR [2] = 0, OLC = 0: Selects input image data.

- **Black & Blank Pedestal**
  This block adds sync signals at the luminance side to luminance signals.

- **Interpolator +LPF**
  This block executes data interpolation and the elimination of high frequency components by LPF for input chrominance signals. Both 4:2:2 and 4:1:1 signals are processed.

- **I²C Control Logic**
  This is the serial interface block based on I²C standard of Phillips Corporation.
  Internal registers MR and CR can be set from the master side.
  When writing to the internal registers other than MR [5] (black level control) and CR [1:0] (overlay level), written contents are immediately set to them. It is during the vertical blanking period that written contents are set to MR [5] and CR [1:0].

- **Sync Generator & Timing Controller**
  This block generates sync signals and control signals.
  This block is operated in slave mode, which performs external synchronization, and in master mode, which internally generates sync signals.

- **Color Burst Generator**
  Outputs U and V components of amplitude of burst signals.

- **Subcarrier Generator**
  Executes color subcarrier generation.

- **Interpolation Filter (IPF)**
  This block performs upsampling at CLK X 2 (double speed CLKX1) for luminance signals and chrominance signals modulated with CLKX1. Interpolation processing is executed in this process.

INPUT DATA FORMAT

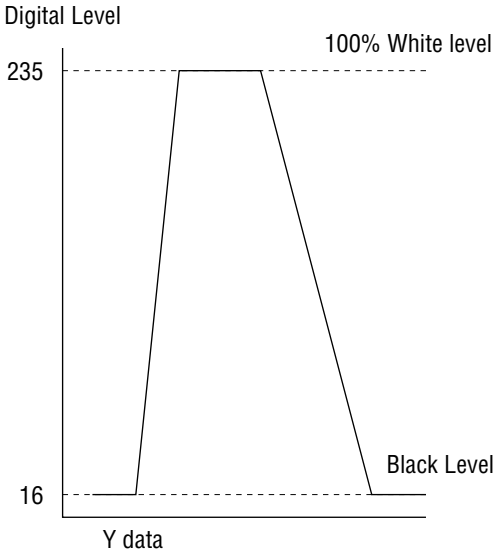
Input Digital Level

The content conforms to CCIR601 (ITU-601).

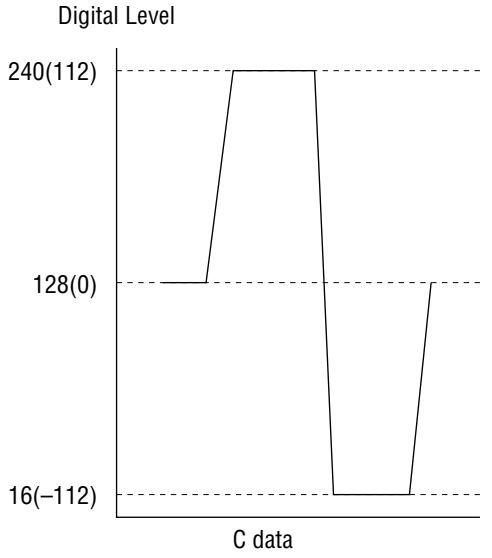
For chrominance input Cb and Cr, 2's complement and offset binary formats are available by setting of internal registers.

Input values outside the specified range are limited by internal clipping processing.

The valid input levels of luminance signal and chrominance signal are shown below.



Input luminance signal level

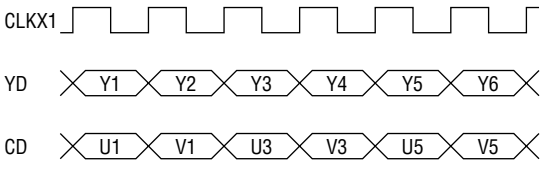


Note) Values are in offset binary format.
(Values in parenthesis are in 2's complement format.)

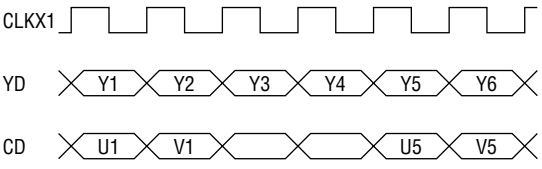
Input chrominance signal level

Basic Pixel Sampling Ratio

4:2:2 and 4:1:1 sampling are supported. An internal register can control the sampling ratio.



4:2:2 sampling



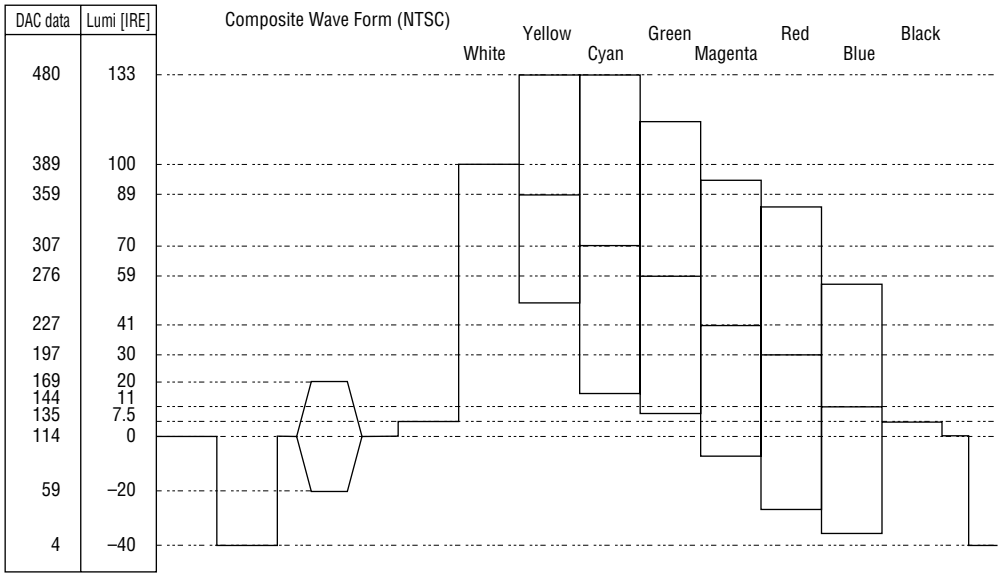
4:1:1 sampling

OUTPUT FORMAT

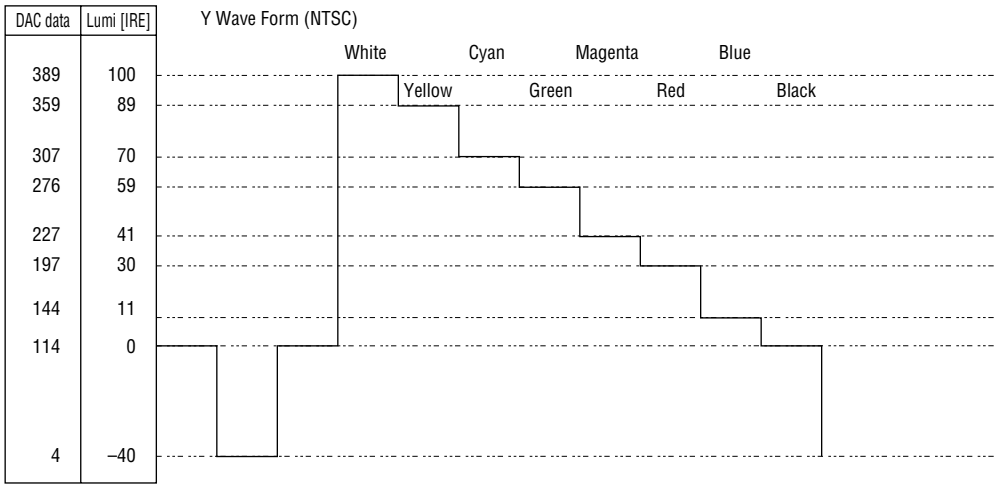
Output Level

When the output level of the operation mode is NTSC, the content of the output level differs depending on setup level setting by internal registers.
When the setup level is set, data is output with Black-White as 92.5 IRE.
When the setup level is not set, data is output with Black-White as 100 IRE.
However, the setup level setting above is valid only when NTSC is selected as operation mode, and setup level does not exist when PAL is selected as the operation mode.

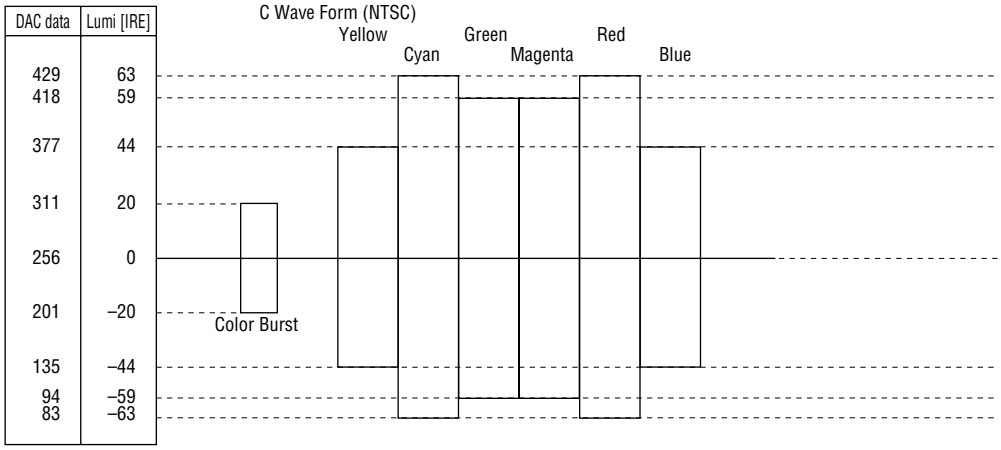
When the contents of 100% luminance order color bar are input to the encoder, the DAC input level is as follows.



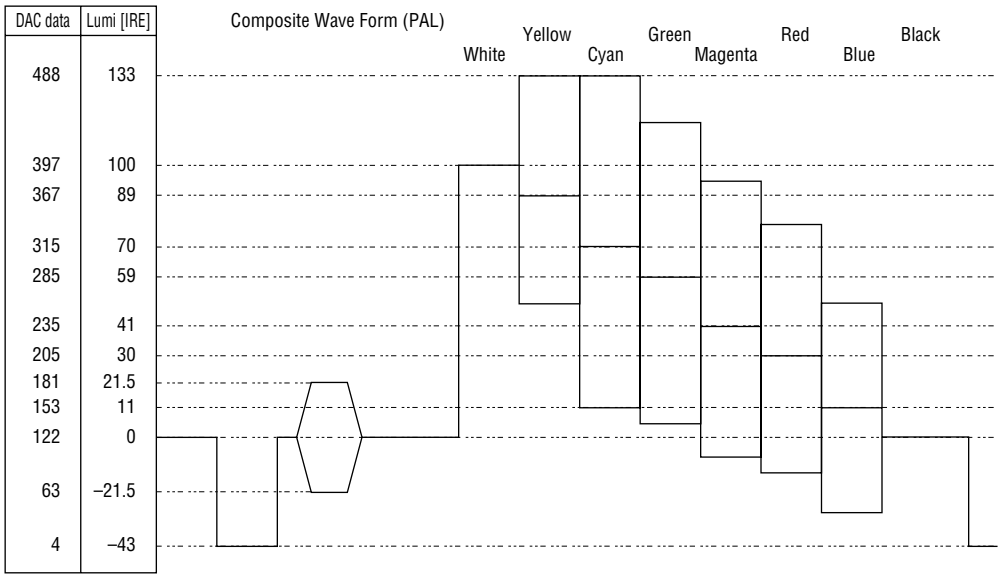
NTSC composite signal (setup: 7.5 IRE)



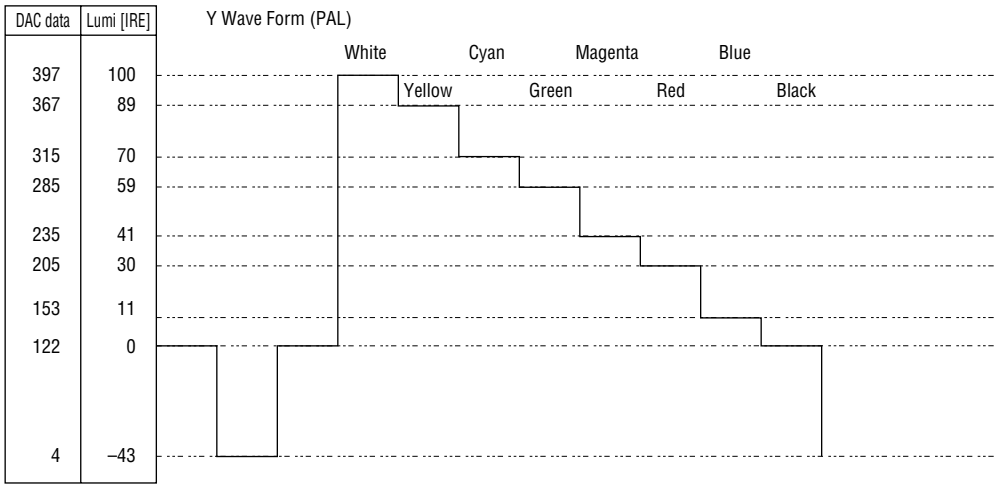
NTSC Y signal output (setup: 0)



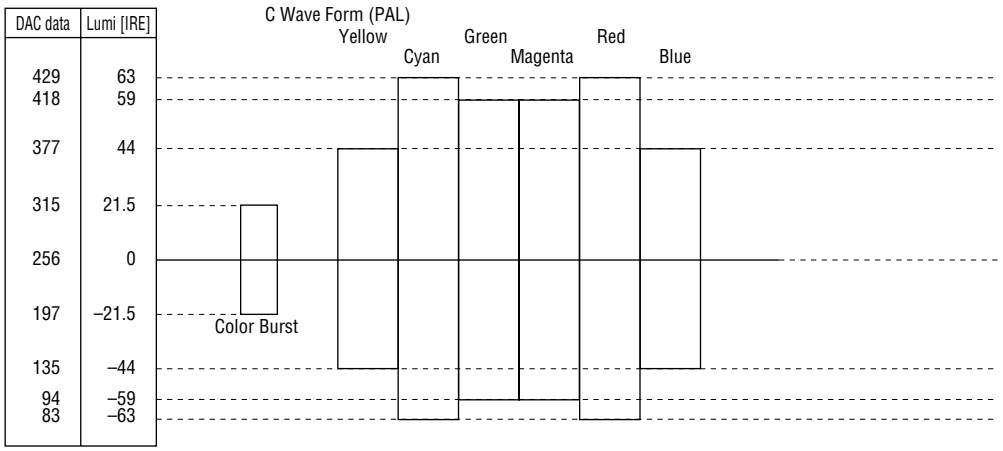
NTSC C signal output (setup: 0)



PAL composite signal



PAL Y signal output



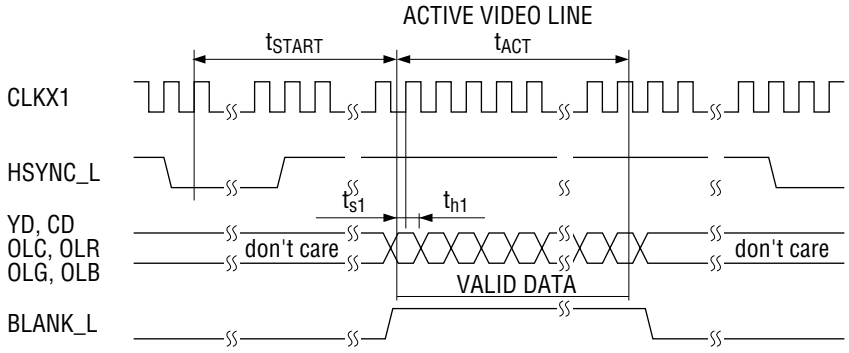
PAL C signal output

CLOCK TIMING

Input Data Timing

Input data and sync signals are fed into the encoder at the rising edge of the clock.

Input data is handled as valid pixel data when t_{START} passes after the falling edge of HSYNC_L. Chrominance signal of input data at this time is regarded as Cb.



Video data input timing

Input data is recognized as valid pixel data when input signal BLANK_L is high in the t_{ACT} period.
When BLANK_L is high during the blanking period, however, input data is not output as valid pixel data since processing to maintain blanking period is internally in-progress.

The values of t_{START} differ slightly in master mode and slave mode. The values of t_{START} are as follows.

In master mode

Operation mode	t_{STA}(Ts)
CCIR 601 NTSC	126
Square Pixel NTSC	141
4Fsc NTSC	115
CCIR PAL	134
Square Pixel PAL	154

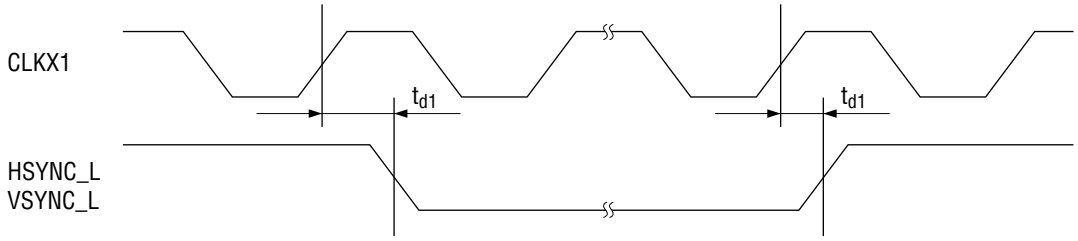
In slave mode

Operation mode	t_{STA}(Ts)
CCIR 601 NTSC	129
Square Pixel NTSC	144
4Fsc NTSC	118
CCIR PAL	137
Square Pixel PAL	157

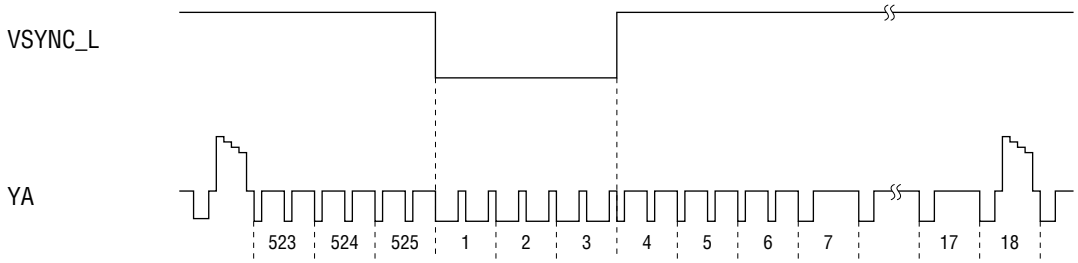
$t_{STA}-t_{S1}=t_{START}$

Internal Synchronization Output Timing

Input and output timing of HSYNC_L and VSYNC_L in master mode is as follows.



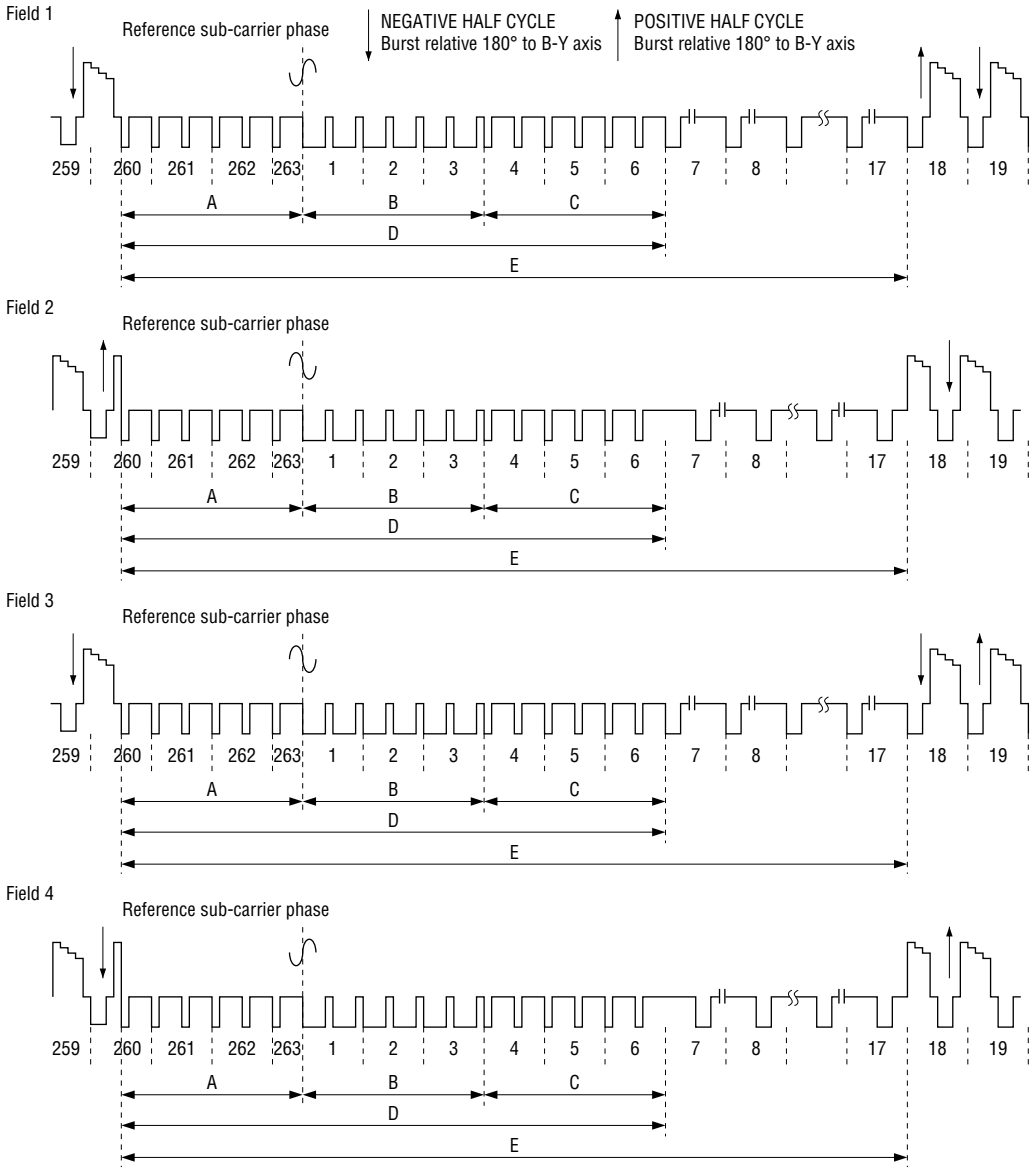
Output timing of internal synchronization CLK1, HSYNC_L and VSYNC_L



Output timing of internal synchronization VSYNC_L

Output Timing

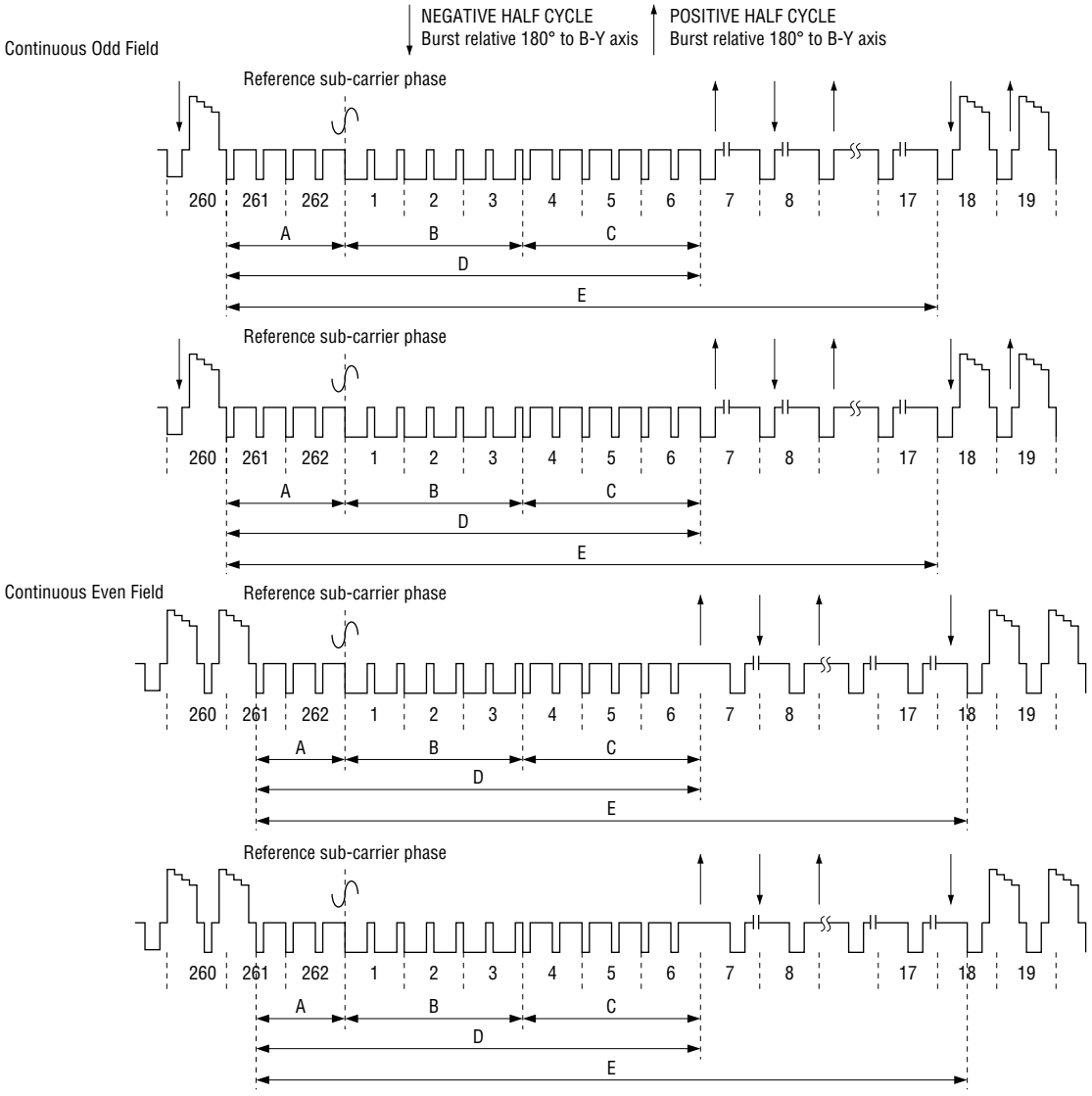
Output timing conforms to CCIR Rep 624-4.
When the operation method is NTSC/PAL and the scanning method is interlace/noninterlace, the output wave form content of composite signals are as follows.



Output timing (interlaced NTSC)

Symbol	Name	Period
		Odd field (Even field)
A	First equalizing pulse period (3H)	259.5 to 262.5H
B	Vertical synchronization period (3H)	1 to 3H
C	Second equalizing pulse period (3H)	4 to 6H
D	Burst pause period	1 to 6,259.5 to 262.5H
E	Vertical blanking period (20H)	1 to 17,259.5 to 262.5H

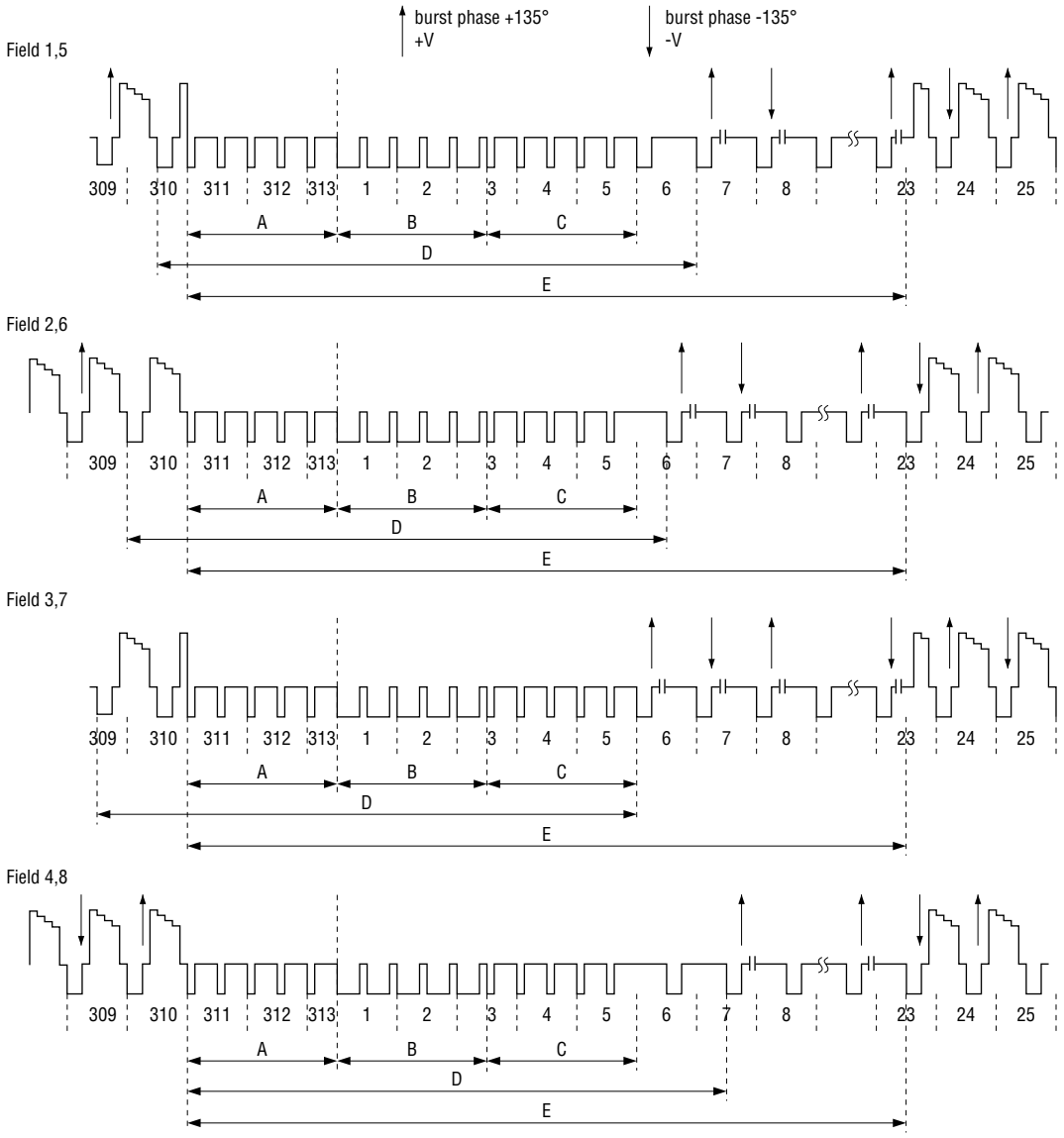
Output timing (interlaced NTSC)



Output timing (noninterlaced NTSC)

Symbol	Name	Period	
		Continuous odd field	Continuous even field
A	First equalizing pulse period (2H)	261 to 262H	261.5 to 262H
B	Vertical synchronization period (3H)	1 to 3H	1 to 3H
C	Second equalizing pulse period (2H)	4 to 6H	4 to 6H
D	Burst pause period	261 to 6H	261.5 to 6H
E	Vertical blanking period (19H)	261 to 17H	261.5 to 17.5H

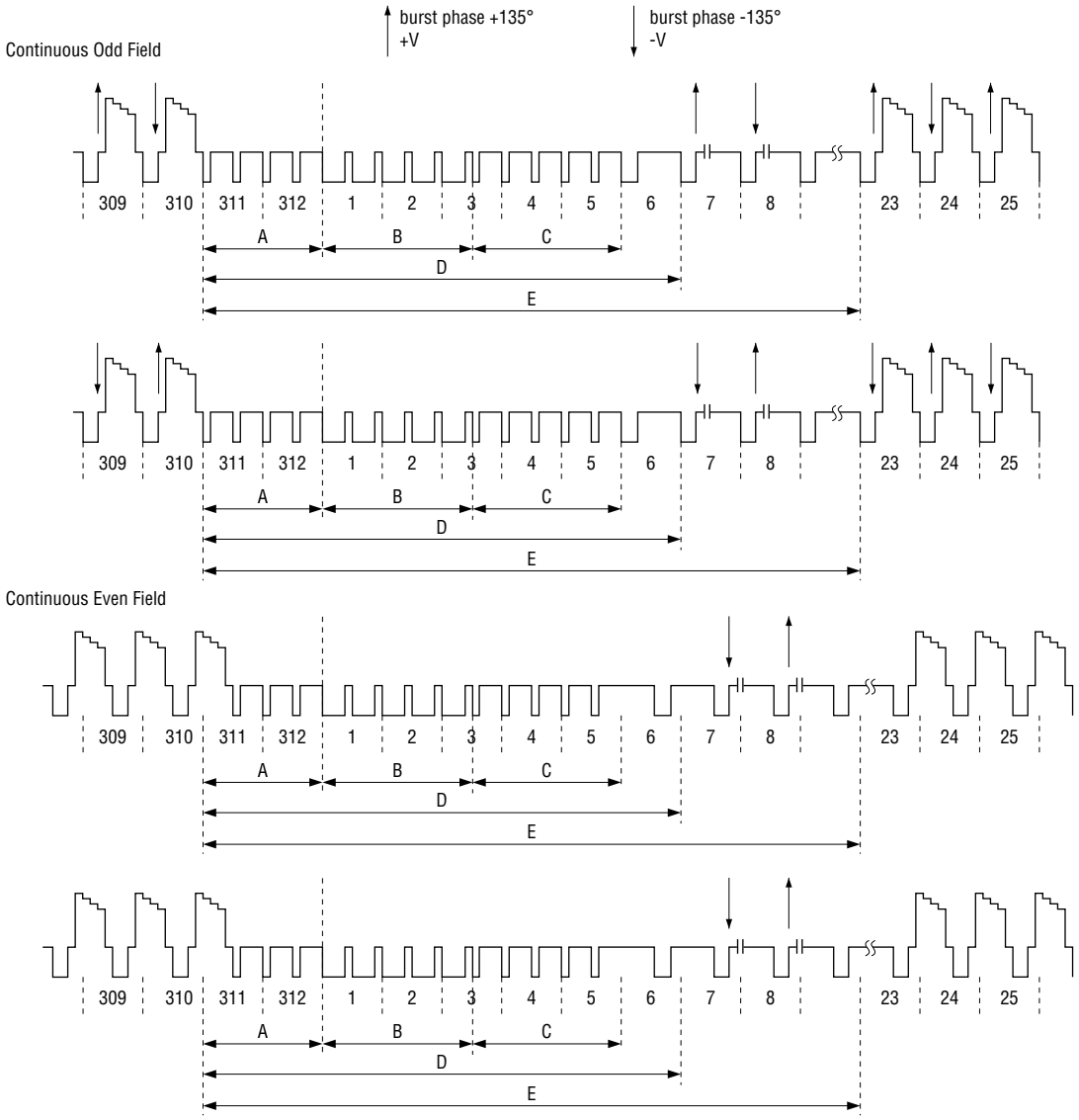
Output timing (noninterlaced NTSC)



Output timing (Interlaced PAL)

Symbol	Name	Period			
		Filed 1,5	Filed 2,6	Filed 3,7	Filed 4,8
A	First equalizing pulse period (2.5H)	311 to 312.5H	311 to 312.5H	311 to 312.5H	311 to 312.5H
B	Vertical synchronization period (2.5H)	1 to 2.5H	1 to 2.5H	1 to 2.5H	1 to 2.5H
C	Second equalizing pulse period (2.5H)	2.5 to 5H	2.5 to 5H	2.5 to 5H	2.5 to 5H
D	Burst pause period	1 to 6,310 to 312.5H	1 to 5.5,308.5 to 312.5H	1 to 5,311 to 312.5H	1 to 6.5,309.5 to 312.5H
E	Vertical blanking period (25H)	1 to 22.5,311 to 312.5H	1 to 22.5,311 to 312.5H	1 to 22.5,311 to 312.5H	1 to 22.5,311 to 312.5H

Output timing (Interlaced PAL)



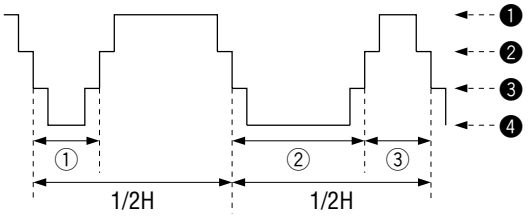
Output timing (Noninterlaced PAL)

Symbol	Name	Period	
		Continuous odd field	Continuous even field
A	First equalizing pulse period (2H)	311 to 312H	311.5 to 312H
B	Vertical synchronization period (2.5H)	1 to 2.5H	1 to 2.5H
C	Second equalizing pulse period (2.5H)	2.5 to 5H	2.5 to 5H
D	Burst pause period	311 to 6H	311.5 to 6H
E	Vertical blanking period (24H)	311 to 22H	311.5 to 22.5H

Output timing (Noninterlaced PAL)

<Equalizing pulse vertical synchronization period>

Equalizing pulse vertical synchronization period



①Equalizing pulse width
②Vertical sync pulse width
③Serration
❶blanking level
❷(synchronizing+{blanking level) × (2/3)
❸(synchronizing+{blanking level) × (1/3)
❹Synchronzing level

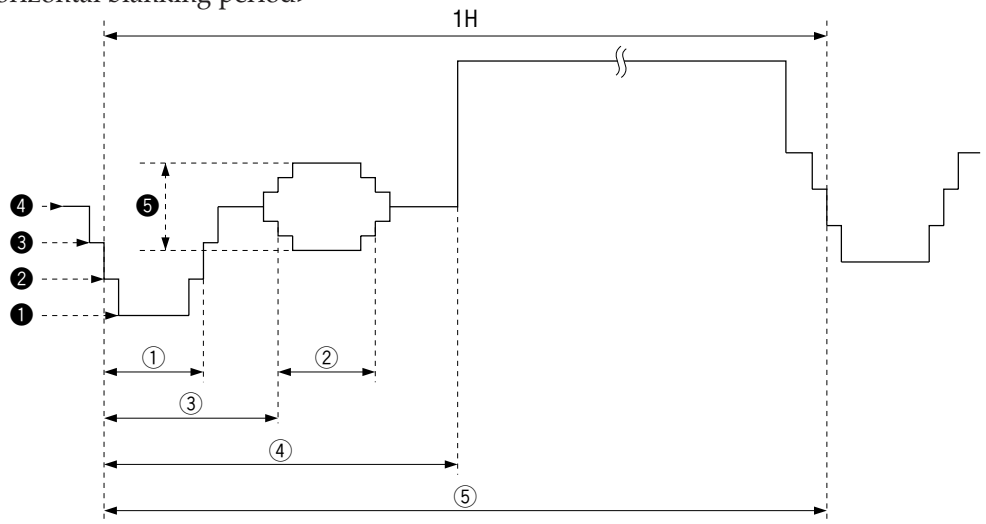
Equalizing pulse vertical synchronization period

Setting content of equalizing pulse vertical synchronization period (Ts is sampling clock cycle in each mode)

	①	②	③	1/2H
NTSC CCIR601	31Ts	398Ts	64Ts	429Ts
PAL CCIR601	32Ts	369Ts	63Ts	432Ts
NTSC Square Pixel	28Ts	332Ts	58Ts	390Ts
NTSC 4Fsc	33Ts	387Ts	68Ts	455Ts
PAL Square Pixel	35Ts	403Ts	69Ts	472Ts

Equalizing pulse vertical synchronization period

<Horizontal blanking period>



①Horizontal sync pulse width
②Burst signal output period
③Burst signal start
④Horizontal blanking period (excluding front porch)
⑤Front porch start
❶Synchronzing level
❷(synchronizing+{blanking level) × (1/3)
❸(synchronizing+{blanking level) × (2/3)
❹blanking level
❺peak to peak value of burst

Horizontal blanking period

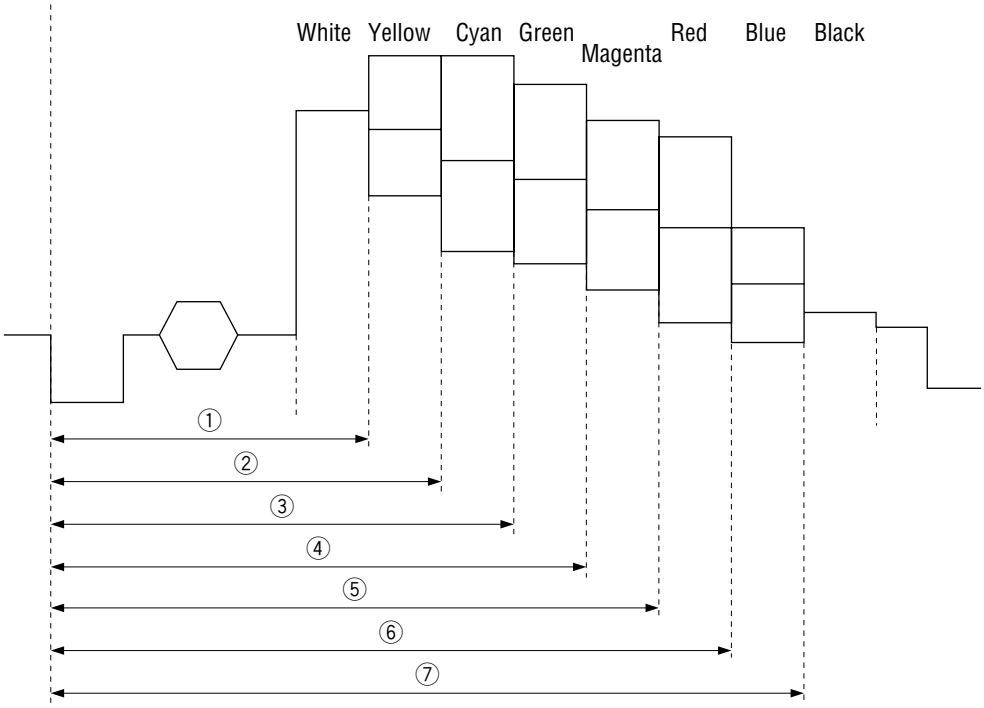
Setting content of horizontal blanking period (Ts is sampling clock cycle in each mode)

	①	②	③	④	⑤	Total dots/1H
NTSC CCIR601	63Ts	31Ts	71Ts	127Ts	838Ts	858
PAL CCIR601	63Ts	31Ts	75Ts	142Ts	844Ts	864
NTSC Square Pixel	58Ts	31Ts	65Ts	116Ts	762Ts	780
NTSC 4Fsc	67Ts	36Ts	75Ts	135Ts	889Ts	910
PAL Square Pixel	69Ts	34Ts	82Ts	155Ts	922Ts	944

Setting content of horizontal blanking period

Internally Generated Color Bar Output Timing

This function outputs a 100% and 75% luminance order color bar by setting internal registers. Output timing of each color of the color bar is as follows.



Each color of color bar output timing

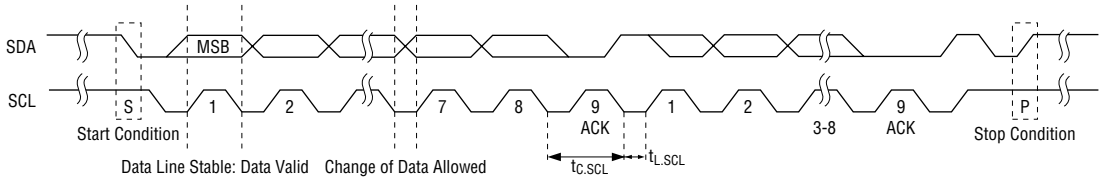
Operation mode	hblank	①	②	③	④	⑤	⑥	⑦	1H
NTSC CCIR601	127Ts	216Ts	305Ts	394Ts	483Ts	572Ts	661Ts	750Ts	858Ts
NTSC Square Pixel	116Ts	197Ts	278Ts	359Ts	440Ts	521Ts	602Ts	682Ts	780Ts
NTSC 4Fsc	135Ts	230Ts	325Ts	419Ts	513Ts	607Ts	701Ts	795Ts	910Ts
PAL CCIR601	142Ts	230Ts	318Ts	406Ts	494Ts	582Ts	670Ts	757Ts	864Ts
PAL Square Pixel	155Ts	251Ts	347Ts	443Ts	539Ts	635Ts	731Ts	827Ts	944Ts

(Ts is sampling clock cycle)

Each color of color bar output timing

I²C-bus Interface Input/Output Timing

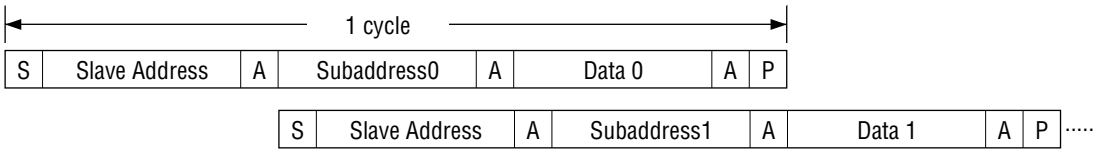
Basic input/output timing of I²C-bus interface is shown below.



I²C-bus basic input/output timing

I²C BUS FORMAT

Basic input format of I²C-bus interface is shown below.



Symbol	Description
S	Start condition
Slave Address	Slave address 1000100 or 1000000, 8th bit is write signal.
A	Acknowledge. Generated by slave
Subaddress	Subaddress byte
Data n	Data byte and acknowledge continues until data byte stop condition is met.
P	Stop condition

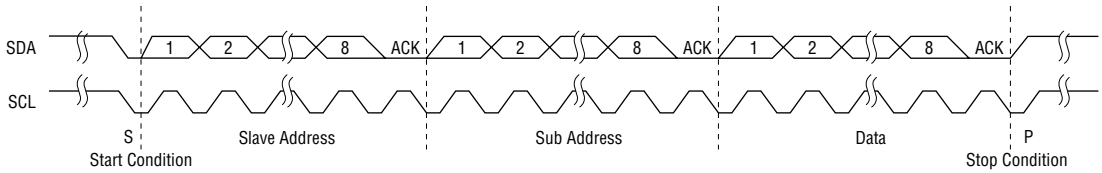
It is required to input the above-mentioned format from the start condition to the stop condition each time of writing a subaddress.
For example, when writing the subaddresses 0 to 2, the format should be input three times.

In case data of more than one byte are transferred,

The 4th byte data and following data each are written over the same subaddress.
If one of the following matters occurs, the encoder will not return "A" (Acknowledge).

- The slave address does not match.
- A non-existent subaddress is specified.
- The read/write attribute of a register does not match "X" (read/write control bit).

The input timing is shown below.



CONTENTS OF INTERNAL REGISTER SETTING

All registers can be written by accessing 8 bits.
"0" is read from an undefined bit.
The contents of internal registers are shown below. (A value with "*" is the default.)

Mode Register (MR) (Default value after system reset: 10H)

MR[7]	Override	Selects setting of external terminal or internal register *0: setting of external terminal is valid 1: setting of internal registers is valid
MR[6]	Chroma format	Chrominance signal input format *0: Offset binary 1: 2's Complement
MR[5]	Black level control	Black level setting (setup) Note) Valid only for NTSC. *0: Black level 7.5 IRE 1: Black level 0 IRE
MR[4]	Synchronization mode	Selects master/slave operation of sync signal generator. 0: slave mode *1: master mode
MR[3]	Pixel sampling ratio	Sampling ratio *0: 4:2:2 1: 4:1:1
MR[2:0]	Video mode select	Selects operation mode *000: CCIR 601 NTSC 13.5 MHz 001: NTSC Square Pixel 12.27 MHz 010: NTSC 4Fsc 14.32 MHz 100: CCIR 601 PAL 13.5 MHz 101: PAL Square Pixel 14.75 MHz

Command Register (CR) (Default value after system reset: 1BH)

CR[7:5]	Undefined	Undefined
CR[4]	Genlock	Selects SCH phase management status 0: Genlock Off (subcarrier is self generated) *1: Genlock On (management of SCH phase is executed)
CR[3]	Non-Interlace	Scanning method in master mode 0: Non-Interlace *1: Interlace
CR[2]	Color bar	Output control of luminance order color bar for adjustment *0: input image data or overlay data 1: luminance order color bar
CR[1:0]	Overlay level	Luminance signal output level control of overlay signals and luminance order color bar for adjustment 00: 25% 01: 50% 10: 75% *11: 100%

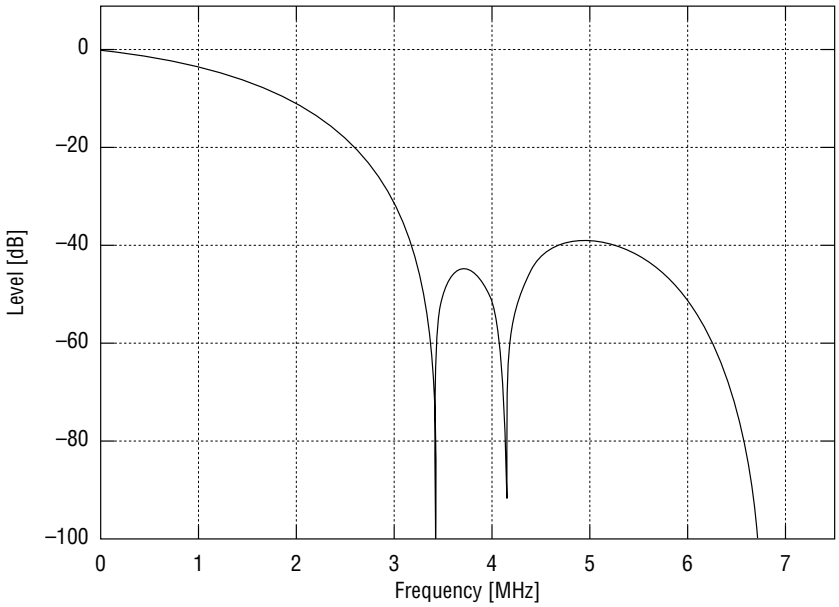
Register function	Subaddress	Data byte							
		D7	D6	D5	D4	D3	D2	D1	D0
Mode Register (MR)	0	MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
Command Register (CR)	1	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0

FILTER CHARACTERISTICS

The characteristics of LPF used for color signal processing and interpolation filters used for upsampling processing are shown below.

LPF for 411 color signals

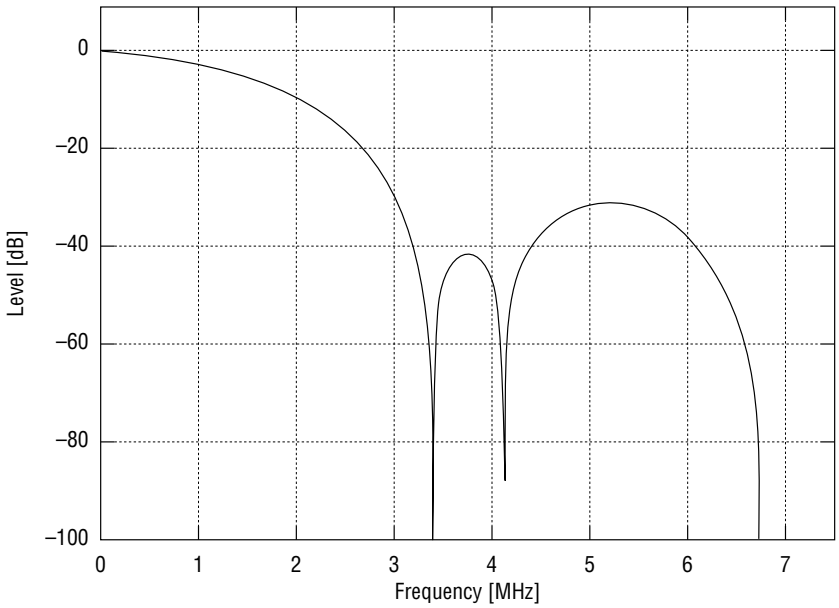
The following characteristics are when the clock frequency is 13.5 MHz.



411 Interpolation+LPF Frequency Characteristic

LPF for 422 color signals

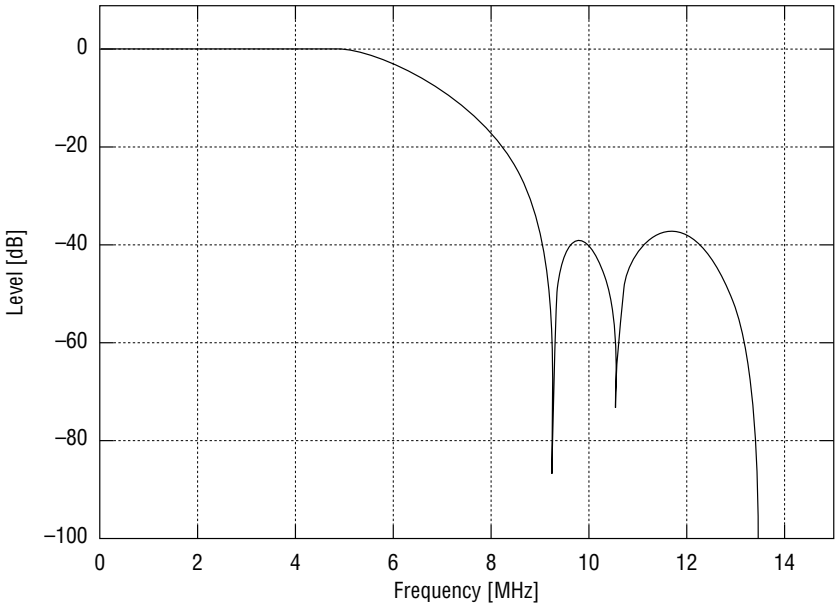
The following characteristics are when the clock frequency is 13.5 MHz.



422 Interpolation + LPF Frequency Characteristic

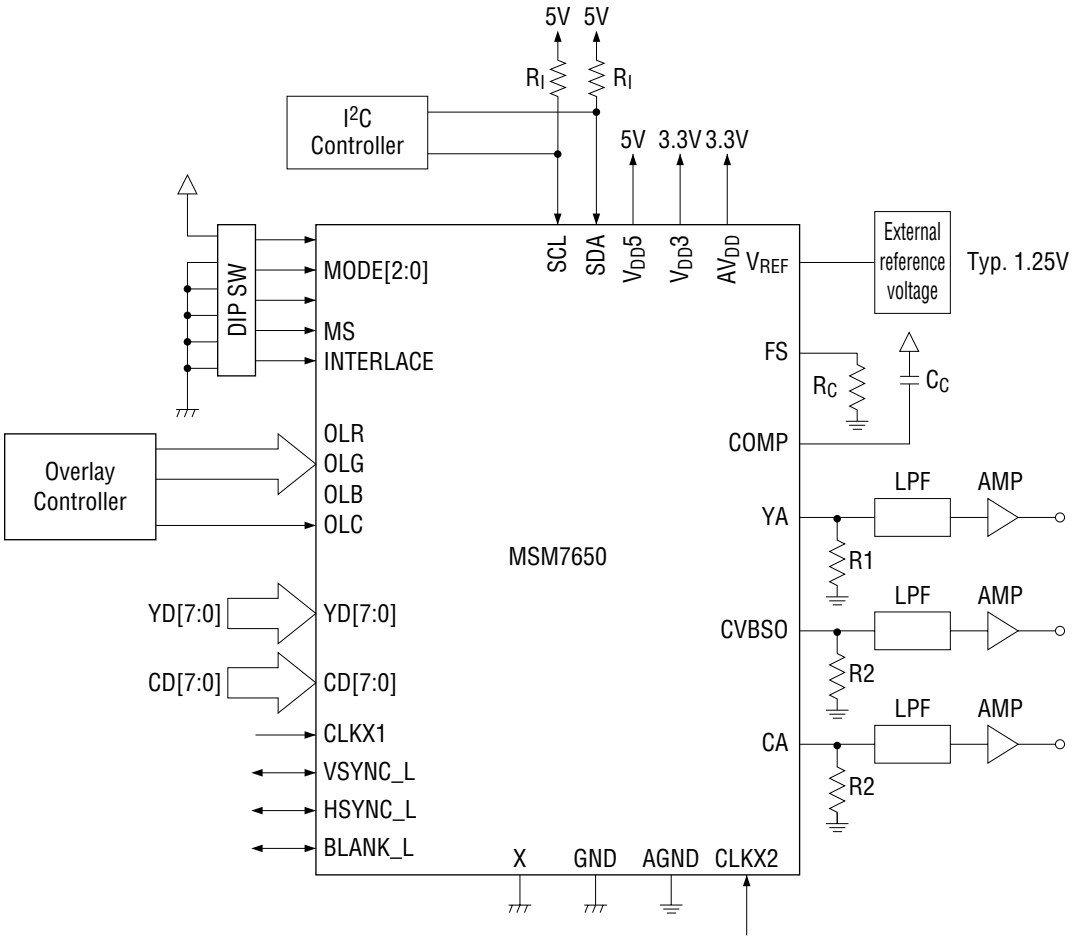
Up Sampling Filter

The following characteristics are when the clock frequency is 27 MHz.

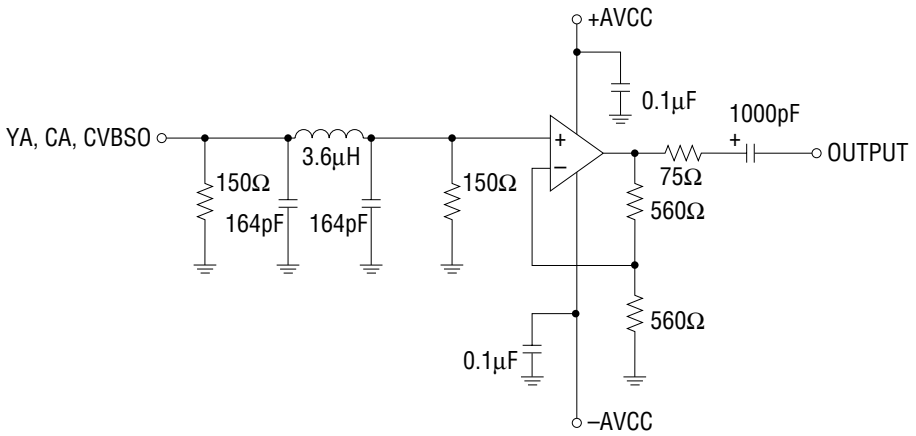


Up Sampling Filter Frequency Characteristic

APPLICATION CIRCUIT EXAMPLE



Recommended Analog Output Circuit



PACKAGE OUTLINES AND DIMENSIONS