OKI Semiconductor

This version: Aug. 1998

MSM7732

Audio CODEC

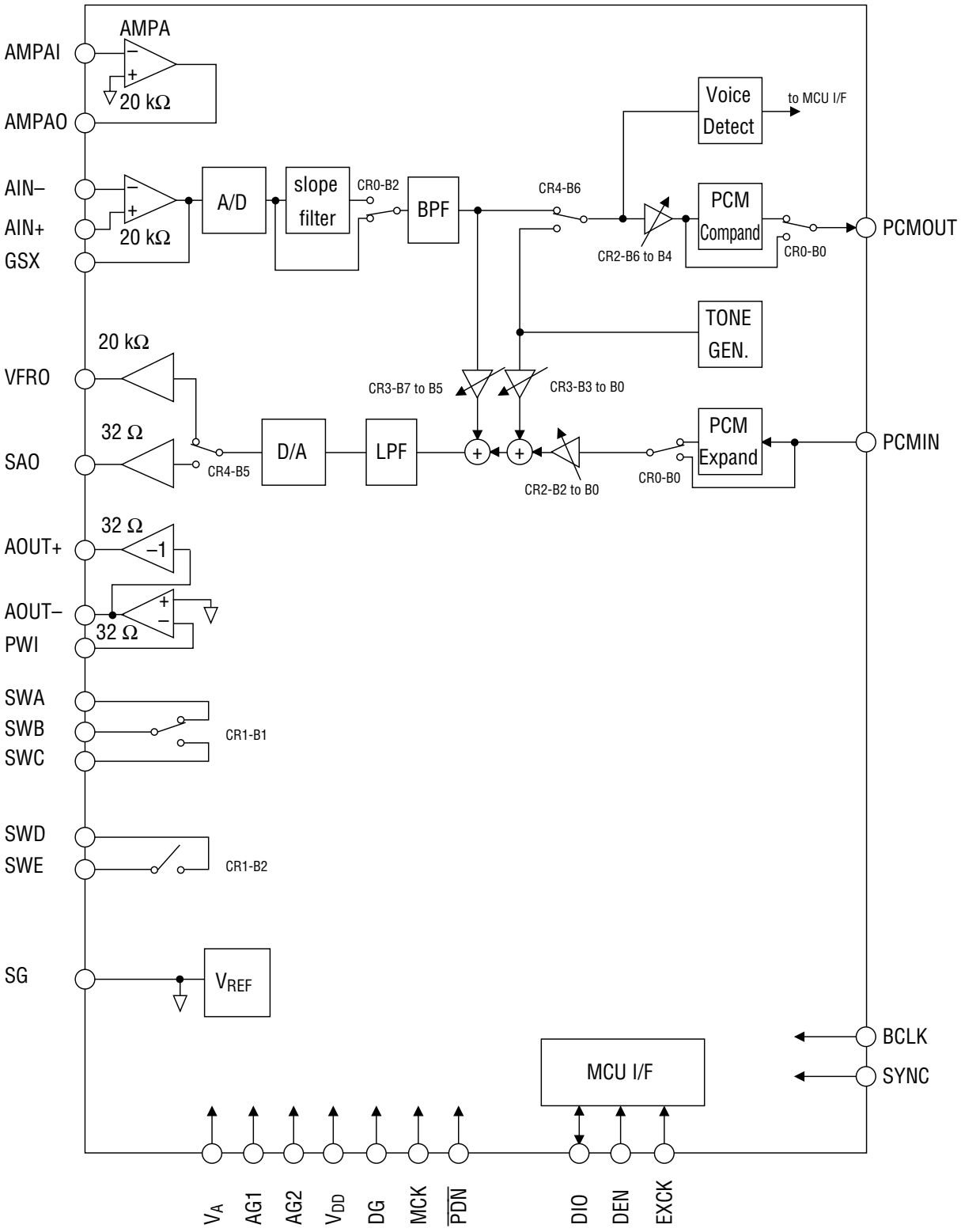
GENERAL DESCRIPTION

The MSM7732 is a single-channel full duplex CODEC LSI device which performs mutual transcoding between analog voice band signals ranging from 300 to 3400 Hz and the 64 kbps PCM serial data.
Provided with such functions as DTMF Tone generation, transmit/receive data gain control, and side-tone path, the MSM7732 is best suited for telephone terminals in digital wireless systems.

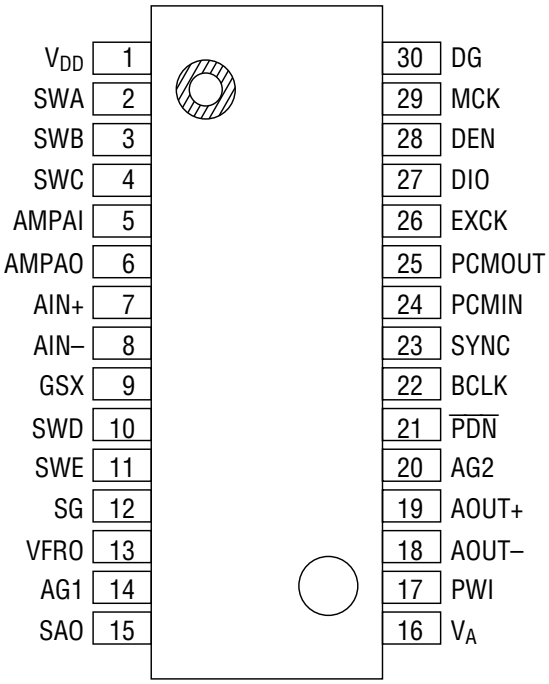
FEATURES

- Single 3 V power supply V_{DD}: 2.4 V to 3.3 V
- Coding format: PCM μ-law/PCM A-law/14-bit linear mode selectable
- PCM interface timing: Long frame synchronous timing/short frame synchronous timing
- Transmit/receive full-duplex operation
- Serial PCM transmission data rate: 64 kbps to 2048 kbps
- Low power consumption
  Operating mode: 18 mW max. (V_{DD} = 3.0 V)
  Power-down mode: 0.06 mW max. (V_{DD} = 3.0 V)
- Analog output stage:
  35 mW (differential type) amplifier output for driving receiver speaker:
  Capable of driving a 32 Ω load
  8.8 mW (single type) amplifier output for driving earphones speaker:
  Capable of driving a 32 Ω load
- Transmit/receive mute, transmit/receive programmable gain control
- Side tone path
- Built-in DTMF tone generator
- Transmit slope filter selectable
- Serial MCU interface control
- Package:
  30-pin plastic SSOP (SSOP30-P-56-0.65-K) (Product name: MSM7732MB)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



30-Pin Plastic SSOP

PIN DESCRIPTIONS

Pin	Symbol	Type	Description
1	V_{DD}	—	Power supply (3.0 V)
2	SWA	I/O	Analog switch A
3	SWB	I/O	Analog switch B
4	SWC	I/O	Analog switch C
5	AMPAI	I	Amplifier A inverting input
6	AMPAO	O	Amplifier A output
7	AIN+	I	Transmit side amplifier non-inverting input
8	AIN–	I	Transmit side amplifier inverting input
9	GSX	O	Transmit side amplifier output
10	SWD	I/O	Analog switch D
11	SWE	I/O	Analog switch E
12	SG	O	Analog signal ground (1.4 V)
13	VFRO	O	Receive side voice output
14	AG1	—	Analog ground 1 (0 V)
15	SAO	O	Receive side sounder amplifier output
16	V_A	—	Analog power supply (3.0 V)
17	PWI	I	Receive side voice amplifier input
18	AOUT–	O	Receive side voice amplifier output–
19	AOUT+	O	Receive side voice amplifier output+
20	AG2	—	Analog ground 2 (0 V)
21	$\overline{PDN}$	I	Power down control input
22	BCLK	I	PCM data shift clock input
23	SYNC	I	PCM data shift sync signal input
24	PCMIN	I	Receive side PCM signal input
25	PCMOUT	O	Transmit side PCM signal output
26	EXCK	I	Microcontroller interface data clock input
27	DIO	I/O	Microcontroller interface data input/output
28	DEN	I	Microcontroller interface data enable signal
29	MCK	I	Master clock input (2.048 MHz)
30	DG	—	Digital ground (0 V)

PIN FUNCTIONAL DISCRIPTION

AIN+, AIN–, GSX

Transmit analog inputs and the output for transmit gain adjustment.
AIN– connects to inverting input of the internal transmit amplifier. AIN+ connects to non-inverting input of the internal transmit amplifier. GSX connects to the internal transmit amplifier output. Refer to Figure 1 for gain adjustment.

VFRO, SAO, AOUT+, AOUT–, PWI

Receive analog outputs and the outputs and inputs for receive gain adjustment.
VFRO is the receive filter output for the voice signal. SAO is the receive filter output for an acoustic component of the sound tone. SAO can directly drive 32 Ω load. AOUT+ and AOUT– are differential analog signal outputs which can directly drive 32 Ω load. Refer to Figure 1. These outputs are in a high impedance state during power-down mode.

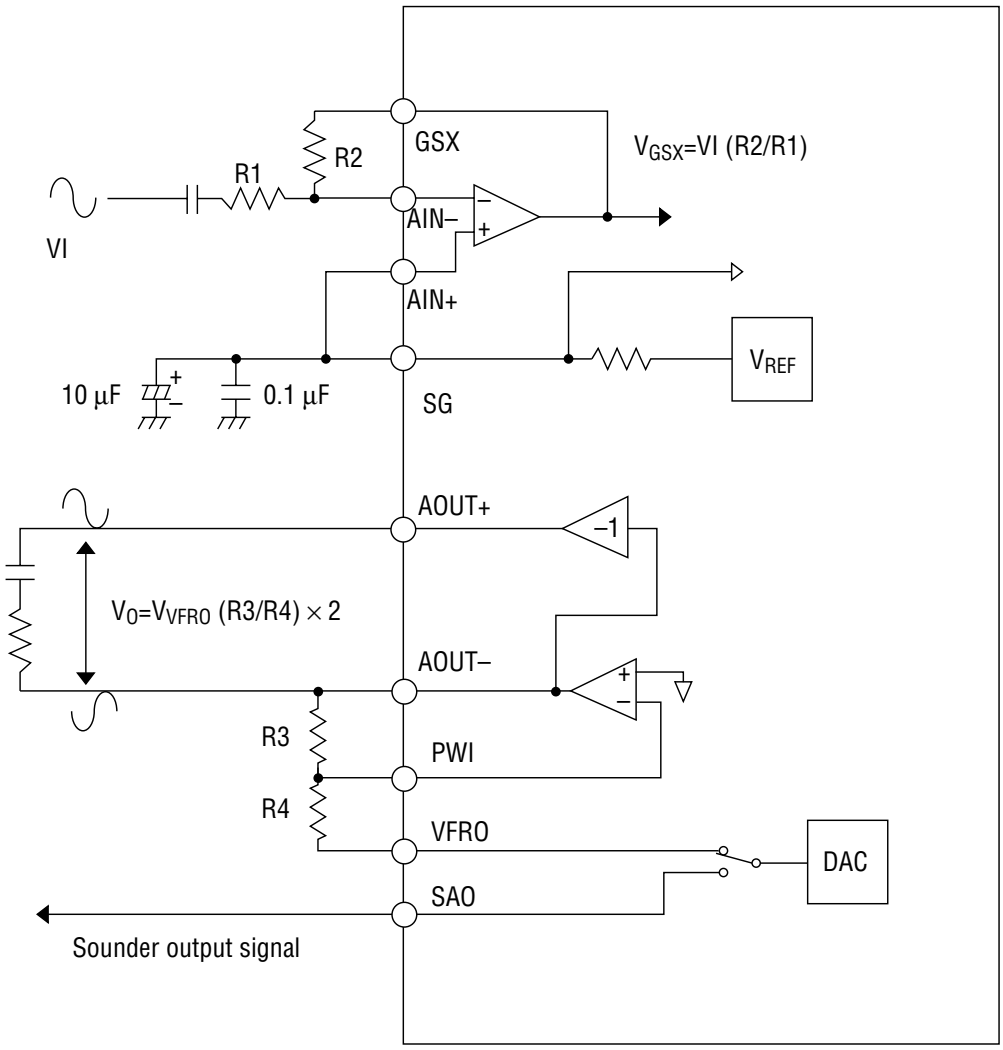


Figure 1 Analog Input/Output Interface

SG
Analog signal ground.
The output voltage of this pin is approximately 1.4 V. Put the bypass capacitors (10 µF in parallel with 0.1 µF ceramic type) between this pin and AG to get the specified noise characteristics. During power-down, this output voltage is 0 V. When using the SG pin, connect this device to an external buffer.

AMPAI, AMPAO
Used for amplifier-A. The pin AMPAI connects to inverting input of the amplifier-A, and the pin AMPAO connects to output of the amplifier-A.

SWA, SWB, SWC
Used for internal analog switch. The pin SWB connects to the pin SWA or the pin SWC. This is controlled by CR1-B1.

SWD, SWE
Used for internal analog switch. The pin SWD connects to the pin SWE or not. This is controlled by CR1-B2.

V_{DD}, V_A
+3 V power supply for analog. V_{DD} is the digital power supply. V_A is the analog power supply. Connect these device pins as close as possible on the board.

DG, AG1, AG2
Ground. DG is the digital system ground. AG1 and AG2 is the analog system ground. The DG pin must be kept as close as possible to AG1 and AG2 on the PCB.

$\overline{\text{PDN}}$
Power down and reset control input.
When set to logic "0" the system changes to the power down state and control register is reset. Since the power down mode is controlled by a logical OR with CR0-B5 of the control register, set CR0-B5 to logic "0" when using this pin. The reset pulse width must be 200 ns or more.

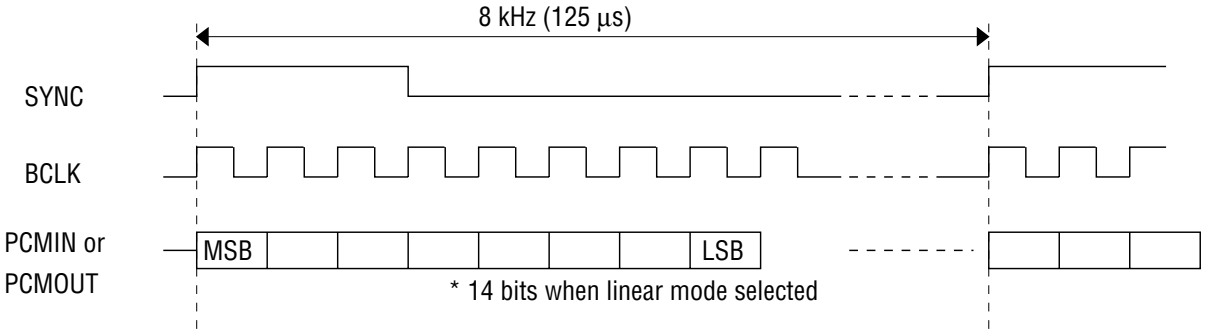
MCK
Master clock input.
The frequency must be 2.048 MHz. MCK can be a asynchronous with SYNC and BCLK.

BCLK
Shift clock input for the PCM data.
The frequency is set in the range of 64 kHz to 2048 kHz.

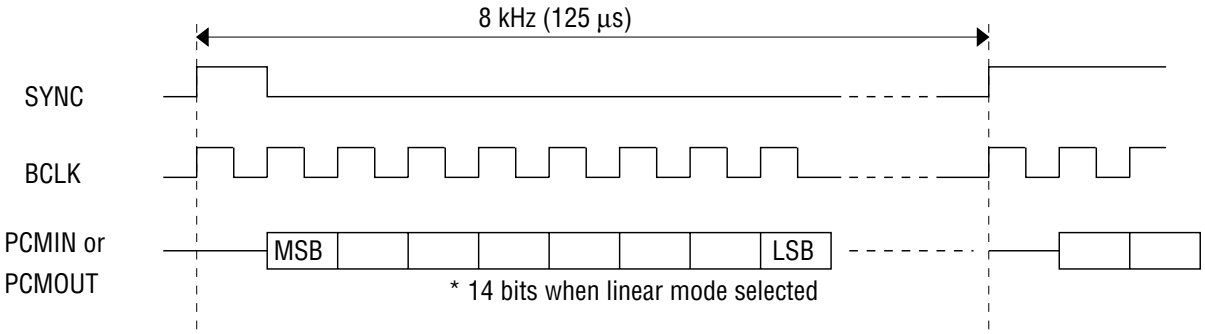
SYNC
Synchronous signal input for PCM data.
Synchronize this signal with BCLK signal. This signal is used to indicate the MSB of the PCM data stream.

PCMOUT
Transmit PCM data output.
This PCM output signal is output from MSB synchronously with the rising edge of BCLK and SYNC.
Refer to Figure 2.

PCMIN
Receive PCM data input.
This PCM input signal is shifted in on the falling edge of BCLK and is input from MSB.
Refer to Figure 2.



(a) Long frame synchronous interface

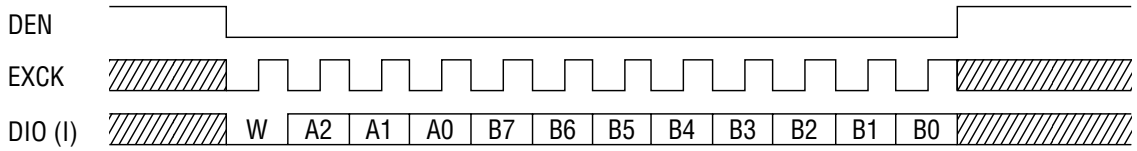


(b) Short frame synchronous interface

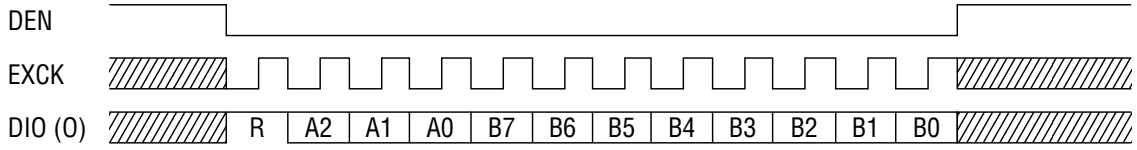
Figure 2 PCM Interface Basic Timing

DEN, EXCK, DIO

Serial control ports for microcontroller interface.
Reading and writing data is performed by an external CPU through these pins. Eight registers with eight bits are provided on the device.
DEN is the "Enable" control signal input, EXCK is the data shift clock input, DIO is the data input/output. Figure 3 shows the timing. Table 1 shows the register map.



(a) Write Timing



(b) Read Timing

Figure 3 Serial Control Port Access

Table 1

Register Name	Address A2	A1	A0	Description B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR0	0	0	0	A/μ SEL	PON AOUT	PDN ALL	PDN TX	PDN RX	SLP	SLP SEL	LNR	R/W
CR1	0	0	1	—	—	—	—	SHORT FRAME	SW DE	SW C/A	RX PAD	R/W
CR2	0	1	0	TX ON/OFF	TX GAIN2	TX GAIN1	TX GAIN0	RX ON/OFF	RX GAIN2	RX GAIN1	RX GAIN0	R/W
CR3	0	1	1	Side Tone GAIN2	Side Tone GAIN1	Side Tone GAIN0	TONE ON/OFF	TONE GAIN3	TONE GAIN2	TONE GAIN1	TONE GAIN0	R/W
CR4	1	0	0	DTMF/ Others SEL	TONE SEND	SAO/ VFRO	TONE4	TONE3	TONE2	TONE1	TONE0	R/W
CR5	1	0	1	—	—	—	—	—	—	—	—	—
CR6	1	1	0	VOX ON/OFF	ON LVL1	ON LVL0	—	—	—	—	—	R/W
CR7	1	1	1	VOX OUT	TX NOISE LVL1	TX NOISE LVL0	—	—	—	—	—	R

R/W: Read/Write enable R: Read only register

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	—	–0.3 to +5	V
Analog Input Voltage	V_{AIN}	—	–0.3 to V_{DD}+0.3	V
Digital Input Voltage	V_{DIN}	—	–0.3 to V_{DD}+0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{DD} = 2.4 to 3.3V, Ta = –40 °C to +85 °C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	Voltage must be fixed	2.4	3.0	3.3	V
Operating Temperature	Ta	—	–40	—	+85	°C
Input High Voltage	V_{IH}	To all digital input pins	0.45×V_{DD}	—	V_{DD}	V
Input Low Voltage	V_{IL}	To all digital input pins	0	—	0.16×V_{DD}	V
Digital Input Rise Time	t_{IR}	To all digital input pins	—	—	50	ns
Digital Input Fall Time	t_{IF}	To all digital input pins	—	—	50	ns
Digital Output Load	C_{DL}	To all digital output pins	—	—	100	pF
Bypass Capacitor for SG	C_{SG}	Between SG and AG	10+0.1	—	—	µF
Master Clock Frequency	F_{MCK}	MCK	–0.01%	2.048	+0.01%	MHz
Bit Clock Frequency	F_{BCLK1}	BCLK (A/µ-law)	64	—	2048	kHz
	F_{BCLK2}	BCLK (Linear)	128	—	2048	kHz
Synchronous Signal Frequency	F_{SYNC}	SYNC	—	8.0	—	kHz
Clock Duty Ratio	D_{CLK}	MCK, BCLK, EXCK	40	50	60	%
PCM Sync Pulse Setting Time	t_{BS}	BCLK↔SYNC See Fig. 5	100	—	—	ns
Synchronous Signal Width	t_{WS}	SYNC See Fig. 5	1BCLK	—	100	µs
PCM Setup Time	t_{DS}	See Fig. 5	100	—	—	ns
PCM Hold Time	t_{DH}	See Fig. 5	100	—	—	ns

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 2.4 V to 3.3 V, Ta = –40 °C to +85 °C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current	I_{DD1}	Operating mode (no signal, V_{DD} = 3.0 V)	0	6.0	11.0	mA
	I_{DD2}	Operating mode (no signal, V_{DD} = 3.0 V) Either AOUT+/AOUT– or SAO is active	0	9.0	20.0	mA
	I_{DD3}	Power-down mode (V_{DD} = 3.0 V, Ta = 25°C)	0	1.0	10.0	µA
Input Leakage Current	I_{IH}	$V_I = V_{DD}$	—	—	2.0	µA
	I_{IL}	V_I = 0V	—	—	0.5	µA
Output High Voltage	V_{OH}	I_{OH} = 0.4mA	0.5×V_{DD}	—	V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = –1.2mA	0	0.2	0.4	V
Input Capacitance	C_{IN}	—	—	5	—	pF

Analog Interface Characteristics

(V_{DD} = 2.4 V to 3.3 V, Ta = –40 °C to +85 °C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Resistance	R_{IN}	AMPAI, AIN+, AIN–, PWI	10	—	—	MΩ
Output Load Resistance	R_{L1}	AMPAO, GSX, VFRO	20	—	—	kΩ
	R_{L2}	SAO, AOUT+, AOUT–	32	—	—	Ω
Output Load Capacitance	C_L	Analog output pins	—	—	100	pF
Output Voltage Level (*1)	V_{O1}	AMPAO, GSX, VFRO (R_L = 20 kΩ) SAO (R_L = 32 Ω)	—	—	1.3	V_{PP}
	V_{O2}	AOUT+, AOUT– differential output (V_{DD} = 2.7 to 3.3 V, R_L = 32 Ω)	—	—	3.0	V_{PP}
Output Distortion	THD	AOUT+, AOUT–, SAO (V_{DD} = 2.7 to 3.3 V, R_L = 32 Ω)	—	—	1.0	%
Offset Voltage	V_{OF1}	AMPAO, GSX	–20	—	+20	mV
	V_{OF2}	VFRO, SAO, AOUT+, AOUT–	–100	—	+100	mV
SG Output Voltage	V_{SG}	SG	—	1.4	—	V
SG Output Impedance	R_{SG}	SG	—	40	80	kΩ
Switch Impedance	R_{SW}	All internal Analog switches	50	—	300	Ω

*1 –7.7 dBm (600 Ω) = 0 dBm0, +3.14 dBm0 = 1.3 V_{PP}

Digital Interface Characteristics

(V_{DD} = 2.4 V to 3.3 V, Ta = –40 °C to +85 °C)

Parameter	Symbol	Condition	Reference	Min.	Typ.	Max.	Unit
Digital Output Delay Time	t_{SDX}, t_{SDR}	1 LSTTL + 100 pF Pull-up resistor : 500 Ω	Fig. 5	0	—	200	ns
	t_{XD1}, t_{RD1}			0	—	200	ns
	t_{XD2}, t_{RD2}			0	—	200	ns
	t_{XD3}, t_{RD3}			0	—	200	ns
Serial Port I/O Setting Time	t_1	Cload = 50 pF	Fig. 6	50	—	—	ns
	t_2			50	—	—	ns
	t_3			50	—	—	ns
	t_4			50	—	—	ns
	t_5			100	—	—	ns
	t_6			50	—	—	ns
	t_7			50	—	—	ns
	t_8			0	—	100	ns
	t_9			50	—	—	ns
	t_{10}			50	—	—	ns
	t_{11}			0	—	50	ns
	t_{12}			200	—	—	ns
EXCK Clock Frequency	F_{ECK}	EXCK	—	—	—	10	MHz

AC Characteristics

(V_{DD} = 2.4 V to 3.3 V, Ta = –40 °C to +85 °C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
		Freq. (Hz)	Level (dBm0)				
Transmit Frequency Response	L_{OSS} T1	0 to 60	0	25	—	—	dB
	L_{OSS} T2	300 to 3000		–0.15	—	+0.20	dB
	L_{OSS} T3	1020		Reference			dB
	L_{OSS} T4	3300		–0.15	—	+0.20	dB
	L_{OSS} T5	3400		0	—	0.80	dB
	L_{OSS} T6	3968.75		13	—	—	dB
Receive Frequency Response	L_{OSS} R1	0 to 3000	0	–0.15	—	+0.20	dB
	L_{OSS} R2	1020		Reference			dB
	L_{OSS} R3	3300		–0.15	—	+0.20	dB
	L_{OSS} R4	3400		0	—	0.80	dB
	L_{OSS} R5	3968.75		13	—	—	dB
Transmit Signal to Distortion Ratio (*1)	SD T1	1020	3	35	—	—	dB
	SD T2		0	35	—	—	dB
	SD T3		–30	35	—	—	dB
	SD T4		–40	28	—	—	dB
	SD T5		–45	23	—	—	dB
Receive Signal to Distortion Ratio (*1)	SD R1	1020	3	35	—	—	dB
	SD R2		0	35	—	—	dB
	SD R3		–30	35	—	—	dB
	SD R4		–40	28	—	—	dB
	SD R5		–45	23	—	—	dB
Transmit Gain Tracking	GT T1	1020	3	–0.2	—	+0.2	dB
	GT T2		–10	Reference			dB
	GT T3		–40	–0.2	—	+0.2	dB
	GT T4		–50	–0.5	—	+0.5	dB
	GT T5		–55	–1.2	—	+1.2	dB
Receive Gain Tracking	GT R1	1020	3	–0.2	—	+0.2	dB
	GT R2		–10	Reference			dB
	GT R3		–40	–0.2	—	+0.2	dB
	GT R4		–50	–0.5	—	+0.5	dB
	GT R5		–55	–1.2	—	+1.2	dB
Idle Channel Noise (*1)	N_{IDLT}	—	AIN = SG	—	—	–68	dBm0p
	N_{IDLR}		(*2)	—	—	–72	dBm0p
Absolute Signal Amplitude (*3)	A_{VT}	1020 (GSX)	0	0.285	0.320	0.359	Vrms
	A_{VR}	1020 (VFRO)	0	0.285	0.320	0.359	Vrms
Power Supply Noise Rejection Ratio	P_{SRRT}	Noise Freq.: 0 to 50 kHz	—	30	—	—	dB
	P_{SRRR}	Noise LEVEL: 50mV_{PP}		30	—	—	dB

*1 P-message filter used

*2 PCMIN input code "11010101" (A-law)
"11111111" (μ-law)

*3 0.320 Vrms = 0 dBm0 = –7.7 dBm (600 Ω)

AC Characteristics (DTMF and Other Tones)

(V_{DD} = 2.4 V to 3.3 V, Ta = –40 °C to +85 °C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Frequency Difference	D_{FT}	DTMF tones, Other various tones		–1.5	—	+1.5	%
Original (Reference) Tones Signal Output Level (*4)	V_{TL}	Transmit side tone (Gain setting 0 dB)	DTMF (low group)	–18	–16	–14	dBm0
	V_{TH}		DTMF (high group), other tones	–16	–14	–12	dBm0
	V_{RL}	Receive side tone (Gain setting –6 dB)	DTMF (low group)	–10	–8	–6	dBm0
	V_{RH}		DTMF (high group), other tones	–8	–6	–4	dBm0
Relative Level of DTMF Tones	R_{DTMF}	V_{TH}/V_{TL}, V_{RH}/V_{RL}		1	2	3	dB

*4 Not including programmable gain set values

AC Characteristics (Gain Settings)

(V_{DD} = 2.4 V to 3.3 V, Ta = –40 °C to +85 °C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmit/Receive Gain Setting Accuracy	D_G	For all gain set values	–1	0	+1	dB

AC Characteristics (Voice/Silence Detect Function)

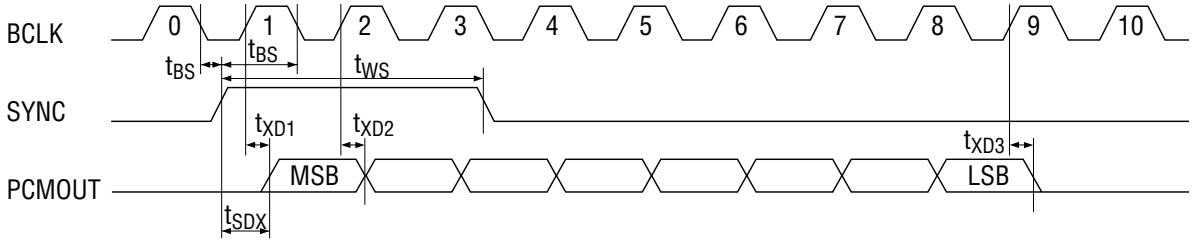
(V_{DD} = 2.4 V to 3.3 V, Ta = –40 °C to +85 °C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Voice/Silence Detection Time	T_{VON}	Silence→voice	Voice/silence differential: 10 dB	—	10 (*5)	—	ms
	T_{VOF}	Voice→silence		140	160	180	ms
Voice/Silence Detection Level Accuracy	D_{VX}	For detection level set values by CR6-B6, B5		–2.5	0	+2.5	dB

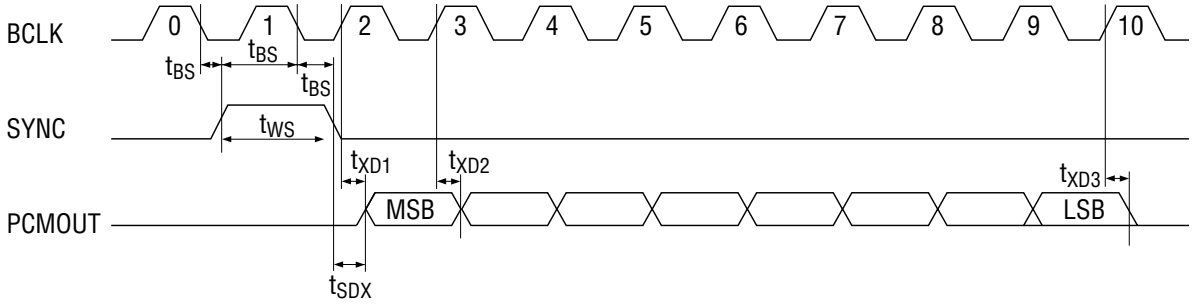
*5 When 1000 Hz single tone is input

TIMING DIAGRAM

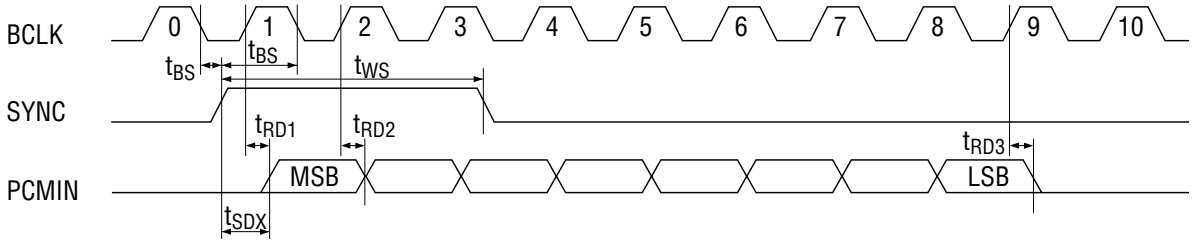
Transmit Side PCM Timing (Long Frame Synchronous Interface)



Transmit Side PCM Timing (Short Frame SYnchronous Interface)



Receive Side PCM Timing (Long Frame Synchronous Interface)



Receive Side PCM Timing (Short Frame Synchronous Interface)

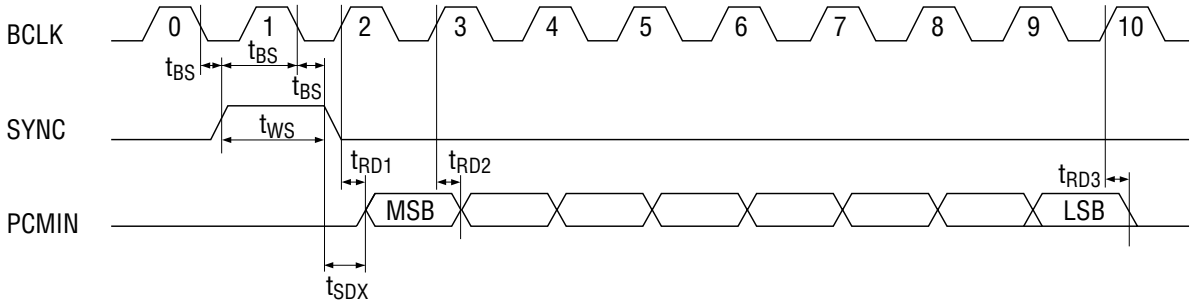


Figure 5 PCM Interface Timing

Serial Port Timing for Microcntroller Interface

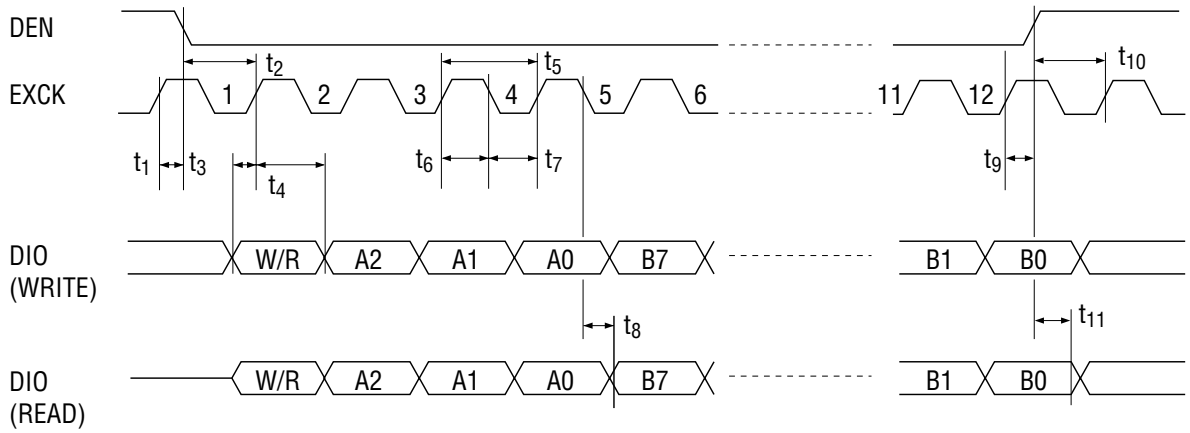


Figure 6 Serial Control Port Interface

FUNCTIONAL DESCRIPTION

Control Registers

(1) CR0 (basic operating mode 1)

	B7	B6	B5	B4	B3	B2	B1	B0
CR0	A/μ SEL	PON AOUT	PDN ALL	PDN TX	PDN RX	SLP	SLP SEL	LNR
Initial Value	0	0	0	0	0	0	0	0

Note: Initial values are the values set when reset is activated by the $\overline{\text{PDN}}$ pin.

B7 ..... PCM companding law select; 0/μ-law, 1/A-law
B6 ..... Power on control for op-amps (AOUT+, AOUT–); 0/Power off, 1/Power on
B5 ..... Power down (entire system); 0/Power on, 1/Power down
ORed with the inverted $\overline{\text{PDN}}$ signal. When using this data, set pin $\overline{\text{PDN}}$ at "1" level.
B4 ..... Power down (Transmit and AMPA); 0/Power on, 1/Power down
B3 ..... Power down (Receive only); 0/Power on, 1/Power down
B2 ..... Slope Filter enable; 0/Slope Filter disable, 1/Slope Filter enable
B1 ..... Slope Filter's frequency response select; 0/CASE1, 1/CASE2 Refer to Figure 4.
B0 ..... PCM interface linear mode select;
0/PCM data,
1/14-bit linear mode (2's complement)

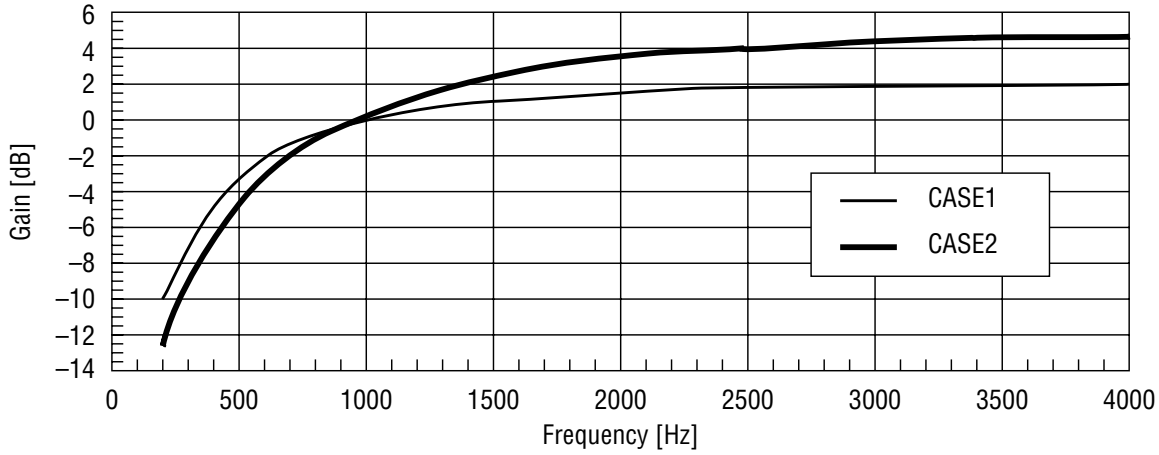


Figure 4 Frequency Response of Slope Filter

(2) CR1 (Basic operating mode 2)

	B7	B6	B5	B4	B3	B2	B1	B0
CR1	—	—	—	—	SHORT FRAME	SW DE	SW C/A	RX PAD
Initial Value	0	0	0	0	0	0	0	0

B7, B6, B5, B4 ..... Not used.
B3 ..... Short Frame Synchronous interface select;
0/Long Frame Synchronous interface, 1/Short Frame Synchronous interface
Refer to Figure 2.
B2 ..... Analog switch control; 0/The SWD and SWE pins are in a high impedance state.
1/The SWD pin is internally connected to the SWE pin.
B1 ..... Analog switch control; 0/The SWB pin is internally connected to the SWA pin.
1/The SWB pin is internally connected to the SWC pin.
The unconnected pins go into a high impedance state.
B0 ..... Receive side PAD; 0/No pad
1/A pad of 12 dB loss is inserted in the receive side voice path.

(3) CR2 (Transmit/receive gain adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CR2	TX ON/OFF	TX GAIN2	TX GAIN1	TX GAIN0	RX ON/OFF	RX GAIN2	RX GAIN1	RX GAIN0
Initial Value	0	0	1	1	0	0	1	1

B7 ..... Transmit side PCM signal ON/OFF 0/ON, 1/OFF
B6, B5, B4 .... Transmit side signal gain adjustment, refer to Table 2.
B3 ..... Receive side PCM signal ON/OFF 0/ON, 1/OFF
B2, B1, B0 .... Receive side signal gain adjustment, refer to Table 2.

Table 2 Transmit/Receive Gain Settings

B6	B5	B4	Transmit Side Gain	B2	B1	B0	Receive Side Gain
0	0	0	–6 dB	0	0	0	–12 dB
0	0	1	–4 dB	0	0	1	–9 dB
0	1	0	–2 dB	0	1	0	–6 dB
0	1	1	0 dB	0	1	1	–3 dB
1	0	0	+2 dB	1	0	0	0 dB
1	0	1	+4 dB	1	0	1	+3 dB
1	1	0	+6 dB	1	1	0	+6 dB
1	1	1	+8 dB	1	1	1	+9 dB

The above gain settings table shows the transmit/receive voice signal gain settings and the transmit side gain settings for DTMF tones and other tones. Tone signal transmission is enabled by CR4-B6, and the gain setting is set to the levels shown below.

DTMF tones (low group): .....–16 dBm0
DTMF tones (high group) and other tones: .....–14 dBm0

For example, if the transmit gain set value is set to +8 dB (B6, B5, B4) = (1, 1, 1), then the following tones appear at the PCMOUT pin.

DTMF tones (low group): .....–8 dBm0
DTMF tones (high group) and other tones: .....–6 dBm0

(4) CR3 (Side tone and tone generator gain setting)

	B7	B6	B5	B4	B3	B2	B1	B0
CR3	Side Tone GAIN2	Side Tone GAIN1	Side Tone GAIN0	TONE ON/OFF	TONE GAIN3	TONE GAIN2	TONE GAIN1	TONE GAIN0
Initial Value	0	0	0	0	0	0	0	0

B7, B6, B5..... Side tone path gain setting, refer to Table 3.
B4..... Tone generator ON/OFF 0/OFF, 1/ON
B3, B2, B1, B0 .. Tone generator gain adjustment for receive side, refer to Table 4

Table 3 Side Tone Gain Settings

B7	B5	B4	Side Tone Path Gain
0	0	0	OFF
0	0	1	–15 dB
0	1	0	–13 dB
0	1	1	–11 dB
1	0	0	–9 dB
1	0	1	–7 dB
1	1	0	–5 dB
1	1	1	–3 dB

Table 4 Receive Side Tone Generator Gain Settings

B3	B2	B1	B0	Tone Generator Gain	B3	B2	B1	B0	Tone Generator Gain
0	0	0	0	OFF	1	0	0	0	–20 dB
0	0	0	1	–34 dB	1	0	0	1	–18 dB
0	0	1	0	–32 dB	1	0	1	0	–16 dB
0	0	1	1	–30 dB	1	0	1	1	–14 dB
0	1	0	0	–28 dB	1	1	0	0	–12 dB
0	1	0	1	–26 dB	1	1	0	1	–10 dB
0	1	1	0	–24 dB	1	1	1	0	–8 dB
0	1	1	1	–22 dB	1	1	1	1	–6 dB

The receive side tone generator gain settings shown in Table 4 are set with the following levels as a reference.

DTMF tones (low group): .....–2 dBm0
DTMF tones (high group) and other tones: 0 dBm0

For example, if the tone generator gain set value is set to –6 dB (B3, B2, B1, B0) = (1, 1, 1, 1), then tones at the following levels apppear at the SAO or VFRO pin.

DTMF tones (low group): .....–8 dBm0
DTMF tones (high group) and other tones: .....–6 dBm0

(5) CR4 (Tone generator operating mode and frequency select)

	B7	B6	B5	B4	B3	B2	B1	B0
CR4	DTMF/ Others SEL	TONE SEND	SAO/ VFRO	TONE4	TONE3	TONE2	TONE1	TONE0
Initial Value	0	0	0	0	0	0	0	0

B7 ..... DTMF or other tones select; 0/Others, 1/DTMF
B6 ..... Tone transmit enable (Transmit side); 0/Voice signal (transmit), 1/Tone transmit
B5 ..... Tone output pin select (Receive side); 0/VFRO, 1/SAO
B4, B3, B2, B1, B0 ..... Tone frequency setting; refer to Table 5.

Table 5 Tone Generator Frequency Settings

(a) B7 = 1 (DTMF tone)

B4	B3	B2	B1	B0	Frequency	B4	B3	B2	B1	B0	Frequency
*	0	0	0	0	697 Hz + 1209 Hz	*	1	0	0	0	852 Hz + 1209 Hz
*	0	0	0	1	697 Hz + 1336 Hz	*	1	0	0	1	852 Hz + 1336 Hz
*	0	0	1	0	697 Hz + 1477 Hz	*	1	0	1	0	852 Hz + 1477 Hz
*	0	0	1	1	697 Hz + 1633 Hz	*	1	0	1	1	852 Hz + 1633 Hz
*	0	1	0	0	770 Hz + 1209 Hz	*	1	1	0	0	941 Hz + 1209 Hz
*	0	1	0	1	770 Hz + 1336 Hz	*	1	1	0	1	941 Hz + 1336 Hz
*	0	1	1	0	770 Hz + 1477 Hz	*	1	1	1	0	941 Hz + 1477 Hz
*	0	1	1	1	770 Hz + 1633 Hz	*	1	1	1	1	941 Hz + 1633 Hz

*Don't Care

(b) B7 = 0 (Other tones)

B4	B3	B2	B1	B0	Frequency	B4	B3	B2	B1	B0	Frequency
0	0	0	0	0	2730 Hz/2560 Hz 8 Hz wamb.	1	0	0	0	0	1200 Hz
0	0	0	0	1	2000 Hz/2667 Hz 8 Hz wamb.	1	0	0	0	1	1300 Hz
0	0	0	1	0	1000 Hz/1333 Hz 8 Hz wamb.	1	0	0	1	0	—
0	0	0	1	1	—	1	0	0	1	1	1477 Hz
0	0	1	0	0	—	1	0	1	0	0	1633 Hz
0	0	1	0	1	—	1	0	1	0	1	2000 Hz
0	0	1	1	0	—	1	0	1	1	0	2100 Hz
0	0	1	1	1	—	1	0	1	1	1	—
0	1	0	0	0	—	1	1	0	0	0	2400 Hz
0	1	0	0	1	400 Hz	1	1	0	0	1	—
0	1	0	1	0	440 Hz	1	1	0	1	0	2500 Hz
0	1	0	1	1	480 Hz	1	1	0	1	1	—
0	1	1	0	0	—	1	1	1	0	0	—
0	1	1	0	1	667 Hz	1	1	1	0	1	2700 Hz
0	1	1	1	0	800 Hz	1	1	1	1	0	—
0	1	1	1	1	1000 Hz	1	1	1	1	1	3000 Hz

(6) CR5 (Not used)

	B7	B6	B5	B4	B3	B2	B1	B0
CR5	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0

B7-B0 ..... Not used

(7) CR6 (Voice/silence detect function control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR6	VOX ON/OFF	ON LVL1	ON LVL0	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0

B7 ..... Voice/silence detect function ON/OFF; 0/OFF, 1/ON
B6, B5 ..... Voice detector level setting (when 1000 Hz single tone is input);
(0, 0): –20 dBm0 (0, 1): –26 dBm0 (1, 0): –32 dBm0 (1, 1): –38 dBm0
B4, B3, B2, B1, B0 ..... Not used. When writing data, write "0".

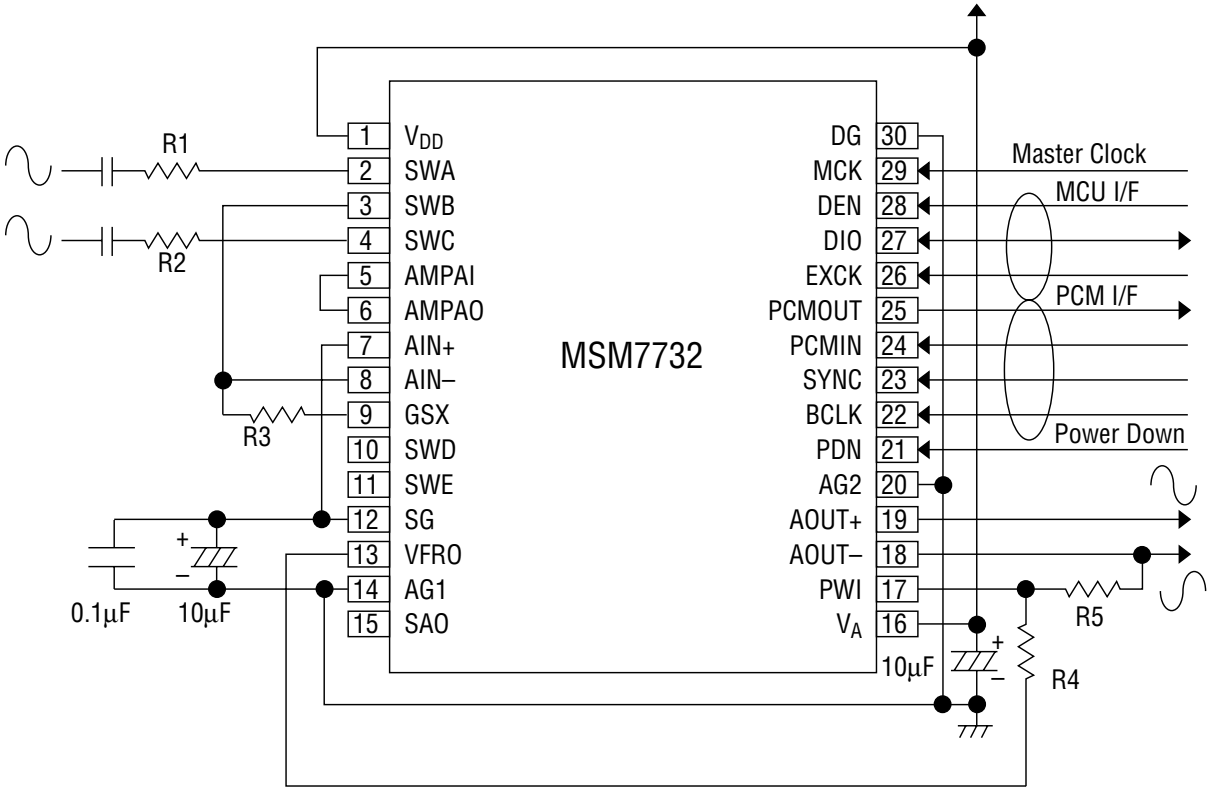
(8) CR7 (Detect register, read only)

	B7	B6	B5	B4	B3	B2	B1	B0
CR7	VOX OUT	TX Noise Level1	TX Noise Level0	—	—	—	—	—
Initial Value	0	0	0	*	*	*	*	*

*For IC testing

B7 ..... Transmit side voice/silence detection; 0/silence, 1/voice detect
B6, B5 Transmit side silence detect level (indicator);
(0, 0): Below –50 dBm0 (0, 1): –40 to –50 dBm0
(1, 0): –30 to –40 dBm0 (1, 1): Above –30 dBm0
Note: These outputs are enabled only when VOX (CR6-B7) = "1".
B4, B3, B2, B1, B0 ..... Not used

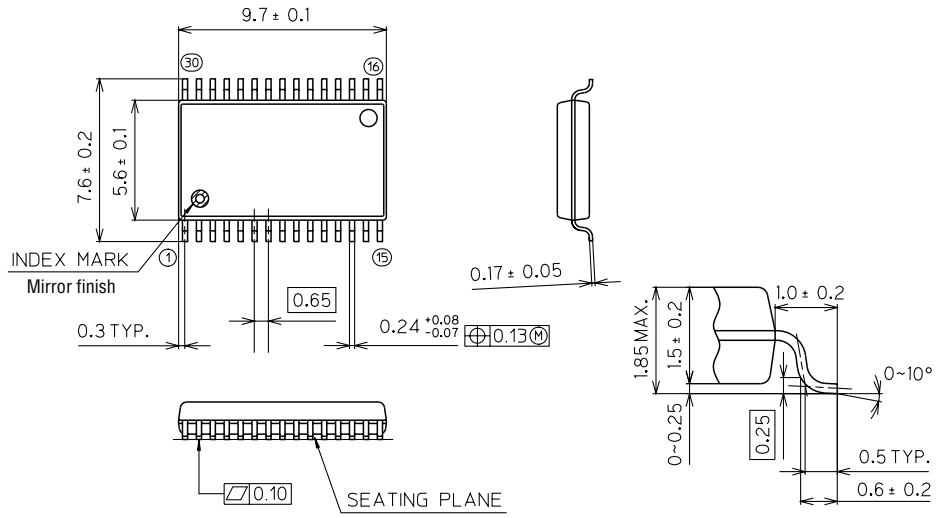
APPLICATION CIRCUIT



PACKAGE DIMENSIONS

(Unit : mm)

SSOP30-P-56-0.65-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 µm or more
Package weight (g)	0.19 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).