OKI Semiconductor

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MSM7708-02

Serial Register Interface ADPCM CODEC for Telephone Recording

GENERAL DESCRIPTION

The MSM7708-02 is a CMOS IC developed for applying to PHS (Personal Handyphone System). This device provides a CODEC function which performs transcoding between the voice band analog signal and 32 kbps ADPCM data. It also provides a serial register interface function for telephone call recording.
Provided with such functions as DTMF tone and several kinds of tone generation, transmit/receive data mute and gain control, side-tone pass, and voice/silence detection, the MSM7708-02 is best suited for PHS handsets.

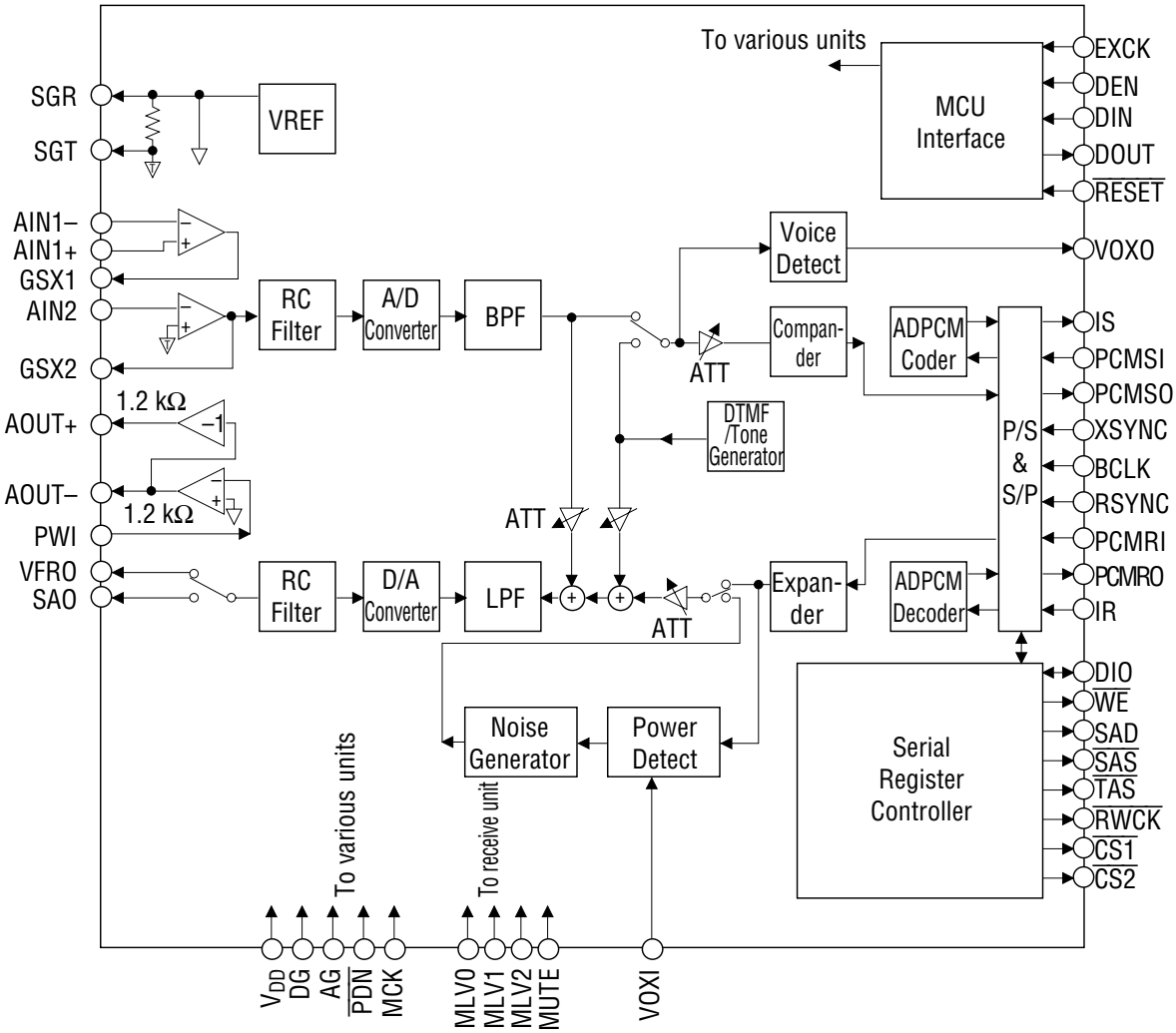
FEATURES

- Single 3 V power supply operation (V_{DD}: 2.7 V to 3.6 V)
- Low power consumption
  When system is operating: 6 mA typ.
  When powered down: 0.02 mA typ.

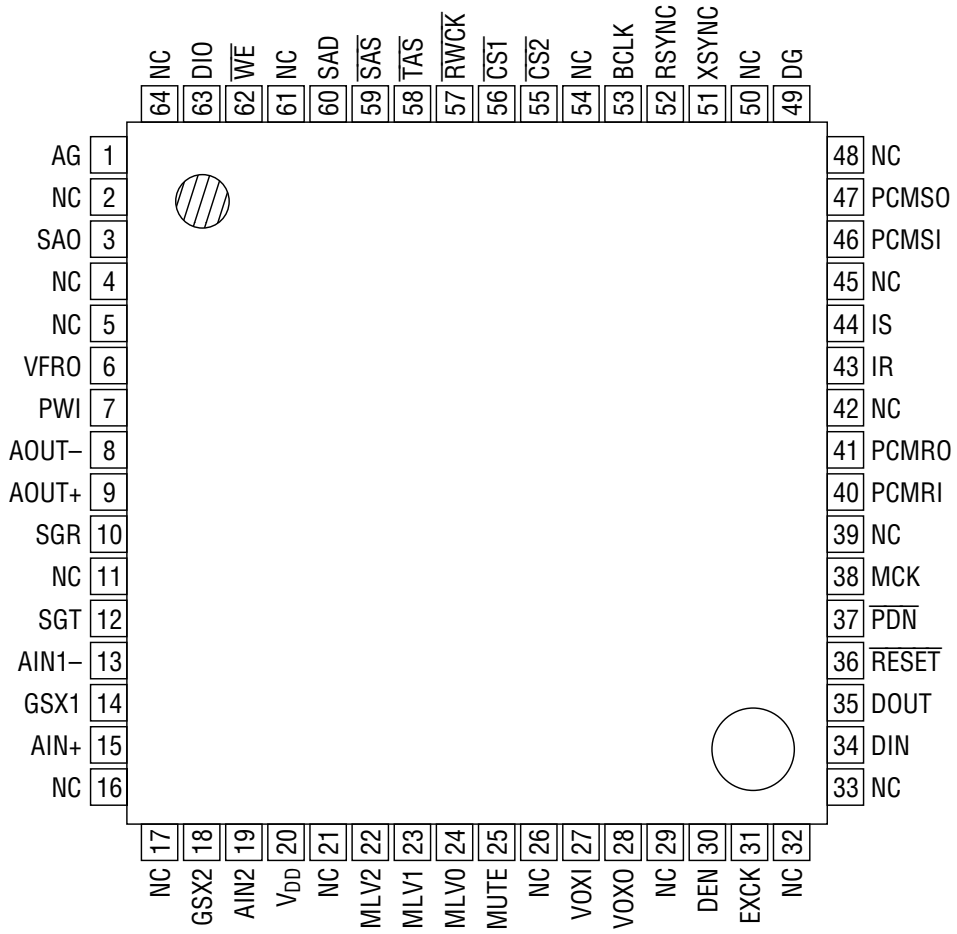
(ADPCM CODEC)
- ADPCM: ITU-T Recommendations G.721 (32 kbps)
- Transmit/receive full duplex capability
- PCM interface code format: μ-law or A-law selectable
- Serial ADPCM and PCM transmission rate: 64 kbps to 2,048 kbps
- Transmit/receive mute function; transmit/receive programmable gain setting
- Side tone generator (8-step level adjustment)
- Built-in DTMF tone, ringing tone, and various tone generators
- Built-in VOX function

(Serial Register Interface)
- Interface for a serial register: 1 Mb (MSM63V89C), 4 Mb (MSM6684), 8 Mb (MSM6685)
- Interface for a serial voice ROM: 1 Mb (MSM6595A), 2 Mb (MSM6596A), 3 Mb (MSM6597A)
- Maximum recording time: 32 s (1 Mb), 128 s (4 Mb), 256 s (8 Mb)
- Maximum recording channels: 32 ch
- Playback data transmit/receive selectable
- Package:
  64-pin plastic TQFP (TQFP64-P-1010-0.50-K) (Product name : MSM7708-02TS-K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



64-Pin Plastic TQFP

NC : No connect pin

PIN DESCRIPTIONS

Pin	Symbol	Type	Description
1	AG	I	Analog ground
2	NC	—	No connection
3	SAO	O	Receive side sounder amplifier output
4	NC	—	No connection
5	NC	—	No connection
6	VFRO	O	Receive side voice output
7	PWI	I	Receive side voice amplifier input
8	AOUT–	O	Receive side voice amplifier output (–)
9	AOUT+	O	Receive side voice amplifier output (+)
10	SGR	O	Receive side analog signal ground
11	NC	—	No connection
12	SGT	O	Transmit side analog signal ground
13	AIN1–	I	Transmit side amplifier 1 inverting input
14	GSX1	O	Transmit side amplifier 1 output
15	AIN1+	I	Transmit side amplifier 1 non-inverting input
16	NC	—	No connection
17	NC	—	No connection
18	GSX2	O	Transmit side amplifier 2 output
19	AIN2	I	Transmit side amplifier 2 inverting input
20	V_{DD}	I	Power supply
21	NC	—	No connection
22	MLV2	I	Receive side voice path mute level set
23	MLV1	I	Receive side voice path mute level set
24	MLV0	I	Receive side voice path mute level set
25	MUTE	I	Receive side voice path mute enable signal input
26	NC	—	No connection
27	VOXI	I	Receive side voice/silence detect function input
28	VOXO	O	Transmit side voice/silence detect function output
29	NC	—	No connection
30	DEN	I	Enable signal input for control register
31	EXCK	I	Clock signal input for control register
32	NC	—	No connection
33	NC	—	No connection
34	DIN	I	Address and data input for control
35	DOUT	O	Data output for control register
36	$\overline{\text{RESET}}$	I	$\overline{\text{RESET}}$ control input for control register
37	$\overline{\text{PDN}}$	I	Power down control input
38	MCK	I	Master clock input
39	NC	—	No connection
40	PCMRI	I	Receive side PCM signal input

PIN DESCRIPTIONS (Continued)

Pin	Symbol	Type	Description
41	PCMRO	O	Receive side PCM signal output
42	NC	—	No connection
43	IR	I	Receive side ADPCM signal input
44	IS	O	Transmit side ADPCM signal output
45	NC	—	No connection
46	PCMSI	I	Transmit side PCM signal input
47	PCMSO	O	Transmit side PCM signal output
48	NC	—	No connection
49	DG	I	Digital ground
50	NC	—	No connection
51	XSYNC	I	Transmit side PCM and ADPCM data sync signal input
52	RSYNC	I	Receive side PCM and ADPCM data sync signal input
53	BCLK	I	PCM and ADPCM data shift clock input
54	NC	—	No connection
55	$\overline{CS2}$	O	Voice ROM chip select output
56	$\overline{CS1}$	O	Serial register chip select output
57	$\overline{RWCK}$	O	Serial register data clock output
58	$\overline{TAS}$	O	Serial register transfer address-strobe output
59	$\overline{SAS}$	O	Serial register address-strobe output
60	SAD	O	Serial register address data output
61	NC	—	No connection
62	$\overline{WE}$	O	Serial register write enable output
63	DIO	I/O	Serial register data input/output
64	NC	—	No connection

PIN AND FUNCTIONAL DESCRIPTIONS

AIN1+, AIN1-, AIN2, GSX1, GSX2

The transmit analog input and the output for transmit gain adjustment.
The pin AIN1– (AIN2) connects to inverting input of the internal transmit amplifier, and the pin AIN1+ connects to non-inverting input of the internal transmit amplifier. The pin GSX1 (GSX2) connects to output of the internal transmit amplifier. Gain adjustment should be referred to Fig. 1.

VFRO, AOUT+, AOUT-, PWI

Used for the receive analog output and the output for receive gain adjustment.
VFRO is an output of the receive filter. AOUT+ and AOUT– are differential analog signal outputs which can directly drive Z_L = 350 Ω+120 nF or the 1.2 kΩ load. Gain adjustment should be referred to Fig. 1.
These outputs are in high impedance state during power down.

SAO

Differential analog output for a sounder.
Variable tones including "Audio sound", "DTMF tone", "S tone", "F tone", and "R tone", and telephone call signals can be output to either VFRO pin or SAO pin by CR0 - B1 of the control register. These output pins are in the high impedance state during power down.

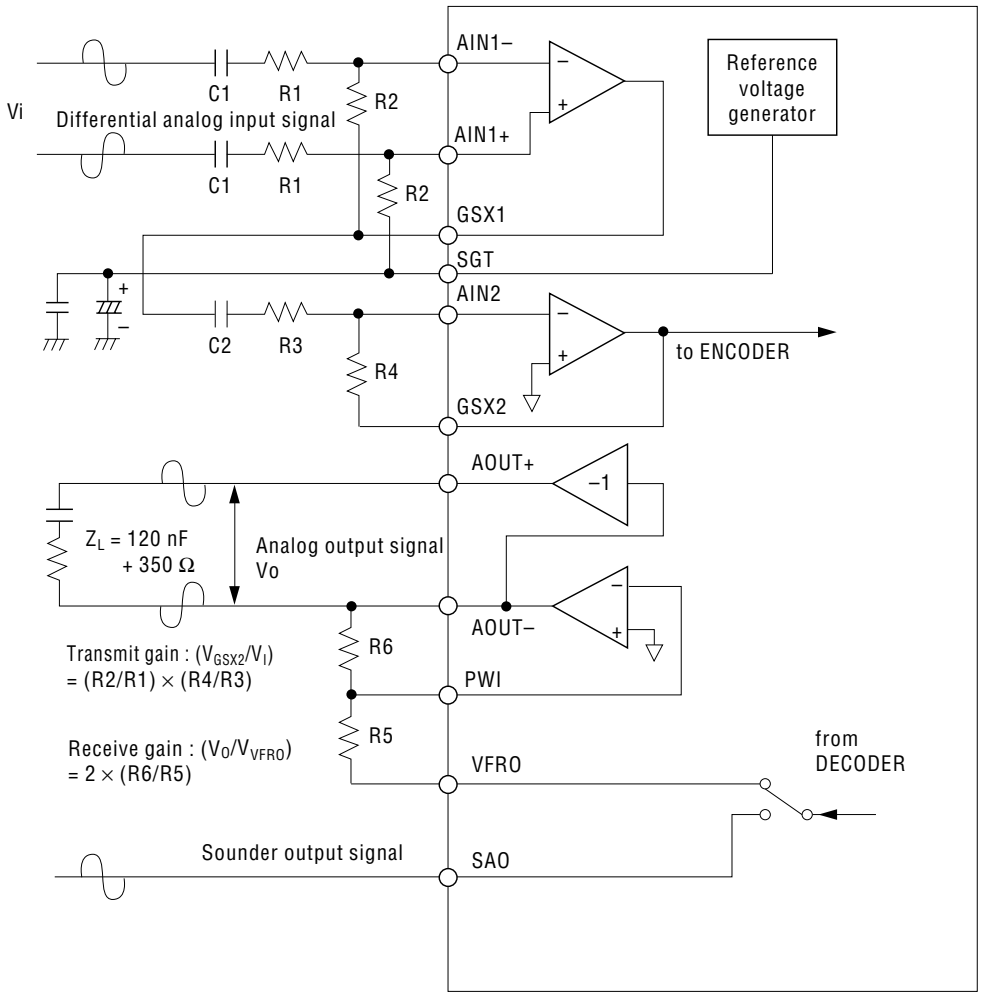


Figure 1 Analog Interface

SGT, SGR

Outputs of the analog signal ground voltage.
SGT outputs the analog signal ground voltage of the transmit system, and SGR outputs the same for the receive system. The output voltage value is approximately 1.4 V. Connect bypass 10 µF and 0.1 µF (ceramic type) capacitors between these pins and the AG pin. To reduce the response time of the receiver power on, it is recommended to apply 1 µF and 0.1 µF bypass capacitors. During power down, the output changes to 0 V.

V_{DD}

Power supply.

DG, AG

Ground.
DG is the digital system ground. AG is the analog system ground. Since DG and AG are separated in the device, connect them as close as possible on the circuit board.

$\overline{PDN}$

Power down control input.
When set to a digital "0", the system changes to the power down state and control register is not reset. Since the power down mode is controlled by CRC0 - B5 of the control register ORed with the signal from the $\overline{PDN}$ pin, set CRC0 - B5 to digital "0" when using this pin.

$\overline{RESET}$

Reset control input of the CODEC control register.
When set to digital "0," each bit of the control register is reset and the internal circuit changes to the power down state. During normal operation, set this pin to digital "1".

MCK

Master clock input.
The clock frequency is 19.2 MHz. MCK can be asynchronous with XSYNC, RSYNC, and BCLK.

PCMSO

Transmit PCM data output.
This PCM output signal is output from MSB synchronously with the rising edge of BCLK and XSYNC.

PCMSI

Transmit PCM data input.
This signal is converted to the ADPCM data. The PCM signal is shifted in on the falling edge of BCLK. Normally, this pin is connected to PCMSO.

PCMRO

Receive PCM data output.
This PCM signal is the output signal after ADPCM decoder processing. This signal is serially output from MSB synchronously with the rising edge of BCLK and RSYNC.

PCMRI

Receive PCM data input.
This PCM input signal is shifted in on the rising edge of BCLK and is input from MSB. Normally, this pin is connected to PCMRO.

IS

Transmit ADPCM signal output.
This signal is the output signal after ADPCM encoding, and is serially output from MSB synchronously with the rising edge of BCLK and XSYNC. This pin is an open drain output which remains in a high impedence state during power down. It requires pull-up resistor.

IR

Receive ADPCM signal input.
This input signal is shifted in serially on the rising edge of BCLK synchronously with RSYNC and is input from MSB.

BCLK

Shift clock input for the PCM data (PCMSO, PCMSI, PCMRO, PCMRI) and the ADPCM data(IS, IR) . The frequency is in the 64 kHz to 2048 kHz range.

XSYNC

8 kHz synchronous signal input for transmit PCM and ADPCM data.
This signal should be synchronized with BCLK. XSYNC is used for indicating the MSB of the transmit serial PCM and ADPCM data stream.

RSYNC

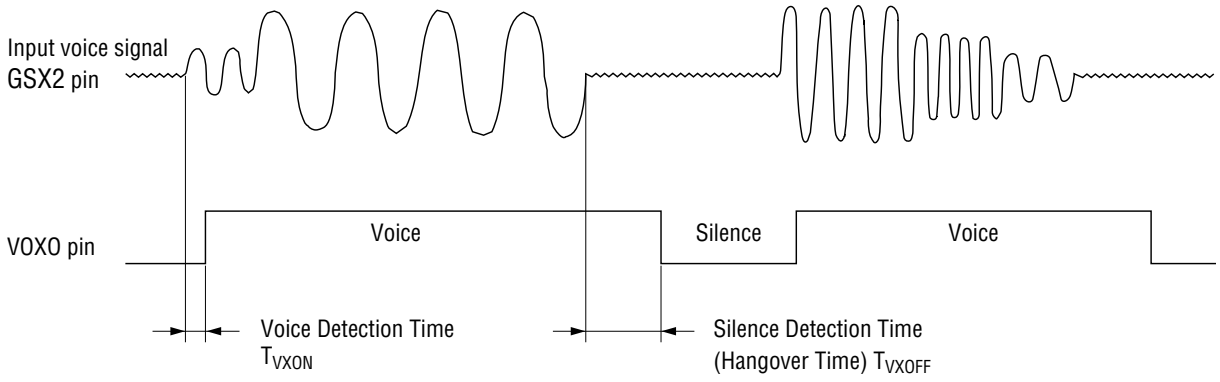
8 kHz synchronous signal input for receive PCM and ADPCM data.
This signal should be synchronized with BCLK signal. RSYNC is used for indicating the MSB of the receive serial PCM and ADPCM data stream.

VOXO

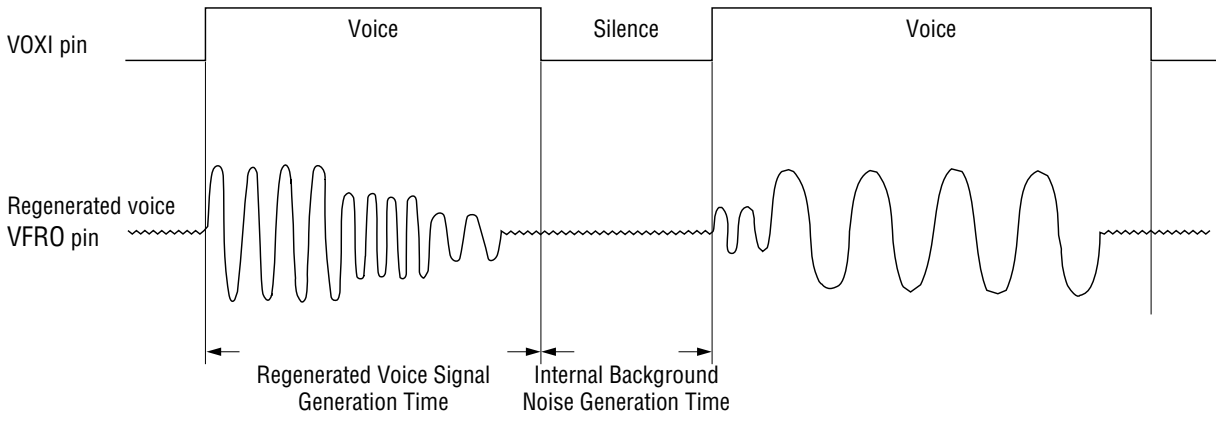
Transmit side voice/silence detect signal output.
This output is valid when CR6 - B7 is set to "1". VOXO shows the presence or absence of the transmit voice signal by detecting the signal. "1" and "0" set to this pin correspond to the presence and the absence, respectively. This result also appears at the register data CR7 - B7. The signal detect threshold is set by the control register CR6 - B6, B5. When control register CR0 - B6 is set to "1" and VOXI input is "1" during the voice detection (VOXO = "1"), receive signal is automatically suppressed by 6 dB.

VOXI

Receive side voice/silence detect signal input.
This output is valid when CR6 - B7 is set to "1". A "1" level at VOXI indicates the presence of voice signal, in which case the decoder block processes normal receive signal and the voice signal appears at analog output pins. A "0" level indicates the absence of voice signal, in which case the background noise generated in this device is transferred to the analog output pins. The background noise amplitude is set by the control register CR6 - B1, B0. Since this signal is ORed with the register CR6 - B3, set the control register CR6 - B3 to "0" when using this pin. When control register CR0 - B6 is set to "1" and VOXI input is "1" during the voice detection (VOXO = "1") receive signal is automatically suppressed by 6 dB.



(a) Transmission Side Voice/Silence Detect Function Timing Diagram



(b) Receive Side Voice/Silence Detect Function Timing Diagram

Note: The VOXO and VOXI pin functions are enabled when CR6 - B7 is set to "1".

Figure 2 Voice/Silence Detect Function

DEN, EXCK, DIN, DOUT

Serial control ports for MCU interface.
Reading and writing data is performed by an external CPU through these pins. 14-byte control registers (CR0 - 13) are provided in this device.
DEN is the "Enable" control signal input, EXCK is the data shift clock input, DIN is the address and data input, and DOUT is the data output.
Input/output timing is shown in Fig. 3.

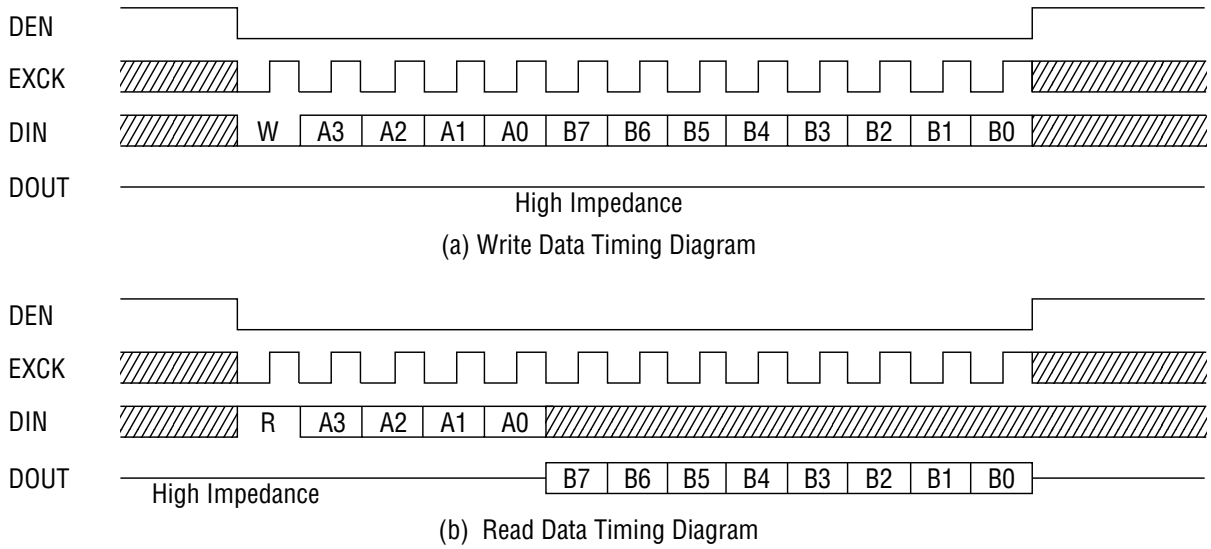


Figure 3 MCU Interface Input/Output Timing

MUTE

This pin is used to enable the receive side voice path mute level.
To set the mute level, set this pin to "1".

MLV0, MLV1, MLV2

This pin is used to set the receive side voice path mute level.
For the control method, refer to the control register description (CR1). Since these signals are ORed with CR1 - B2, B1, and B0 internally, set these register data to "0" when using this pin.

The register map is shown in Table 1.

Table 1 Control Register (CR0 to CR13) Map

Register Name	Address				Data Description								R/W
	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	
CR0	0	0	0	0	A/μ SEL	Spprs ON	PDN ALL	PDN TX	PDN RX	SA,VF OUT	SAO/ VFRO	AOUT PON	R/W
CR1	0	0	0	1	TX MUTE	RX ON/OFF	ADPCM RESET	TX ON/OFF	RX MUTE	RX MLV2	RX MLV1	RX MLV0	R/W
CR2	0	0	1	0	TX GAIN3	TX GAIN2	TX GAIN1	TX GAIN0	RX GAIN3	RX GAIN2	RX GAIN1	RX GAIN0	R/W
CR3	0	0	1	1	Side Tone GAIN2	Side Tone GAIN1	Side Tone GAIN0	TONE ON/OFF	TONE GAIN3	TONE GAIN2	TONE GAIN1	TONE GAIN0	R/W
CR4	0	1	0	0	DTMF/ OTHERS SEL	TONE SEND	TONE5	TONE4	TONE3	TONE2	TONE1	TONE0	R/W
CR5	0	1	0	1	SEND/ REC	ROW/ SR	4M8M/ 1M	—	—	—	CMD1	CMD0	R/W
CR6	0	1	1	0	VOX ON/OFF	ON LVL1	ON LVL0	OFF TIME	VOX IN	RX NOISE LEVEL SEL	RX NOISE LVL1	RX NOISE LVL0	R/W
CR7	0	1	1	1	VOX OUT	SILENCE LVL1	SILENCE LVL0	—	—	—	BUSY	RPM	R
CR8	1	0	0	0	ST0	ST1	ST2	ST3	ST4	ST5	ST6	ST7	R/W
CR9	1	0	0	1	ST8	ST9	ST10	ST11	ST12	—	—	—	R/W
CR10	1	0	1	0	SPY0	SPY1	SPY2	SPY3	SPY4	SPY5	SPY6	SPY7	R/W
CR11	1	0	1	1	SP0	SP1	SP2	SP3	SP4	SP5	SP6	SP7	R/W
CR12	1	1	0	0	SP8	SP9	SP10	SP11	SP12	—	—	—	R/W
CR13	1	1	0	1	CH0	CH1	CH2	CH3	CH4	—	ADRD	ADWT	R/W

Note : Details are explained in the Control Register Description.

R/W: Both read and write are supported R: Read-only register

(Register Controllers)

DIO

This I/O pin is used to output the write data and fetch the read data.
Connect this pin to the DIN and DOUT pins of the serial register and to the DOUT pin of the serial voice ROM.

$\overline{WE}$

This output pin is used to select the read or write mode.
Connect this pin to the $\overline{WE}$ pin of the serial register.

SAD

This pin is used to output the read/write start address data.
Connect this pin to the SAD pin of the serial register and to the SADX pin of the serial voice ROM.

$\overline{SAS}$

This clock output pin is used to write the serial address.
Connect this pin to the $\overline{SAS}$ pin of the serial register and to the $\overline{SASX}$ and $\overline{SASY}$ pins of the serial voice ROM.

$\overline{TAS}$

This output pin is used to set the serial address input from the SAD pin into the address counter inside the serial register/serial voice ROM.
Connect this pin to the $\overline{TAS}$ pin of the serial register/serial voice ROM.

$\overline{RWCK}$

This clock output pin is used to write or read data to or from the serial register.
Connect this pin to the $\overline{RWCK}$ pin of the serial register and to the $\overline{RDCK}$ pin of the serial voice ROM.

$\overline{CS1}$, $\overline{CS2}$

$\overline{CS1}$ and $\overline{CS2}$ are chip select pins.
Connect $\overline{CS1}$ to the $\overline{CS}$ pin of the serial register, and $\overline{CS2}$ to the $\overline{CS}$ pin of the serial voice ROM.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	—	–0.3 to +5	V
Analog Input Voltage	V_{AIN}	—	–0.3 to V_{DD} + 0.3	V
Digital Input Voltage	V_{DIN}	—	–0.3 to V_{DD} + 0.3	V
Operating Temperature	T_{op}	—	–25 to +70	°C
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	Voltage must be fixed		2.7	—	3.6	V
High Level Input Voltage	V_{IH}	To all digital input pins		0.45 × V_{DD}	—	V_{DD}	V
Low Level Input Voltage	V_{IL}	To all digital input pins		0	—	0.16 × V_{DD}	V
Digital Input Rise Time	t_{Ir}	To all digital input pins		—	—	50	ns
Digital Input Fall Time	t_{If}	To all digital input pins		—	—	50	ns
Digital Output Load	R_{DL}	IS (Pull-up resistor)		500	—	—	Ω
	C_{DL}	To all digital output pins		—	—	100	pF
Bypass Capacitor for SG	C_{SGT}	Between SGT and AG		10 + 0.1	—	—	µF
	C_{SGR}	Between SGR and AG		1	—	—	µF
Master Clock Frequency	F_{MCK}	MCK		–0.01%	19.2	0.01%	MHz
Master Clock Duty Ratio	D_{MCK}	MCK		40	50	60	%
Bit Clock Frequency	F_{BCK}	BCLK		64	—	2048	kHz
Synchronous Signal Frequency	F_{SYNC}	XSYNC, RSYNC		—	8.0	—	kHz
Clock Duty Ratio	D_{CK}	BCLK, EXCK		40	50	60	%
Transmit Sync Pulse Setting Time	t_{XS}, t_{SX}	BCLK↔XSYNC	Fig.4	100	—	—	ns
Receive Sync Pulse Setting Time	t_{RS}, t_{SR}	BCLK↔RSYNC		100	—	—	ns
Synchronous Signal Width	t_{WS}	XSYNC, RSYNC		1 BCLK	—	100	µs
PCM, ADPCM Setup Time	t_{DS}	—		100	—	—	ns
PCM, ADPCM Hold Time	t_{DH}	—		100	—	—	ns

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current	I_{DD1}	When operating (When no signal, and V_{DD} = 3.0 V)	—	6.0	11.0	mA
	I_{DD2}	When powered down (When V_{DD} = 3.0 V)	—	0.02	0.1	mA
Input Leakage Current	I_{IH}	$V_I = V_{DD}$	—	—	2.0	µA
	I_{IL}	V_I = 0 V	—	—	0.5	µA
High Level Output Voltage	V_{OH1}	I_{OH} = 0.4 mA	0.5 × V_{DD}	—	V_{DD}	V
	V_{OH2}	I_{OH} = 1 µA	0.8 × V_{DD}	—	V_{DD}	V
Low Level Output Voltage	V_{OL}	I_{OL} = –1.2 mA (IS pin is pulled up with 500 Ω resistor)	0	0.2	0.4	V
Output Leakage Current	I_O	IS pin	—	—	10	µA
Input Capacitance	C_{IN}	—	—	5	—	pF

Analog Interface Characteristics

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Resistance	R_{IN}	AIN+, AIN–, AIN2, PWI	10	—	—	MΩ
Output Resistance Load	R_{L1}	GSX1, GSX2, VFRO, SAO	20	—	—	kΩ
	R_{L2}	AOUT+, AOUT–	1.2	—	—	kΩ
Output Capacitance Load	C_{L1}	GSX1, GSX2, VFRO, SAO	—	—	100	pF
	C_{L2}	AOUT+, AOUT–	—	—	100	pF
Output Voltage Level (*1)	V_{O1}	GSX1, GSX2, VFRO, SAO(R_L = 20 kΩ)	—	—	1.3	V_{PP}
	V_{O2}	AOUT+, AOUT– (R_L = 1.2 kΩ)	—	—	1.3	V_{PP}
Offset Voltage	V_{OF1}	VFRO, SAO	–100	—	+100	mV
	V_{OF2}	GSX1, GSX2, AOUT+, AOUT–	–20	—	+20	mV
SGT, SGR Output Voltage	V_{SG}	SGT, SGR	—	1.4	—	V
SGT Output Impedance	R_{SGT}	SGT	—	40	80	kΩ
SGR Output Impedance	R_{SGR}	SGR	—	8	12	kΩ

*1 –7.7 dBm (600 Ω) = 0 dBm0, +3.14 dBm0 = 1.30 V_{PP}.

Digital Interface Characteristics

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition	Reference	Min.	Typ.	Max.	Unit
Digital Output Delay Time PCM, ADPCM Interface	t_{SDX}, t_{SDR}	1 LSTTL + 100 pF pull-up resistor : 500 Ω Items in parenthesis mean C load = 10 pF, and the pull-up resistor ≤ 2 kΩ	Fig. 4	0	—	200 (100)	ns
	t_{XD1}, t_{RD1}			0	—	200 (100)	ns
	t_{XD2}, t_{RD2}			0	—	200 (100)	ns
	t_{XD3}, t_{RD3}			0	—	200 (100)	ns
Serial Port Digital I/O Timing Characteristics	t_1	C load = 50 pF	Fig. 5	50	—	—	ns
	t_2			50	—	—	ns
	t_3			50	—	—	ns
	t_4			50	—	—	ns
	t_5			100	—	—	ns
	t_6			50	—	—	ns
	t_7			50	—	—	ns
	t_8			0	—	100	ns
	t_9			50	—	—	ns
	t_{10}			50	—	—	ns
	t_{11}			0	—	50	ns
	t_{12}			200	—	—	ns
EXCK Clock Frequency	F_{EXCK}	EXCK	—	—	—	10	MHz

Serial Register Interface Characteristics

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition	Reference	Min.	Typ.	Max.	Unit
Control Register Data Input	t_{CRW}	Write	Fig. 6	—	—	200	ns
	t_{CRR}	Reset		—	—	200	ns
Busy Bit	t_{BSR}	Setup time		—	—	10	µs
	t_{BSH}	Valid time		—	—	450	µs
RPM Bit	t_{RPR}	Setup time		—	—	15	µs
	t_{RPF}	Hold time after stop command		—	—	140	µs

AC Characteristics

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
		Frequency (Hz)	Level dBm0				
Transmit Frequency Response	L_{OSS} T1	0 to 60	0	25	—	—	dB
	L_{OSS} T2	300 to 3000		–0.15	—	+0.20	dB
	L_{OSS} T3	1020		Reference			dB
	L_{OSS} T4	3300		–0.15	—	+0.80	dB
	L_{OSS} T5	3400		0	—	0.80	dB
	L_{OSS} T6	3968.75		13	—	—	dB
Receive Frequency Response	L_{OSS} R1	0 to 3000	0	–0.15	—	+0.20	dB
	L_{OSS} R2	1020		Reference			dB
	L_{OSS} R3	3300		–0.15	—	+0.80	dB
	L_{OSS} R4	3400		0	—	0.80	dB
	L_{OSS} R5	3968.75		13	—	—	dB
Transmit Signal to Distortion Ratio (*1)	SD T1	1020	3	35	—	—	dB
	SD T2		0	35	—	—	dB
	SD T3		–30	35	—	—	dB
	SD T4		–40	28	—	—	dB
	SD T5		–45	23	—	—	dB
Receive Signal to Distortion Ratio (*1)	SD R1	1020	3	35	—	—	dB
	SD R2		0	35	—	—	dB
	SD R3		–30	35	—	—	dB
	SD R4		–40	28	—	—	dB
	SD R5		–45	23	—	—	dB
Transmit Gain Tracking	GT T1	1020	3	–0.2	—	+0.2	dB
	GT T2		–10	Reference			dB
	GT T3		–40	–0.2	—	+0.2	dB
	GT T4		–50	–0.5	—	+0.5	dB
	GT T5		–55	–1.2	—	+1.2	dB
Receive Gain Tracking	GT R1	1020	3	–0.2	—	+0.2	dB
	GT R2		–10	Reference			dB
	GT R3		–40	–0.2	—	+0.2	dB
	GT R4		–50	–0.5	—	+0.5	dB
	GT R5		–55	–1.2	—	+1.2	dB

*1 P-message filter used

AC Characteristics (Continued)

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition			Min.	Typ.	Max.	Unit
		Frequency (Hz)	Level dBm0	Other				
Idle Channel Noise (*1)	N_{IDLT}	—	AIN = SG	—	—	—	–68 (–75.7)	dBm0p (dBmp)
	N_{IDLR}	—	(*2)	—	—	—	–72 (–79.7)	
Absolute Level (*3)	A_{VT}	1020	0	GSX2	0.285	0.320	0.359	Vrms
	A_{VR}			VFRO	0.285	0.320	0.359	Vrms
Power Supply Noise Rejection Ratio	P_{SRRT}	Noise frequency: 0 to 50 kHz	Noise level: 50 mVpp	—	30	—	—	dB
	P_{SRRR}				30	—	—	dB

*1 P-message filter used
*2 PCMRI input: "11010101" (A-law), "11111111" (μ-law)
*3 0.320 Vrms = 0 dBm0 = –7.7 dBm (600 Ω)
ADPCM unit characteristics are fully compliant with ITU-T Recommendation G.721.

AC Characteristics (DTMF and Other Tones)

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Frequency Deviation	D_{FT1}	DTMF tones, Other various tones		–1.5	—	+1.5	%
	D_{FT2}	Tone scale		–1.0	—	+1.0	%
Tone Reference Output Level (*1)	V_{TL}	Transmit side tone	DTMF (low group)	–18	–16	–14	dBm0
	V_{TH}	(Gain setting 0 dB)	DTMF (high group), other	–16	–14	–12	dBm0
	V_{RL}	Receive side tone	DTMF (low group)	–10	–8	–6	dBm0
	V_{RH}	(Gain setting –6 dB)	DTMF (high group), other	–8	–6	–4	dBm0
DTMF Tone Level Relative Value	R_{DTMF}	V_{TH}/V_{TL}, V_{RH}/V_{RL}		1	2	3	dB

*1. Not including programmable gain set values

AC Characteristics (Gain Settings)

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmit/Receive Gain Setting Accuracy	D_G	For all gain set values	–1	0	+1	dB

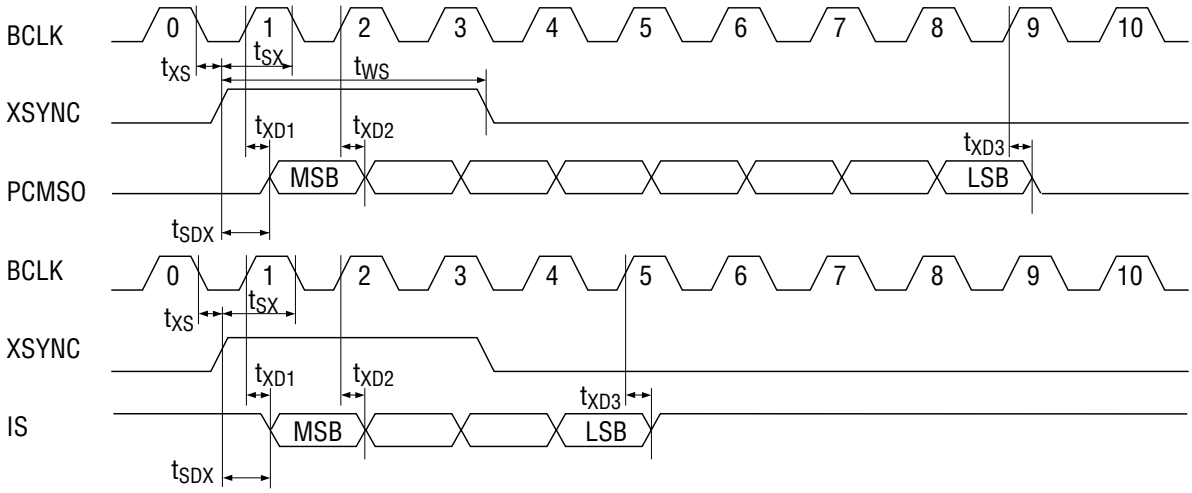
AC Characteristics (Voice/Silence Detect Function)

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Transmit Voice/Silence Detection Time	T_{VXON}	Silence→voice	VOXO pin: See Fig. 2	—	5	—	ms
	T_{VXOF}	Voice→silence	Voice/silence differential: 10 dB	140/300	160/320	180/340	ms
Transmit Voice Detection Level Accuracy	D_{VX}	For detection level set values by CRM6 - B6, B5		–2.5	0	2.5	dB

TIMING DIAGRAM

Transmit Side PCM, ADPCM Timing



Receive Side PCM, ADPCM Timing

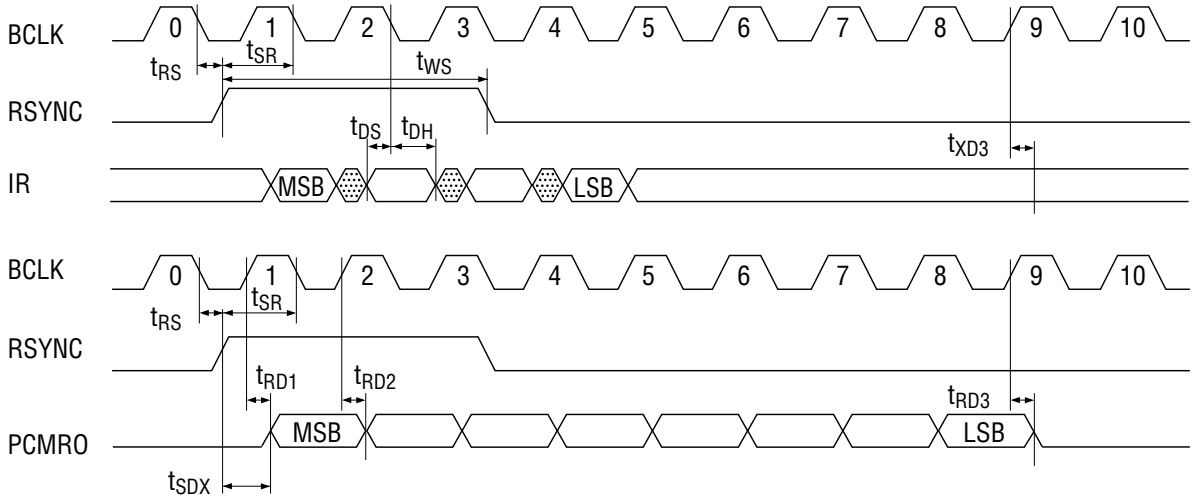


Figure 4 PCM, ADPCM Interface

Serial Port Timing for Microcontroller Interface

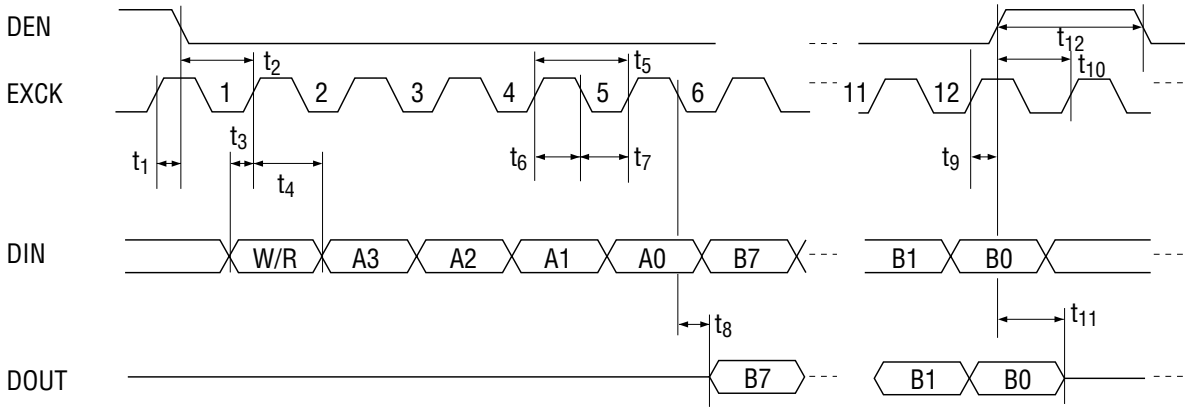
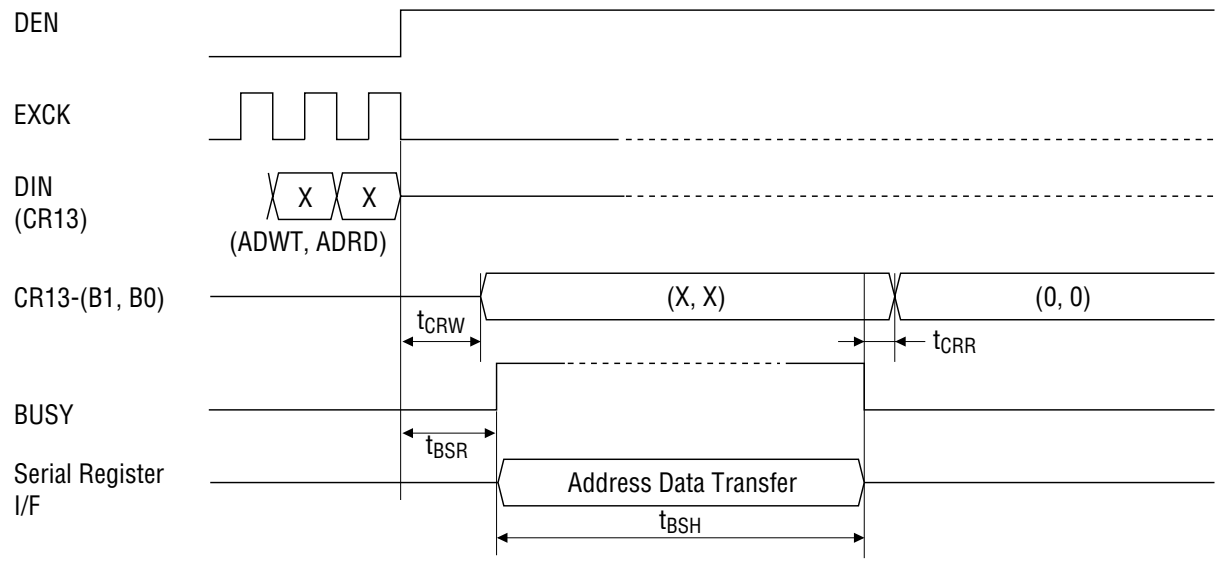


Figure 5 Serial Control Port Interface

Address Write/Read Mode Timing



Record/Playback Mode Timing

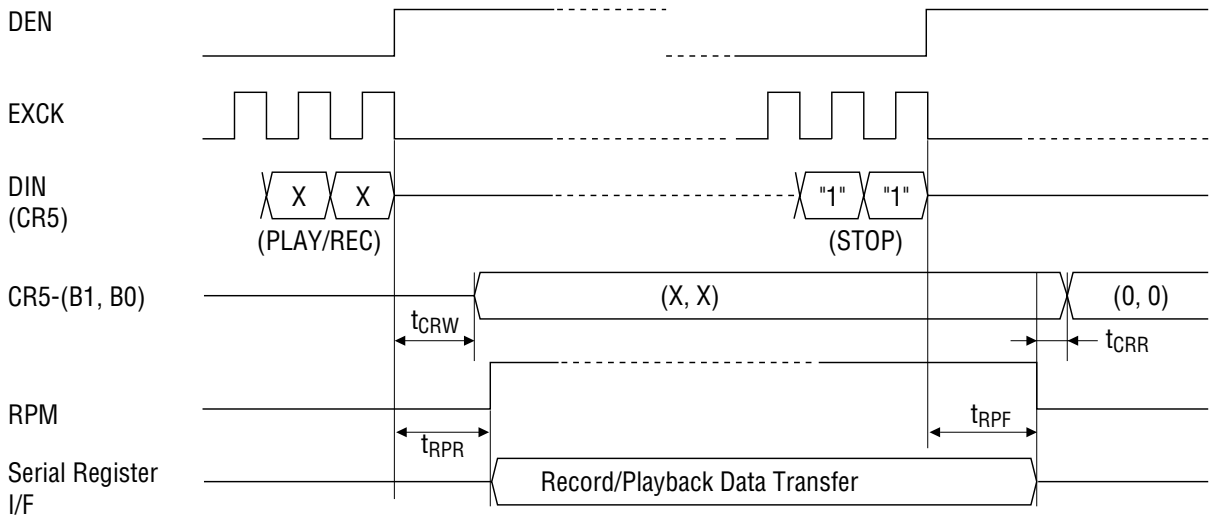


Figure 6 Serial Register Interface

FUNCTIONAL DESCRIPTION

Control Register Description

(1) CR0 (Basic Operation Mode Settings)

	B7	B6	B5	B4	B3	B2	B1	B0
CR0	A/μ SEL	—	PDN ALL	PDN TX	PDN RX	SA, VF OUT	SAO/ VFRO	AOUT PON
Initial value	0	0	0	0	0	0	0	0

B7: .....PCM interface companding law selection 0: μ-law1: A-law
B6: .....Automatic suppression function control 0: suppression off
1: suppression on
When transmit voice is detected, receive level is suppressed automatically by 6 dB.
B5: .....Power down (entire unit) 0: Power ON 1: Power down
ORed with the inverted external power down signal. When using this data, set $\overline{\text{PDN}}$ to "1".
B4: .....Power down (transmit side only) 0: Power ON 1: Power down
B3: .....Power down (receive side only) 0: Power ON 1: Power down
B2: .....The sounder output amp (SAO) and receiver system output amp (VFRO) operation control
0: The output pin selected by CR0 - B1 operates.
1: The sounder system output (SAO) and receiver system output (VFRO) both operate.
B1: .....Selection of sounder system output (SAO) or receiver system output
0: VFRO 1: SAO
SGR potential is output to the non selected pin.
B0: .....AOUT+, AOUT– power on control
0: AOUT+, – power down
1: AOUT+, – power on

(2) CR1 (ADPCM Operation Mode Settings)

	B7	B6	B5	B4	B3	B2	B1	B0
CR1	TX MUTE	RX ON/OFF	ADPCM RESET	TX ON/OFF	RX MUTE	RX MLV2	RX MLV1	RX MLV0
Initial value	0	0	0	0	0	0	0	0

B7: .....Transmit side ADPCM data MUTE 1: MUTE
B6: .....Receive side PCM signal ON/OFF 0: ON 1: OFF
B5: .....Transmit/Receive side ADPCM RESET (in accordance with the G.721)
1: RESET
B4: .....Transmit side PCM signal ON/OFF 0: ON 1: OFF
PCM idle pattern is transmitted when set OFF
B3: .....Receive side ADPCM data MUTE 1: MUTE
Mute operation set by B2, 1, 0 is available, provided this bit is valid when MUTE pin is "0".
B2, 1, 0: .....Receive side voice path mute level settings
(MLV2, MLV1, MLV0) = (0, 0, 0) : through
(0, 0, 1) : –6 dB
(0, 1, 0) : –12 dB
(0, 1, 1) : –18 dB
(1, 0, 0) : –24 dB
(1, 0, 1) : –30 dB
(1, 1, 0) : –36 dB
(1, 1, 1) : MUTE

Note: The above settings are not applied to various tone, side tone, and background noise.

(3) CR2 (PCM CODEC Operation Mode Settings and Transmit/Receive Gain Adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CR2	TX GAIN3	TX GAIN2	TX GAIN1	TX GAIN0	RX GAIN3	RX GAIN2	RX GAIN1	RX GAIN0
Initial value	0	0	0	0	0	0	0	0

B7, B6, B5, B4: .... Transmit side signal gain adjustment (refer to Table 2)
B3, B2, B1, B0: .... Receive side signal gain adjustment (refer to Table 2)

Table 2 Transmit/Receive Gain Settings

B7	B6	B5	B4	Transmit Side Gain	B3	B2	B1	B0	Receive Side Gain
1	0	0	0	–16 dB	1	0	0	0	–16 dB
1	1	0	1	–14 dB	1	1	0	1	–14 dB
1	0	1	0	–12 dB	1	0	1	0	–12 dB
1	0	1	1	–10 dB	1	0	1	1	–10 dB
1	1	0	0	–8 dB	1	1	0	0	–8 dB
1	1	0	1	–6 dB	1	1	0	1	–6 dB
1	1	1	0	–4 dB	1	1	1	0	–4 dB
1	1	1	1	–2 dB	1	1	1	1	–2 dB
0	0	0	0	0 dB	0	0	0	0	0 dB
0	0	0	1	+2 dB	0	0	0	1	+2 dB
0	0	1	0	+4 dB	0	0	1	0	+4 dB
0	0	1	1	+6 dB	0	0	1	1	+6 dB
0	1	0	0	+8 dB	0	1	0	0	+8 dB
0	1	0	1	+10 dB	0	1	0	1	+10 dB
0	1	1	0	+12 dB	0	1	1	0	+12 dB
0	1	1	1	+14 dB	0	1	1	1	+14 dB

The above gain settings table shows the transmit/receive voice signal gain settings and the transmit side gain settings for DTMF tones and other tones. Tone signal transmission is enabled by CR4 - B6 (discussed later), and the gain setting is set to the levels shown below.

DTMF tones (low group): ..... –16 dBm0
DTMF tones (high group) and other tones: ... –14 dBm0

For example, if the transmit gain set value is set to +8 dB (B7, B6, B5, B4) = (0, 1, 0, 0), then the following tones appear at the PCMSO pin.

DTMF tones (low group): ..... –8 dBm0
DTMF tones (high group) and other tones: ... –6 dBm0

However, the gain of the receive side tone and the gain of the side tones (path from transmit side to receive side) are set by the CR3 register.

(4) CR3 (Side Tone and Tone Generator Gain Adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CR3	Side Tone GAIN2	Side Tone GAIN1	Side Tone GAIN0	TONE ON/OFF	TONE GAIN3	TONE GAIN2	TONE GAIN1	TONE GAIN0
Initial value	0	0	0	0	0	0	0	0

B7, B6, B5: ..... Side tone gain adjustment (refer to Table 3)
B4: ..... Tone generator ON/OFF 0: OFF 1: ON
B3, B2, B1, B0: . Tone generator Receive side gain adjustment (refer to Table 4)

Table 3 Side Tone Gain Settings

B7	B6	B5	Side Tone Gain
0	0	0	OFF
0	0	1	–15 dB
0	1	0	–13 dB
0	1	1	–11 dB
1	0	0	– 9 dB
1	0	1	– 7 dB
1	1	0	– 5 dB
1	1	1	– 3 dB

Table 4 Receive Side Tone Generator Gain Settings

B3	B2	B1	B0	Tone Generator Gain	B3	B2	B1	B0	Tone Generator Gain
0	0	0	0	–36 dB	1	0	0	0	–20 dB
0	0	0	1	–34 dB	1	0	0	1	–18 dB
0	0	1	0	–32 dB	1	0	1	0	–16 dB
0	0	1	1	–30 dB	1	0	1	1	–14 dB
0	1	0	0	–28 dB	1	1	0	0	–12 dB
0	1	0	1	–26 dB	1	1	0	1	–10 dB
0	1	1	0	–24 dB	1	1	1	0	– 8 dB
0	1	1	1	–22 dB	1	1	1	1	– 6 dB

The receive side tone generator gain settings shown in Table 4 are set with the following levels as a reference.

DTMF tones (low group): ..... –2 dBm0
DTMF tones (high group) and other tones: ... 0 dBm0

For example, if the tone generator gain set value is set to –6 dB (B3, B2, B1, B0)=(1, 1, 1, 1), then tones at the following levels appear at the SAO or VFRO pin.

DTMF tones (low group): ..... –8 dBm0
DTMF tones (high group) and other tones: ... –6 dBm0

(5) CR4 (Tone Generator Operation Mode and Frequency Settings)

	B7	B6	B5	B4	B3	B2	B1	B0
CR4	DTMF/ OTHERS SEL	TONE SEND	TONE5	TONE4	TONE3	TONE2	TONE1	TONE0
Initial value	0	0	0	0	0	0	0	0

B7: ..... Selection of DTMF signal and other tones
(S tone, F tone, R tone, etc.) 0: Other tones 1: DTMF tones
B6: ..... Transmission side tone transmit
0: Voice signal transmit 1: Tone transmit
B5, B4, B3, B2, B1, B0: .. Tone frequency setting (refer to Table 5)

Table 5 DTMF Signal and Other Tone Settings

(a) When B7 = 1 (DTMF Tones)

B5	B4	B3	B2	B1	B0	Description	B5	B4	B3	B2	B1	B0	Description
*	*	0	0	0	0	697 Hz + 1209 Hz	*	*	1	0	0	0	852 Hz + 1209 Hz
*	*	0	0	0	1	697 Hz + 1336 Hz	*	*	1	0	0	1	852 Hz + 1336 Hz
*	*	0	0	1	0	697 Hz + 1477 Hz	*	*	1	0	1	0	852 Hz + 1477 Hz
*	*	0	0	1	1	697 Hz + 1633 Hz	*	*	1	0	1	1	852 Hz + 1633 Hz
*	*	0	1	0	0	770 Hz + 1209 Hz	*	*	1	1	0	0	941 Hz + 1209 Hz
*	*	0	1	0	1	770 Hz + 1336 Hz	*	*	1	1	0	1	941 Hz + 1336 Hz
*	*	0	1	1	0	770 Hz + 1477 Hz	*	*	1	1	1	0	941 Hz + 1477 Hz
*	*	0	1	1	1	770 Hz + 1633 Hz	*	*	1	1	1	1	941 Hz + 1633 Hz

(b) When B7 = 0 (Other than DTMF Tones)

B5	B4	B3	B2	B1	B0		Description	B5	B4	B3	B2	B1	B0	Description
0	0	0	0	0	0	Tone Scale	784.0 Hz (G)	1	0	0	0	0	0	1100 Hz
0	0	0	0	0	1		830.6 Hz (G+)	1	0	0	0	0	1	1200 Hz
0	0	0	0	1	0		880.0 Hz (A)	1	0	0	0	1	0	1300 Hz
0	0	0	0	1	1		932.3 Hz (A+)	1	0	0	0	1	1	1400 Hz
0	0	0	1	0	0		987.8 Hz (B)	1	0	0	1	0	0	1500 Hz
0	0	0	1	0	1		1046.5 Hz (C)	1	0	0	1	0	1	1600 Hz
0	0	0	1	1	0		1108.7 Hz (C+)	1	0	0	1	1	0	1700 Hz
0	0	0	1	1	1		1174.7 Hz (D)	1	0	0	1	1	1	1800 Hz
0	0	1	0	0	0		1244.5 Hz (D+)	1	0	1	0	0	0	1900 Hz
0	0	1	0	0	1		1318.5 Hz (E)	1	0	1	0	0	1	2000 Hz
0	0	1	0	1	0		1396.9 Hz (F)	1	0	1	0	1	0	2100 Hz
0	0	1	0	1	1		1480.0 Hz (F+)	1	0	1	0	1	1	2200 Hz
0	0	1	1	0	0		1568.0 Hz (G)	1	0	1	1	0	0	2300 Hz
0	0	1	1	0	1		1661.2 Hz (G+)	1	0	1	1	0	1	2400 Hz
0	0	1	1	1	0		1760.0 Hz (A)	1	0	1	1	1	0	2500 Hz
0	0	1	1	1	1		1864.7 Hz (A+)	1	0	1	1	1	1	2600 Hz
0	1	0	0	0	0		1975.5 Hz (B)	1	1	0	0	0	0	2700 Hz
0	1	0	0	0	1		2093.0 Hz (C)	1	1	0	0	0	1	2800 Hz
0	1	0	0	1	0		2217.5 Hz (C+)	1	1	0	0	1	0	2900 Hz
0	1	0	0	1	1		2349.3 Hz (D)	1	1	0	0	1	1	3000 Hz
0	1	0	1	0	0		2489.0 Hz (D+)	1	1	0	1	0	0	2760 Hz
0	1	0	1	0	1		2637.0 Hz (E)	1	1	0	1	0	1	—
0	1	0	1	1	0		2793.8 Hz (F)	1	1	0	1	1	0	—
0	1	0	1	1	1		2960.0 Hz (F+)	1	1	0	1	1	1	—
0	1	1	0	0	0		3136.0 Hz (G)	1	1	1	0	0	0	—
0	1	1	0	0	1	400 Hz		1	1	1	0	0	1	—
0	1	1	0	1	0	500 Hz		1	1	1	0	1	0	—
0	1	1	0	1	1	600 Hz		1	1	1	0	1	1	—
0	1	1	1	0	1	700 Hz		1	1	1	1	0	0	—
0	1	1	1	0	1	800 Hz		1	1	1	1	0	1	—
0	1	1	1	1	0	900 Hz		1	1	1	1	1	0	—
0	1	1	1	1	1	1000 Hz		1	1	1	1	1	1	—

(6) CR5 (Serial Register Interface Control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR5	SEND/ REC	ROM/ SR	4M8M/ 1M	—	—	—	CMD1	CMD0
Initial value	0	0	0	0	0	0	0	0

B7: .....Connection between register and ADPCM
0: with ADPCM receive side 1: ADPCM Transmit side
B6: .....Voice ROM/Serial register selection
0: Serial Register 1: Voice ROM
B5: .....Connecting serial register capacity
0: 1 Mb (MSM63V89C)
1: 4 Mb (MSM6684), 8 Mb (MSM6685)
B4 - B2: .....Reserved for test. Should be set "0"
B1, B0: .....Serial register I/F Instruction command
(CMD1, CMD0) = (0, 0) : NOP
(0, 1) : PLAY (Playback)
(1, 0) : REC (Recording)
(1, 1) : STOP (Stop)

* (CMD1, CMD0) are reset (0, 0) after command execution.
Instruction commands of Play and REC should not be set when busy (CR5 - B1) and RPM (CR5 - B0) are "1".

(7) CR6 (VOICE/SILENCE Detect Function Control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR6	VOX ON/OFF	ON LVL1	ON LVL0	OFF TIME	VOX IN	RX NOISE LEVEL SEL	RX NOISE LVL1	RX NOISE LVL0
Initial value	0	0	0	0	0	0	0	0

B7: .....Voice/Silence detect function ON/OFF 0: OFF 1: ON
B6, B5: .....Transmit side voice/silence detector level settings
(0,0): –20 dBm0 (0,1): –25 dBm0
(1,0): –30 dBm0 (1,1): –35 dBm0
B4: .....Hangover time (refer to Fig. 1) settings 0: 160 ms 1: 320 ms
B3: .....Receive side Voice/Silence detect input signal
0: Internal background noise transmit 1: Voice receive signal transmit
When using this data, set the VOXI pin to "0".
B2: .....Receive side background noise level setting
0: Internal automatic setting 1: External (by B1, B0) setting
Internal automatic setting → Set to the voice signal level when B3 (VOXI) changes from "1" to "0".
B1, B0: .....External setting background noise level
(0,0): No noise (0,1): –55 dBm0
(1,0): –45 dBm0 (1,1): –35 dBm0

(8) CR7 (Detect Register: Read-only)

	B7	B6	B5	B4	B3	B2	B1	B0
CR7	VOX OUT	Silent Level 1	Silent Level 0	—	—	—	Busy	RPM
Initial value	0	0	0	0	0	0	0	0

B7: .....Transmit side voice/silence detection 0: Silence 1: Voice
B6, B5: .....Transmit side silence level (indicator)
(0,0):Below –60 dBm0 (0,1): –50 to –60 dBm0
(1,0): –40 to –50 dBm0 (1,1): Above –40 dBm0

Note: These outputs are enabled when the voice/silence detect function is turned on by CR6 - B7.

B4, B3, B2: .Not used
B1: .....Serial Register I/F monitoring
Monitors address read and write operation of serial register interface.
0: Stop 1: Read or Write
B0: .....Monitors serial register recording or playback.
0: Stop 1: Recording or playing back

(9) CR8 (Start X address 0-7)

	B7	B6	B5	B4	B3	B2	B1	B0
CR8	ST0	ST1	ST2	ST3	ST4	ST5	ST6	ST7
Initial value	0	0	0	0	0	0	0	0

CR9 (Start X address 8-12)

	B7	B6	B5	B4	B3	B2	B1	B0
CR9	ST8	ST9	ST10	ST11	ST12	—	—	—
Initial value	0	0	0	0	0	0	0	0

CR8 (B7 - B0), CR9 (B7 - B3): Record and Playback start address store register

(10) CR10 (Stop Y address 0-7)

	B7	B6	B5	B4	B3	B2	B1	B0
CR10	SPY0	SPY1	SPY2	SPY3	SPY4	SPY5	SPY6	SPY7
Initial value	0	0	0	0	0	0	0	0

CR10 (B7 - B0): Record and Playback stop Y address store register

(11) CR11 (Stop X address 0-7)

	B7	B6	B5	B4	B3	B2	B1	B0
CR11	SP0	SP1	SP2	SP3	SP4	SP5	SP6	SP7
Initial value	0	0	0	0	0	0	0	0

CR12 (Stop X address 8-12)

	B7	B6	B5	B4	B3	B2	B1	B0
CR12	SP8	SP9	SP10	SP11	SP12	—	—	—
Initial value	0	0	0	0	0	0	0	0

CR11 (B7 - B0), CR12 (B7 - B3): Record and Playback stop X address store register

Note: The data in CR8 - CR12 may be changed under the following conditions. If so, rewrite the data.

(1) When REC or Play command is executed during the state of start address = stop address

(2) When stop command is executed during the state of no operation of serial register interface (Busy = RPM = "0")

(12) CR13 (Channel Selection)

	B7	B6	B5	B4	B3	B2	B1	B0
CR13	CH0	CH1	CH2	CH3	CH4	—	ADRD	ADWT
Initial value	0	0	0	0	0	0	0	0

B7 - B3 ..... Channel selection (All 32 channels are selected with Hex cord)
B2 ..... Since reserved for TEST, this bit should always be set to "0".
B1 ..... Address read instruction
0: NOP
1: When set to "1", start/stop address corresponding to the channels specified by B7 to B3 is transferred from serial register channel index area to CR8 - CR12. After transfer, this bit is reset to "0".
B0 ..... Address write instruction
0: NOP
1: When set to "1", start/stop address corresponding to the channels specified by B7 to B3 is transferred from CR8 - CR12 to serial register channel index area. After transfer, this bit is reset to "0".

Note : Writing to ADRD and ADWT is inhibited when BUSY (CR7 - B1) or RPM (CR7 - B0) is "1".

DATA CONFIGURATION IN THE EXTERNAL SERIAL REGISTER

X Address Space

The address space of the external serial register is accessed based on (word direction indicated by the X address) × (1 Kb depth in Y direction). The maximum X address in word direction depends on the total memory of serial registers connected. Since the leading 32 words (32 Kb) of the serial register are used as the channel index area, X address 020h onward can be used as the voice data area.

CR5-B5	0	1	1
Total Memory Capacity (device name)	1 Mb (MSM63V89C)	4 Mb (MSM6684)	8 Mb (MSM6685)
Number of words	1K words	4K words	8K words
X address*	000h to 3FFh	0000h to 0FFFh	0000h to 1FFFh

* 0000h to 001Fh is used as the channel index area.

Y Address Space

For 1 Kb ADPCM data in Y direction, 4 bits × 256 samples = 1024 bits are stored in the 1 Kb memory area. One Y address is allocated to one sample (4 bits) of ADPCM data and addressing is made with 00h to FFh.

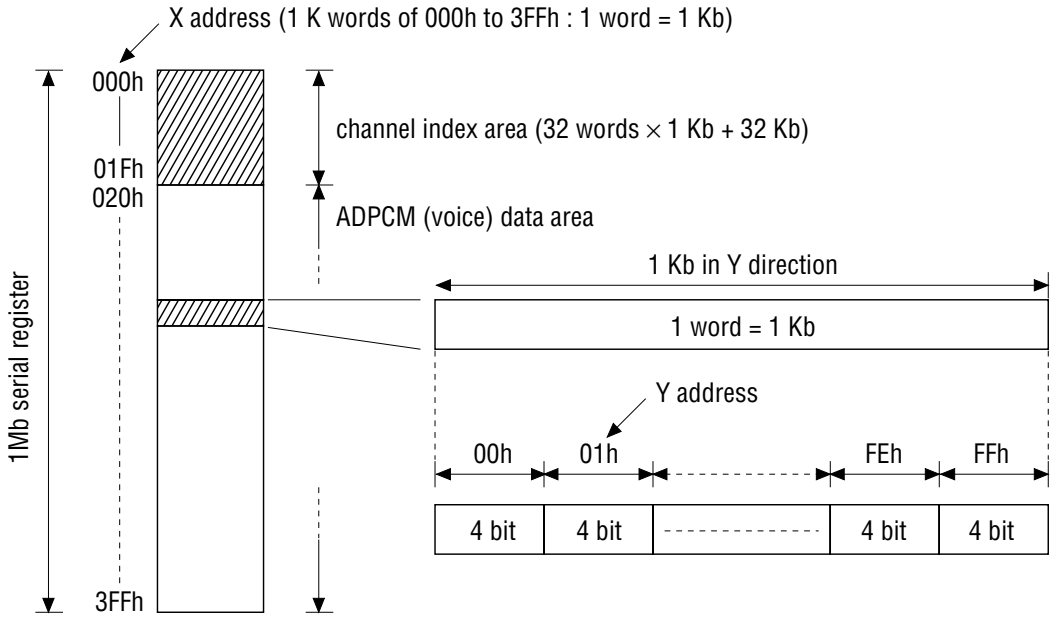


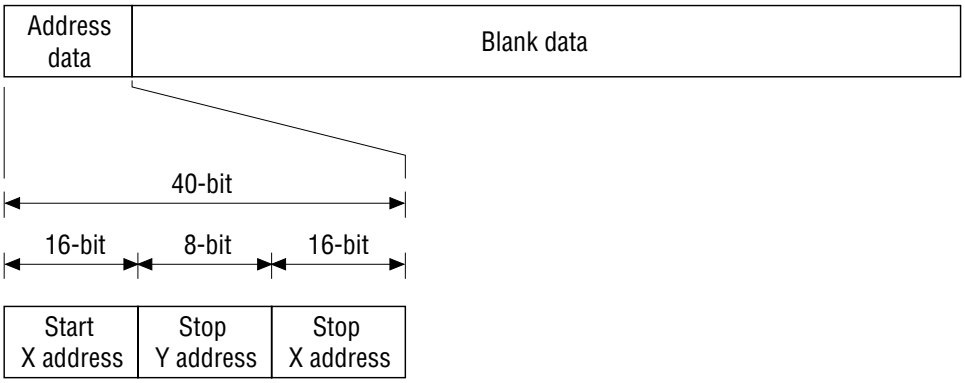
Figure 7 Address Space of the 1 Mb Serial Register

Channel Index Area of the Serial Register

One channel (1 Kb) of the channel index area consists of the 40 bits of address data.

(1) Stop Y address
The Y address is represented by 8 bits and addressing is made with 00h to FFh.

(2) Start X address, stop X address
The X address is represented by 16 bits (valid 13 bits). If, for example, the serial register is 1Mb, the 1K-word X address space is addressed with 000h to 3FFh.



Start X address (ST0 to ST12)	ST0	ST1	----------	ST11	ST12	—	—	—
Stop Y address (SPY0 to SPY7)	SPY0	SPY1	----------		SPY6	SPY7		
Stop X address (ST0 to SP12)	SP0	SP1	----------	SP11	SP12	—	—	—

Figure 8 Channel Index Area of the Serial Register

METHODS OF RECORDING AND PLAYBACK

Recording Method (See the flow chart in Figure 9.)

(1) • Set up the connection between the serial register/voice ROM and ADPCM transmit-receive system. (See Figure 11.) (CR5 - B7)
• Specify the serial register/voice ROM. (CR5 - B6)
• Set the external capacity. (CR5 - B5)
• Set the NOP command. (CR5 - B1 = "0", B0 = "0")

(2) • Set the start/stop address. (CR8 to CR12)

(3) • Set the channel. (CR13 - B7 to B3)
• Set the ADWT (address write) instruction. (CR13 - B1 = "0", B0 = "1")

(4) • The start/stop address of the channel set by the ADWT instruction is stored in the channel index area. When status register BUSY (CR7 - B1) changes from "1" to "0", storage is complete.

(5) • Start recording by setting the REC (recording) command (CR5 - B1 = "1", B0 = "0"). In this case, the basic setting of CR5 - B7 to B5 should be the same as (1).

(6) • Check the recording start with the status register RPM bit (CR7 - B0 = "1").

(7) • To interrupt during recording, set the STOP (stop) command (CR5 - B1 = "1", B0 = "1"). In this case, to store the address counter contents in the channel index area as a new stop address, the following settings are required:
• Set the channel.
• Set the ADWT instruction.
• When the BUSY bit changes from "1" to "0", settings are complete.

(8) • When the address counter reaches the stop address, recording is complete. Check completion of recording with RPM bit = "0".

Note: If the stop address value is smaller than the start address value, recording is made to the last address of the serial register.

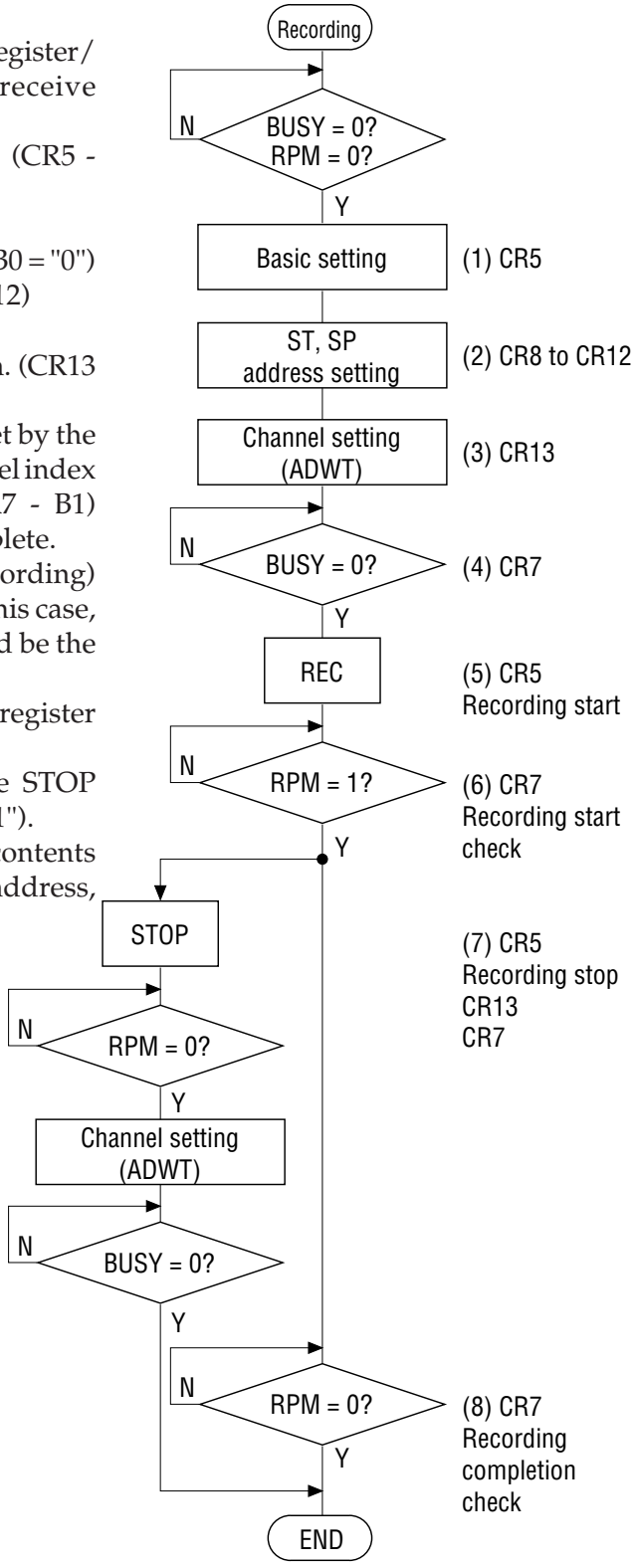


Figure 9 Flow Chart of Recording

Playback Method (See the flow chart in Figure 10.)

(1) • Set up the connection between the serial register/voice ROM and ADPCM transmit-receive system. (See Figure 11.) (CR5 - B7)
• Specify the serial register/voice ROM. (CR5 - B6)
• Set the external capacity. (CR5 - B5)
• Set the NOP command. (CR5 - B1 = "0", B0 = "0")

(2) • Set the channel. (CR13 - B7 to B3)
• Set the ADRD (address read) instruction. (CR13 - B1 = "1", B0 = "0")

(3) • For playback of the voice ROM, set the start/stop address here.

(4) • The start/stop address of the channel set by the ADRD instruction is fetched from the channel index area.
When status register BUSY (CR7 - B1) changes from "1" to "0", fetching is complete.

(5) • Start playback by setting the PLAY (playback) command (CR5 - B1 = "0", B0 = "1"). In this case, basic setting of CR5 - B7 to B5 should be the same as (1).

(6) • Check the playback start with the status register RPM bit (CR7 - B0 = "1").

(7) • To stop playback set the STOP (stop) command (CR5 - B1 = "1", B0 = "1").

(8) • When the address counter reaches the stop address, playback is complete.
Check completion of playback with RPM bit = "0".

Note: If the stop address value is smaller than the start address value, playback is made to the last address of the serial register.

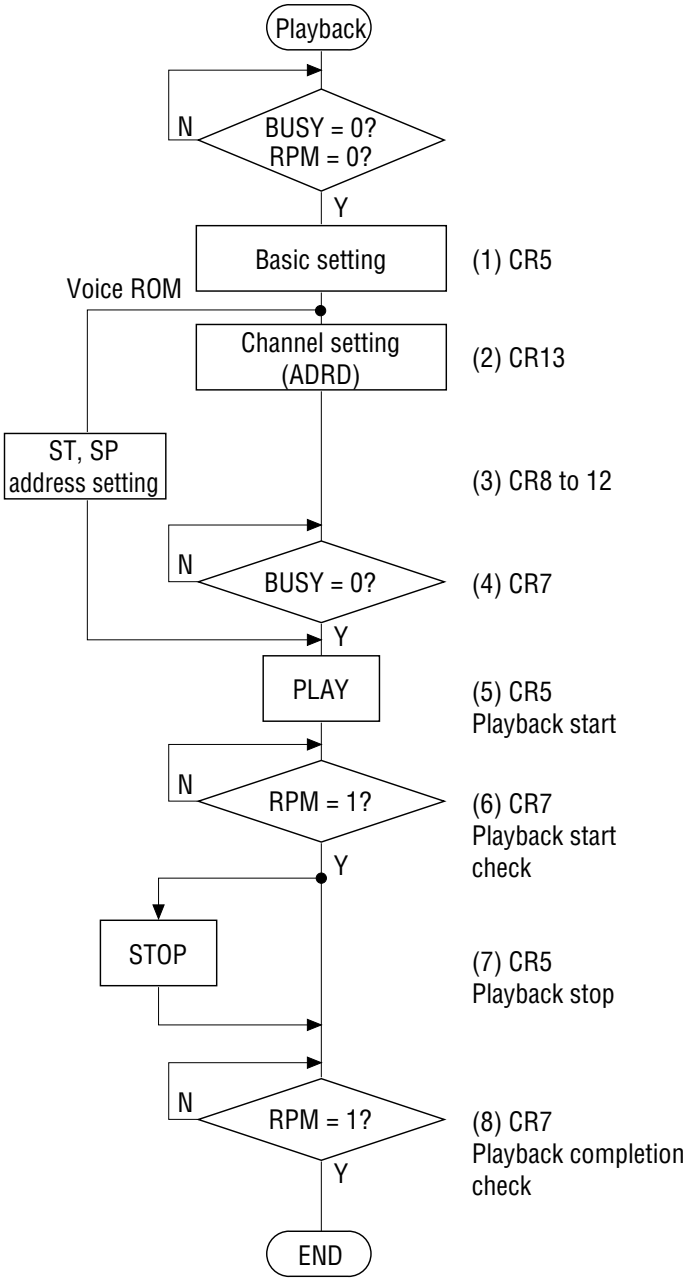


Figure 10 Flow Chart of Playback

SIGNAL FLOW IN RECORDING/PLAYBACK

When the serial register is connected to each ADPCM transmit and receive system, the flow of recording/playback signal is as follows:

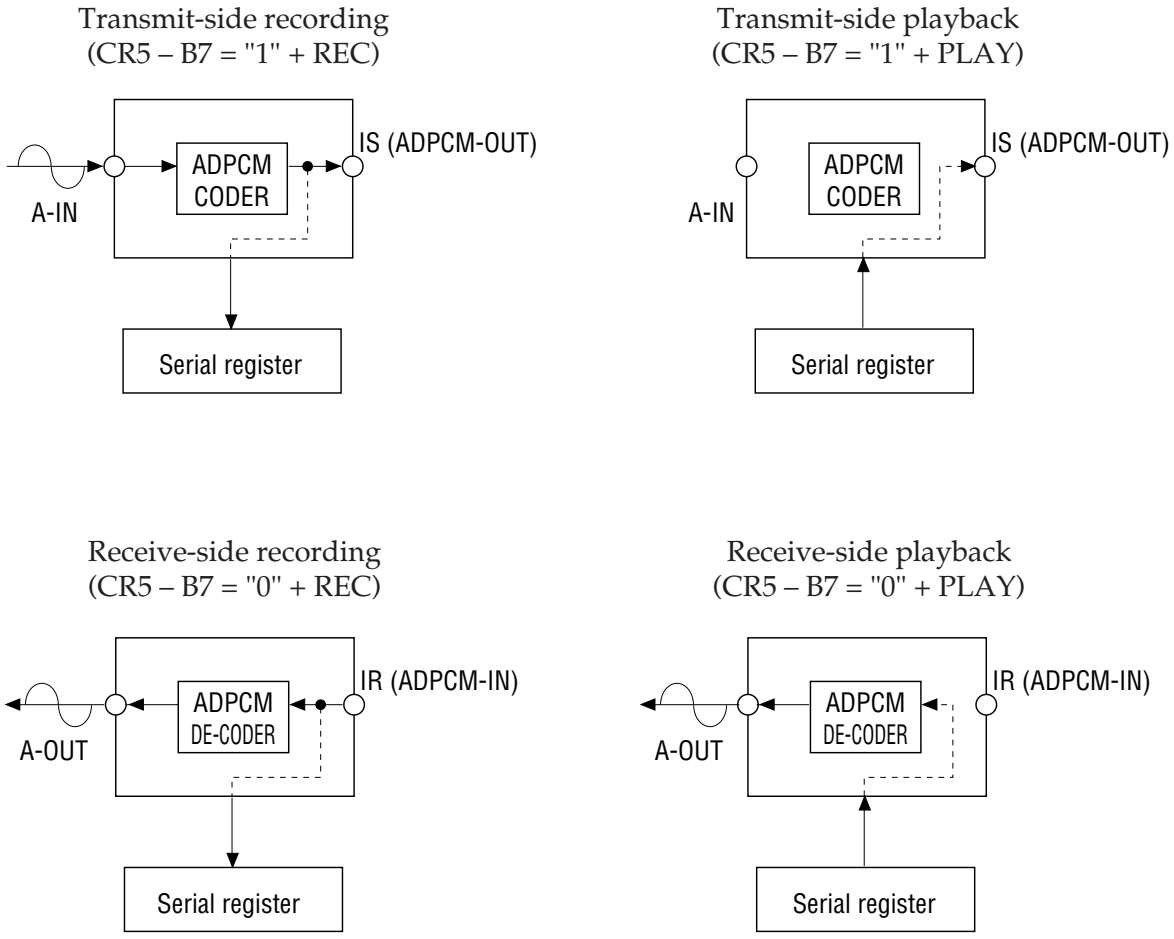
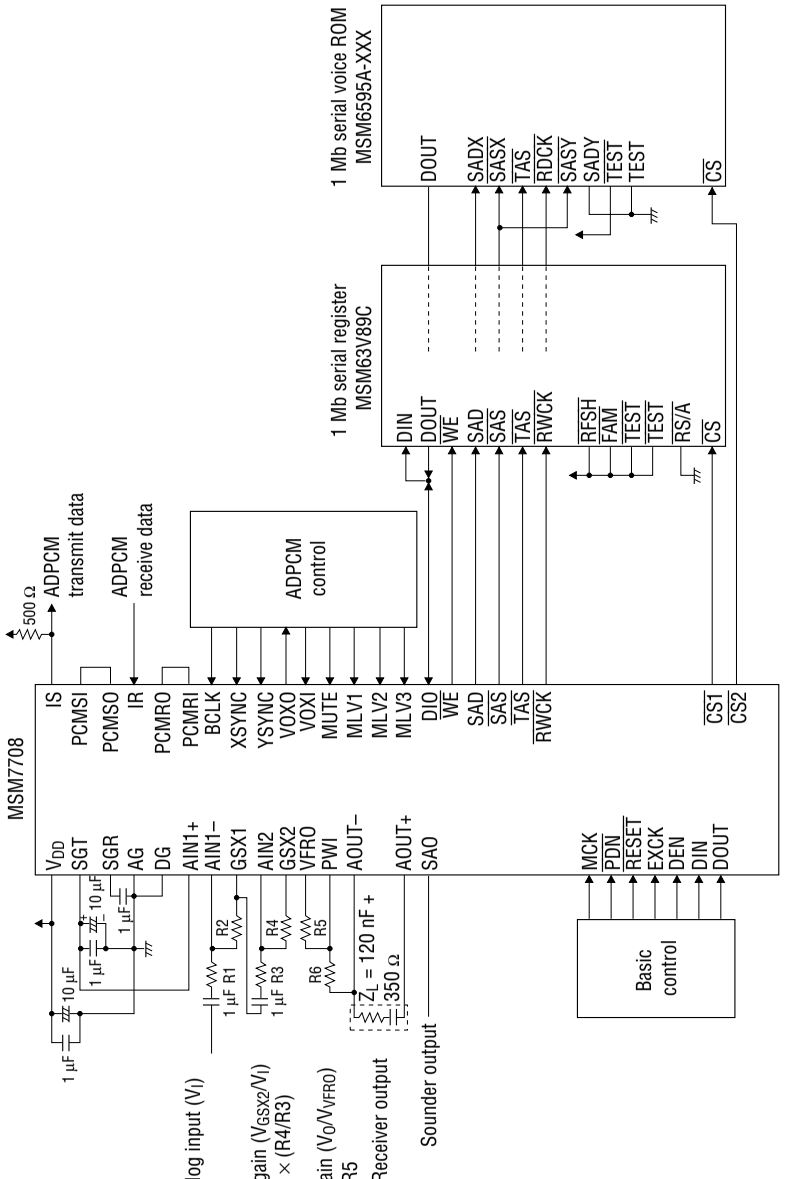


Figure 11 Signal Flow in Transmit/Receive Side Recording/Playback

APPLICATION CIRCUIT

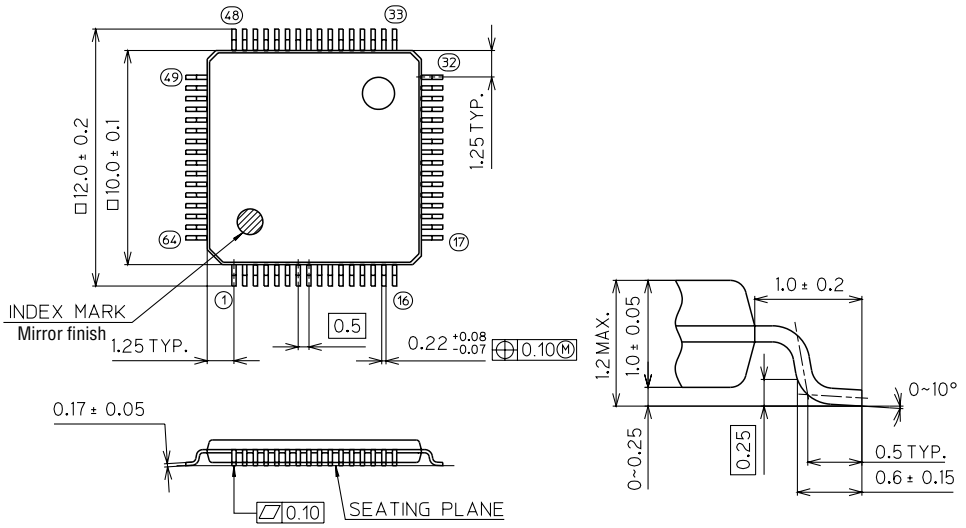
An application circuit is shown below using a 1 Mb serial register and a 1 Mb serial voice ROM.



PACKAGE DIMENSIONS

(Unit : mm)

TQFP64-P-1010-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.26 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).