OKI Semiconductor

This version: Aug. 1998
Previous version: Nov. 1996

MSM7704-01/02/03

2ch Single Rail CODEC

GENERAL DESCRIPTION

The MSM7704-01/7704-02/7704-03 are two-channel CODEC CMOS ICs for voice signals ranging from 300 to 3400 Hz. These devices contain filters for A/D and D/A conversion.
Designed especially for a single-power supply and low-power applications, these devices contain two-channel AD/DA converters in a single chip and achieve a reduced footprint and a reduced number of external components.
The MSM7704-01/7704-02/7704-03 are best suited for an analog interface to an echo canceller DSP used in digital telephone terminals, digital PABXs, and hands free terminals.

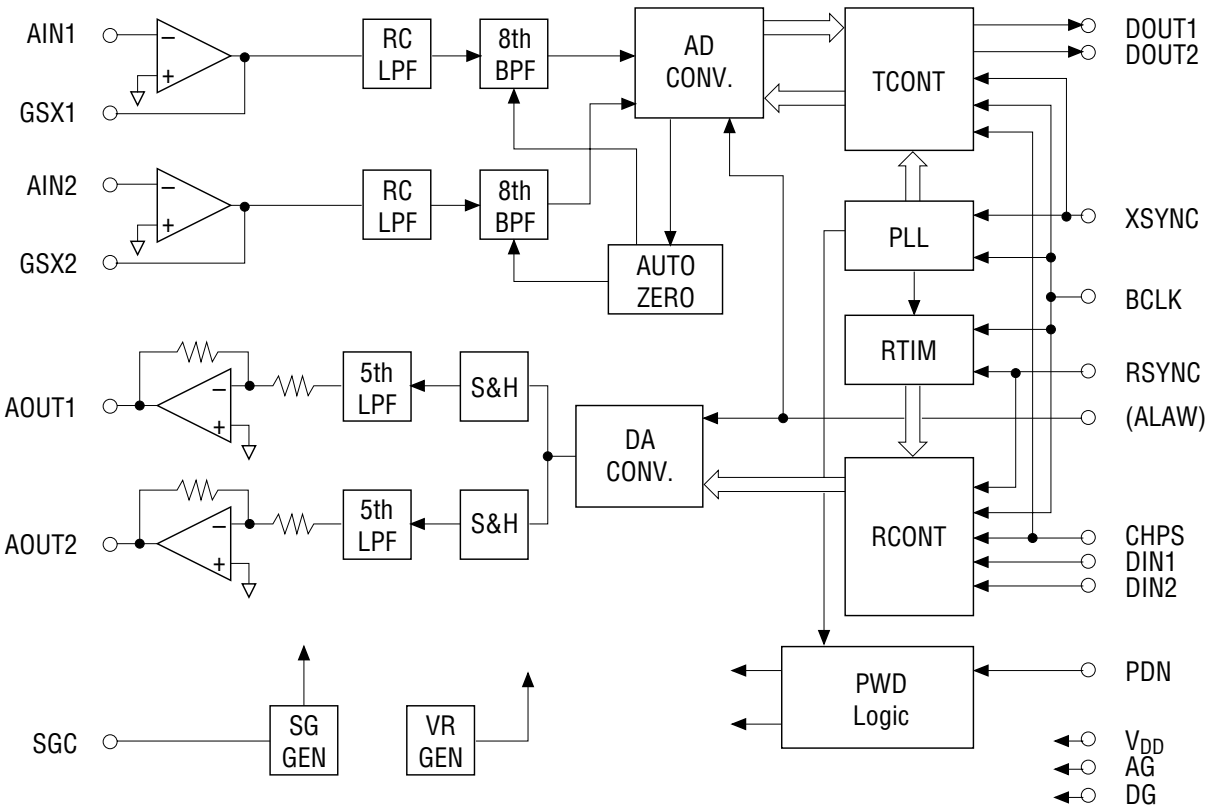
FEATURES

- Single power supply: +2.7 V to +3.8 V
- Power consumption

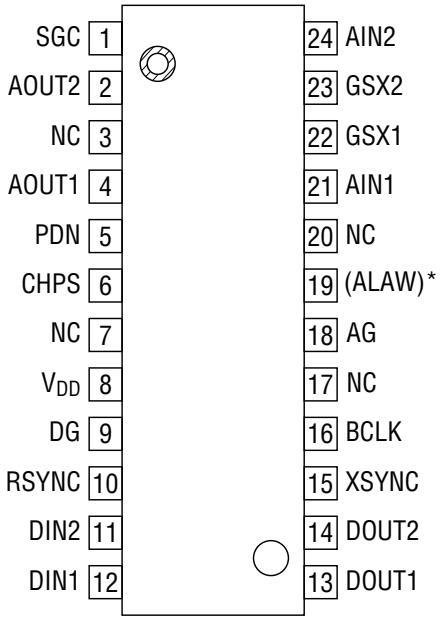
Operating mode:	30 mW Typ.	50 mW Max.
Power-saving mode:	3 mW Typ.	6 mW Max.
Power-down mode:	0.03 mW Typ.	0.3 mW Max.

- ITU-T Companding law
  - MSM7704-01: μ/A-law pin-selectable
  - MSM7704-02: μ-law
  - MSM7704-03: A-law
- Built-in PLL eliminates a master clock
- The PCM interface can be switched between 2 channel serial/parallel
- Transmission clock: 64/128/256/512/1024/2048 kHz
  96/192/384/768/1536/1544/200 kHz
  (During 2 channel serial mode, the 64 and 96 kHz clocks are disabled)
- Adjustable transmit gain
- Built-in reference voltage supply
- Analog output can directly drive a 1.2 kΩ load
- Package:
  24-pin plastic SOP (SOP24-P-430-1.27-K) (Product name : MSM7704-01GS-K)
  (Product name : MSM7704-02GS-K)
  (Product name : MSM7704-03GS-K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC : No connect pin

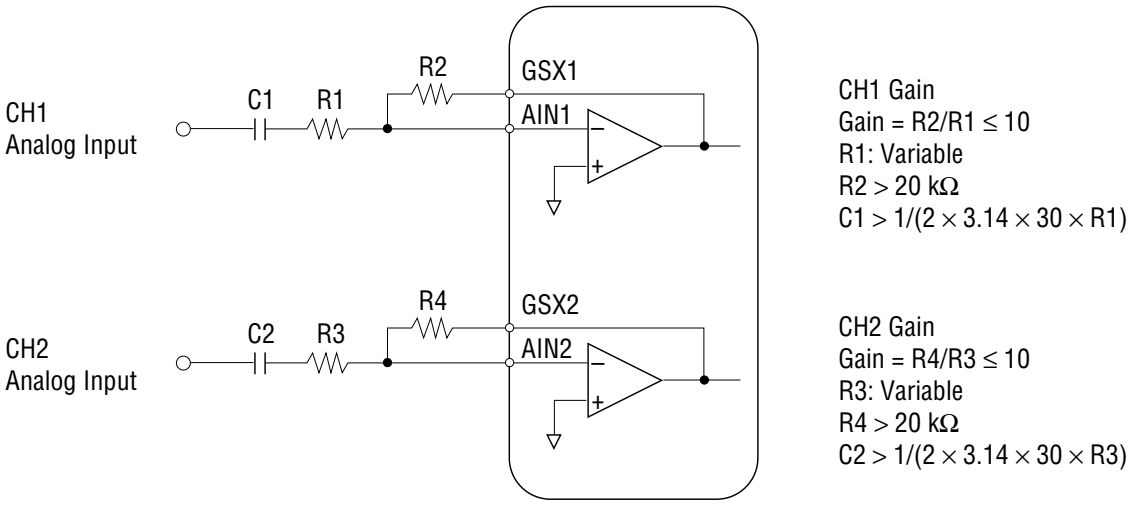
24-Pin Plastic SOP

* The ALAW pin is only applied to the MSM7704-01GS-K.

PIN AND FUNCTIONAL DESCRIPTIONS

AIN1, AIN2, GSX1, GSX2

AIN1 and AIN2 are the transmit analog inputs for channels 1 and 2.
GSX1 and GSX2 are the transmit level adjustments for channels 1 and 2.
AIN1 and AIN2 are inverting inputs for the op-amps. GSX1 and GSX2 are connected to the outputs of the op-amps and are used to adjust the level, as shown below.
When AIN1 and AIN2 are not used, connect AIN1 to GSX1 and AIN2 to GSX2. During power saving mode and power down mode, the GSX1 and GSX2 outputs are in high impedance state.



AOUT1, AOUT2

AOUT1 is the receive analog output for channel 1 and AOUT2 is used for channel 2.
The output signal has an amplitude of 2.0 V_{PP} above and below the signal ground voltage (SG : 1/2 V_{DD}). When the digital signal of +3 dBmO is input to DIN1 and DIN2, it can drive a load of 1.2 kΩ or more.
During power saving mode, or power down mode, these outputs are at the voltage level of SG with a high impedance.

V_{DD}

Power supply for +3 V.
A power supply for an analog circuit in the system to which the device is applied should be used. A bypass capacitor of 0.1 µF to 1 µF with excellent high-frequency characteristics and a capacitor of 10 µF to 20 µF should be connected between this pin and the AG pin if needed.

DIN1

PCM signal input for channel 1 when the parallel mode is selected.
D/A conversion is performed with the serial PCM signal input to this pin, the RSYNC signal synchronous with the serial PCM signal, and the BCLK signal, and then the analog output is output from AOUT1 pin.
The data rate of the PCM signal is equal to the frequency of the BCLK signal.
The PCM signal is shifted at the falling edge of the BCLK signal and latched into the internal register when shifted by eight bits.
The start of the PCM data (MSD) is identified at the rising edge of RSYNC.
When the serial mode is selected, this pin is not used and should be connected to GND (0 V).

DIN2

PCM signal input for channel 2 when the parallel mode is selected.
D/A conversion is performed with the serial PCM signal input to this pin, the RSYNC signal synchronous with the serial PCM signal, and the BCLK signal, and then the analog output is output from AOUT2 pin.
The data rate of the PCM signal is equal to the frequency of the BCLK signal.
The PCM signal is shifted at the falling edge of the BCLK signal and latched into the internal register when shifted by eight bits.
The start of the PCM data (MSD) is identified at the rising edge of RSYNC.
When the serial mode is selected, this pin is used for the 2ch multiplexed PCM signal input.

BCLK

Shift clock signal input for the DIN1, DIN2, DOUT1, and DOUT2 signals.
The frequency, equal to the data rate, is 64, 96, 128, 192, 256, 384, 512, 768, 1024, 1536, 1544, 2048, or 200 kHz. Setting this signal to logic "1" or "0" drives both transmit and receive circuits to the power saving state.

RSYNC

Receive synchronizing signal input.
Eight bits PCM data required are selected from a series of PCM signal to the DIN1 and DIN2 pins by the receive synchronizing signal.
All timing signals in the receive section are synchronized by this synchronizing signal. This signal must be synchronized in phase with the BCLK (generated from the same clock source as BCLK). The frequency should be 8 kHz ±50 ppm to guarantee the AC characteristics which are mainly the frequency characteristics of the receive section.
However, unless the frequency characteristics of the system used are strictly specified, this device can operate in the range of 6 kHz to 9 kHz, but the electrical characteristics specified in the data sheet are not guaranteed.

XSYNC

Transmit synchronizing signal input.
PCM output signal from the DOUT1 and DOUT2 pins is output in synchronization with this transmit synchronizing signal. This synchronizing signal triggers the PLL and synchronizes all timing signals of the transmit section.
This synchronizing signal must be synchronized in phase with BCLK.
The frequency should be 8 kHz ±50 ppm to guarantee the AC characteristics which are mainly the frequency characteristics of the transmit section.
However, unless the frequency characteristics of the system used are strictly specified, this device can operate in the range of 6 kHz to 9 kHz, but the electrical characteristics are not guaranteed.
Setting this signal to logic "1" or "0" drives both transmit and receive circuits to power saving state.

DOUT1

PCM signal output of channel 1 when the parallel mode is selected.
The PCM output signal is output from MSD in a sequential order, synchronizing with the rising edge of the BCLK signal.
MSD may be output at the rising edge of the XSYNC signal, based on the timing between BCLK and XSYNC.
This pin is in a high impedance state except during 8-bit PCM output. It is also in a high impedance state during power-saving state or power-down state.
When the serial mode is selected, this pin is configured to be the output of serial multiplexed 2ch PCM signal.
A pull-up resistor must be connected to this pin because it is an open drain output.
This device is compatible with the ITU-T recommendation on coding law and output coding format.
The MSM7704-03 (A-law) outputs the character signal, inverting the even bits.

Input/Output Level	PCMIN/PCMOUT	
	MSM7704-02 (μ-law)	MSM7704-03 (A-law)
	MSD	MSD
+Full scale	1 0 0 0 0 0 0 0	1 0 1 0 1 0 1 0
+0	1 1 1 1 1 1 1 1	1 1 0 1 0 1 0 1
–0	0 1 1 1 1 1 1 1	0 1 0 1 0 1 0 1
–Full scale	0 0 0 0 0 0 0 0	0 0 1 0 1 0 1 0

DOUT2

PCM signal output for channel 2 when the parallel mode is selected.
The PCM output signal is output from MSD in a sequential order, at the rising edge of the BCLK signal.
MSD may be output at the rising edge of the XSYNC signal, based on the timing between BCLK and XSYNC.
This pin is in a high impedance state except during 8-bit PCM output. It is also in a high impedance state during power-saving state or power-down state.
When the serial mode is selected, this pin is left open.
A pull-up resistor must be connected to this pin because it is an open drain output.
This device is compatible with the ITU-T recommendation on coding law and output coding format.
The MSM7704-03 (A-law) outputs the character signal inverting the even bits.

CHPS

Control signal input for the mode selection of PCM input and output.
When this signal is at a logic "1" level, the PCM input and output are in the parallel mode. The PCM data of CH1 and CH2 is input to DIN1 and DIN2 and output from DOUT1 and DOUT2 with the same timing.
When this signal is at a logic "0" level, the PCM input and output are in the serial mode. The PCM data of CH1 and CH2 is input to DIN2 and output from DOUT1 as time division multiplexed data.
The parallel mode is conveniently applied to the digital interface to the echo canceller device, and the serial mode is applied to the digital interface to PCM multiplexer's for PABXs.

PDN

Power down control signal.
When PDN is at a logic "0" level, both transmit and receive circuits are in power down state.

AG

Analog signal ground.

DG

Ground for the digital signal circuits.
This ground is separate from the analog signal ground. The DG pin must be connected to the AG pin on the printed circuit board to make a common analog ground.

SGC

Used to generate the signal ground voltage level by connecting a bypass capacitor.
Connect a 0.1 µF capacitor with excellent high frequency characteristics between the AG pin and the SGC pin.

ALAW

Control signal input of the companding law selection.
Provides only for the MSM7704-01GS-K. The CODEC will operate in the µ-law when this pin is at a logic "0" level and the CODEC will operate in the A-law when this pin is at a logic "1" level. The CODEC operates in the µ-law if the pin is left open, since this pin is internally pulled down.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	—	0 to 7	V
Analog Input Voltage	V_{AIN}	—	–0.3 to V_{DD} + 0.3	V
Digital Input Voltage	V_{DIN}	—	–0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	Voltage must be fixed	2.7	3.0	3.8	V
Operating Temperature	Ta	—	–30	+25	+85	°C
Analog Input Voltage	V_{AIN}	Gain = 1	—	—	1.4	V_{PP}
Digital Input High Voltage	V_{IH}	XSYNC, RSYNC, BCLK, DIN1, DIN2, PDN, CHPS	0.45 × V_{DD}	—	V_{DD}	V
Digital Input Low Voltage	V_{IL}		0	—	0.16 × V_{DD}	V
Clock Frequency	F_C	BCLK = (eliminates 64, 96 kHz, when 2ch serial mode)	64, 128, 256, 512, 1024, 2048, 96, 192, 384, 768, 1536, 1544, 200			kHz
Sync Pulse Frequency	F_S	XSYNC, RSYNC	—	8.0	—	kHz
Clock Duty Ratio	D_C	BCLK	40	50	60	%
Digital Input Rise Time	t_{Ir}	XSYNC, RSYNC, BCLK, DIN1, DIN2, PDN, CHPS	—	—	50	ns
Digital Input Fall Time	t_{If}		—	—	50	ns
Transmit Sync Pulse Setting Time	t_{XS}	BCLK→XSYNC, See Timing Diagram	100	—	—	ns
	t_{SX}	XSYNC→BCLK, See Timing Diagram	100	—	—	ns
Receive Sync Pulse Setting Time	t_{RS}	BCLK→RSYNC, See Timing Diagram	100	—	—	ns
	t_{SR}	RSYNC→BCLK, See Timing Diagram	100	—	—	ns
Sync Pulse Width	t_{WS}	XSYNC, RSYNC	1 BCLK	—	100	µs
DIN Set-up Time	t_{DS}	DIN1, DIN2	100	—	—	ns
DIN Hold Time	t_{DH}	DIN1, DIN2	100	—	—	ns
Digital Output Load	R_{DL}	Pull-up resistor, DOUT1, DOUT2	0.5	—	—	kΩ
	C_{DL}	DOUT1, DOUT2	—	—	100	pF
Analog Input Allowable DC Offset	V_{off}	Transmit gain stage, Gain = 1	V_{DD}/2 –100	—	V_{DD}/2 +100	mV
		Transmit gain stage, Gain = 10	V_{DD}/2 –10	—	V_{DD}/2 +10	mV
Allowable Jitter Width	—	XSYNC, RSYNC	—	—	500	ns

ELECTRICAL CHARACTERISTICS

DC and Digital Interface Characteristics

(V_{DD} = 2.7 V to 3.8 V, Ta = –30°C to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current	I_{DD1}	Operating mode, No signal	—	10.0	14.0	mA
	I_{DD2}	Power-save mode, PDN = 1, XSYNC or BCLK OFF	—	1.0	4.0	mA
	I_{DD3}	Power-down mode, PDN = 0 Digital input is at 0 V	—	0.01	0.05	mA
Input High Voltage	V_{IH}	—	$0.45 \times V_{DD}$	—	V_{DD}	V
Input Low Voltage	V_{IL}	—	0.0	—	$0.16 \times V_{DD}$	V
High Level Input Leakage Current	I_{IH}	—	—	—	2.0	µA
Low Level Input Leakage Current	I_{IL}	—	—	—	0.5	µA
Digital Output Low Voltage	V_{OL}	Pull-up resistance > 500 Ω	0.0	0.2	0.4	V
Digital Output Leakage Current	I_O	—	—	—	10	µA
Input Capacitance	C_{IN}	—	—	5	—	pF

Transmit Analog Interface Characteristics

(V_{DD} = 2.7 V to 3.8 V, Ta = –30°C to +85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Input Resistance	R_{INX}	AIN1, AIN2		10	—	—	MΩ
Output Load Resistance	R_{LGX}	GSX1, GSX2		20	—	—	kΩ
Output Load Capacitance	C_{LGX}	with respect to SG		—	—	30	pF
Output Amplitude	V_{OGX}			–0.7	—	+0.7	V
Offset Voltage	V_{OSGX}		Gain = 1	–20	—	+20	mV

Receive Analog Interface Characteristics

(V_{DD} = 2.7 V to 3.8 V, Ta = –30°C to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output Load Resistance	R_{LAO}	AOUT1, AOUT2 (each) with respect to SG	1.2	—	—	kΩ
Output Load Capacitance	C_{LAO}	AOUT1, AOUT2	—	—	50	pF
Output Amplitude	V_{OAO}	AOUT1, AOUT2, R_L = 1.2 kΩ with respect to SG	–1	—	+1	V
Offset Voltage	V_{OSAO}	AOUT1, AOUT2 with respect to SG	–100	—	+100	mV

AC Characteristics

(V_{DD} = 2.7 V to 3.8 V, Ta = –30°C to +85°C)

Parameter	Symbol	Freq. (Hz)	Level (dBm0)	Condition	Min.	Typ.	Max.	Unit
Transmit Frequency Response	Loss T1	60	0		20	26	—	dB
	Loss T2	300			–0.15	+0.07	+0.20	dB
	Loss T3	1020			Reference			dB
	Loss T4	2020			–0.15	–0.04	+0.20	dB
	Loss T5	3000			–0.15	+0.06	+0.20	dB
	Loss T6	3400			0	0.4	0.80	dB
Receive Frequency Response	Loss R1	300	0		–0.15	–0.03	+0.20	dB
	Loss R2	1020			Reference			dB
	Loss R3	2020			–0.15	+0.02	+0.20	dB
	Loss R4	3000			–0.15	+0.12	+0.20	dB
	Loss R5	3400			0.0	0.46	0.80	dB
Transmit Signal to Distortion Ratio	SD T1	1020	3	*1	35	43	—	dB
	SD T2		0		35	41	—	
	SD T3		–30		35	38	—	
	SD T4		–40		28	31.5	—	
	SD T5		–45		23	27	—	
Receive Signal to Distortion Ratio	SD R1	1020	3	*1	36	43	—	dB
	SD R2		0		36	41	—	
	SD R3		–30		36	40	—	
	SD R4		–40		30	33.5	—	
	SD R5		–45		25	30	—	
Transmit Gain Tracking	GT T1	1020	3		–0.3	+0.01	+0.3	dB
	GT T2		–10		Reference			
	GT T3		–40		–0.3	0	+0.3	
	GT T4		–50		–0.5	–0.03	+0.5	
	GT T5		–55		–1.2	–0.05	+1.2	
Receive Gain Tracking	GT R1	1020	3		–0.3	–0.06	+0.3	dB
	GT R2		–10		Reference			
	GT R3		–40		–0.4	+0.2	+0.4	
	GT R4		–50	*2	–1.0	+0.62 +0.20	+1.0	
	GT R5		–55	*2	–1.2	+0.65 +0.3	+1.2	

*1 Psophometric filter is used
*2 Upper is specified for the μ-law, lower for the A-law

AC Characteristics (Continued)

(V_{DD} =2.7 V to 3.8 V, Ta = –30°C to +85°C)

Parameter	Symbol	Freq. (Hz)	Level (dBm0)	Condition	Min.	Typ.	Max.	Unit
Idle Channel Noise	Nidle T	—	—	AIN = SG *1 *2	—	–73.5	–69	dBm0p
						–71.5	–68	
	Nidle R	—	—	*1 *3	—	–76	–74	
Absolute Level (Initial Difference)	AV T	1020	0	V_{DD} = 3.0 V Ta = 25°C *4	0.338	0.350	0.362	Vrms
	AV R				0.483	0.500	0.518	
Absolute Level (Deviation of Temperature and Power)	AV Tt			V_{DD} = 2.7 V to 3.8 V Ta = –30 to +85°C *4	–0.2	—	+0.2	dB
	AV Rt				–0.2	—	+0.2	dB
Absolute Delay	Td	1020	0	A to A BCLK = 64 kHz	—	—	0.60	ms
Transmit Group Delay	t_{gd} T1	500	0	*5	—	0.19	0.75	ms
	t_{gd} T2	600			—	0.11	0.35	
	t_{gd} T3	1000			—	0.02	0.125	
	t_{gd} T4	2600			—	0.05	0.125	
	t_{gd} T5	2800			—	0.07	0.75	
Receive Group Delay	t_{gd} R1	500	0	*5	—	0.00	0.75	ms
	t_{gd} R2	600			—	0.00	0.35	
	t_{gd} R3	1000			—	0.00	0.125	
	t_{gd} R4	2600			—	0.09	0.125	
	t_{gd} R5	2800			—	0.12	0.75	
Crosstalk Attenuation	CR T	1020	0	TRANS → RECV	75	80	—	dB
	CR R			RECV → TRANS	70	76	—	
	CR CH			CH to CH	75	80	—	

*1 Psophometric filter is used
*2 Upper is specified for the μ-law, lower for the A-law
*3 Input "0" code to PCMIN
*4 AVT is defined between GSX and DOUT and AVR between DIN and AOUT
*5 Minimum value of the group delay distortion

AC Characteristics (Continued)

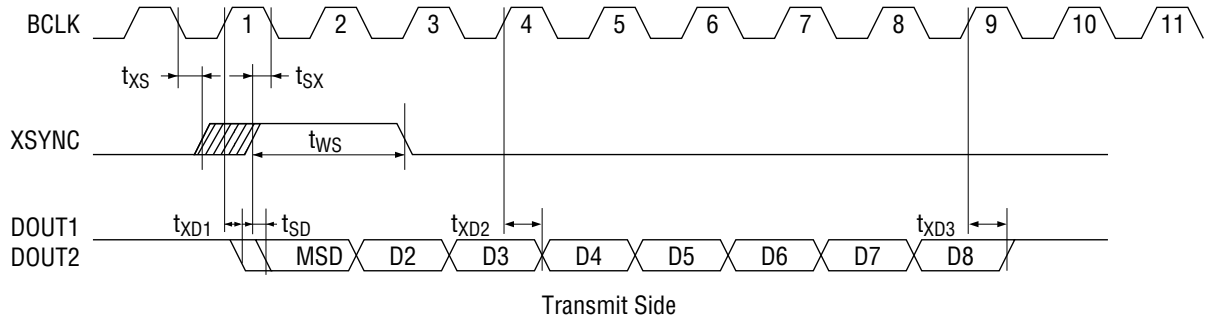
(V_{DD} = 2.7 V to 3.8 V, Ta = –30°C to +85°C)

Parameter	Symbol	Freq. (Hz)	Level (dBm0)	Condition	Min.	Typ.	Max.	Unit
Discrimination	DIS	4.6 kHz to 72 kHz	0	0 to 4000 Hz	30	32	—	dB
Out-of-band Spurious	S	300 to 3400	0	4.6 kHz to 100 kHz	—	–37.5	–35	dBm0
Intermodulation Distortion	IMD	fa = 470 fb = 320	–4	2fa – fb	—	–52	–35	dBm0
Power Supply Noise Rejection Ratio	PSR T	0 to 50 kHz	50 mV_{PP}	*6	—	30	—	dB
	PSR R							
Digital Output Delay Time	t_{SD}	C_L = 100 pF + 1 LSTTL			20	—	200	ns
	t_{XD1}				20	—	200	
	t_{XD2}				20	—	200	
	t_{XD3}				20	—	200	

*6 The measurement under idle channel noise

TIMING DIAGRAM

Transmit Timing



Receive Timing

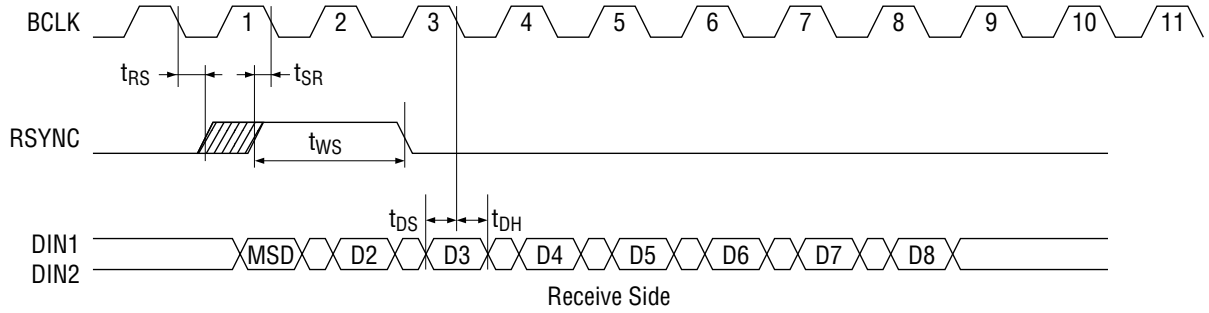


Figure 1 Timing Diagram in the Parallel Mode (CHPS = 1)

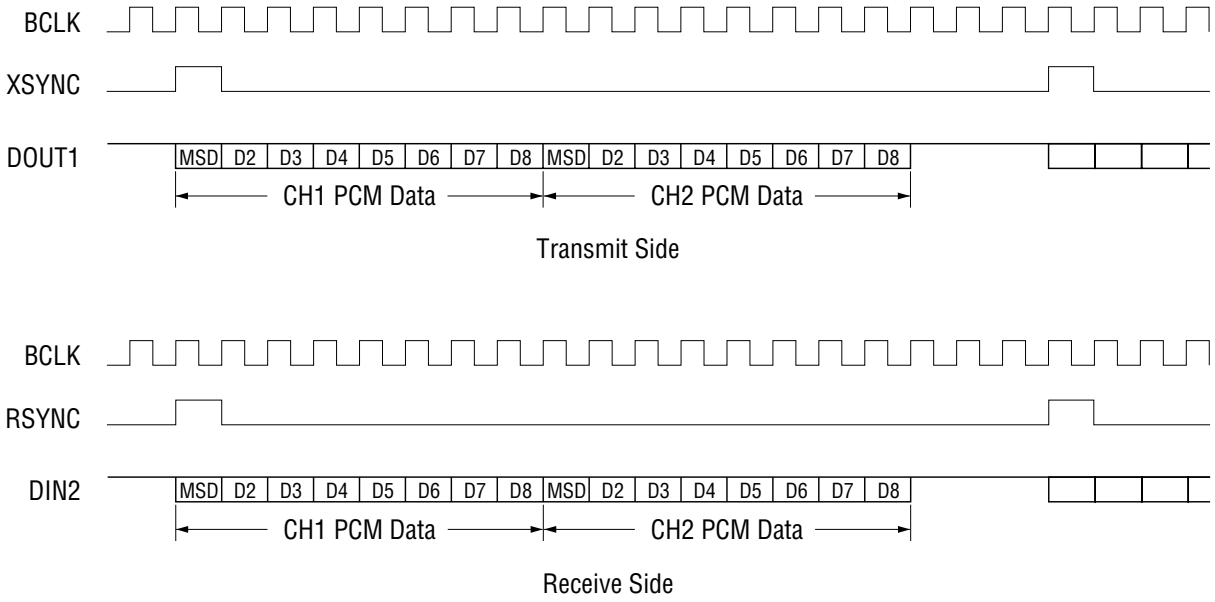
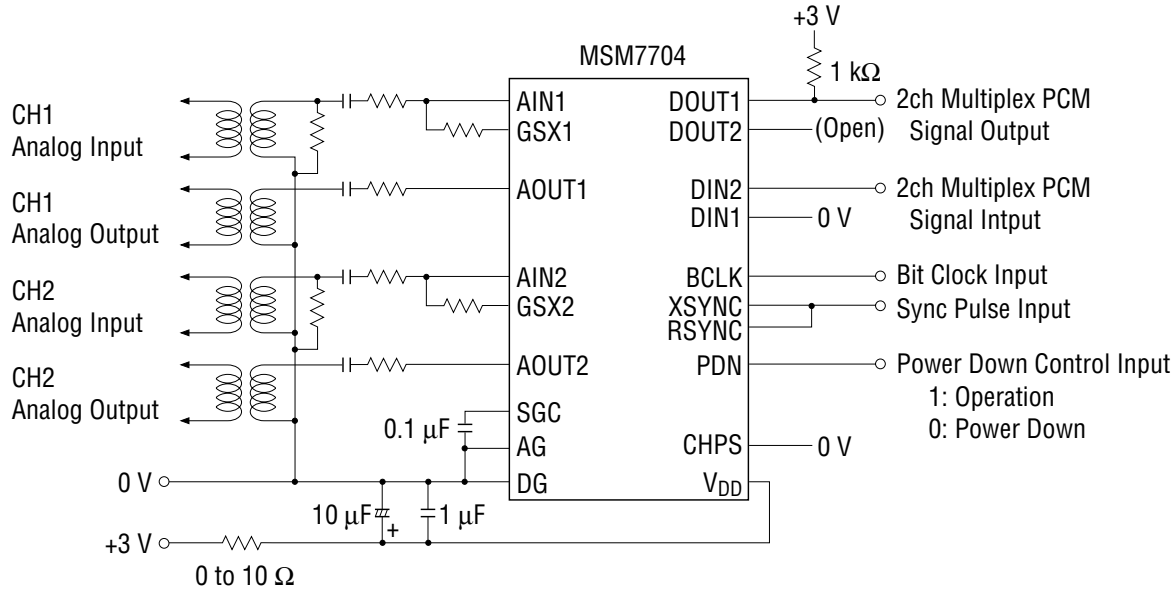


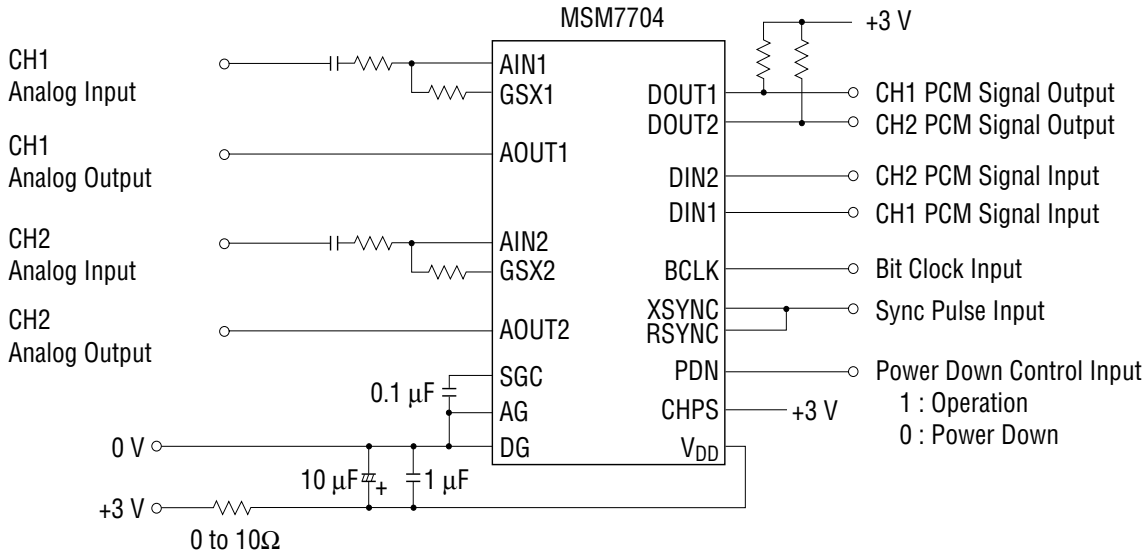
Figure 2 Timing Diagram in the Serial Mode (CHPS = 0)

APPLICATION CIRCUIT

Example of Basic Connection (PCM Serial Mode Operation)



PCM Parallel Mode



The AOUT1 and AOUT2 output signals swing ±1.0 V above and below the offset level of V_{DD}/2.

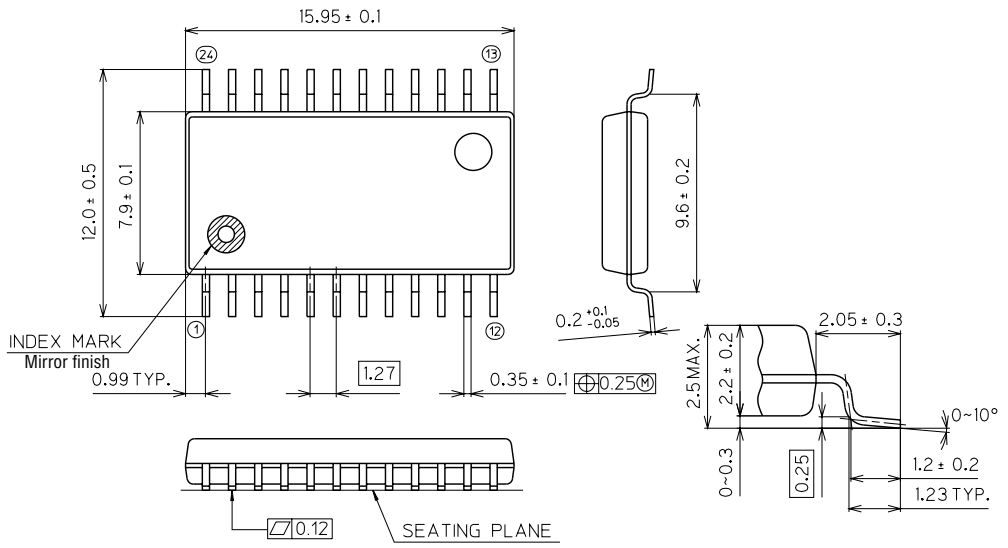
RECOMMENDATIONS FOR ACTUAL DESIGN

- To assure proper electrical characteristics, use bypass capacitors with excellent high frequency characteristics for the power supply and keep them as close as possible to the device pins.
- Connect the AG pin and the DG pin each other as close as possible. Connect to the system ground with low impedance.
- Mount the device directly on the board when mounted on PCBs. Do not use IC sockets. If an IC socket is unavoidable, use the short lead type socket.
- When mounted on a frame, use electro-magnetic shielding, if any electro-magnetic wave source such as power supply transformers surround the device.
- Keep the voltage on the V_{DD} pin not lower than –0.3 V even instantaneously to avoid latch-up phenomenon when turning the power on.
- Use a low noise (particularly, low level type of high frequency spike noise or pulse noise) power supply to avoid erroneous operation and the degradation of the characteristics of these devices.

PACKAGE DIMENSIONS

(Unit : mm)

SOP24-P-430-1.27-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 µm or more
Package weight (g)	0.58 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).