
MSM7584C

 $\pi/4$ Shift QPSK MODEM/ADPCM CODEC

GENERAL DESCRIPTION

The MSM7584C is a CMOS IC developed for use with digital cordless telephones. The device provides a $\pi/4$ shift QPSK modem function and a CODEC function which performs transcoding between the voice band analog signal and 32 kbps ADPCM data.

The MSM7584C is ideal for use in a handset of the PHS (Personal Handyphone System).

FEATURES

($\pi/4$ Shift QPSK Modem)

- Built-in root Nyquist filter (α (rolloff rate) = 0.5) for the baseband limiter
- Differential I and Q analog outputs
- The DC offset and gain can be adjusted with respect to the differential I and Q analog outputs
- Completely digitized $\pi/4$ shift QPSK demodulator system
- Input IF signal frequency of 1.2 MHz or 10.8 MHz is available.
- Built-in A/D converter for RSSI detection

(ADPCM CODEC)

- ADPCM : ITU-T Recommendations G.721 (32 kbps)
- Transmit/receive full duplex capability
- PCM interface code format: selectable between μ -law and A-law
- Built-in transmit/receive mute function and transmit/receive programmable gain setting function
- Side tone path formation and level adjustment capabilities
- Built-in DTMF tone and other tones
- Built-in VOX function
- Built-in speech recording/playing interface
- Built-in 150 Ω driving OP AMP
- Built-in various analog switches

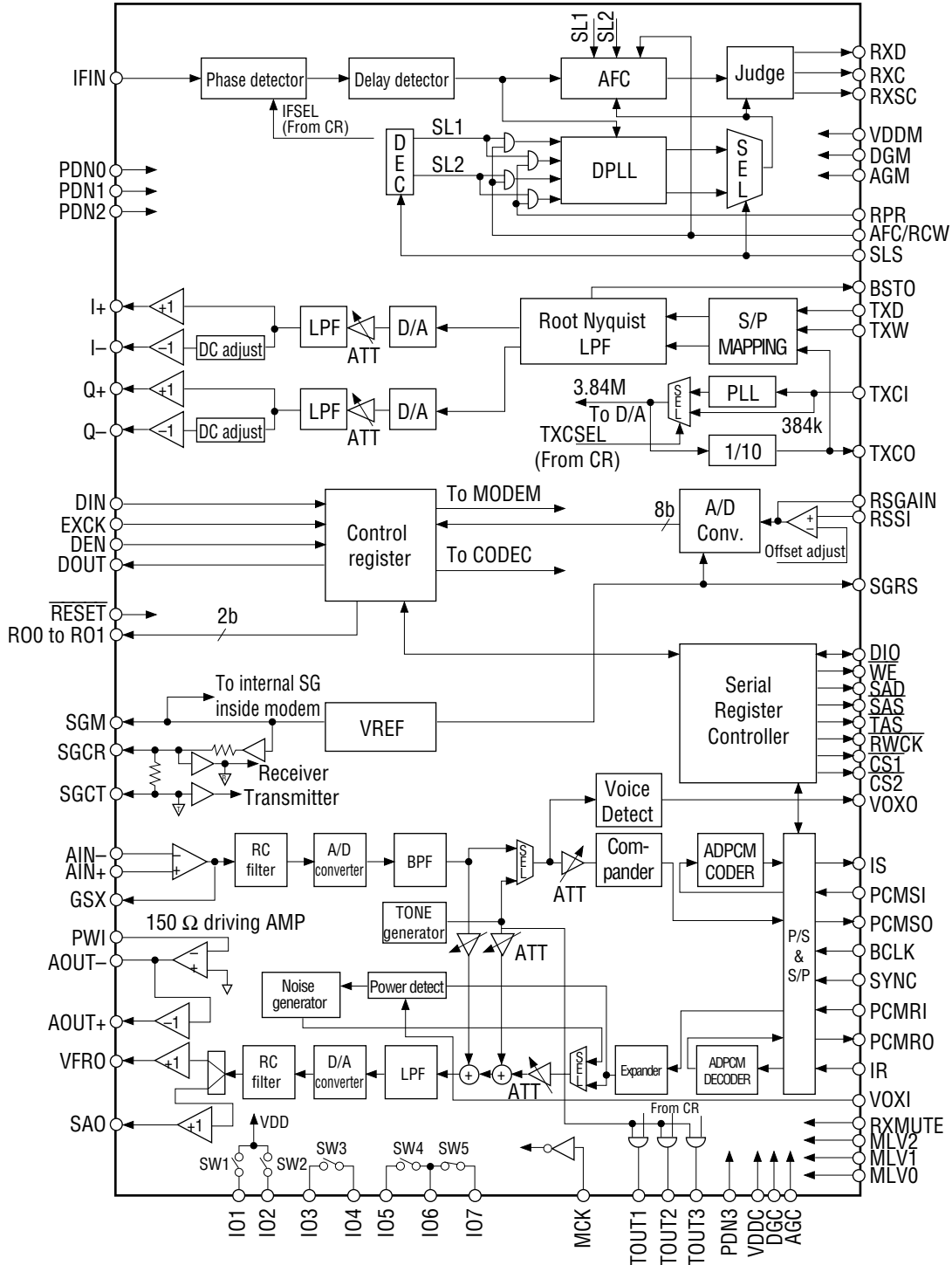
(Common)

- Single 3V power supply (V_{DD} : 2.7 V to 3.6 V)
- Mode setting through serial interface
- Low power consumption

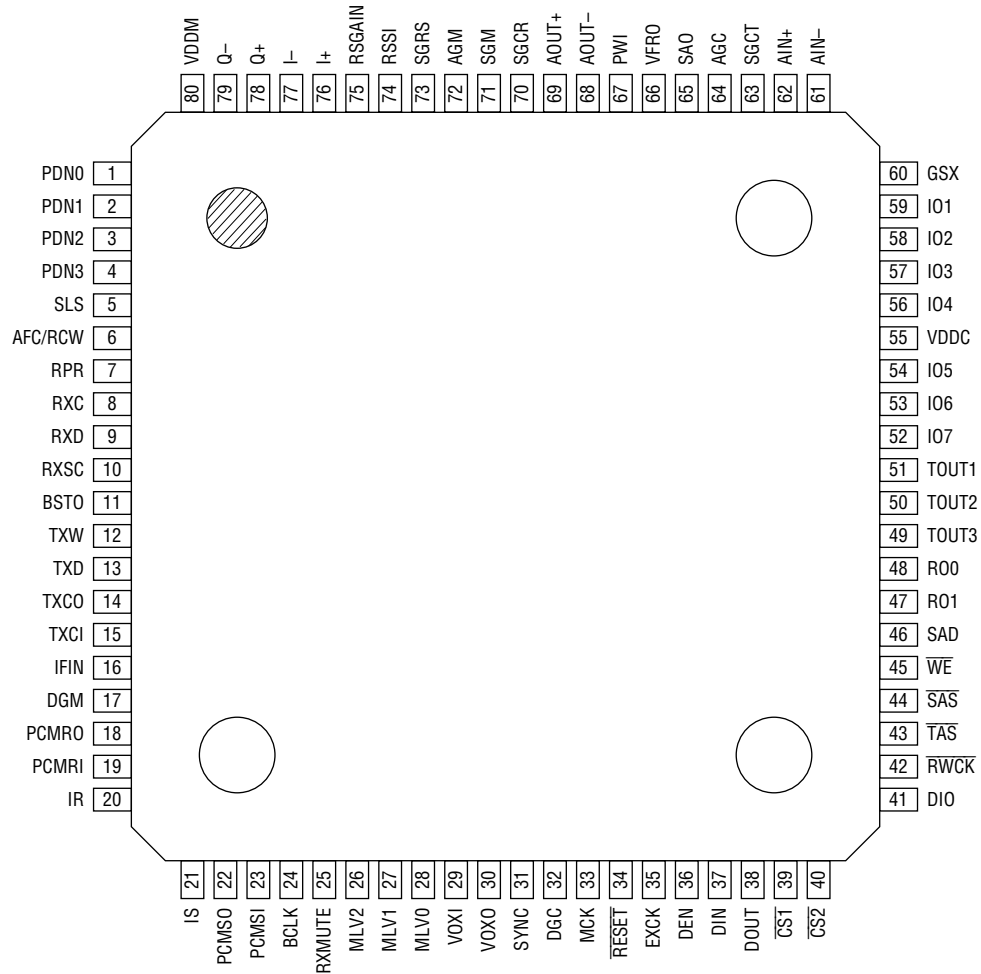
When the modem unit is operating :	13 mA Typ. ($V_{DD} = 3.0$ V)
When the ADPCM CODEC unit is operating :	7 mA Typ. ($V_{DD} = 3.0$ V)
When in the power down mode :	0.03 mA Typ. ($V_{DD} = 3.0$ V)

- Package:
80-pin plastic TQFP (TQFP80-P-1212-0.50-K) (Product name : MSM7584CTS-K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



80-Pin Plastic TQFP

PIN AND FUNCTIONAL DESCRIPTIONS

(ADPCM CODEC)

AIN+, AIN-, GSX

Transmit analog inputs and transmit level adjustment pin.

The AIN- input is connected to the inverting input of the internal transmit amplifier and AIN+ input is connected to the non-inverting input. The GSX pin is connected to the output pin of the amplifier.

See Figure 1 for level adjustment.

VFRO, SAO

Receive analog output and sounder output.

VFRO is a receive filter output pin and SAO is a sounder output pin. These outputs can directly drive the load of over 10 k Ω . When the system is in the power down mode, these outputs become high impedance.

AOUT+, AOUT-, PWI

Input and outputs for internal operation amplifier.

See Figure 1 for connection. When the system is in the power down mode, these outputs become high impedance. The AOUT- and AOUT+ outputs can directly drive the load of over 150 Ω .

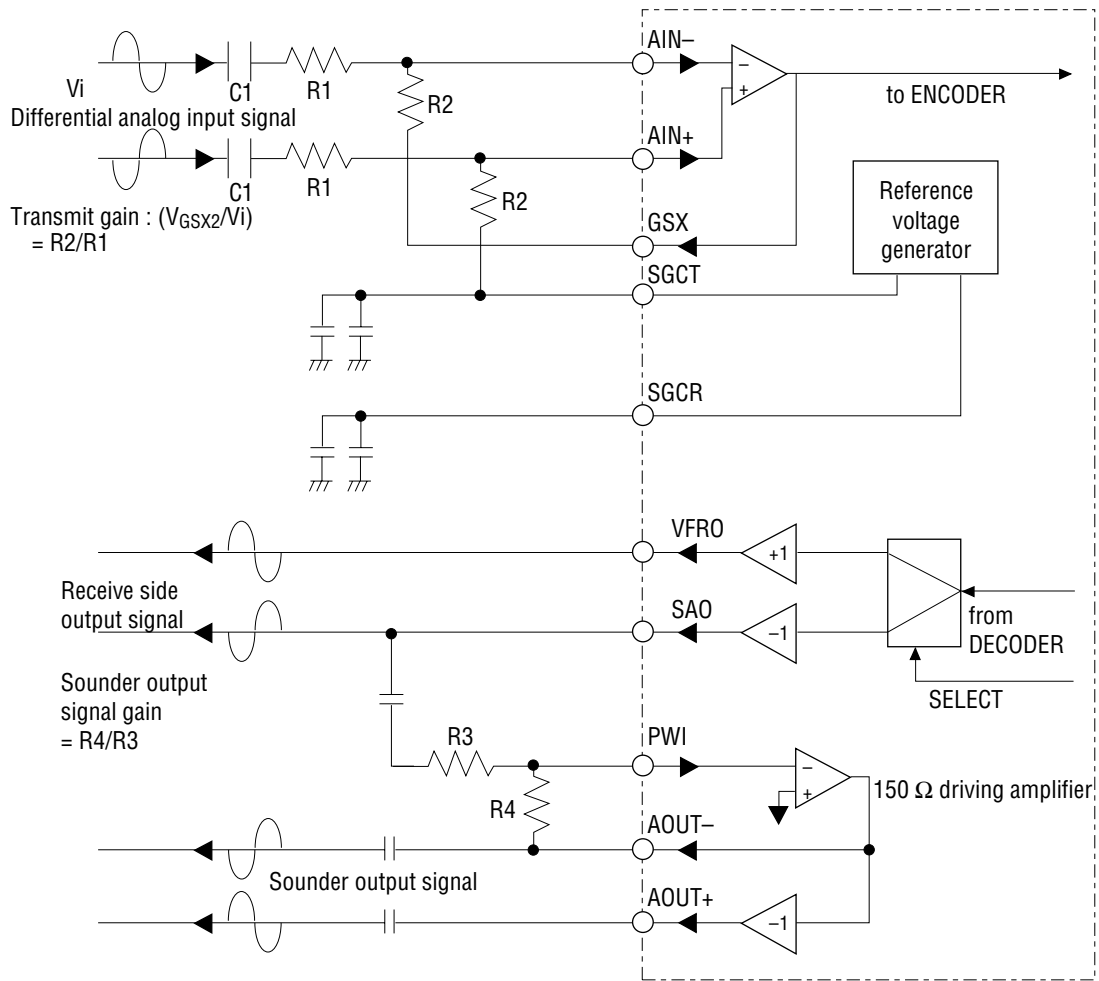


Figure 1 Analog Interface

SGCT, SGCR

Outputs for CODEC analog signal ground.

The output voltage is approximately 1.4 V. Insert 10 μ F and 0.1 μ F bypass capacitors (ceramic type) between these pins and the AG pin. When the device is in power down mode, the output is 0 V.

SGCT is used for transmitting and SGCR is for receiving.

AGC

ADPCM CODEC analog ground (0 V).

DGC

ADPCM CODEC digital ground (0 V).

Since this pin is internally separated from AGC and AGM (modem ground pin), this pin must be connected to these pins as close as possible on the circuit board.

VDDC

ADPCM CODEC 3 V power supply.

Connect this pin to the MODEM power Supply VDDM.

PDN3

ADPCM CODEC power down control input.

When this pin is set to "0" level, the device enters power down mode.

During normal operation mode, set this pin to "1" level.

The power down mode is controlled by CR0 - B5 of the control register ORed with the signal from the PDN3 pin. Therefore, when using this pin, set CR0 - B5 to digital "0".

PCMSO

Transmit PCM data output.

This PCM output signal is output from MSB synchronously with the rising edge of BCLK and XSYNC.

PCMSI

Transmit PCM data input.

This signal is converted to the ADPCM data. The PCM signal is shifted in on the falling edge of BCLK. Normally, this pin is connected to PCMSO.

PCMRO

Receive PCM data output.

The PCM signal is the output signal after ADPCM decoder processing. This signal is serially output from the MSB synchronously with the rising edge of BCLK and RSYNC.

PCMRI

Receive PCM data input.

The PCM input signal is shifted in on the rising edge of BCLK input from MSB. Normally, this pin is connected to PCMRO.

IS

Transmit ADPCM signal output.

This signal is the output signal after ADPCM encoding, and is serially output from MSB synchronously with the rising edge of BCLK and XSYNC. This pin is an open drain output which requires a pull-up resistor and goes to a high impedance state during power-down mode.

IR

Receive ADPCM signal input.

Input data is shifted in serially from MSB on the rising edge of BCLK synchronously with RSYNC.

BCLK

Shift clock input for the PCM data (PCMSO, PCMSI, PCMRO, PCMRI) and the ADPCM data (IS, IR) .

The frequency ranges from 64 kHz to 2048 kHz.

SYNC

8 kHz synchronous signal input for transmit/receive PCM and ADPCM data.

This signal should be synchronous with BCLK. SYNC is used for indicating MSB of the transmit serial PCM and ADPCM data stream.

RXMUTE

Receive voice path mute control input. When this pin is at "0" level, the device enters normal mode. When at "1" level, the voice level is muted to the value which has been set by MLV2, MLV1, MLV0.

This pin is internally ORed like CR1-B3. Therefore, when using this pin, set CR1-B3 to digital "0".

MLV2, MLV1, MLV0

Receive voice path mute level setup signals. See the control register map for control method. These signals are internally ORed with CR1-B2, B1, B0, respectively. Therefore, when using this pin, set these register data to digital "0".

VOXO

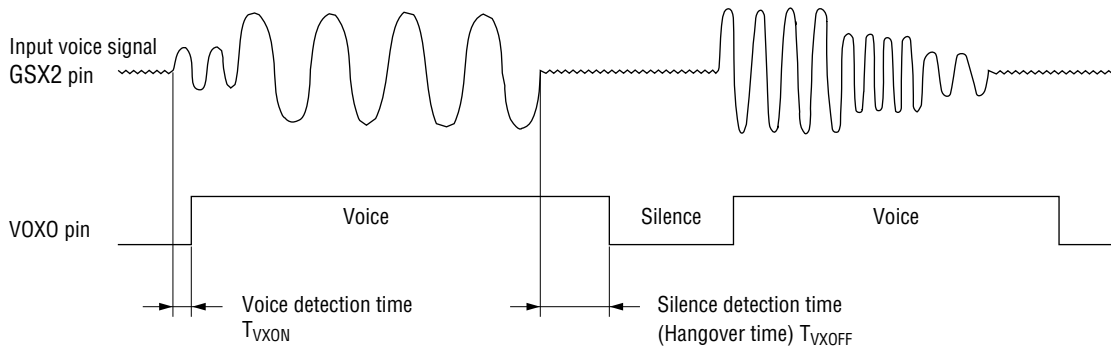
Transmit VOX function signal output.

VOX function is used to recognize the presence or absence of the transmit voice signal by detecting the signal energy. "1" and "0" levels on this pin correspond to the presence and the absence, respectively. This result also appears at the register CR7 - B7. The signal energy detect threshold is set by the control register data CR6 - B6, B5.

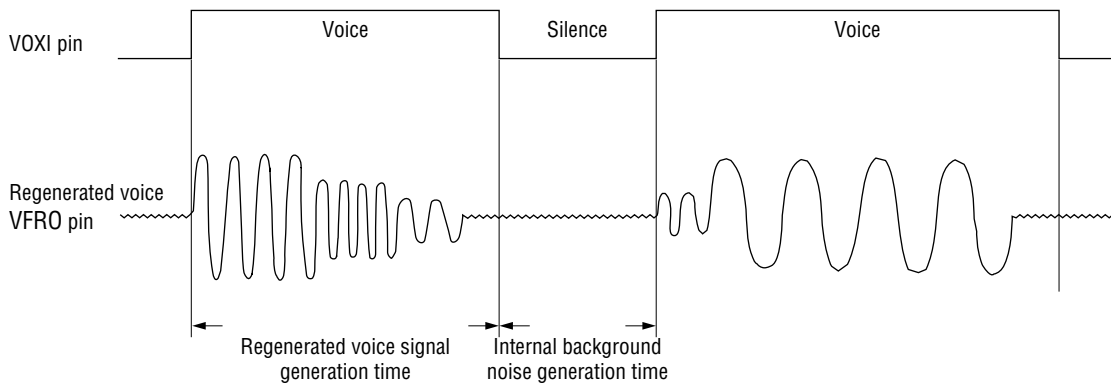
VOXI

Signal input for receive VOX function.

The "1" level on VOXI indicates the presence of voice signal, in which case the decoder block processes normal receive signal and the voice signal appears at analog output pins. The "0" level indicates the absence of voice signal, in which case the background noise generated in this device is transferred to the analog output pins. The background noise amplitude is set by the control register CR6. Because this signal is ORed with the register data CR6 - B3, the control register data CR6 - B3 should be set to digital "0".



(a) Transmission Side VOX Function Timing Diagram



(b) Receive Side VOX Function Timing Diagram

Note: The VOXO and VOXI pin function are enabled when CR6 - B7 is set to "1".

Figure 2 VOX Function

(Voice Recording Serial Controller)**DIO**

Input/output pin that outputs write data and to input read data.

Connect this pin to the DIN pin, DOUT pin of the serial registers and the DOUT pin of the serial voice ROM. If neither a serial register nor a serial voice ROM is connected, pull this pin up with an approx. 50 kΩ resistor.

 $\overline{\text{WE}}$

Output that selects the read mode or write mode.

Connect this pin to the $\overline{\text{WE}}$ pin of the serial registers.

SAD

Read/write start address output.

Connect this pin to the SAD pin of the serial registers and the SADX pin of the serial voice ROM.

 $\overline{\text{SAS}}$

Output of clocks for writing serial address.

Connect this pin to the $\overline{\text{SAS}}$ pin of the serial registers and the $\overline{\text{SASX}}$ and $\overline{\text{SASY}}$ pins of the serial voice ROM.

 $\overline{\text{TAS}}$

Strobe signal output that sets the serial address which is entered from the SAD pin, to the address counter inside the serial register/serial voice ROM.

Connect this pin to the $\overline{\text{TAS}}$ pins of the serial registers and serial voice ROM.

 $\overline{\text{RWCK}}$

Output of clocks for reading data from or writing data to the serial registers.

Connect this pin to the $\overline{\text{RWCK}}$ pin of the serial registers and the $\overline{\text{PDCK}}$ pin of the serial voice ROM.

 $\overline{\text{CS1}}$, $\overline{\text{CS2}}$

Chip select pins.

Connect $\overline{\text{CS1}}$ to the $\overline{\text{CS}}$ pin of the serial registers.

Connect $\overline{\text{CS2}}$ to the $\overline{\text{CS}}$ pin of the serial voice ROM.

(Modem)**TXD**

384 kbps transmit data input.

TXCI

Transmit clock input.

When the control register CR14 - B6 is "0", a 384 kHz clock pulse synchronous with TXD should be input to this pin. This clock pulse should be continuous because this device use APLL to generate an internal clock pulse.

When CR14 - B6 is "1", a 3.84 MHz clock pulse should be input to this pin. When the 3.84 MHz clock pulse is applied, a 384 kHz clock pulse, which is generated by dividing the TXCI by 10, is output to the TXCO pin. The transmit data, synchronous to the 384 kHz clock pulse, should be input to the TXD. In this case the devices do not use APLL, and the 3.84 MHz clock pulse need not be continuous. (Refer to Fig. 3)

TXCO

Transmit clock output.

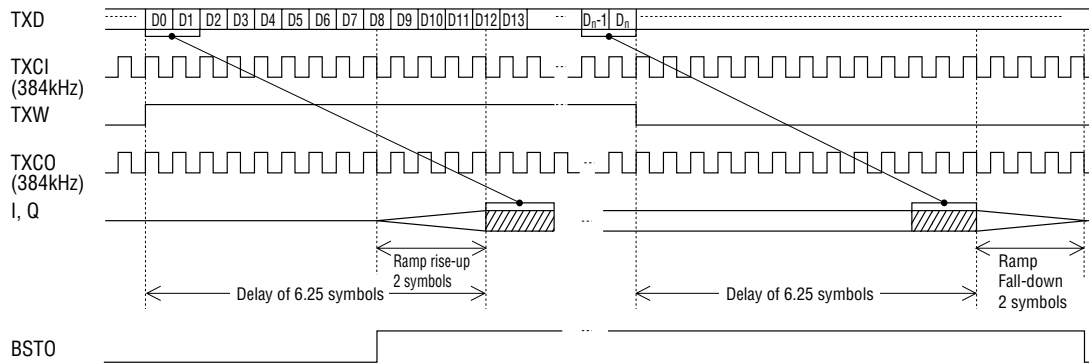
When CR14 - B6 is "0", TXCO outputs the 384 kHz clock pulse (APLL output) for monitoring purposes. When CR14 - B6 is "1", this pin outputs a 384 kHz clock pulse generated by dividing the TXCI input by 10. (Refer to Fig. 3)

TXW

Transmit data window signal input.

The transmit timing signal for the burst data is input to this pin. If TXW is "1", the modulation data is output. (Refer to Fig. 3)

(1) CR14 – B6 = "0"



(2) CR14 – B6 = "1"

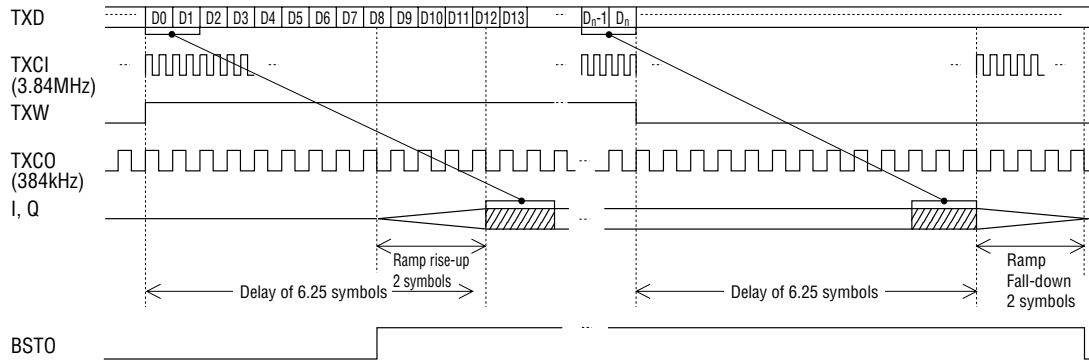


Figure 3 Transmit Timing Diagram

BSTO

BSTO is the modulator side burst output position specification signal.

The burst time and position of the I and Q analog output including the lamp bits are output. (Refer to Fig. 3)

I+, I-

Quadrature modulation signal I Component differential analog output.

Their output levels are 500 mV_{PP} (maximum) with 1.6 Vdc as the center value. The output pin load conditions are: $R \geq 10 \text{ k}\Omega$, $C \leq 20 \text{ pF}$. The gain of these pins can be adjusted using the control register CR15 - B7 to B4, and the offset voltage at the I- pin can be adjusted using CR16 - B7 to B3.

Q+, Q-

Quadrature modulation signal Q component differential analog outputs.

Their output levels are 500 mV_{PP} (maximum) with 1.6 Vdc as the center value. The output pin load conditions are: $R \geq 10 \text{ k}\Omega$, $C \leq 20 \text{ pF}$. The gain of these pins can be adjusted using the control register CR15 - B7 to B4, and the offset voltage at the Q- pin can be adjusted by using CR17 - B7 to B3.

SGM

MODEM internal reference voltage output.

The output voltage value is approximately 2.0 V. Insert a bypass capacitor of approximately 0.1 μF between this pin and the AGM pin.

PDN0, PDN1, PDN2

Various power down controls.

PDN0 controls the standby mode/communication mode; PDN1 controls the modulator; PDN2 controls the demodulator. Refer to Table 1 for details.

Table 1 Description of Modem Power Down Control

	PDN0	PDN2	PDN1	Operation State	Mode Name
Standby Mode	0	0/1	0	Entire system is powered down. The control register is not reset.	Mode A
	0	0/1	1	Modulator unit is powered off. (VREF and PLL also powered off.) Demodulator unit is powered on.	Mode B
Communication Mode	1	0	0	Modulator unit is powered off. (VREF and PLL are powered on.) I and Q outputs are in a high impedance state. Only the demodulator clock regenerator unit is powered on.	Mode C
	1	0	1	Modulator unit is powered off. (VREF and PLL are powered on.) I and Q outputs are in a high impedance state. Demodulator unit is powered on.	Mode D
	1	1	0	Modulator unit is powered on. Only the demodulator clock regenerator unit is powered on.	Mode E
	1	1	1	Modulator unit is powered on. Demodulator unit is powered on.	Mode F

VDDM

+3 V power supply for the modem unit.

Connect this pin to the ADPCM CODEC power supply VDDC on the board.

AGM

Modem analog signal ground.

DGM

Modem digital signal ground.

Since this pin is internally separated from AGM, AGC, and DGC, this pin must be connected to these pins on the board.

MCK

Master clock input. The clock frequency is 19.2 MHz.

The master clock must always be input to the ADPCM CODEC and MODEM except the device being in power down mode because the both units share the master clock.

If the input level is less than 2 V, the master clock must be input after DC-component is cut by an approx. 1000 pF capacitor. (See the application circuit example.)

IFIN

Modulated signal input for the demodulator unit.

The CR14 - B4 can select an IF frequency of 1.2 MHz or 10.8 MHz.

RXD, RXC, RXSC

Receive data, receive clock (384 kHz), receive symbol clock (192 kHz) outputs.

When the power is turned on, outputs in which a clock regeneration circuit selected by SLS appear on these output pin.

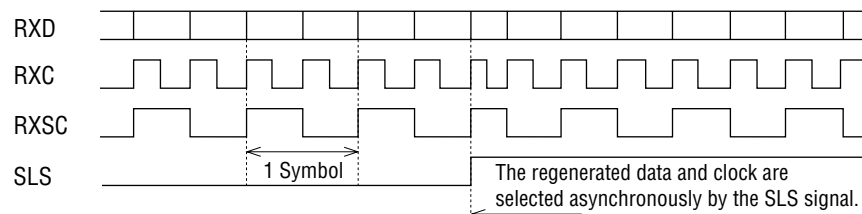


Figure 4 Timing Diagram of RXD, RXC, and RXSC

SLS

Receive side operation slot selection signal.

This device has two clock regeneration circuits and two AFC data memory registers. If SLS is at "0" level, slot 1 is selected; if SLS is at "1" level, slot 2 is selected.

RPR

High-speed phase clock control signal input for the clock regeneration circuit.

If this pin is at "1" level, the clock regeneration circuit enters the high-speed phase clock mode. When the phase difference is less than a defined value, the circuit shifts to the low-speed phase clock mode automatically. If this pin is at "0" level, the circuit is always in the low-speed phase clock mode.

AFC/RCW

AFC operation and clock regeneration range specification signal input.

As shown in Figure 5, AFC information is reset when AFC/RCW and RPR go to "1" level. The AFC operation starts after a certain time elapses.

The average number of AFC operation times is small when RPR is at "1" level.

The average number of AFC operation times is large when RPR is at "0" level.

If AFC/RCW is at "0" level, DPLL will not adjust the phase.

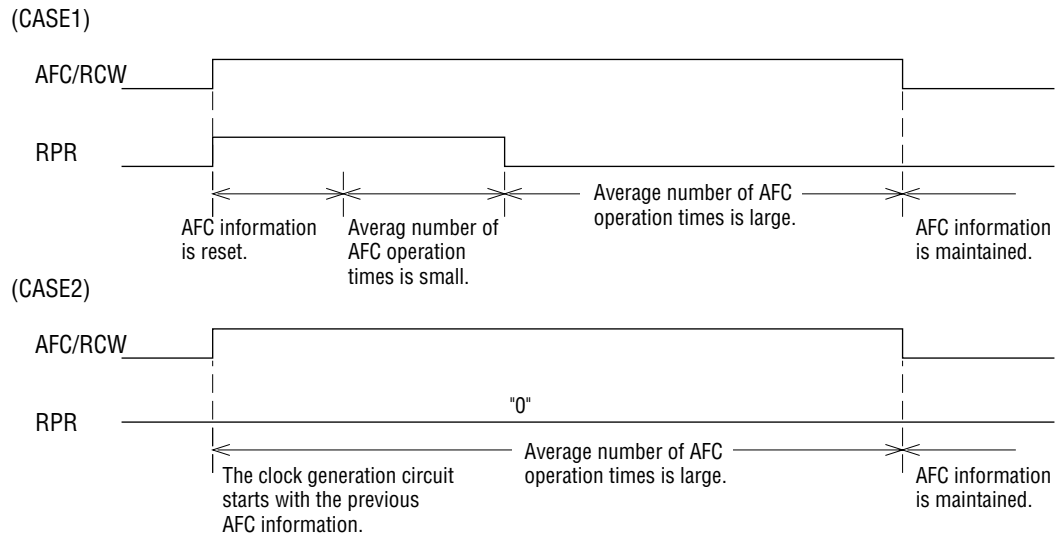


Figure 5 AFC Control Timing Diagram

(Common)

RESET

Device reset input.
The control registers CR0 to CR22 all are reset to the initial values by setting this pin to "0" level.

R0, R1

Output ports for the control register CR21.
The data written in CR21 - B0 and B1 are output on the R0 and R1 pins.
These pins become high impedance when the device is reset.

DEN, EXCK, DIN DOUT

Serial control ports for the microcontroller interface.
The device has 23 bytes of control registers. Data is written and read by the external CPU using these ports. DEN is an enable signal input, EXCK is a data shift clock signal input, DIN is an address/data input, and DOUT is a data output.
The input/output timing is shown in Fig. 6.

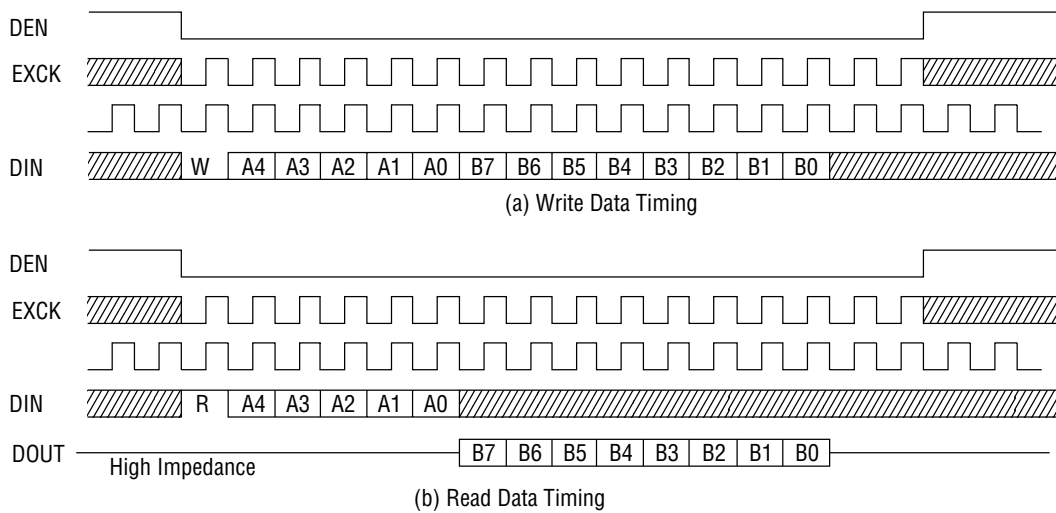


Figure 6 MCU Interface I/O Timing

The control register map is shown in Table 2.
As shown in Fig. 6, data should be written or read in continuous pulses of the EXCK signal or in 16 bits.

IO1 to IO7

Input/output for internal analog switches.
See the control register map (CR22) and circuit configuration for connection information and control method.

TOUT1, TOUT2, TOUT3

Sign bit outputs for the tone generator.
The outputs are controlled by the control register CR22. See the control register map and circuit configuration for connection information and control method.

Table 2 Control Register Map

Register name	Address					Data Description								Register function
	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	
CR0	0	0	0	0	0	A/μ	—	PDN ALL	PDN TX	PDN RX	SA,VF_OUT	SA0/VFRO	SA,VF_PDN	ADPCM control
CR1	0	0	0	0	1	TX ON/OFF	RX ON/OFF	ADPCM RST	TX MUTE	RX MUTE	MLV2	MLV1	MLV0	
CR2	0	0	0	1	0	TX GAIN3	TX GAIN2	TX GAIN1	TX GAIN0	RX GAIN3	RX GAIN2	RX GAIN1	RX GAIN0	
CR3	0	0	0	1	1	S_TONE2	S_TONE1	S_TONE0	T ON/OFF	Tone G3	Tone G2	Tone G1	Tone G0	
CR4	0	0	1	0	0	DTMF/OT	TONE_SEND	TONE5	TONE4	TONE3	TONE2	TONE1	TONE0	
CR5	0	0	1	0	1	SEND/REC	ROM/SR	4M8M/1M	—	—	—	CMD1	CMD0	VOX play mode control
CR6	0	0	1	1	0	VOX ON/OFF	ON LVL1	ON LVL0	OFF TIME	VOX IN	RX_N SEL	N_LV1	N_LV0	
CR7	0	0	1	1	1	VOX OUT	Silence L1	Silence L0	—	—	—	BUSY	RPM	
CR8	0	1	0	0	0	ST0	ST1	ST2	ST3	ST4	ST5	ST6	ST7	
CR9	0	1	0	0	1	ST8	ST9	ST10	ST11	ST12	—	—	—	
CR10	0	1	0	1	0	SPY0	SPY1	SPY2	SPY3	SPY4	SPY5	SPY6	SPY7	
CR11	0	1	0	1	1	SP0	SP1	SP2	SP3	SP4	SP5	SP6	SP7	
CR12	0	1	1	0	0	SP8	SP9	SP10	SP11	SP12	—	—	—	
CR13	0	1	1	0	1	CH0	CH1	CH2	CH3	CH4	—	ADRD	ADWT	
CR14	0	1	1	1	0	—	TXC SEL	MOD OFF	IFSEL	—	—	—	—	
CR15	0	1	1	1	1	Ich GAIN3	Ich GAIN2	Ich GAIN1	Ich GAIN0	Qch GAIN3	Qch GAIN2	Qch GAIN1	Qch GAIN0	
CR16	1	0	0	0	0	Ich Offset4	Ich Offset3	Ich Offset2	Ich Offset1	Ich Offset0	—	—	—	
CR17	1	0	0	0	1	Qch Offset4	Qch Offset3	Qch Offset2	Qch Offset1	Qch Offset0	—	—	—	
CR18	1	0	0	1	0	MODEM TEST3	MODEM TEST2	MODEM TEST1	MODEM TEST0	Local INV1	Local INV0	—	—	
CR19	1	0	0	1	1	AD07	AD06	AD05	AD04	AD03	AD02	AD01	AD00	RSSI A/D control
CR20	1	0	1	0	0	AD Offset4	AD Offset3	AD Offset2	AD Offset1	AD Offset0	—	RS PDN	SEL RS	General I/O
CR21	1	0	1	0	1	—	—	—	—	—	—	RO1	RO0	
CR22	1	0	1	1	0	SW1 CONT	SW2 CONT	SW3 CONT	SW4/5 CONT	AOUT PDN	TOUT3 CONT	TOUT2 CONT	TOUT1 CONT	Switches control

(RSSI-ADC)**RSSI, RSGAIN**

RSSI input and level adjustment.

RSSI is connected to the inverting input pin of the internal amplifier. RSGAIN is connected to the output pin of the amplifier.

Adjust the gain and DC so that the signal amplitude is between 0.7 V and 2.1 V on the RSGAIN pin. See Fig. 7 for connection.

$$\text{Gain: } A = R2/R1 = 1.4 / (V_{\text{max}} - V_{\text{min}})$$

if $R1 + R2 \geq 20 \text{ k}\Omega$

$$\text{DC adjustment value : } V_{\text{adj}} = A / (1+A) \times ((V_{\text{max}} + V_{\text{min}}) / 2 - 1.4)$$

Set the register CR20 to the DC adjustment value nearest to V_{adj} .
See the control register map (CR20) for setup values.

SGRS

Internal reference voltage output for the RSSI - ADC.

The output voltage is 2.0 V. Insert an approx. 0.1 μF bypass capacitor between this pin and the AGM pin.

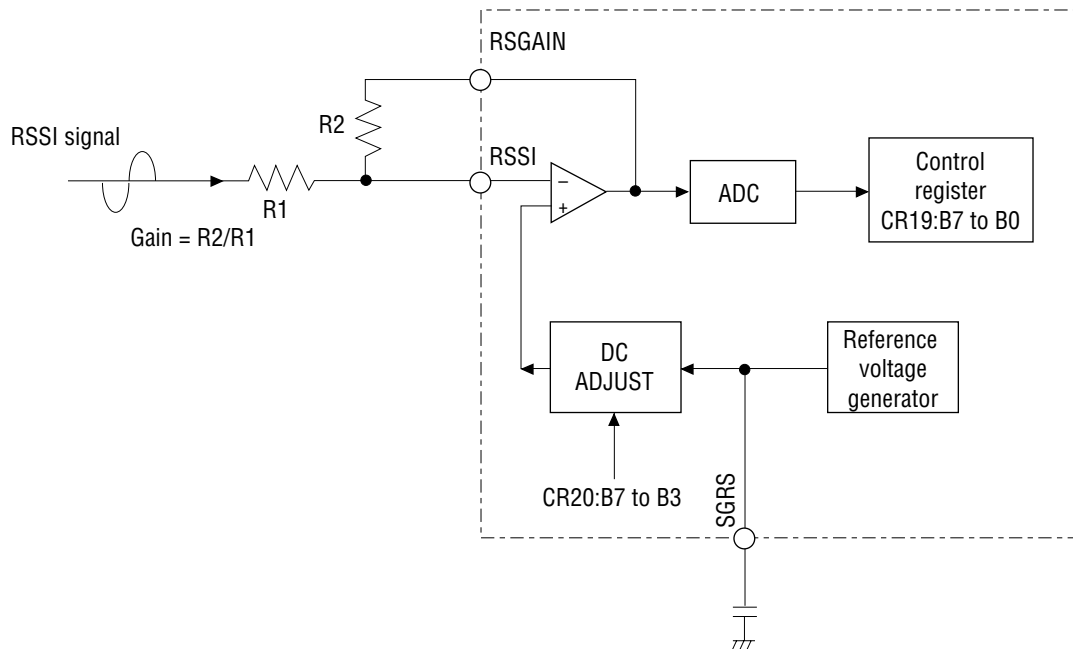


Figure 7 RSSI-ADC Interface

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V _{DD}	—	-0.3 to +5	V
Analog Input Voltage	V _{AIN}	—	-0.3 to V _{DD} + 0.3	V
Digital Input Voltage	V _{DIN}	—	-0.3 to V _{DD} + 0.3	V
Operating Temperature	T _{op}	—	-25 to +70	°C
Storage Temperature	T _{STG}	—	-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{DD} = 2.7 V to 3.6 V, Ta = -25°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit		
Power Supply Voltage	V _{DD}	—	2.7	—	3.6	V		
Operating Temperature Range	Ta	—	-25	—	+70	°C		
High Level Input Voltage	V _{IH}	Input pins fully digital	0.45 × V _{DD}	—	V _{DD}	V		
Low Level Input Voltage	V _{IL}	Input pins fully digital	0	—	0.16 × V _{DD}	V		
Digital Input Rise Time	t _{ir}	Input pins fully digital	—	—	50	ns		
Digital Input Fall Time	t _{if}	Input pins fully digital	—	—	50	ns		
Digital Output Load	R _{DL}	IS (Pull-up resistor)	500	—	—	Ω		
	C _{DL}	Input pins fully digital	—	—	100	pF		
Bypass Capacitor for SG	C _{SG1}	Between SGCT/R and AGC	10 + 0.1	—	—	μF		
Bypass Capacitor for SG	C _{SG2}	Between SGM, AGM and SGRS, AGM	0.1	—	—	μF		
Master Clock Frequency	F _{MCK}	MCK	—	19.2	—	MHz		
Master Clock Duty Ratio	D _{MCK}	MCK	40	50	60	%		
Modem Unit	Modulator Side Input Frequency	F _{TXC1}	TXCI (When CR14 - B6 = "0")	—	384	—	kHz	
		F _{TXC2}	TXCI (When CR14 - B6 = "1")	—	3.84	—	MHz	
	Clock Duty Ratio	D _{CKM}	IFCK, TXCI, EXCK	40	50	60	%	
	IF Input Duty Ratio	D _{CIF}	IFIN	45	50	55	%	
	Transmit Sync Pulse Setting Time	t _{xSM} , t _{sXM}	TXCI↔TXW	Fig.10	—	—	200	ns
t _{dSM} , t _{dHM}		TXCI↔TXD	—		—	200	ns	
CODEC Unit	Bit Clock Frequency	F _{BCK}	BCLK	64	—	2048	kHz	
	Synchronous Signal Frequency	F _{SYNC}	XSYNC, RSYNC	—	8.0	—	kHz	
	Clock Duty Ratio	D _{CKC}	BCLK, EXCKC	40	50	60	%	
	Transmit Sync Pulse Setting Time	t _{xSC} , t _{sXC}	BCLK↔XSYNC	Fig.8	100	—	—	ns
	Receive Sync Pulse Setting Time	t _{rSC} , t _{sRC}	BCLK↔RSYNC		100	—	—	ns
	Synchronous Signal Width	t _{wSC}	XSYNC, RSYNC		1 BCLK	—	125μs-1BCLK	μs
	PCM, ADPCM Setup Time	t _{DSC}	—		100	—	—	ns
PCM, ADPCM Hold Time	t _{DHC}	—	100		—	—	ns	

ELECTRICAL CHARACTERISTICS

DC Characteristics

 $(V_{DD} = 2.7\text{ V to } 3.6\text{ V, } T_a = -25^\circ\text{C to } +70^\circ\text{C})$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current (Modem) (When CODEC is in a Power Down State)	I _{DD1}	Mode A (When $V_{DD} = 3.0\text{ V}$)	—	0.03	0.1	mA
	I _{DD2}	Mode B (When $V_{DD} = 3.0\text{ V}$)	—	4.5	10.0	mA
	I _{DD3}	Mode C (When $V_{DD} = 3.0\text{ V}$)	—	4.5	10.0	mA
	I _{DD4}	Mode D (When $V_{DD} = 3.0\text{ V}$)	—	10.5	22.0	mA
	I _{DD5}	Mode E (When $V_{DD} = 3.0\text{ V}$)	—	8.5	18.0	mA
	I _{DD6}	Mode F (When $V_{DD} = 3.0\text{ V}$)	—	13.0	27.0	mA
Power Supply Current (CODEC) (When Modem is in a Power Down State)	I _{DD7}	When operating*	—	7.0	15.0	mA
	I _{DD8}	(When no signal, and $V_{DD} = 3.0\text{ V}$)	—	11.0	18.0	mA
	I _{DD9}	When powered down (When $V_{DD} = 3.0\text{ V}$)	—	0.03	0.1	mA
Power Supply Current (RSSI-ADC)	I _{DD10}	CR22-B3 = "1" (When $V_{DD} = 3.0\text{ V}$)	—	2.0	4.0	mA
Input Leakage Current	I _{IH}	$V_I = V_{DD}$	—	—	2.0	μA
	I _{IL}	$V_I = 0\text{ V}$	—	—	0.5	μA
High Level Output Voltage	V _{OH1}	I _{OH} = 0.4 mA	$0.5 \times V_{DD}$	—	V_{DD}	V
	V _{OH2}	I _{OH} = 1 μA	$0.8 \times V_{DD}$	—	V_{DD}	V
Low Level Output Voltage	V _{OL}	I _{OL} = -1.2 mA (IS pin is pulled up with 500 Ω resistor)	0	0.2	0.4	V
Output Leakage Current	I _O	IS pin	—	—	10	μA
Input Capacitance	C _{IN}	—	—	5	—	pF

* I_{DD7} applies when CRC0 - B0 = "0" and CR22 - B3 = "0"; I_{DD8} applies when operating in other conditions.

Analog Interface Characteristics (RSSI - ADC)(V_{DD} = 2.7 V to 3.6 V, T_a = -25°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Resistance	R _{INAD}	RSSI	10	—	—	MΩ
Output Resistance Load	R _{LCAD}	RSGAIN	10	—	—	kΩ
Output Capacitance Load	C _{LAD}	RSGAIN	—	—	—	pF
Input Voltage Range	V _{INAD}	When a RSGAIN signal is output.	0.7	—	2.1	V
Offset Voltage Adjust Range	O _{VLAD}	—	-400	—	375	mV
Offset Voltage Adjust Accuracy	O _{VSAD}	When offset voltage is adjusted per LSB step.	-12.5	—	12.5	mV
A/D Conversion Resolution	R _{ESAD}	One LSB step	—	5.5	—	mV

Digital Interface Characteristics (RSSI - ADC)(V_{DD} = 2.7 V to 3.6 V, T_a = -25°C to +70°C)

Parameter	Symbol	Condition	Reference	Min.	Typ.	Max.	Unit
Output Delay Time	t _{DAD}	C _{load} = 50 pF	Fig.12	—	5	—	μs

Analog Interface Characteristics (Modem)(V_{DD} = 2.7 V to 3.6 V, T_a = -25°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output Resistance Load	R _{LIQ}	I+, I-, Q+, Q-	10	—	—	kΩ
Output Capacitance Load	C _{LIQ}	I+, I-, Q+, Q-	—	—	20	pF
Output DC Voltage Level	V _{DCM}	I+, I-, Q+, Q- (TXW = 0)	1.55	1.6	1.65	V
Output AC Voltage Level	V _{ACM}	I+, I-, Q+, Q- (For TXD = 0 continuous input)	—	360	—	mV _{PP}
Output DC Voltage Adjustment Level Range	D _{CVL}	—	—	±45	—	mV
Output AC Voltage Adjustment Level Range	A _{CVL}	—	—	±4	—	%
Out-of-band Spectrum	P600	600 kHz detuning	—	—	60	dB
	P900	900 kHz detuning	—	—	65	dB
Modulation Accuracy	E _{VM}	—	—	1.0	3.0	% rms
Demodulator Side IF Input Level	I _{FV}	IFIN input level	0.5	—	V _{DD}	V _{PP}
IFIN Input Impedance	R _{IF}	DC impedance	—	20	—	kΩ
SGM Output Voltage	V _{SGM}	—	—	2.0	—	V
SGM Output Impedance	R _{SGM}	—	—	1.5	—	kΩ
MCK Input Level	I _X	—	0.7	—	2.0	V _{PP}
MCK Input Impedance	R _X	DC impedance	—	20	—	kΩ

Digital Interface Characteristics (Modem)(V_{DD} = 2.7 V to 3.6 V, T_a = -25°C to +70°C)

Parameter	Symbol	Condition	Reference	Min.	Typ.	Max.	Unit
Transmit Digital I/O Setting Time	t _{XDM1,2}	Cload = 50 pF	Fig. 10	0	—	200	ns
	t _{XDM3,4}			0	—	400	ns
Receive Digital I/O Setting Time	t _{RDM1,2}	Cload = 50 pF	Fig. 11	0	—	200	ns

Analog Interface Characteristics (CODEC) $(V_{DD} = 2.7 \text{ V to } 3.6 \text{ V, } T_a = -25^\circ\text{C to } +70^\circ\text{C})$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Resistance	R_{INC}	AIN+, AIN-, PWI	10	—	—	$M\Omega$
Output Resistance Load	R_{LC1}	GSX	20	—	—	$k\Omega$
	R_{LC2}	VFRO, SAO	10	—	—	$k\Omega$
	R_{LC3}	AOUT	150	—	—	Ω
Output Capacitance Load	C_{LC1}	GSX	—	—	100	pF
	C_{LC2}	VFRO, SAO	—	—	100	pF
	C_{LC3}	AOUT	—	—	100	pF
Output Voltage Level (*1)	V_{OC1}	GSX ($R_L = 20 \text{ k}\Omega$)	—	—	1.3	V_{PP}
	V_{OC2}	VFRO, SAO ($R_L = 10 \text{ k}\Omega$)	—	—	1.3	V_{PP}
	V_{OC3}	AOUT ($R_L = 150 \Omega$)	—	—	1.3	V_{PP}
Offset Voltage	V_{OFC1}	VFRO, SAO	-100	—	100	mV
	V_{OFC2}	GSX, AOUT	-20	—	20	mV
SGCT, SGCR Output Voltage	V_{SGC}	SGCT, SGCR	—	1.4	—	V
SGCT Output Impedance	R_{SGCT}	SGCT	—	40	80	$k\Omega$
SGCR Output Impedance	R_{SGCR}	SGCR	—	4	8	$k\Omega$
Analog Switch OFF Resistance	R_{SWof}	SW1 to SW5	50	—	—	$M\Omega$
Analog Switch ON Resistance	R_{SWon}	SW1 to SW5	50	100	200	Ω

*1 $-7.7 \text{ dBm (} 600 \Omega) = 0 \text{ dBm}_0, +3.14 \text{ dBm}_0 = 1.30 V_{PP}$

Digital Interface Characteristics (CODEC)

($V_{DD} = 2.7\text{ V to }3.6\text{ V}$, $T_a = -25^\circ\text{C to }+70^\circ\text{C}$)

Parameter	Symbol	Condition	Reference	Min.	Typ.	Max.	Unit
Digital Output Delay Time PCM, ADPCM Interface	t_{SDXC}, t_{SDRC}	Clod = 50 pF pull-up resistor: 500 Ω Items in parenthesis mean Clod = 10 pF, and the pull-up resistor $\leq 2\text{ k}\Omega$	Fig. 8	0	—	200 (100)	ns
	t_{XDC1}, t_{RDC1}			0	—	200 (100)	ns
	t_{XDC2}, t_{RDC2}			0	—	200 (100)	ns
	t_{XDC3}, t_{RDC3}			0	—	200 (100)	ns
Serial Port Digital I/O Timing Characteristics	t_{C1}	Clod = 50 pF	Fig. 9	50	—	—	ns
	t_{C2}			50	—	—	ns
	t_{C3}			50	—	—	ns
	t_{C4}			50	—	—	ns
	t_{C5}			100	—	—	ns
	t_{C6}			50	—	—	ns
	t_{C7}			50	—	—	ns
	t_{C8}			0	—	100	ns
	t_{C9}			50	—	—	ns
	t_{C10}			50	—	—	ns
	t_{C11}			0	—	50	ns
	t_{C12}			200	—	—	ns
EXCK Clock Frequency	F_{exck}	EXCK	—	—	—	10	MHz

Serial Interface Characteristics(V_{DD} = 2.7 V to 3.6 V, T_a = -25°C to +70°C)

Parameter	Symbol	Condition	Refer- ence	Min.	Typ.	Max.	Unit
Control Register Data Input	t _{CRW}	Write	Fig.15	—	—	200	ns
	t _{CRR}	Reset		—	—	200	ns
BUSY Bit	t _{BSR}	Rising		—	—	10	μs
	t _{BSH}	Active time		—	—	450	μs
RPM Bit	t _{RPR}	Rising		—	—	10	μs
	t _{RPF}	Falling at Stop command		—	—	135	μs

AC Characteristics (CODEC)

(V_{DD} = 2.7 V to 3.6 V, T_a = -25°C to +70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
		Frequency (Hz)	Level dBm0				
Transmit Frequency Response	L _{oss} T1	0 to 60	0	25	—	—	dB
	L _{oss} T2	300 to 3 k		-0.15	—	0.20	dB
	L _{oss} T3	1020		Reference			dB
	L _{oss} T4	3300		-0.15	—	0.80	dB
	L _{oss} T5	3400		0	—	0.80	dB
	L _{oss} T6	3968.75		13	—	—	dB
Receive Frequency Response	L _{oss} R1	0 to 3000	0	-0.15	—	0.20	dB
	L _{oss} R2	1020		Reference			dB
	L _{oss} R3	3300		-0.15	—	0.80	dB
	L _{oss} R4	3400		0	—	0.80	dB
	L _{oss} R5	3968.75		13	—	—	dB
Transmit Signal to Distortion Ratio (*1)	SD T1	1020	3	35	—	—	dB
	SD T2		0	35	—	—	dB
	SD T3		-30	35	—	—	dB
	SD T4		-40	28	—	—	dB
	SD T5		-45	23	—	—	dB
Receive Signal to Distortion Ratio (*1)	SD R1	1020	3	35	—	—	dB
	SD R2		0	35	—	—	dB
	SD R3		-30	35	—	—	dB
	SD R4		-40	28	—	—	dB
	SD R5		-45	23	—	—	dB
Transmit Gain Tracking	GT T1	1020	3	-0.2	—	0.2	dB
	GT T2		-10	Reference			dB
	GT T3		-40	-0.2	—	0.2	dB
	GT T4		-50	-0.5	—	0.5	dB
	GT T5		-55	-1.2	—	1.2	dB
Receive Gain Tracking	GT R1	1020	3	-0.2	—	0.2	dB
	GT R2		-10	Reference			dB
	GT R3		-40	-0.2	—	0.2	dB
	GT R4		-50	-0.5	—	0.5	dB
	GT R5		-55	-1.2	—	1.2	dB

*1 P-message filter used

AC Characteristics (CODEC) (Continued)

(V_{DD} = 2.7 V to 3.6 V, Ta = -25°C to +70°C)

Parameter	Symbol	Condition			Min.	Typ.	Max.	Unit
		Frequency (Hz)	Level dBm0	Other				
Idle Channel Noise (*1)	N _{IDLT}	—	AIN = SG	—	—	—	-68 (-75.7)	dBm0p (dBmp)
	N _{IDLR}	—	(*2)	—	—	—	-72 (-79.7)	
Absolute Level (*3)	A _{VT}	1020	0	GSX2	0.285	0.320	0.359	Vrms
	A _{VR}			VFR0	0.285	0.320	0.359	Vrms
Power Supply Noise Rejection Ratio	P _{SRRT}	Noise frequency: 0 kHz to 50 kHz	Noise level: 50 mV _{PP}	—	30	—	—	dB
	P _{SRRR}				30	—	—	dB

*1 P-message filter used

*2 PCMRI input: "11010101" (A-law), "11111111" (μ-law)

*3 0.320 Vrms = 0 dBm0 = -7.7 dBm (600 Ω)

ADPCM characteristics are fully compliant with ITU-T Recommendation G.721.

AC Characteristics (DTMF and Other Tones)

(V_{DD} = 2.7 V to 3.6 V, Ta = -25°C to +70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Frequency Deviation	D _{FT1}	DTMF tones		-7	—	7	Hz
	D _{FT2}	Other various tones		-7	—	7	Hz
Tone Reference Output Level (*1)	V _{TL}	Transmit side tone	DTMF (low group)	-18	-16	-14	dBm0
	V _{TH}		DTMF (high group), other	-16	-14	-12	dBm0
	V _{RL}	Receive side tone	DTMF (low group)	-4	-2	0	dBm0
	V _{RH}		DTMF (high group), other	-2	0	2	dBm0
DTMF Tone Level Relative Value	R _{DTMF}	V _{TH} /V _{TL} , V _{RH} /V _{RL}		1	2	3	dB

*1 Not including programmable gain set values

AC Characteristics (Gain Settings)

(V_{DD} = 2.7 V to 3.6 V, Ta = -25°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmit/Receive Gain Setting Accuracy	D _G	For all gain set values	-1	0	1	dB

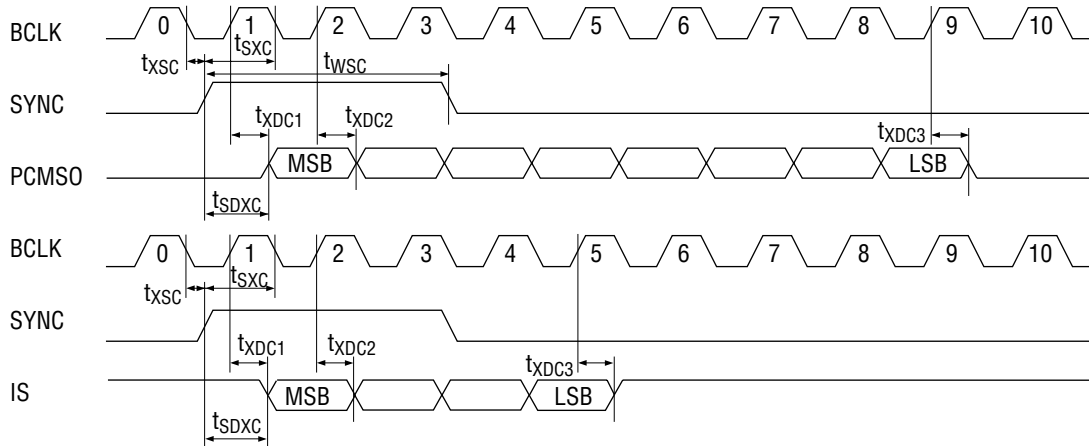
AC Characteristics (VOX Function)

(V_{DD} = 2.7 V to 3.6 V, Ta = -25°C to +70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Transmit VOX Detection Time (Voice and Silence Detection Time)	T _{VXON}	Silence→voice	VOX0 pin: See Fig. 2 Voice/silence differential: 10 dB	—	5	—	ms
	T _{VXOF}	Voice→silence		140/300	160/320	180/340	ms
Transmit VOX Detection Level Accuracy (Voice Detection Level)	D _{VX}	For detection level set values by CR6 - B6, B5		-2.5	0	2.5	dB

**TIMING DIAGRAM
(ADPCM CODEC)**

Transmit Side PCM, ADPCM Timing



Receive Side PCM, ADPCM Timing

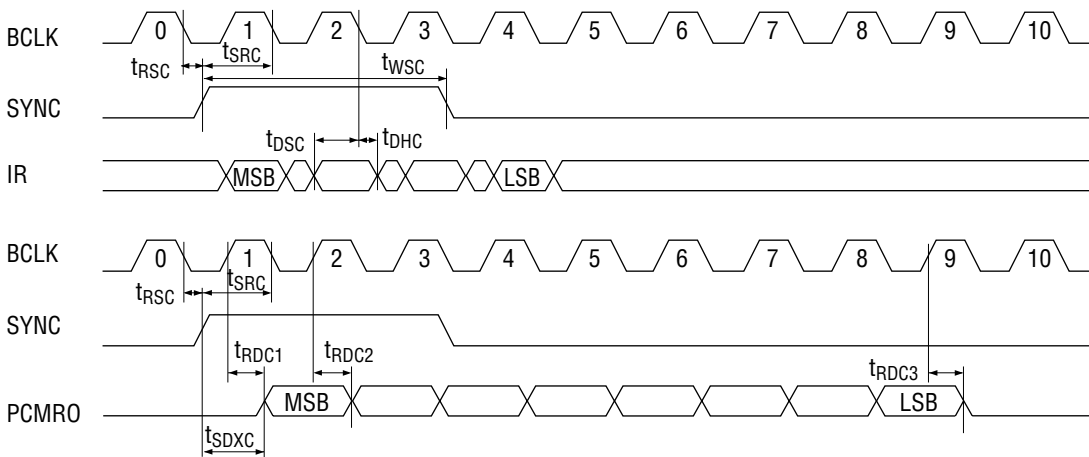


Figure 8 PCM, ADPCM Interface

Serial Port Timing for Microcontroller Interface

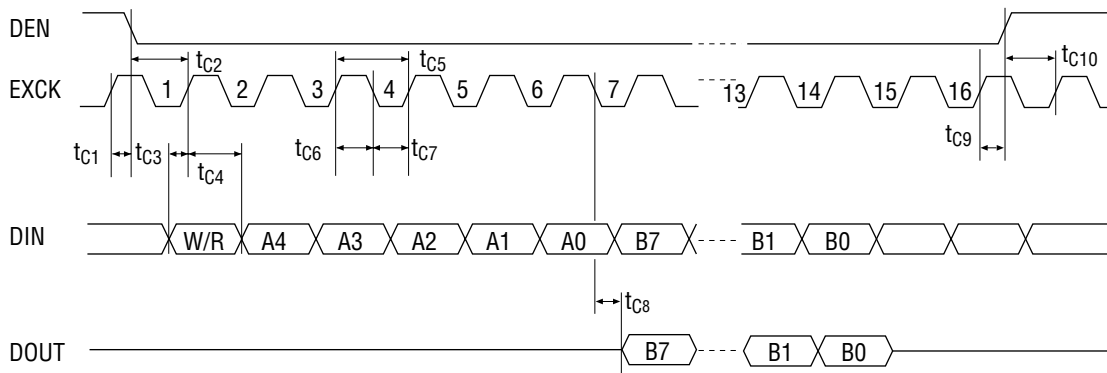
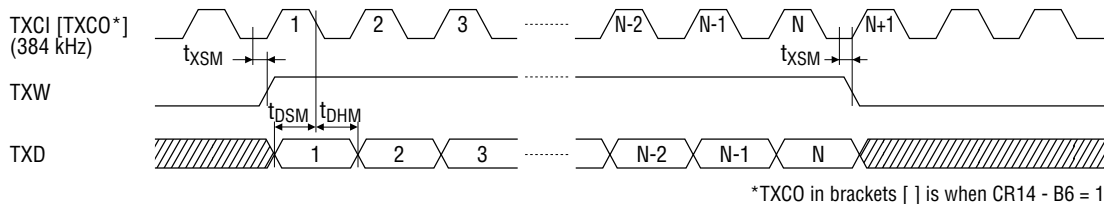


Figure 9 Serial Control Port Interface

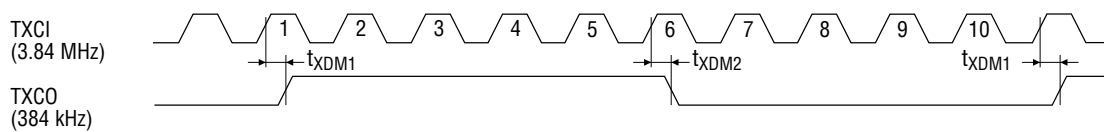
TIMING DIAGRAM

(Modem)

Transmit Data Input Timing



Transmit Clock (TXCO) Output Timing (When CR14 - B6 = 1)



Transmit Burst Position (BSTO) Output Timing (When CR14 - B6 = 0)

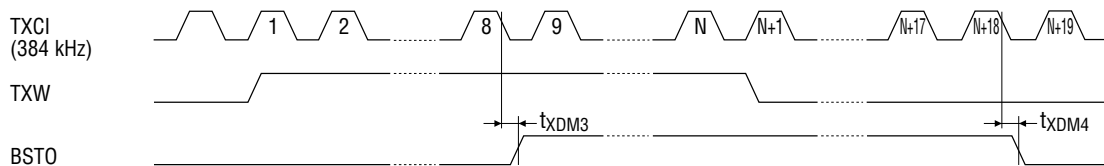


Figure 10 Modem Transmit Side (Modulator Side) Digital I/O Timing

Receive Side Data I/O Timing

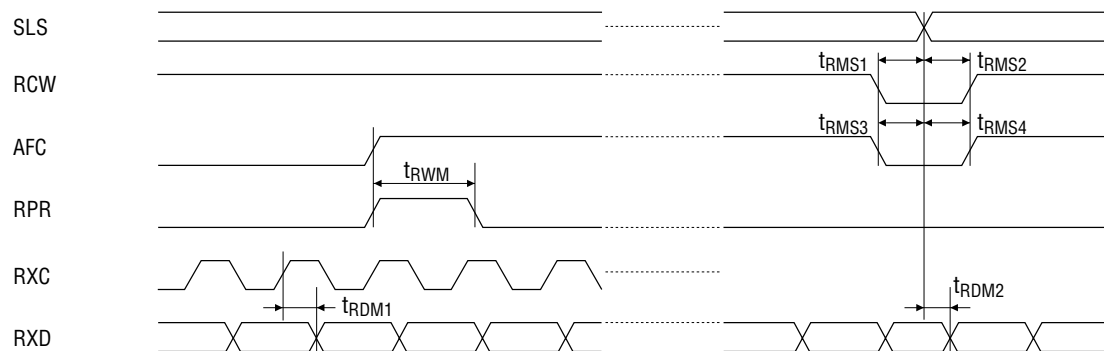
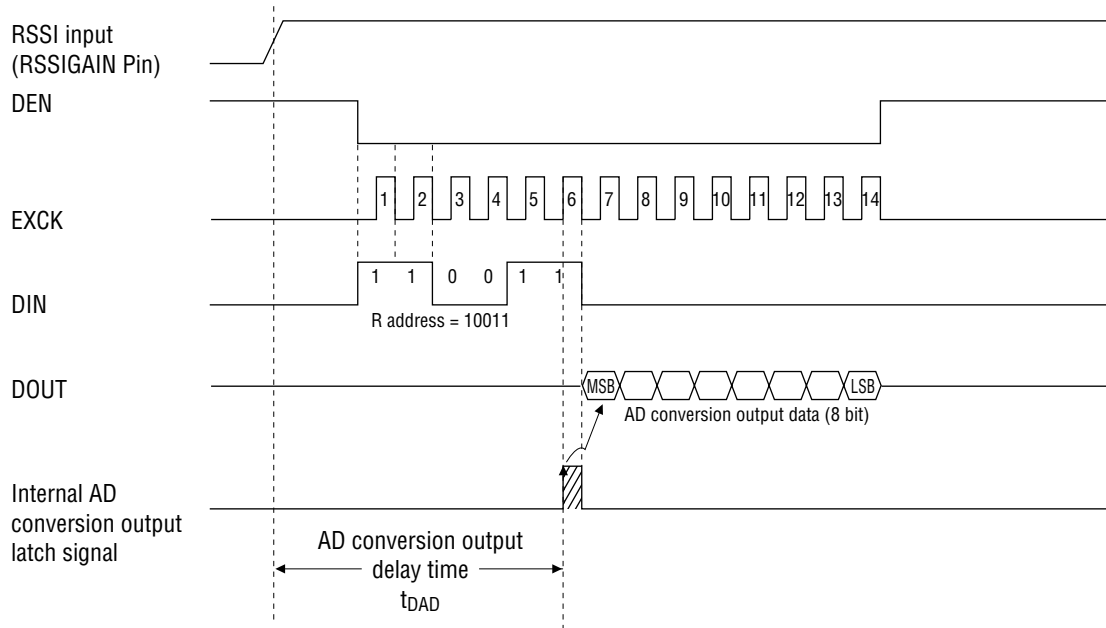


Figure 11 Receive Side (Demodulator Side) Digital I/O Timing

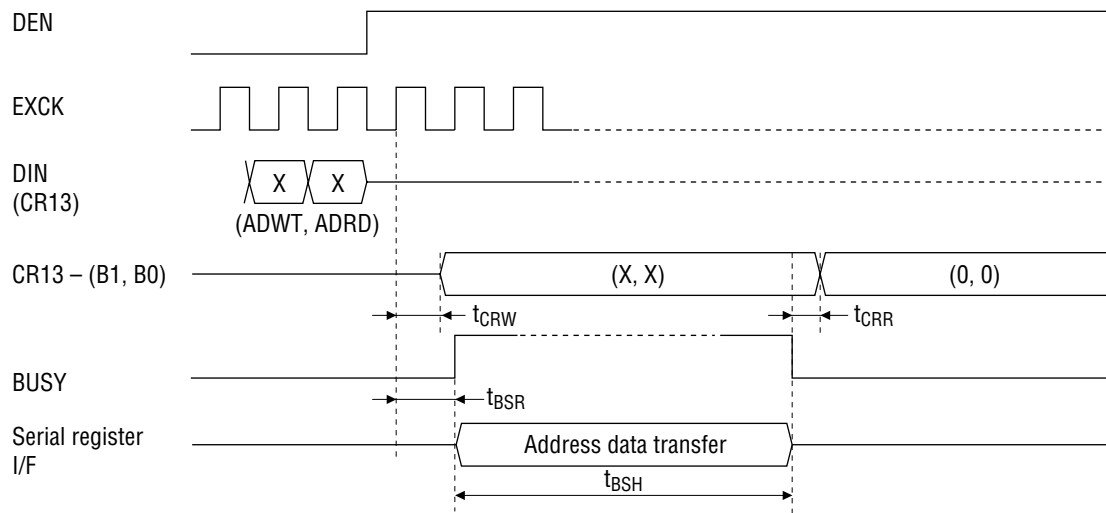
TIMING DIAGRAM
(RSSI - ADC)
RSSI - ADC Output Timing



- Notes:
1. AD conversion output data corresponds to the RSSI analog input value between the rising edge of the 6th EXCK clock pulse and the start point of the AD conversion output delay time (t_{DAD}).
 2. Normal AD conversion output data is output approximately 1ms after the power down mode is cancelled.

Figure 12 RSSI - ADC Output Timing

TIMING DIAGRAM
(Serial Register Interface)
Address Write/Read Timing



Recording/Playback Timing

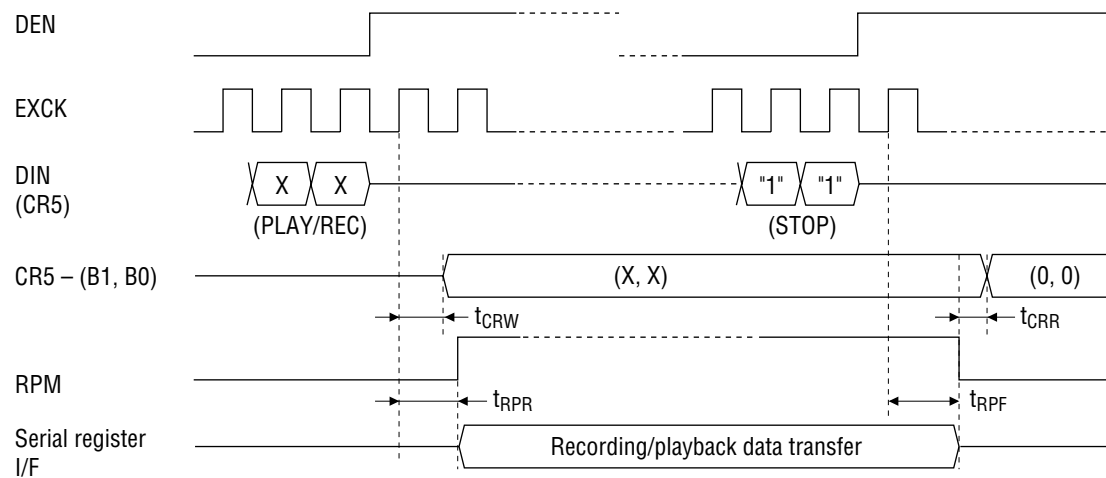


Figure 13 Serial Register Interface

Mode State Transition Time in Modem

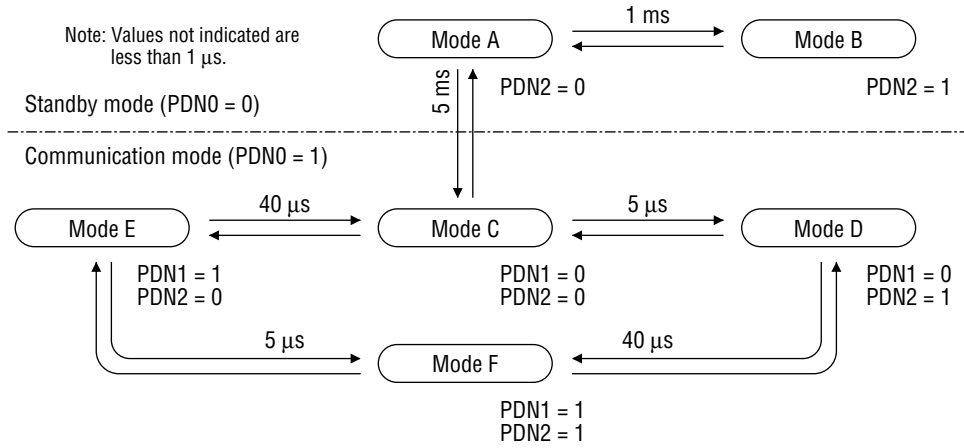


Figure 14 Transition Between Power-Down Mode and Power-ON Mode

Timing Diagram for Demodulator Control in Modem (Example)

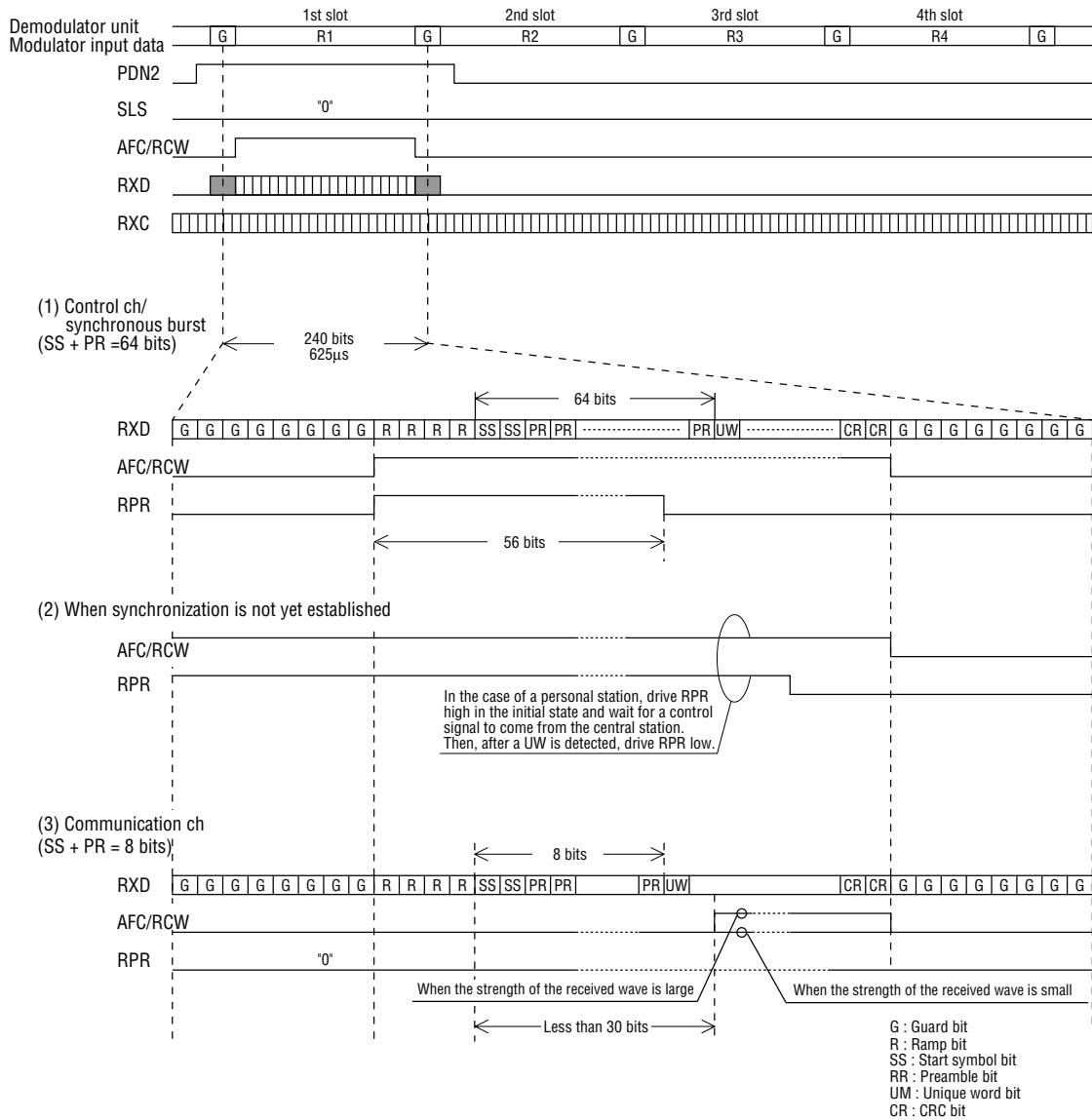


Figure 15 Modem Unit Demodulator Timing Diagram Example

FUNCTIONAL DESCRIPTION

**Control Register Description Table
(ADPCM CODEC)**

(1) CR0 (Basic Operation Mode Settings)

	B7	B6	B5	B4	B3	B2	B1	B0
CR0	A/ μ SEL	—	PDN ALL	PDN TX	PDN RX	SA, VF _OUT	SAO/VFRO	SA, VF _PDN
Initial Value (*)	0	0	0	0	0	0	0	0

* The initial value means a value which is set when the device is reset using the RESET signal.

- B7:PCM interface companding selection 0: μ -law 1: A-law
- B6:Not used
- B5:Power down (entire unit) 0: Power ON 1: Power down
 ORed with the inverting external power down signal PDN3. When using
 this data, set PDN3 to "1".
- B4:Power down (transmit side only) 0: Power ON 1: Power down
- B3:Power down (receive side only) 0: Power ON 1: Power down
- B2:Output from VFRO and SAO at a time
 0: Receive side output signals are output from a pin selected by B1.
 1: Receive side output signals are output from VFRO and SAO at a time.
- B1:Receive side output switch control
 0: Receive side output signals appear on the SAO (Sounder Amplifier
 Output) pin.
 1: These signals appear on the VFRO (Receiver Amplifier Output) pin.
- B0:Power down control for sounder output amplifier (SAO) and receiver
 output amplifier (VFRO).
 0: When SAO is selected by CR0 - B1, VFRO is powered down.
 When VFRO is selected, SAO is powered down.
 1: Both SAO and VFRO are powered ON.

(2) CR1 (ADPCM Operation Mode Settings)

	B7	B6	B5	B4	B3	B2	B1	B0
CR1	TX ON/OFF	RX ON/OFF	ADPCM RESET	TX MUTE	RX MUTE	MLV2	MLV1	MLV0
Initial Value	0	0	0	0	0	0	0	0

- B7: Transmit side PCM signal ON/OFF. 0: ON 1: OFF
OFF: PCM idle pattern is transmitted.
- B6: Receive side PCM signal ON/OFF. 0: ON 1: OFF
OFF: PCM idle pattern is transmitted.
- B5: ADPCM reset (as specified by G. 721) 1: reset
- B4: Transmit side MUTE.
0: Transmit MUTE OFF.
1: Transmit MUTE ON.
Transmit output is in an idle state.
- B3: Receive side MUTE. This bit is ORed with the external control pin RXMUTE.
0: Receive side MUTE OFF.
1: Receive side MUTE ON. The receive side output signals are attenuated by the values represented by a combination of bits B2, B1, and B0 of the CR1. (For voice path only.)
- B2, B1, B0: An attenuation value is selected at receive side MUTE (CR1 - B3 = "1") (see Table 3). These bits are ORed with the external pins MLV2, MLV1, and MLV0.

Table 3 MUTE Level Settings

B2	B1	B0	Attenuation value
0	0	0	0dB loss
0	0	1	- 6dB loss
0	1	0	-12dB loss
0	1	1	-18dB loss
1	0	0	-24dB loss
1	0	1	-30dB loss
1	1	0	-36dB loss
1	1	1	MUTE (idle state)

(3) CR2 (PCMCODEC Operation Mode Settings and Transmit/Receive Gain Adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CR2	TX GAIN3	TX GAIN2	TX GAIN1	TX GAIN0	RX GAIN3	RX GAIN2	RX GAIN1	RX GAIN0
Initial Value	0	0	0	0	0	0	0	0

B7, B6, B5, B4: Transmit side signal gain adjustment (see Table 4)

B3, B2, B1, B0: Receive side signal gain adjustment (see Table 4)

Table 4 Receive/Transmit Gain Settings

Transmit/ receive gain	B7	B6	B5	B4	B3	B2	B1	B0
-16dB	1	0	0	0	1	0	0	0
-14dB	1	0	0	1	1	0	0	1
-12dB	1	0	1	0	1	0	1	0
-10dB	1	0	1	1	1	0	1	1
- 8dB	1	1	0	0	1	1	0	0
- 6dB	1	1	0	1	1	1	0	1
- 4dB	1	1	1	0	1	1	1	0
- 2dB	1	1	1	1	1	1	1	1
0dB	0	0	0	0	0	0	0	0
2dB	0	0	0	1	0	0	0	1
4dB	0	0	1	0	0	0	1	0
6dB	0	0	1	1	0	0	1	1
8dB	0	1	0	0	0	1	0	0
10dB	0	1	0	1	0	1	0	1
12dB	0	1	1	0	0	1	1	0
14dB	0	1	1	1	0	1	1	1

The above gain settings table shows the transmit/receive voice signal gain settings and the transmit side gain settings for DTMF tones and other tones. Tone signal transmission is enabled by CR4 - B6 (discussed later), and the gain setting is set to the levels shown below.

DTMF tones (low group):..... -16 dBm0

DTMF tones (high group) and other tones: ... -14 dBm0

For example, if the transmit gain set value is set to +8 dB (B7, B6, B5, B4) = (0, 1, 0, 0), then the following tones appear at the PCMSO pin.

DTMF tones (low group):..... -8 dBm0

DTMF tones (high group) and other tones: ... -6 dBm0

-3 dBm0 (mixed tone)

However, the gain of the receive side tone and the gain of the side tones (path from transmit side to receive side) are set by the CR3 register.

(4) CR3 (Side Tone and Tone Generator Gain Adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CR3	Side Tone GAIN2	Side Tone GAIN1	Side Tone GAIN0	TONE ON/OFF	TONE GAIN3	TONE GAIN2	TONE GAIN1	TONE GAIN0
Initial Value	0	0	0	0	0	0	0	0

B7, B6, B5: Side tone gain adjustment (refer to Table 5)
 B4: Tone generator ON/OFF 0: OFF 1: ON
 B3, B2, B1, B0: . Tone generator Receive side gain adjustment (refer to Table 6)

Table 5 Side Tone Gain Settings

B7	B6	B5	Side Tone Gain
0	0	0	OFF
0	0	1	-15 dB
0	1	0	-13 dB
0	1	1	-11 dB
1	0	0	-9 dB
1	0	1	-7 dB
1	1	0	-5 dB
1	1	1	-3 dB

Table 6 Receive Side Tone Generator Gain Settings

B3	B2	B1	B0	Tone Generator Gain	B3	B2	B1	B0	Tone Generator Gain
0	0	0	0	-32 dB	1	0	0	0	-16 dB
0	0	0	1	-30 dB	1	0	0	1	-14 dB
0	0	1	0	-28 dB	1	0	1	0	-12 dB
0	0	1	1	-26 dB	1	0	1	1	-10 dB
0	1	0	0	-24 dB	1	1	0	0	-8 dB
0	1	0	1	-22 dB	1	1	0	1	-6 dB
0	1	1	0	-20 dB	1	1	1	0	-4 dB
0	1	1	1	-18 dB	1	1	1	1	-2 dB

The receive side tone generator gain settings shown in Table 6 are set with the following levels as a reference.

DTMF tones (low group): -2 dBm0

DTMF tones (high group) and other tones: ... 0 dBm0

For example, if the tone generator gain set value is set to -6 dB (B3, B2, B1, B0)=(1, 1, 0, 1), then tones at the following levels appear at the SAO+ /SAO- or VFRO pin.

DTMF tones (low group): -8 dBm0

DTMF tones (high group) and other tones: ... -6 dBm0

-3 dBm0 (mixed tone)

(5) CR4 (Tone Generator Operation Mode and Frequency Settings)

	B7	B6	B5	B4	B3	B2	B1	B0
CR4	DTMF/ OTHERS SEL	TONE SEND	TONE5	TONE4	TONE3	TONE2	TONE1	TONE0
Initial Value	0	0	0	0	0	0	0	0

B7:..... Selection of DTMF signal and other tones
 (S tone, F tone, R tone, etc.) 0: Other tones 1: DTMF signal
 B6:..... Transmission side tone transmit
 0: Voice signal transmit 1: Tone transmit
 B5, B4, B3, B2, B1, B0: Tone frequency setting (refer to Table 7)

Table 7 Tone Generator Frequency Settings

(a) When B7 = 1 (DTMF Tones)

B5	B4	B3	B2	B1	B0	Description	B5	B4	B3	B2	B1	B0	Description
*	*	0	0	0	0	697 Hz + 1209 Hz	*	*	0	0	0	0	852 Hz + 1209 Hz
*	*	0	0	0	1	697 Hz + 1336 Hz	*	*	0	0	0	1	852 Hz + 1336 Hz
*	*	0	0	1	0	697 Hz + 1477 Hz	*	*	0	0	1	0	852 Hz + 1477 Hz
*	*	0	0	1	1	697 Hz + 1633 Hz	*	*	0	0	1	1	852 Hz + 1633 Hz
*	*	0	1	0	0	770 Hz + 1209 Hz	*	*	0	1	0	0	941 Hz + 1209 Hz
*	*	0	1	0	1	770 Hz + 1336 Hz	*	*	0	1	0	1	941 Hz + 1336 Hz
*	*	0	1	1	0	770 Hz + 1477 Hz	*	*	0	1	1	0	941 Hz + 1477 Hz
*	*	0	1	1	1	770 Hz + 1633 Hz	*	*	0	1	1	1	941 Hz + 1633 Hz

(b) When B7 = 0 (Other than DTMF Tones)

B5	B4	B3	B2	B1	B0	Description	B5	B4	B3	B2	B1	B0	Description
0	0	0	0	0	0	400/500 Hz 8 Hz Wamble	1	0	0	0	0	0	1100 Hz Single tone
0	0	0	0	0	1	800/1 Hz 8 Hz Wamble	1	0	0	0	0	1	1142 Hz Single tone
0	0	0	0	1	0	400/500 Hz 16 Hz Wamble	1	0	0	0	1	0	1200 Hz Single tone
0	0	0	0	1	1	400/1 Hz 16 Hz Wamble	1	0	0	0	1	1	1210 Hz Single tone
0	0	0	1	0	0	667/800 Hz 16 Hz Wamble	1	0	0	1	0	0	1250 Hz Single tone
0	0	0	1	0	1	800/1 Hz 16 Hz Wamble	1	0	0	1	0	1	1300 Hz Single tone
0	0	0	1	1	0	1 k/1.33 kHz 16 Hz Wamble	1	0	0	1	1	0	1333 Hz Single tone
0	0	0	1	1	1	2.7 k/1 kHz 16 Hz Wamble	1	0	0	1	1	1	1360 Hz Single tone
0	0	1	0	0	0	2 k/2.1 kHz 16 Hz Wamble	1	0	1	0	0	0	1410 Hz Single tone
0	0	1	0	0	1	2 k/2.7 kHz 8 Hz Wamble	1	0	1	0	0	1	1455 Hz Single tone
0	0	1	0	1	0	2.6 k/2.7 kHz 16 Hz Wamble	1	0	1	0	1	0	1477 Hz Single tone
0	0	1	0	1	1	3.2 k/3.31 kHz 16 Hz Wamble	1	0	1	0	1	1	1500 Hz Single tone
0	0	1	1	0	0	400 kHz 16 Hz Wamble	1	0	1	1	0	0	3310 Hz Single tone
0	0	1	1	0	1	2 kHz 16 Hz Wamble	1	0	1	1	0	1	1600 Hz Single tone
0	0	1	1	1	0	2.7 kHz 16 Hz Wamble	1	0	1	1	1	0	1635 Hz Single tone
0	0	1	1	1	1	400 kHz 10 Hz Wamble	1	0	1	1	1	1	1710 Hz Single tone
0	1	0	0	0	0	350 + 440 kHz Mixed tone	1	1	0	0	0	0	1800 Hz Single tone
0	1	0	0	0	1	400 + 480 kHz Mixed tone	1	1	0	0	0	1	1900 Hz Single tone
0	1	0	0	1	0	480 + 620 kHz Mixed tone	1	1	0	0	1	0	2000 Hz Single tone
0	1	0	0	1	1	350 kHz Single tone	1	1	0	0	1	1	2100 Hz Single tone
0	1	0	1	0	0	400 kHz Single tone	1	1	0	1	0	0	2200 Hz Single tone
0	1	0	1	0	1	440 kHz Single tone	1	1	0	1	0	1	2285 Hz Single tone
0	1	0	1	1	0	480 kHz Single tone	1	1	0	1	1	0	2400 Hz Single tone
0	1	0	1	1	1	500 kHz Single tone	1	1	0	1	1	1	2500 Hz Single tone
0	1	1	0	0	0	533 kHz Single tone	1	1	1	0	0	0	2600 Hz Single tone
0	1	1	0	0	1	571 kHz Single tone	1	1	1	0	0	1	2670 Hz Single tone
0	1	1	0	1	0	620 kHz Single tone	1	1	1	0	1	0	2700 Hz Single tone
0	1	1	0	1	1	667 kHz Single tone	1	1	1	0	1	1	2820 Hz Single tone
0	1	1	1	0	0	727 kHz Single tone	1	1	1	1	0	0	2910 Hz Single tone
0	1	1	1	0	1	800 kHz Single tone	1	1	1	1	0	1	3000 Hz Single tone
0	1	1	1	1	0	888 kHz Single tone	1	1	1	1	1	0	3110 Hz Single tone
0	1	1	1	1	1	1000 kHz Single tone	1	1	1	1	1	1	3200 Hz Single tone

(6) CR5 (Control of Serial Register I/F)

	B7	B6	B5	B4	B3	B2	B1	B0
CR5	SEND/ REC	ROM/ SR	4M8M/ 1M	—	—	—	CMD1	CMD0
Initial Value	0	0	0	0	0	0	0	0

- B7: Register I/F connection.
 0: Connection with ADPCM receiver
 1: Connection with ADPCM transmitter
- B6: Switching between voice ROM and serial register.
 0: Serial register
 1: Voice ROM
- B5: Capacitance of serial register to be connected.
 0: 1 Mbit (MSM6389)
 1: 4 Mbit (MSM6684), 8 Mbit (MSM6685)
- B1, B0: Serial register I/F command (CMD1, CMD0) =
 (0. 0): NOP
 (0. 1): PLAY
 (1. 0): REC (RECORD)
 (1. 1): STOP

Note: CMD1 and CMD0 are reset to "0" after the instruction is executed.
 The PLAY and REC instructions must not be executed when BUSY (CR5 - B1) and RPM (CR5 - B0) are set to "1".

(9) CR8 (Start X-address 0 to 7)

	B7	B6	B5	B4	B3	B2	B1	B0
CR8	ST0	ST1	ST2	ST3	ST4	ST5	ST6	ST7
Initial Value	0	0	0	0	0	0	0	0

CR9 (Start X-address 8 to 12)

	B7	B6	B5	B4	B3	B2	B1	B0
CR9	ST8	ST9	ST10	ST11	ST12	—	—	—
Initial Value	0	0	0	0	0	0	0	0

CR8 (B7 to B0), CR9 (B7 to B3) : Recording/playback start X-address storage register

(10) CR10 (Start Y-address 0 to 7)

	B7	B6	B5	B4	B3	B2	B1	B0
CR10	SPY0	SPY1	SPY2	SPY3	SPY4	SPY5	SPY6	SPY7
Initial Value	0	0	0	0	0	0	0	0

CR10 (B7 to B0) : Recording/playback stop Y-address storage register

(11) CR11 (Stop X-address 0 to 7)

	B7	B6	B5	B4	B3	B2	B1	B0
CR11	SP0	SP1	SP2	SP3	SP4	SP5	SP6	SP7
Initial Value	0	0	0	0	0	0	0	0

CR12 (Stop X-address 8 to 12)

	B7	B6	B5	B4	B3	B2	B1	B0
CR12	SP8	SP9	SP10	SP11	SP12	—	—	—
Initial Value	0	0	0	0	0	0	0	0

CR11 (B7 to B0), CR12 (B7 to B3) : Recording/playback stop X-address storage register

(12) CR13 (Channel Selection)

	B7	B6	B5	B4	B3	B2	B1	B0
CR13	CH0	CH1	CH2	CH3	CH4	—	ADRD	ADWT
Initial Value	0	0	0	0	0	0	0	0

- B7 - B3: Channel selection (all 32 channels are selected by HEX code)
- B2: Not used
- B1: Address Read instruction
 - 0: NOP
 - 1: When "1" is written in this bit, the start/stop addresses corresponding to the channels specified by B7 - B3 are transferred from the channel index area of the serial register to CR8 - CR12. These bits are reset to "0"s after the addresses are transferred.
- B0: Address write instruction
 - 0: NOP
 - 1: When "1" is written in this bit, the start/stop address corresponding to the channel specified by B7 - B3 is transferred from CR8 - 12 to the channel index area of the serial register. These bits are reset to "0"s after the addresses are transferred.

Note: When BUSY (CR7 - B1) and RPM (CR7 - B0) are set to "1", writing to ADRD and ADWT is not allowed.

(Modem)

(13) CR14 (Basic Operation Mode Setting)

	B7	B6	B5	B4	B3	B2	B1	B0
CR14	—	TXC SEL	MOD OFF	IFSEL	—	—	TEST1	TEST0
Initial Value	0	0	0	0	0	0	0	0

- B7, B3, B2: Not used
- B6: Transmission timing clock selection
 - 0: TXCI input: 384 kHz TXCO output: APLL 384 kHz output
Transmit data TXD is input synchronously with the rising edge of TXCI. APLL is ON.
 - 1: TXCI input: 3.84 MHz TXCO output: 384 kHz (TXCI divided by 10)
Transmit data TXD is input synchronously with the rising edge of TXCO. APLL is OFF.
- B5: Modulation OFF/ON control
 - 0: Modulation ON 1: Modulation OFF (fixed phase)
- B4: Receive side input IF frequency selection
 - 0: 1.2 MHz
 - 1: 10.8 MHz
- B1, B0: Device test control bits
 - These bits should be set to "0" for normal use.

(14) CR15 (I and Q Gain Adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CR15	Ich GAIN3	Ich GAIN2	Ich GAIN1	Ich GAIN0	Qch GAIN3	Qch GAIN2	Qch GAIN1	RX Qch GAIN0
Initial Value	0	0	0	0	0	0	0	0

B7 - B4:I+ and I- output gain setting: 3 mV steps (refer to Table 8)

B3 - B0:Q+ and Q- output gain setting: 3 mV steps (refer to Table 8)

Table 8 I and Q Channel Amplitude Value

CR1 - B7	B6	B5	B4	Description
CR1 - B3	B2	B1	B0	
0	1	1	1	Amplitude Value : 1.042 (Reference Value)
0	1	1	0	1.036
0	1	0	1	1.030
0	1	0	0	1.024
0	0	1	1	1.018
0	0	1	0	1.012
0	0	0	1	1.006
0	0	0	0	1.000 (Reference Value)
0	1	1	1	0.994
0	1	1	0	0.988
0	1	0	1	0.982
0	1	0	0	0.976
0	0	1	1	0.970
0	0	1	0	0.964
0	0	0	1	0.958
0	0	0	0	0.952

(15) CR16 (I- Output Offset Voltage Adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CR16	Ich Offset4	Ich Offset3	Ich Offset2	Ich Offset1	Ich Offset0	—	—	—
Initial Value	0	0	0	0	0	0	0	0

B7 - B3:I- output pin offset voltage adjustment (refer to Table 9)
 B2 - B0:Not used

(16) CR17 (Q- Output Offset Voltage Adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CR17	Qch Offset4	Qch Offset3	Qch Offset2	Qch Offset1	Qch Offset0	—	—	—
Initial Value	0	0	0	0	0	0	0	0

B7 - B3:Q- output pin offset voltage adjustment (refer to Table 9)
 B2 - B0:Not used

Table 9 Ich and Qch Offset Adjustment Values

CR11 - B7	B6	B5	B4	B3	Offset Voltage (mV)	CR11 - B7	B6	B5	B4	B3	Offset Voltage (mV)
CR12 - B7	B6	B5	B4	B3		CR12 - B7	B6	B5	B4	B3	
0	1	1	1	1	+45	1	1	1	1	1	-3
0	1	1	1	0	+42	1	1	1	1	0	-6
0	1	1	0	1	+39	1	1	1	0	1	-9
0	1	1	0	0	+36	1	1	1	0	0	-12
0	1	0	1	1	+33	1	1	0	1	1	-15
0	1	0	1	0	+30	1	1	0	1	0	-18
0	1	0	0	1	+27	1	1	0	0	1	-21
0	1	0	0	0	+24	1	1	0	0	0	-24
0	0	1	1	1	+21	1	0	1	1	1	-27
0	0	1	1	0	+18	1	0	1	1	0	-30
0	0	1	0	1	+15	1	0	1	0	1	-33
0	0	1	0	0	+12	1	0	1	0	0	-36
0	0	0	1	1	+9	1	0	0	1	1	-39
0	0	0	1	0	+6	1	0	0	1	0	-42
0	0	0	0	1	+3	1	0	0	0	1	-45
0	0	0	0	0	0	1	0	0	0	0	-48

(17) CR18

	B7	B6	B5	B4	B3	B2	B1	B0
CR18	—	—	—	—	LOCAL INV1	LOCAL INV0	—	—
Initial Value	0	0	0	0	0	0	0	0

B7 - B4:Not used

B3, B2:Local inversion mode setting bits

(These bits are used when the demodulator side IF input is phase inverted in the system configuration)

(0, 0): Normal mode

(1, 1): Local inversion mode

B1, B0:Not used

(18) CR19

	B7	B6	B5	B4	B3	B2	B1	B0
CR19	AD07	AD06	AD05	AD04	AD03	AD02	AD01	AD00
Initial Value	0	0	0	0	0	0	0	0

B7 - B0:8bit output data from the RSSI-AD converter is written.

The output results are listed in Table 10.

Table 10

BBBBBBB 76543210	RSGAIN pin voltage (V)
11111111	2.1000
11111110	2.0945
to	to
10000001	1.4055
10000000	1.4000
01111111	1.3945
to	to
00000001	0.7055
00000000	0.7000

(19) CR20 (SRRI-ADC Offset Voltage Adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CR20	AD Offset4	AD Offset3	AD Offset2	AD Offset1	AD Offset0	—	RS PDN	—
Initial Value	0	0	0	0	0	0	0	0

B7 - B3:RSGAIN pin DC adjustment value (Table 11)

Table 11

CR20					Adjustment Value	CR20					Adjustment Value
B7	B6	B5	B4	B3	(mV)	B7	B6	B5	B4	B3	(mV)
0	1	1	1	1	375	1	1	1	1	1	-25
0	1	1	1	0	350	1	1	1	1	0	-50
0	1	1	0	1	325	1	1	1	0	1	-75
0	1	1	0	0	300	1	1	1	0	0	-100
0	1	0	1	1	275	1	1	0	1	1	-125
0	1	0	1	0	250	1	1	0	1	0	-150
0	1	0	0	1	225	1	1	0	0	1	-175
0	1	0	0	0	200	1	1	0	0	0	-200
0	0	1	1	1	175	1	0	1	1	1	-225
0	0	1	1	0	150	1	0	1	1	0	-250
0	0	1	0	1	125	1	0	1	0	1	-275
0	0	1	0	0	100	1	0	1	0	0	-300
0	0	0	1	1	75	1	0	0	1	1	-325
0	0	0	1	0	50	1	0	0	1	0	-350
0	0	0	0	1	25	1	0	0	0	1	-375
0	0	0	0	0	0	1	0	0	0	0	-400

B1:RSSI - ADC power down control

0: Power down

1: Power ON

B2, B0:Not used

(20) CR21 (General I/O)

	B7	B6	B5	B4	B3	B2	B1	B0
CR21	—	—	—	—	—	—	R01	R00
Initial Value	0	0	0	0	0	0	0	0

B7 - B2:Not used

B1 - B0:Data written in B1 and B0 is output to the RO1 and RO0 pins.

(21) CR22 (Control of Switches)

	B7	B6	B5	B4	B3	B2	B1	B0
CR22	SW1 CONT	SW2 CONT	SW3 CONT	SW4/5 CONT	AOUT PDN	AOUT3 CONT	AOUT2 CONT	AOUT1 CONT
Initial Value	0	0	0	0	0	0	0	0

B7, B6:SW1, SW2 control 0: Open 1: Closed

B5:SW3 control 0: Open 1: Closed

B4: SW4/5 control
 0: SW4 open, SW5 closed
 1: SW4 closed, SW5 open

B3: Sounder amplifier power down control
 0: Power ON
 1: Power down

B2, B1, B0: TOUT3 - 1 control
 0: TOUT3 - 1 disabled
 1: TOUT3 - 1 enabled

Note: Set the unused bits of CR0 - CR22 to "0".

DATA CONFIGURATION IN THE EXTERNAL SERIAL REGISTER

X Address Space

The address space of the external serial register is accessed based on (word direction indicated by the X address) × (1 Kb depth in Y direction). The maximum X address in word direction depends on the total memory capacity of serial registers connected. Since the leading 32 words (32 Kb) of the serial register are used as the channel index area, X address 020h onward can be used as the voice data area.

CR5-B5	0	1	1
Total Memory Capacity (device name)	1 Mb (MSM6389)	4 Mb (MSM6684)	8 Mb (MSM6685)
Number of words	1K words	4K words	8K words
X address*	000h to 3FFh	0000h to 0FFFh	0000h to 1FFFh

* 0000h to 001Fh are used as the channel index area.

Y Address Space

For 1 Kb ADPCM data in Y direction, 4 bits × 256 samples = 1024 bits are stored in the 1 Kb memory area. One Y address is allocated to one sample (4 bits) of ADPCM data and addressing is made with 00h to FFh.

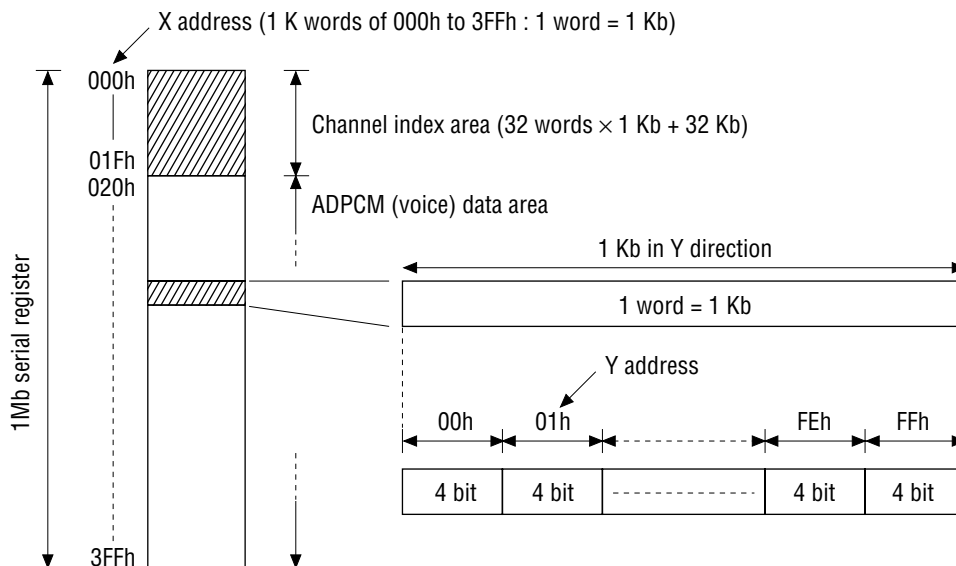
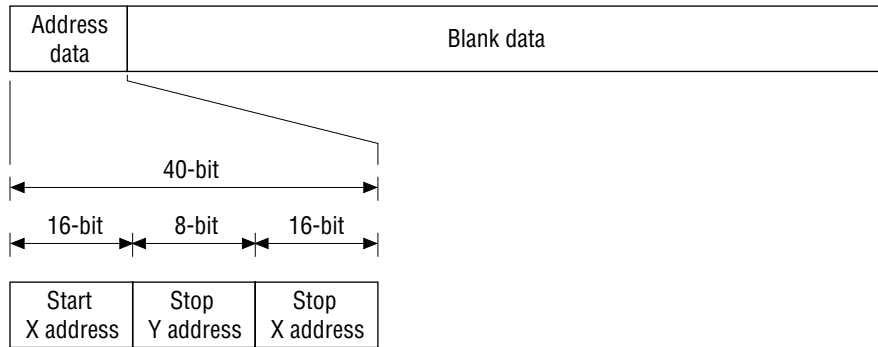


Figure 16 Address Space of 1 Mb Serial Register

Channel Index Area of the Serial Register

One channel (1 Kb) of the channel index area consists of the 40 bits of address data.

- (1) Stop Y address
The Y address is represented by 8 bits and addressing is made with 00h to FFh.
- (2) Start X address, stop X address
The X address is represented by 16 bits (valid 13 bits). If, for example, the serial register is 1Mb, the 1K-word X address space is addressed with 000h to 3FFh.



Start X address (ST0 to ST12)	<table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 12.5%; border: 1px solid black; text-align: center;">ST0</td> <td style="width: 12.5%; border: 1px solid black; text-align: center;">ST1</td> <td style="width: 35%; border: 1px solid black; text-align: center;">-----</td> <td style="width: 12.5%; border: 1px solid black; text-align: center;">ST11</td> <td style="width: 12.5%; border: 1px solid black; text-align: center;">ST12</td> <td style="width: 12.5%; border: 1px solid black; text-align: center;">—</td> <td style="width: 12.5%; border: 1px solid black; text-align: center;">—</td> <td style="width: 12.5%; border: 1px solid black; text-align: center;">—</td> </tr> </table>	ST0	ST1	-----	ST11	ST12	—	—	—
ST0	ST1	-----	ST11	ST12	—	—	—		
Stop Y address (SPY0 to SPY7)	<table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 12.5%; border: 1px solid black; text-align: center;">SPY0</td> <td style="width: 12.5%; border: 1px solid black; text-align: center;">SPY1</td> <td style="width: 35%; border: 1px solid black; text-align: center;">-----</td> <td style="width: 12.5%; border: 1px solid black; text-align: center;">SPY6</td> <td style="width: 12.5%; border: 1px solid black; text-align: center;">SPY7</td> </tr> </table>	SPY0	SPY1	-----	SPY6	SPY7			
SPY0	SPY1	-----	SPY6	SPY7					
Stop X address (ST0 to SP12)	<table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 12.5%; border: 1px solid black; text-align: center;">SP0</td> <td style="width: 12.5%; border: 1px solid black; text-align: center;">SP1</td> <td style="width: 35%; border: 1px solid black; text-align: center;">-----</td> <td style="width: 12.5%; border: 1px solid black; text-align: center;">SP11</td> <td style="width: 12.5%; border: 1px solid black; text-align: center;">SP12</td> <td style="width: 12.5%; border: 1px solid black; text-align: center;">—</td> <td style="width: 12.5%; border: 1px solid black; text-align: center;">—</td> <td style="width: 12.5%; border: 1px solid black; text-align: center;">—</td> </tr> </table>	SP0	SP1	-----	SP11	SP12	—	—	—
SP0	SP1	-----	SP11	SP12	—	—	—		

Figure 17 Channel Index Area of Serial Register

METHODS OF RECORDING AND PLAYBACK

Recording Method (See the flow chart in Figure 18)

- (1) • Set up the connection between the serial register / voice ROM and ADPCM transmit-receive system. (See Figure 20) (CR5 - B7)
 - Specify the serial register/voice ROM. (CR5 - B6)
 - Set the external capacity. (CR5 - B5)
 - Set the NOP command. (CR5 - B1 = "0", B0 = "0")
- (2) • Set the start/stop address. (CR8 to CR12)
- (3) • Set the channel. (CR13 - B7 to B3)
 - Set the ADWT (address write) instruction. (CR13 - B1 = "0", B0 = "1")
- (4) • The start/stop address of the channel set by the ADWT instruction is stored in the channel index area. When status register BUSY (CR7 - B1) changes from "1" to "0", storage is complete.
- (5) • Start recording by setting the REC (recording) command (CR5 - B1 = "1", B0 = "0").
- (6) • Check the recording start with the status register RPM bit (CR7 - B0 = "1").
- (7) • To interrupt during recording, set the STOP (stop) command (CR5 - B1 = "1", B0 = "1"). In this case, to store the address counter contents in the channel index area as a new stop address, the following settings are required:
 - Set the channel.
 - Set the ADWT instruction.
 - When the BUSY bit changes from "1" to "0", settings are complete.
- (8) • When the address counter reaches the stop address, recording is complete. Check completion of recording with RPM bit = "0".

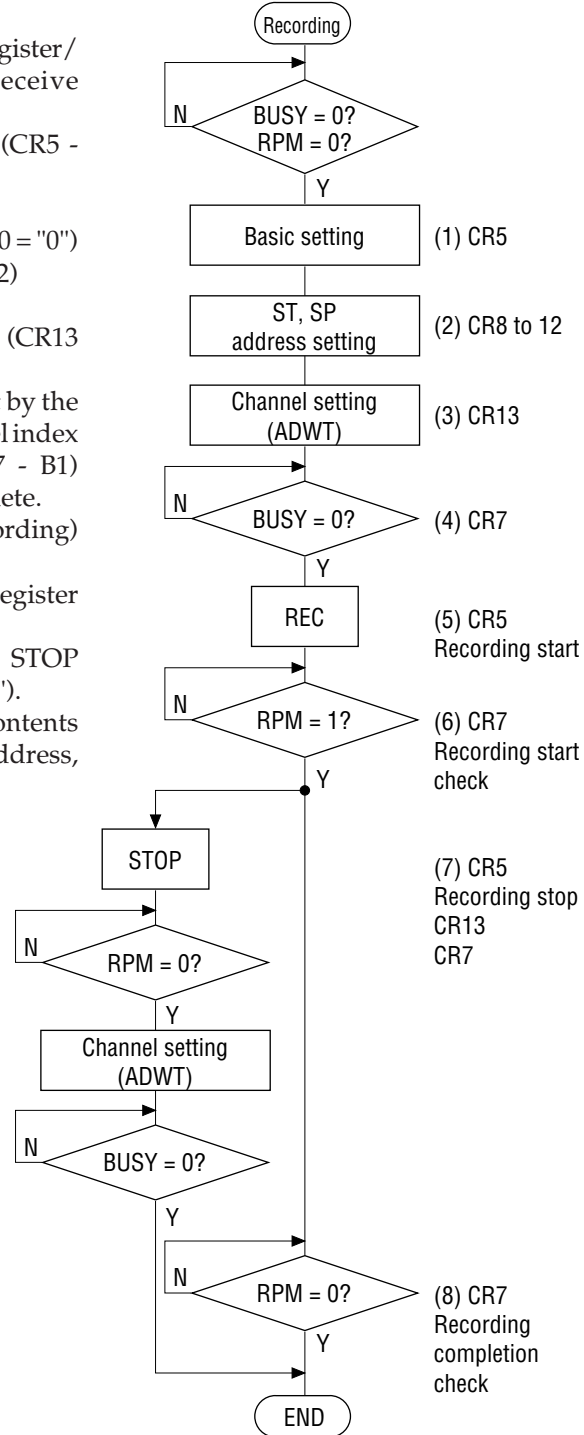


Figure 18 Flow Chart of Recording

Playback Method (See the flow chart in Figure 19)

- (1) • Set up the connection between the serial register/voice ROM and ADPCM transmit-receive system. (See Figure 20) (CR5 - B7)
 - Specify the serial register/voice ROM. (CR5 - B6)
 - Set the external capacity. (CR5 - B5)
 - Set the NOP command. (CR5 - B1 = "0", B0 = "0")
- (2) • Set the channel. (CR13 - B7 to B3)
 - Set the ADRD (address read) instruction. (CR13 - B1 = "1", B0 = "0")
- (3) • The start/stop address of the channel set by the ADRD instruction is fetched from the channel index area.
When status register BUSY (CR7 - B1) changes from "1" to "0", fetching is complete.
- (4) • Start playback by setting the PLAY (playback) command (CR5 - B1 = "0", B0 = "1").
- (5) • Check the playback start with the status register RPM bit (CR7 - B0 = "1").
- (6) • To stop playback set the STOP command (CR5 - B1 = "1", B0 = "1").
- (7) • When the address counter reaches the stop address, playback is complete. Check completion of playback with RPM bit = "0".

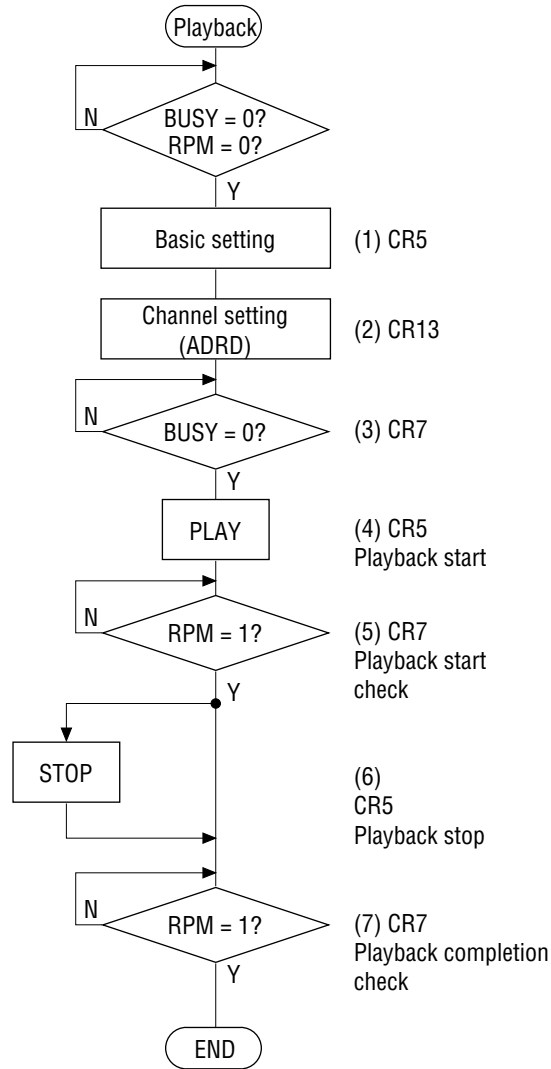


Figure 19 Flow Chart of Playback

SIGNAL FLOW IN RECORDING/PLAYBACK

When the serial register is connected to each ADPCM transmitter and receiver, the flow of recording/playback signal is as follows:

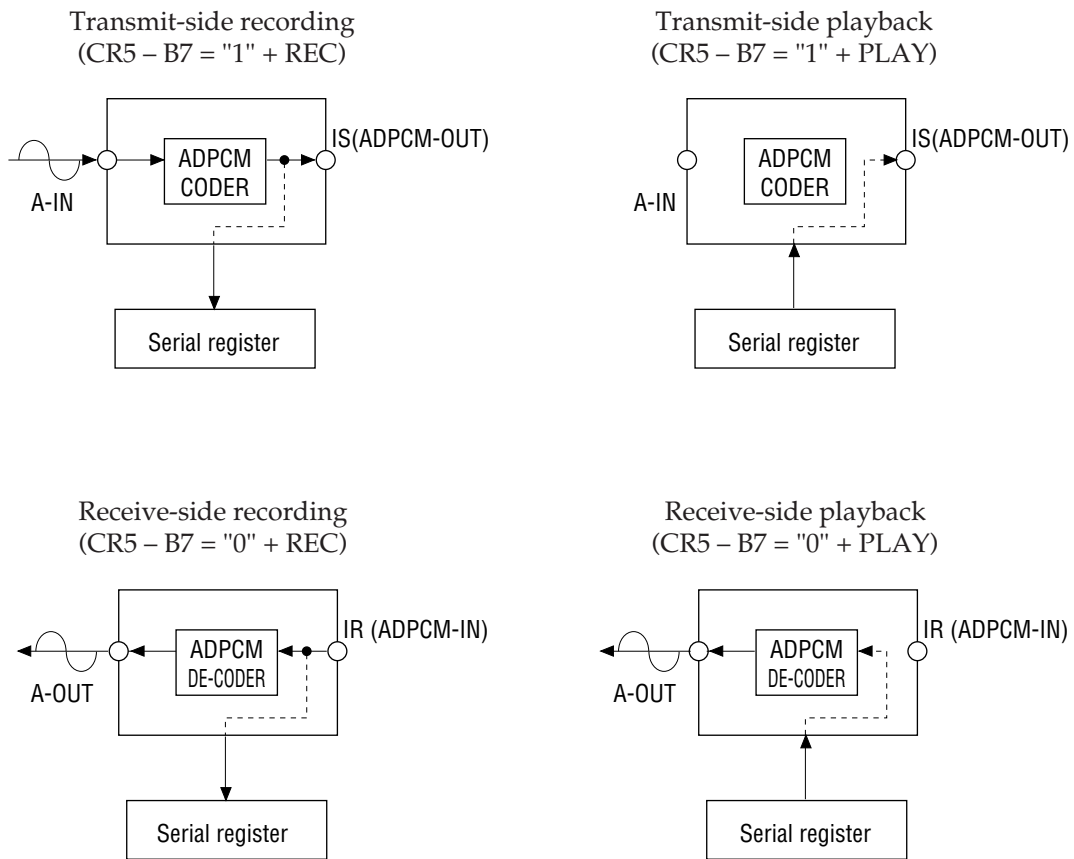
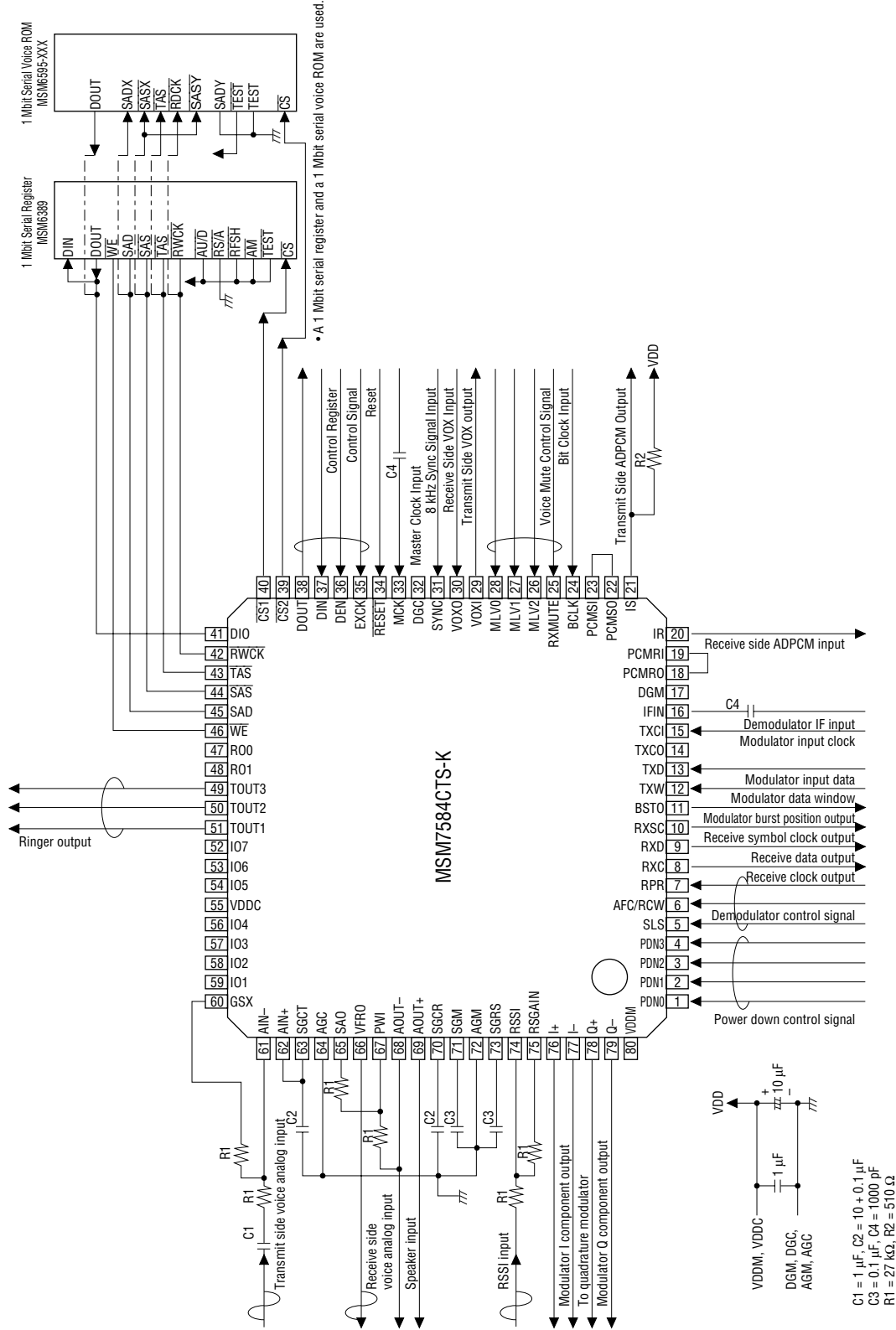


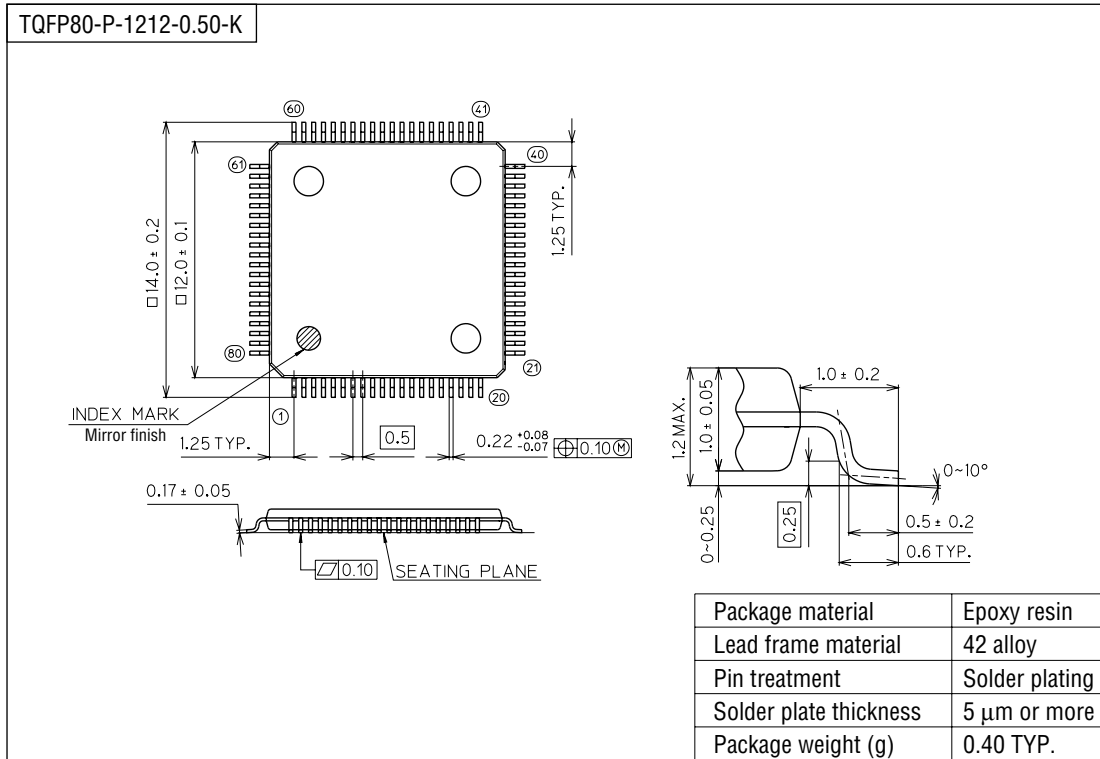
Figure 20 Signal Flow in Transmit/Receive Side Recording/Playback

APPLICATION CIRCUIT



PACKAGE DIMENSIONS

(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).