OKI Semiconductor

This version: Nov. 2001
Previous version: Aug. 1998

MSM7570-01

Multi-Function ADPCM CODEC

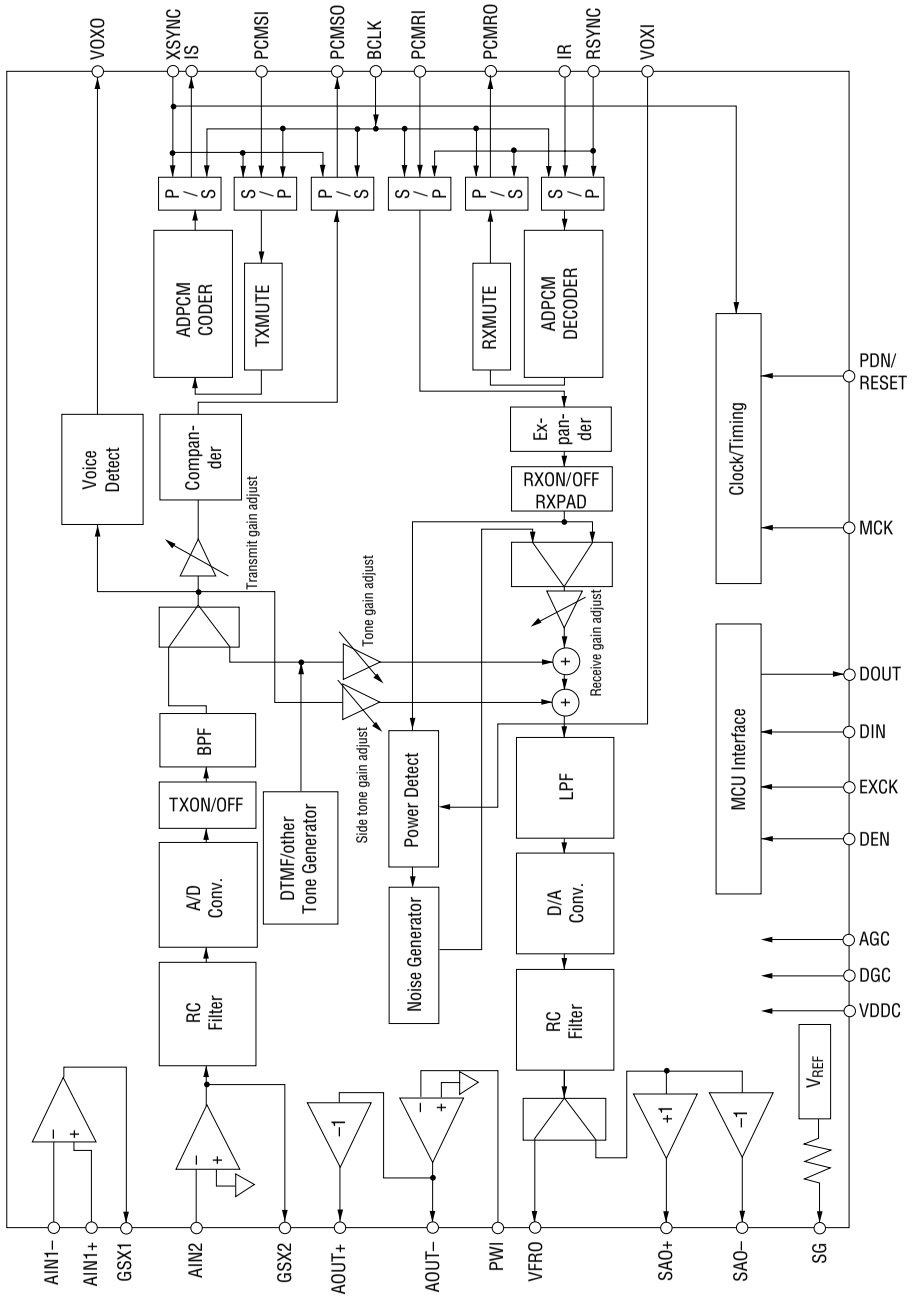
GENERAL DESCRIPTION

The MSM7570-01, developed for advanced digital cordless telephone systems, is a single channel ADPCM CODEC IC which performs mutual transcoding between the analog voice band signal and 32 kbps ADPCM serial data.
This device includes DTMF Tone and several types of tone generation, transmit/receive data mute and gain control, side-tone path and gain control, and VOX function.
Using advanced ciruit technology, the device operates using a single 5 V power supply and have low power consumption.

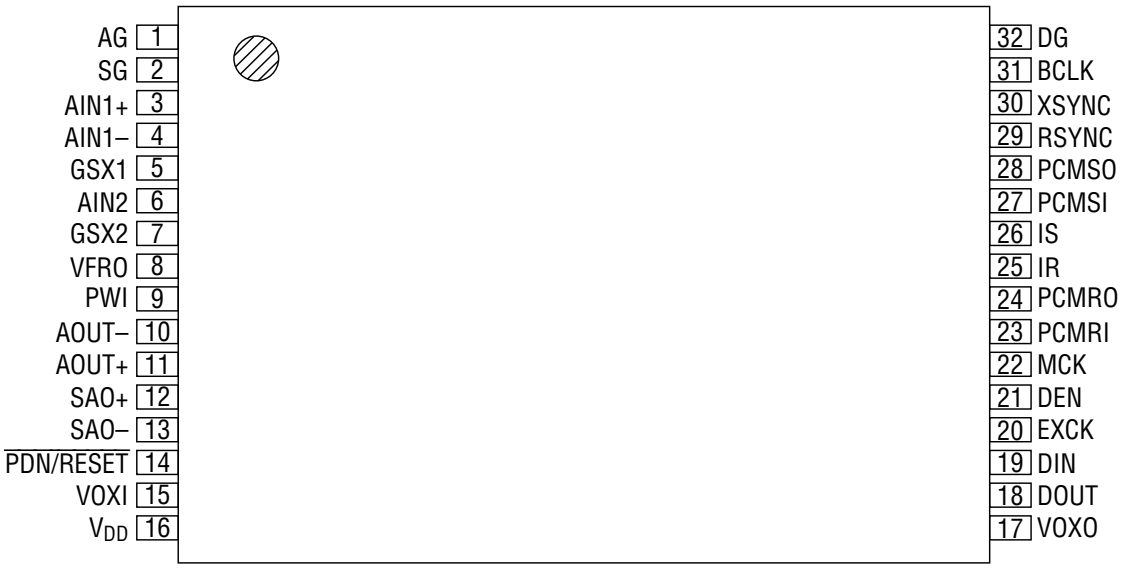
FEATURES

- Single 5 V Power Supply Operation V_{DD}: 4.5 V to 5.5 V
- ADPCM Algorithm : ITU-T G.726 (32 kbps, 24 kbps, 16 kbps)
- Transmit/Receive Full-Duplex Single Channel Operation
- Transmit/Receive Synchronous Mode Only
- PCM Data Format : A-law/μ-law Selectable
- Serial PCM/ADPCM Transmission Data Rate :64 kbps to 2048 kbps
- Low Power Consumption
  - Operating Mode : 70 mW Typ. (V_{DD} = 5.0 V)
  - Power-Down Mode : 0.5 mW Typ. (V_{DD} = 5.0 V)
- Two Analog Input Amplifier Stages : Externally Adjustable Gain
- Analog Output Stage : Push-pull Drive (direct drive of 350 Ω + 120 nF)
- Master Clock Frequency : 12.288/19.200 MHz Selectable
- Transmit/Receive Mute, Transmit/Receive Programmable Gain Control
- Side Tone Path with Programmable Attenuation (8-step Level Adjustment)
- Built-in DTMF Tone Generator
- Built-in Various Ringing/Function Tones Generator
- Built-in Various Ring Back Tone Generator
- Serial MCU Interface Control
- Built-in Sounder Driving Amplifier
- Built-in VOX Control
  - Transmit side : Voice Signal Detect
  - Receive side : Background Noise Generation
- Characteristic Evaluation Board.
- Package:
  32-pin plastic TSOP (TSOP(1)32-P-0814-0.50-1K) (Product name: MSM7570-01TS-K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



32-Pin Plastic TSOP

PIN AND FUNCTIONAL DESCRIPTIONS

AIN1+, AIN1–, AIN2, GSX1, GSX2

Transmit analog inputs and the output for transmit gain adjustment.
AIN1– (AIN2) connects to the inverting input of the internal transmit amplifier. AIN1+ connects to non-inverting input of the internal transmit amplifier. GSX1 (GSX2) connects to the internal transmit amplifier output. Refer to Fig.1 for gain adjustment.

VFRO, AOUT+, AOUT–, PWI

Receive analog outputs and the output for receive gain adjustment.
VFRO is the receive filter output. AOUT+ and AOUT– are differential analog signal outputs which can directly drive $Z_L = 350\ \Omega + 120$ nF or a 1.2 kΩ load. Refer to Fig.1 for gain adjustment.

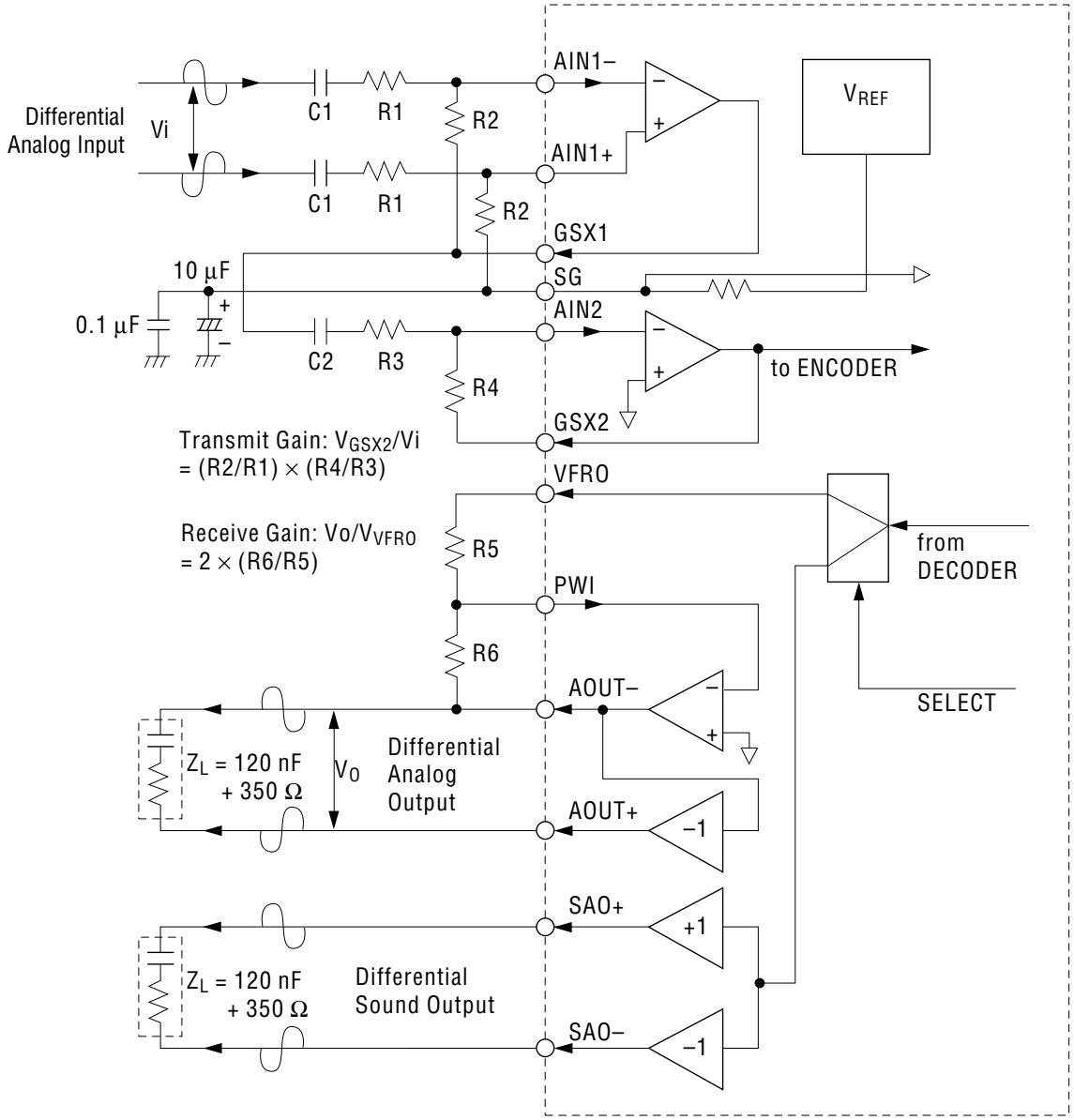


Figure 1 Analog Input/Output Interface

SAO+, SAO–

Differential analog outputs for sound output.
Control register data CR4-B5 determines the output pins (AOUT+ and AOUT- /SAO+ and SAO-) for the voice signal and an acoustic component of the sound tone, DTMF tone, R tone, F tone, and various types of tones at either the VFRO pin or the SAO+ and SAO- pins. The output load conditions of these pins are the same as those of AOUT+ and AOUT-.

SG

Analog signal ground.
The output voltage of this pin is approximately 2.4 V. Put the bypass capacitors (10 µF in parallel with 0.1 µF ceramic type) between this pin and AG to get the specified noise characteristics. During power-down, this output voltage is 0 V. The SG voltage if necessary should be used via a baffer.

AG

Analog ground.

DG

Digital ground.
This ground is separated from the analog signal ground pin (AG). The DG pin must be kept as close as possible to AG on the PCB.

V_{DD}

+5 V power supply.

$\overline{\text{PDN/RESET}}$

Power down and reset control input.
A “0” level makes the IC enter a power down state. At the same time, all control register data is reset to the initial state. Set this pin to “1” during normal operating mode. The power down state is controlled by a logical OR with CR0-B5 of the control register. When using $\overline{\text{PDN/RESET}}$ for power down and reset control, set CR0-B5 to digital “0”. The reset width (during "L") should be 200 ns or more.
Be sure to reset the control registers by executing this power down to keep this pin to digital “0” level for 200ns or longer after the power is turned on and V_{DD} exceeds 4.5V.

MCK

Master clock input.
The frequency must be 12.288 MHz or 19.2 MHz. The applied clock frequency is selected by the control register data CR0-B6. The master clock signal may be asynchronous with BCLK, XSYNC, and RSYNC.

PCMSO

Transmit PCM data output.
PCM is output from MSB in synchronization with the rising edge of BCLK and XSYNC.

PCMSI

Transmit PCM data input.
This signal is converted to the transmit ADPCM data. PCM is shifted in synchronization with the falling edge of BCLK. Normally, this pin is connected to PCMSO.

PCMRO

Receive PCM data output.
PCM is the output signal after ADPCM decoder processing. This signal is output serially from MSB in synchronization with the rising edge of BCLK and RSYNC.

PCMRI

Receive PCM data input.
PCM is shifted on the rising edge of the BCLK and input from MSB. Normally, this pin is connected to PCMRO.

IS

Transmit ADPCM signal output.
After having encoded PCM with ADPCM, this signal is output from MSB in synchronization with the rising edge of BCLK and XSYNC. This pin is an open drain output and remains in a high impedence state during power-down. IS requires a pull-up resistor.

IR

Receive ADPCM signal input.
This input signal is shifted serially on the falling edge of BCLK in synchronization with RSYNC and input from MSB.

BCLK

Shift clock input for the PCM data (PCMSO, PCMSI, PCMRO, PCMRI) and the ADPCM data(IS, IR) .
The frequency is set in the 64 kHz to 2048 kHz range.

XSYNC

Transmit PCM and ADPCM data 8 kHz synchronous signal input.
Synchronize this signal with BCLK signal . XSYNC is used to indicate the MSB of the transmit serial PCM and ADPCM data stream.
Be sure to input the XSYNC signal because it is also used as the input of the timing generator.

RSYNC

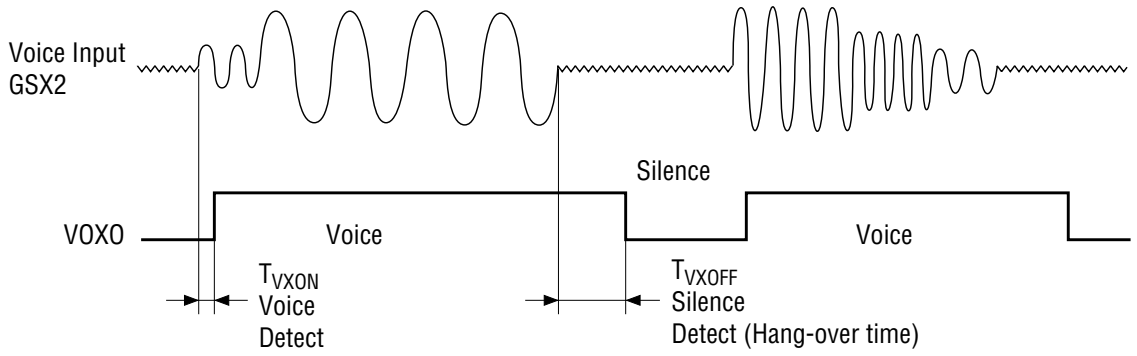
Receive PCM and ADPCM data synchronous signal input.
Synchronize this signal with BCLK signal. RSYNC is used to indicate the MSB of the receive serial PCM and ADPCM data stream.

VOXO

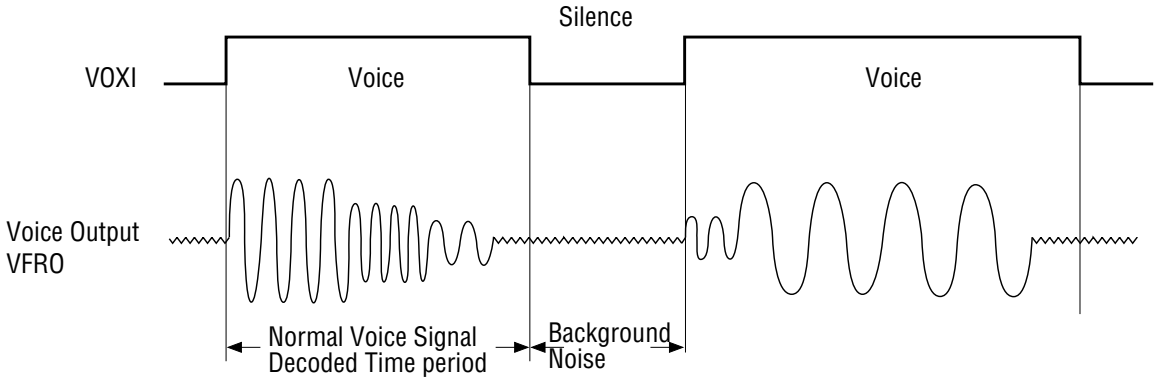
Transmit VOX function signal output.
VOX function recognizes the presence or absence of the transmit voice signal by detecting the signal energy. "1" and "0" levels set on this pin correspond to the presence and the absence of voice, respectively. This result appears at the register data CR7-B7. The signal energy detect threshold is set by the control register data CR6-B6, B5.

VOXI

Signal input for receive VOX function.
A "1" level at VOXI indicates the presence of a voice signal. The decoder block processes normal receive signal, and the voice signal appears at analog output pins . The "0" level indicates the absence of a voice signal. Background noise generated in this device is transferred to the analog output pins. The background noise amplitude is set by the control register CR6. Because this signal is ORed with the register data CR6-B3, set the control register data CR6-B3 to digital "0".



(a) Transmit VOX Function Timing Diagram



(b) Receive VOX Function (CR6-B3: digital "0") Timing Diagram

Note: VOXO, VOXI functions become valid when setting CR6-B7 to digital “1”.

Figure 2 VOX Function

DEN , EXCK, DIN, DOUT

Serial control ports for MCU interface.
Reading and writing data are performed by an external MCU through these pins. Eight registers with eight bits are provided on the devices.
DEN is the "Enable" control signal input, EXCK is the data shift clock input, DIN is the address and data input, and DOUT is the data output.
Fig.3 shows the input/output timing diagram.

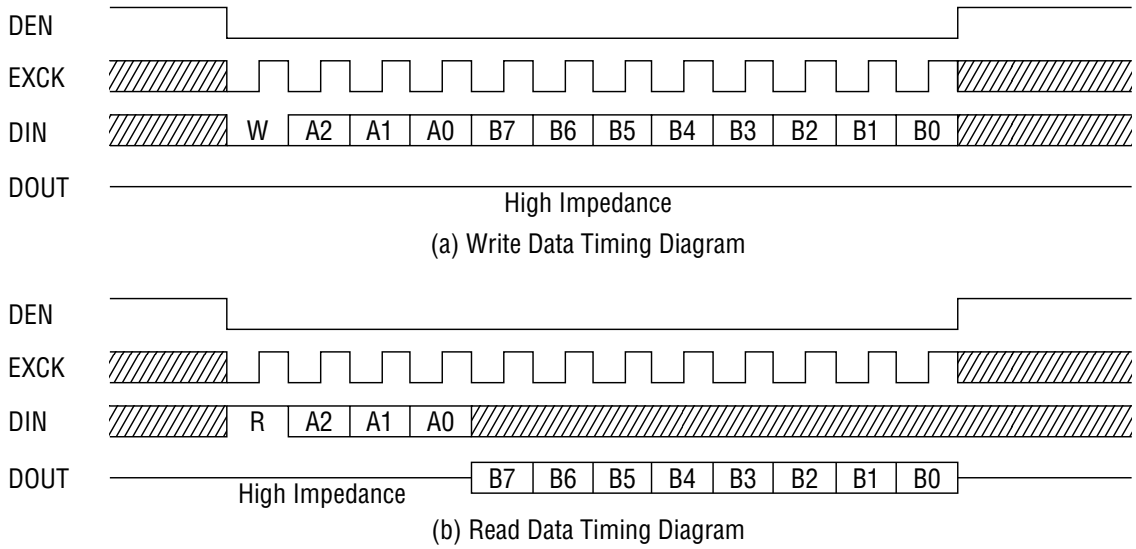


Figure 3 MCU Interface Input/Output Timing

Table 1 shows the register map.

Table-1

Name	Address			Control and Detect Data								R/W
	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	
CR0	0	0	0	A/μ SEL	MCK SEL	PDN ALL	—	—	—	—	PDN SAO/AOUT	R/W
CR1	0	0	1	MODE1	MODE0	TX RESET	RX RESET	TX MUTE	RX MUTE	—	RX PAD	R/W
CR2	0	1	0	TX ON/OFF	TX GAIN2	TX GAIN1	TX GAIN0	RX ON/OFF	RX GAIN2	RX GAIN1	RX GAIN0	R/W
CR3	0	1	1	Side Tone GAIN2	Side Tone GAIN1	Side Tone GAIN0	TONE ON/OFF	TONE GAIN3	TONE GAIN2	TONE GAIN1	TONE GAIN0	R/W
CR4	1	0	0	DTMF/ OTHERS SEL	TONE SEND	SAO/ VFRO	TONE4	TONE3	TONE2	TONE1	TONE0	R/W
CR5	1	0	1	—	—	—	—	—	—	—	—	R/W
CR6	1	1	0	VOX ON/OFF	ON LVL1	ON LVL0	OFF TIME	VOX IN	RX NOISE LEVEL SEL	RX NOISE LVL1	RX NOISE LVL0	R/W
CR7	1	1	1	VOX OUT	TX NOISE LVL1	TX NOISE LVL0	—	—	—	—	—	R

R/W : Read/Write enable R : Read only register.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	—	–0.3 to +7	V
Analog Input Voltage	V_{AIN}	—	–0.3 to V_{DD} + 0.3	V
Digital Input Voltage	V_{DIN}	—	–0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	Voltage must be fixed	4.5	—	5.5	V
Operating Temperature	Ta	—	–25	+25	+70	°C
Digital Input High Voltage	V_{IH}	MCK, XSYNC, RSYNC, PCMRI, PCMSI, BCLK, IR, $\overline{\text{PDN/RESET}}$, DEN, EXCK, DIN	2.2	—	V_{DD}	V
Digital Input Low Voltage	V_{IL}	MCK, XSYNC, RSYNC, PCMRI, PCMSI, BCLK, IR, $\overline{\text{PDN/RESET}}$, DEN, EXCK, DIN	0	—	0.6	V
Master Clock Frequency	f_{MCK1}	MCK (CR0–B6 = "0")	–0.01%	12.288	+0.01%	MHz
	f_{MCK2}	MCK (CR0–B6 = "1")	–0.01%	19.200	+0.01%	MHz
Bit Clock Frequency	f_{BCK}	BCLK	64	—	2048	kHz
Synchronous Signal Frequency	f_{SYMC}	XSYNC, RSYNC	—	8.0	—	kHz
Clock Duty Ratio	D_C	MCK, BCLK, EXCK	30	50	70	%
Digital Input Rise Time	t_{Ir}	MCK, XSYNC, RSYNC, PCMRI, PCMSI, BCLK, IR, $\overline{\text{PDN/RESET}}$, DEN, EXCK, DIN	—	—	50	ns
Digital Input Fall Time	t_{If}	MCK, XSYNC, RSYNC, PCMRI, PCMSI, BCLK, IR, $\overline{\text{PDN/RESET}}$, DEN, EXCK, DIN	—	—	50	ns
Transmit Sync Signal Setting Time	t_{XS}	BCLK to XSYNC	100	—	—	ns
	t_{SX}	XSYNC to BCLK	100	—	—	ns
Receive Sync Signal Setting Time	t_{RS}	BCLK to RSYNC	100	—	—	ns
	t_{SR}	RSYNC to BCLK	100	—	—	ns
Synchronous Signal Width	t_{WS}	XSYNC, RSYNC	1 BCLK	—	100	µs
PCM, ADPCM Set-up Time	t_{DS}	—	100	—	—	ns
PCM, ADPCM Hold Time	t_{DH}	—	100	—	—	ns
Digital Output Load	R_{DL}	IS (Pull-up Resistor)	500	—	—	Ω
	C_{DL}	IS, PCMSO, PCMRO, VOXO, DOUT	—	—	100	pF
Bypass Capacitors for SG	C_{SG}	SG to AG	10 + 0.1	—	—	µF

ELECTRICAL CHARACTERISTICS

DC and Digital Interface Characteristics

(V_{DD} = 4.5 V to 5.5 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current	I_{DD1}	Operating Mode, No Signal, (V_{DD} = 5.0 V)	—	14	28	mA
	I_{DD2}	Power Down Mode, (V_{DD} = 5.0 V)	—	0.1	0.2	mA
Input High Voltage	V_{IH}	—	2.2	—	V_{DD}	V
Input Low Voltage	V_{IL}	—	0.0	—	0.6	V
Input Leakage Current	I_{IH}	$V_I = V_{DD}$	—	—	2.0	µA
	I_{IL}	V_I = 0 V	—	—	0.5	µA
Output Low Voltage	V_{OL}	1 LSTTL, Pull-up: 500 Ω	0.0	0.2	0.4	V
Output Leakage Current	I_O	IS	—	—	10	µA
Input Capacitance	C_{IN}	—	—	5	—	pF
Output Resistance	R_{OSG}	SG	—	25	50	kΩ
SG Warm-up Time	T_{SG}	SG↔GND 10+0.1 µF (Rise time to 90% of max. level)	—	700	—	ns

Transmit Analog Interface Characteristics

(V_{DD} = 4.5 V to 5.5 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Resistance	R_{INX}	AIN1+ , AIN1– , AIN2	10	—	—	MΩ
Output Load Resistance	R_{LGX}	GSX1, GSX2	20	—	—	kΩ
Output Load Capacitance	C_{LGX}	GSX1, GSX2	—	—	100	pF
Output Amplitude	V_{OGX}	GSX1, GSX2, R_L = 20 kΩ	—	—	*2.226	V_{PP}
Input Offset Voltage	V_{OFGX}	Pre–OPAMPs	–20	—	+20	mV

* –3.0 dBm (600 Ω) = 0 dBm0, + 3.14 dBm0 = 2.226 V_{PP} (A-law)
–3.0 dBm (600 Ω) = 0 dBm0, + 3.17 dBm0 = 2.226 V_{PP} (µ-law)

Receive Analog Interface Characteristics

(V_{DD} = 4.5 V to 5.5 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Input Resistance	R_{INPW}	PWI		10	—	—	MΩ
Output Load Resistance	R_{LVF}	VFRO		20	—	—	kΩ
	R_{LAO}	AOUT+, AOUT–, SAO+, SAO–		1.2	—	—	kΩ
Output Capacitance	C_{LVF}	VFRO		—	—	100	pF
	C_{LAO}	AOUT+, AOUT–, SAO+, SAO–		—	—	100	pF
Output Voltage Level	V_{OVF}	VFRO,	R_L = 20 kΩ	—	—	*2.226	V_{PP}
	V_{OAO}	AOUT+, AOUT–, SAO+, SAO–	R_L = 1.2 kΩ	—	—	*2.226	V_{PP}
			Z_L = 350 Ω + 120 nF(See Fig.1)	—	—	*2.226	V_{PP}
Offset Voltage	V_{OFVF}	VFRO		–100	—	+100	mV
	V_{OFAO}	AOUT+, AOUT– (GAIN = 0 dB, Power amp only) SAO+, SAO–		–20	—	+20	mV
Open Loop Gain	G_{DB}	Power amp (0.3 to 3.4 kHz, Z_L = 350 Ω + 120 nF)(See Fig.1)		40	—	—	dB

* –3.0 dBm (600 Ω) = 0 dBm0, + 3.14 dBm0 = 2.226 V_{PP} (A-law)
–3.0 dBm (600 Ω) = 0 dBm0, + 3.17 dBm0 = 2.226 V_{PP} (μ-law)

AC Chracteristics

(V_{DD} = 4.5 V to 5.5 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition			Min.	Typ.	Max.	Unit
		Freq. (Hz)	Level (dBm0)	Others				
Transmit Frequency Response	L_{OSS} T1	0 to 60	0	—	25	—	—	dB
	L_{OSS} T2	300 to 3000			–0.15	—	+0.20	dB
	L_{OSS} T3	1020			Reference			dB
	L_{OSS} T4	3300			–0.15	—	+0.80	dB
	L_{OSS} T5	3400			0	—	0.80	dB
	L_{OSS} T6	3968.75			13	—	—	dB
Receive Frequency Response	L_{OSS} R1	0 to 3000	0	—	–0.15	—	+0.20	dB
	L_{OSS} R2	1020			Reference			dB
	L_{OSS} R3	3300			–0.15	—	+0.80	dB
	L_{OSS} R4	3400			0	—	0.80	dB
	L_{OSS} R5	3968.75			13	—	—	dB
Transmit Signal to Distortion Ratio	SD T1	1020	3	(*1)	35	—	—	dB
	SD T2		0		35	—	—	dB
	SD T3		–30		35	—	—	dB
	SD T4		–40		28	—	—	dB
	SD T5		–45		23	—	—	dB
Receive Signal to Distortion Ratio	SD R1	1020	3	(*1)	35	—	—	dB
	SD R2		0		35	—	—	dB
	SD R3		–30		35	—	—	dB
	SD R4		–40		28	—	—	dB
	SD R5		–45		23	—	—	dB
Transmit Gain Tracking	GT T1	1020	3	—	–0.2	—	+0.2	dB
	GT T2		–10		Reference			dB
	GT T3		–40		–0.2	—	+0.2	dB
	GT T4		–50		–0.5	—	+0.5	dB
	GT T5		–55		–1.2	—	+1.2	dB
Receive Gain Tracking	GT R1	1020	3	—	–0.2	—	+0.2	dB
	GT R2		–10		Reference			dB
	GT R3		–40		–0.2	—	+0.2	dB
	GT R4		–50		–0.5	—	+0.5	dB
	GT R5		–55		–1.2	—	+1.2	dB

*1 Use the P-message weighted filter

AC Characteristics (Continued)

(V_{DD} = 4.5 V to 5.5 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition			Min.	Typ.	Max.	Unit
		Freq. (Hz)	Level (dBm0)	Others				
Idle Channel Noise	N_{IDLT}	—	AIN = SG	(*1)	—	—	–68 (–71)	dBm0p (dBmp)
	N_{IDLR}	—	—	(*1) (*2)	—	—	–72 (–75)	
Absolute Signal Amplitude	A_{VT}	1020	0	GSX2	0.488	0.548 (*3)	0.615	Vrms
	A_{VR}			VFRO	0.488	0.548 (*3)	0.615	Vrms
Power Supply Noise Rejection Ratio	P_{SRRT}	Noise Freq. : 0 to 50 kHz	Noise Level : 50 mV_{PP}	—	30	—	—	dB
	P_{SRRR}				30	—	—	dB
Digital Output Delay Time PCM and ADPCM Interface	t_{SDX}	—	1 LSTTL + 100 pF, Pull-up: 500 Ω	See Fig.4	0	—	200	ns
	t_{SDR}				0	—	200	ns
	t_{XD1} t_{RD1}				0	—	200	ns
	t_{XD2} t_{RD2}				0	—	200	ns
	t_{XD3} t_{RD3}				0	—	200	ns
Serial Port Digital Input/Output Setting Time	t_{M1}	—	C_L = 100 pF	See Fig.5	50	—	—	ns
	t_{M2}				50	—	—	ns
	t_{M3}				50	—	—	ns
	t_{M4}				50	—	—	ns
	t_{M5}				100	—	—	ns
	t_{M6}				50	—	—	ns
	t_{M7}				50	—	—	ns
	t_{M8}				0	—	50	ns
	t_{M9}				50	—	—	ns
	t_{M10}				50	—	—	ns
	t_{M11}				0	—	50	ns
Shift Clock Frequency	f_{EXCK}	—	—	EXCK	—	—	10	MHz

*1 Use the P-message weighted filter

*2 PCMRI input code "11010101"(A-law)
"11111111"(m-law)

*3 0.548 Vrms = 0 dBm0 = –3.0 dBm

Note: All ADPCM coder and decoder characteristics comply with ITU-T Recommendation G.726.

AC Characteristics (DTMF and Other Tones)

(V_{DD} = 4.5 V to 5.5 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Frequency Difference	D_{FT1}	DTMF Tones		–7	—	+7	Hz
	D_{FT2}	Other Tones		–7	—	+7	Hz
Original (reference) Tone Signal Level *4	V_{TL}	Transmit Tones (Gain setting 0 dB)	DTMF (Low)	–18	–16	–14	dBmO
	V_{TH}		DTMF (High) and Other Tones	–16	–14	–12	dBmO
	V_{RL}	Receive Tones (Tone generator gain setting –6 dB)	DTMF (Low)	–10	–8	–6	dBmO
	V_{RH}		DTMF (High) and Other Tones	–8	–6	–4	dBmO
Relative Level of DTMF Tones	R_{DTMF}	V_{TH}/V_{TL}, V_{RH}/V_{RL}		1	2	3	dBmO

*4 Does not contain the setting value set for the programmable gain

AC Characteristics (Programmable Gain Stages)

(V_{DD} = 4.5 V to 5.5 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Gain Accuracy	D_G	All gain stages, to programmed value	–1	0	+1	dB

AC Characteristics (VOX Function)

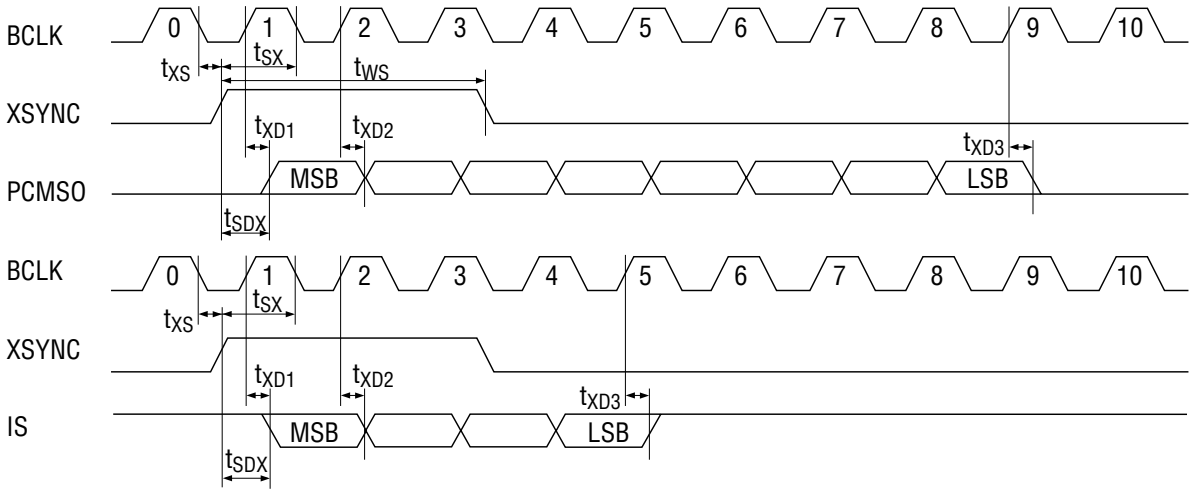
(V_{DD} = 4.5 V to 5.5 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Transmit VOX Detect Time	t_{VXON}	OFF → ON	VOXO, See Fig.2	—	10 *5	—	ms
(Voice Signal ON/OFF Detect Time)	t_{VXOF}	ON → OFF		150/310	160/320	170/330	ms
Transmit VOX Detect Level Accuracy (Threshold Level)	D_{VX}	To the values (CR6-B6, B5)		–2.5	0	+2.5	dB

*5 When single tone is input at 1000 Hz.

TIMING DIAGRAM

Transmit Side PCM/ADPCM Data Interface



Receive Side PCM/ADPCM Data Interface

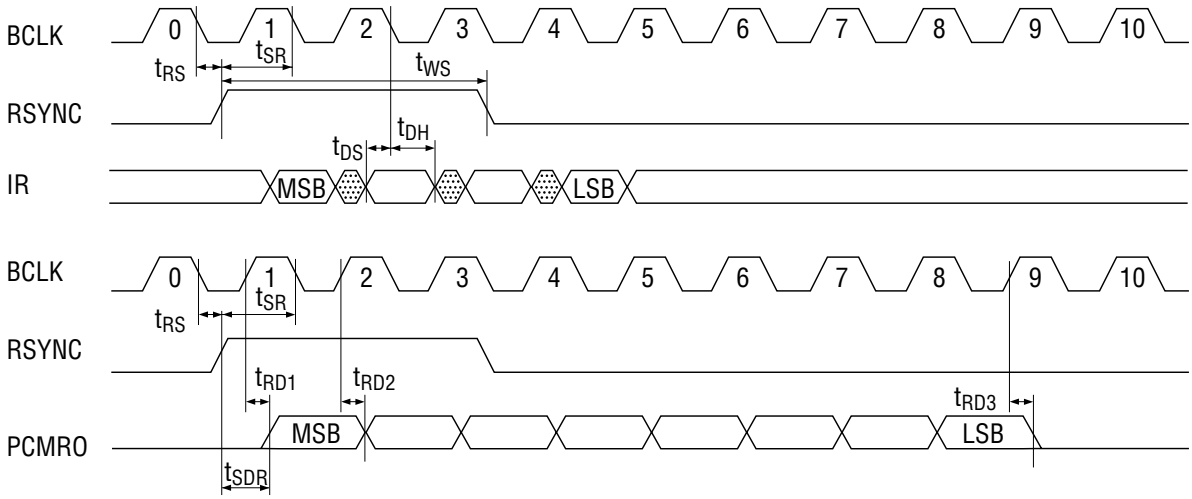


Figure 4 PCM/ADPCM Data Interface

Serial Port Data Transfer for MCU Interface

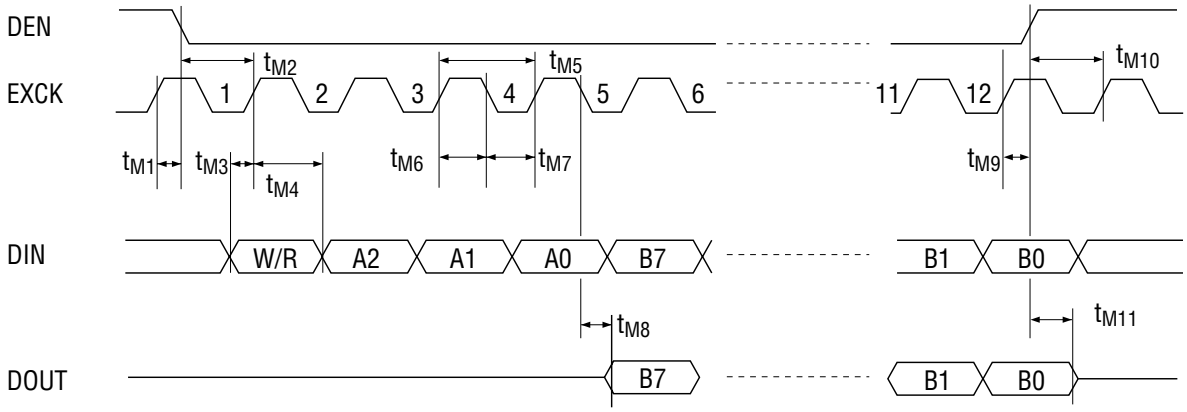


Figure 5 MCU Interface

FUNCTIONAL DESCRIPTION

Control Registers

(1) CR0 (Basic operating mode)

	B7	B6	B5	B4	B3	B2	B1	B0
CR0	A/μ SEL	MCK SEL	PDN ALL	—	—	—	—	PDN SAO/AOUT
Initial Value	0	0	0	0	0	0	0	0

Note : Initial Value : Reset state by $\overline{\text{PDN/RESET}}$

B7 ...PCM Companding law select; 0/μ-law, 1/A-law
B6 ...Master clock frequency select; 0/12.288 MHz, 1/19.200 MHz
B5 ...Power down (entire system); 0/Power on, 1/Power down
When using this data for power down control, set pin $\overline{\text{PDN/RESET}}$ at "1" level.
The control registers are not reset by this signal.
B2 ...Not used
B1 ...Not used
B0 ...Power Down for Sound output amps: (SAO+, SAO–), or Receiver output amp (AOUT+, AOUT–, VFRO);
If this data is set to digital "1", either a pair of sound amplifiers or a pair of reciver amplifiers enters the power down state depending on the set data on CR4-B5.
If this data is set to digital "0", sound amplifiers and receiver amplifiers are in the power-on state.
B4, B3 ... Not used (These pins are used to test the devise. They should be set to "0" during normal operation.)

(2) CR1 (ADPCM block operating mode)

	B7	B6	B5	B4	B3	B2	B1	B0
CR1	MODE1	MODE0	TX RESET	RX RESET	TX MUTE	RX MUTE	—	RX PAD
Initial Value	0	0	0	0	0	0	0	0

B7, B6 ... ADPCM data compression algorithm select;
- (0, 0): 32 kbps
- (0, 1): 64 kbps (data through)
- (1, 0): 24 kbps
- (1, 1): 16 kbps

B5 ... ADPCM of transmit reset (specified by G.726); 1/Reset*
B4 ... ADPCM of receive reset (specified by G.726); 1/Reset*
B3 ... ADPCM transmit data mute, 1/Mute
B2 ... ADPCM receive data mute, 1/Mute
B1 ... Not used
B0 ... Receive side PAD, 1/inserted,12 dB loss
0/no PAD

* The reset width should be 125 µs or more.
The transmitter and receiver can not be reset separately
They must be reset at the same time.

(3) CR2 (PCM CODEC operational mode setting and transmit/receive gain adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CR2	TX ON/OFF	TX GAIN2	TX GAIN1	TX GAIN0	RX ON/OFF	RX GAIN2	RX GAIN1	RX GAIN0
Initial Value	0	0	1	1	0	0	1	1

B7 ... PCM Coder disable; 0/Enable, 1/Disable (transmit PCM idle pattern)
B6, B5, B4 ... Transmit gain adjustment, refer to Table-2.
B3 ... PCM Decoder disable; 0/Enable, 1/Disable (receive PCM idle pattern)
B2, B1, B0 ... Receive gain setting, refer to Table-2.

Table-2

B6	B5	B4	Transmit Gain	B2	B1	B0	Receive Gain
0	0	0	–6 dB	0	0	0	–6 dB
0	0	1	–4 dB	0	0	1	–4 dB
0	1	0	–2 dB	0	1	0	–2 dB
0	1	1	0 dB	0	1	1	0 dB
1	0	0	+2 dB	1	0	0	+2 dB
1	0	1	+4 dB	1	0	1	+4 dB
1	1	0	+6 dB	1	1	0	+6 dB
1	1	1	+8 dB	1	1	1	+8 dB

This programmable gain table should be assigned, not only for transmit/receive voice signal and the transmitted DTMF and other tones. The transmission of these tone signals is enabled by the CR4-B6 data described later. The original (reference) signal amplitude of these tones is analogically defined as follows.

DTMF low-group-tones ..... –16 dBm0
DTMF high-group-tones and others ..... –14 dBm0

For example, when selecting +8 dB (B6, B5, B4) = (1,1,1) as a transmit gain, each tone signal amplitude with an analogical expression on the pin PCMSO becomes as follows .

DTMF low-group tones ..... –8 dBm0
DTMF high-group tones and other tones ..... –6 dBm0

Gain setting for the side tone (path to receive side from transmit side) and the receive side tone is performed by register CR3.

(4) CR3 (Side tone and other tone generator gain setting)

	B7	B6	B5	B4	B3	B2	B1	B0
CR3	Side. Tone GAIN2	Side. Tone GAIN1	Side. Tone GAIN0	TONE ON/OFF	TONE GAIN3	TONE GAIN2	TONE GAIN1	TONE GAIN0
Initial Value	0	0	0	0	0	0	0	0

B7, B6, B5 ... Side tone path gain setting, refer to Table-3.
B4 ... Tone generator enable; 0/Disable, 1/Enable
B3, B2, B1, B0 ... Tone generator gain adjustment for receive side, refer to Table-4

Table-3

B7	B6	B5	Side Tone Path Gain
0	0	0	OFF
0	0	1	–21 dB
0	1	0	–19 dB
0	1	1	–17 dB
1	0	0	–15 dB
1	0	1	–13 dB
1	1	0	–11 dB
1	1	1	–9 dB

Table-4

B3	B2	B1	B0	Tone Generator Gain	B3	B2	B1	B0	Tone Generator Gain
0	0	0	0	–36 dB	1	0	0	0	–20 dB
0	0	0	1	–34 dB	1	0	0	1	–18 dB
0	0	1	0	–32 dB	1	0	1	0	–16 dB
0	0	1	1	–30 dB	1	0	1	1	–14 dB
0	1	0	0	–28 dB	1	1	0	0	–12 dB
0	1	0	1	–26 dB	1	1	0	1	–10 dB
0	1	1	0	–24 dB	1	1	1	0	–8 dB
0	1	1	1	–22 dB	1	1	1	1	–6 dB

The tone generator gain setting table for the receive side, as shown in Table-4, depends upon the following reference level.

DTMF low-group tones ..... –2 dBm0
DTMF high-group tones and others 0 dBm0

For example, when selecting –6 dB (B3, B2, B1, B0) = (1, 1, 1, 1) as a tone generator gain, each DTMF tone signal amplitude on SAO+/SAO– or VFRO is as follows.

DTMF low-group tone ..... –8 dBm0
DTMF high-group tone or other tones ..... –6 dBm0

(5) CR4 (Tone genereator operating mode and frequency select)

	B7	B6	B5	B4	B3	B2	B1	B0
CR4	DTMF/OTHERS SEL	TONE SEND	SAO/ VFRO	TONE4	TONE3	TONE2	TONE1	TONE0
Initial Value	0	0	0	0	0	0	0	0

B7 ... DTMF or other tones select; 0/Others, 1/DTMF
B6 ... Tone transmit enable (Transmit side); 0/Voice signal (transmit), 1/Tone transmit
B5 ... Tone output pin select (Receive side); 0/VFRO, 1/SAO+ and SAO–
B4, B3, B2, B1, B0 ... Tone frequency setting, referred to Table-5-1 and 5-2.

(a) B7 = 1 (DTMF tone)

Table-5-1

B4	B3	B2	B1	B0	Frequency	B4	B3	B2	B1	B0	Frequency
*	0	0	0	0	697 Hz + 1209 Hz	*	1	0	0	0	852 Hz + 1209 Hz
*	0	0	0	1	697 Hz + 1336 Hz	*	1	0	0	1	852 Hz + 1336 Hz
*	0	0	1	0	697 Hz + 1477 Hz	*	1	0	1	0	852 Hz + 1477 Hz
*	0	0	1	1	697 Hz + 1633 Hz	*	1	0	1	1	852 Hz + 1633 Hz
*	0	1	0	0	770 Hz + 1209 Hz	*	1	1	0	0	941 Hz + 1209 Hz
*	0	1	0	1	770 Hz + 1336 Hz	*	1	1	0	1	941 Hz + 1336 Hz
*	0	1	1	0	770 Hz + 1477 Hz	*	1	1	1	0	941 Hz + 1477 Hz
*	0	1	1	1	770 Hz + 1633 Hz	*	1	1	1	1	941 Hz + 1633 Hz

*Unrelated

(b) B7 = 0 (Other tones)

Table-5-2

B4	B3	B2	B1	B0	Frequency	B4	B3	B2	B1	B0	Frequency
0	0	0	0	0	1k/1333 Hz, 16 Hz wamb.	1	0	0	0	0	2000 Hz Single tone
0	0	0	0	1	800/667 Hz, 16 Hz wamb.	1	0	0	0	1	2042 Hz Single tone
0	0	0	1	0	800/1k Hz,16 Hz wamb.	1	0	0	1	0	2514 Hz Single tone
0	0	0	1	1	500/667 Hz,16 Hz wamb.	1	0	0	1	1	500 Hz Single tone
0	0	1	0	0	500/400 Hz,16 Hz wamb.	1	0	1	0	0	667 Hz Single tone
0	0	1	0	1	800/1k Hz, 8 Hz wamb.	1	0	1	0	1	1333 Hz Single tone
0	0	1	1	0	500/400 Hz, 8 Hz wamb.	1	0	1	1	0	2100 Hz Single tone
0	0	1	1	1	400 Hz,16 Hz wamb.	1	0	1	1	1	—
0	1	0	0	0	400 Hz,20 Hz wamb.	1	1	0	0	0	—
0	1	0	0	1	400 Hz Single tone	1	1	0	0	1	—
0	1	0	1	0	425 Hz Single tone	1	1	0	1	0	—
0	1	0	1	1	440 Hz Single tone	1	1	0	1	1	—
0	1	1	0	0	450 Hz Single tone	1	1	1	0	0	—
0	1	1	0	1	800 Hz Single tone	1	1	1	0	1	—
0	1	1	1	0	1000 Hz Single tone	1	1	1	1	0	—
0	1	1	1	1	1300 Hz Single tone	1	1	1	1	1	—

(6) CR5 (Not used)

	B7	B6	B5	B4	B3	B2	B1	B0
CR5	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0

B7 – B0..... Not used

(7) CR6 (VOX function control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR6	VOX ON/OFF	ON LVL1	ON LVL0	OFF TIME	VOX IN	RX NOISE LEVEL SEL	RX NOISE LVL1	RX NOISE LVL0
Initial Value	0	0	0	0	0	0	0	0

B7 ... VOX function enable; 0/Disable, 1/Enable
B6, B5 ... Transmit signal energy detect (Transmit VOX) threshold (at 1000 Hz)
(0, 0): –30 dBm0
(0, 1): –35 dBm0
(1, 0): –40 dBm0
(1, 1): –45 dBm0
B4 ... Hang-over time (Fig.2, T_{VXOFF}); 0/160 ms, 1/320 ms
B3 ... Receive VOX function setting; 0/Background noise transmit, 1/Voice signal detect
When using this data for control, set pin VOXI at "0" level.
B2 ... Background noise amplitude setting; 0/Automatic, 1/Programmable by B1 and B0
Automatic : Set the noise at the voice signal amplitude when B3 (or VOXI) changes from "1" to digital "0".
B1, B0 ... (0, 0): No noise
(0, 1): –55 dBm0
(1, 0): –45 dBm0
(1, 1): –35 dBm0

(8) CR7 (Detect register, read only)

	B7	B6	B5	B4	B3	B2	B1	B0
CR7	VOX OUT	TX NOISE LVL1	TX NOISE LVL0	—	—	—	—	—
Initial Value	0	0	0	*	*	*	*	*

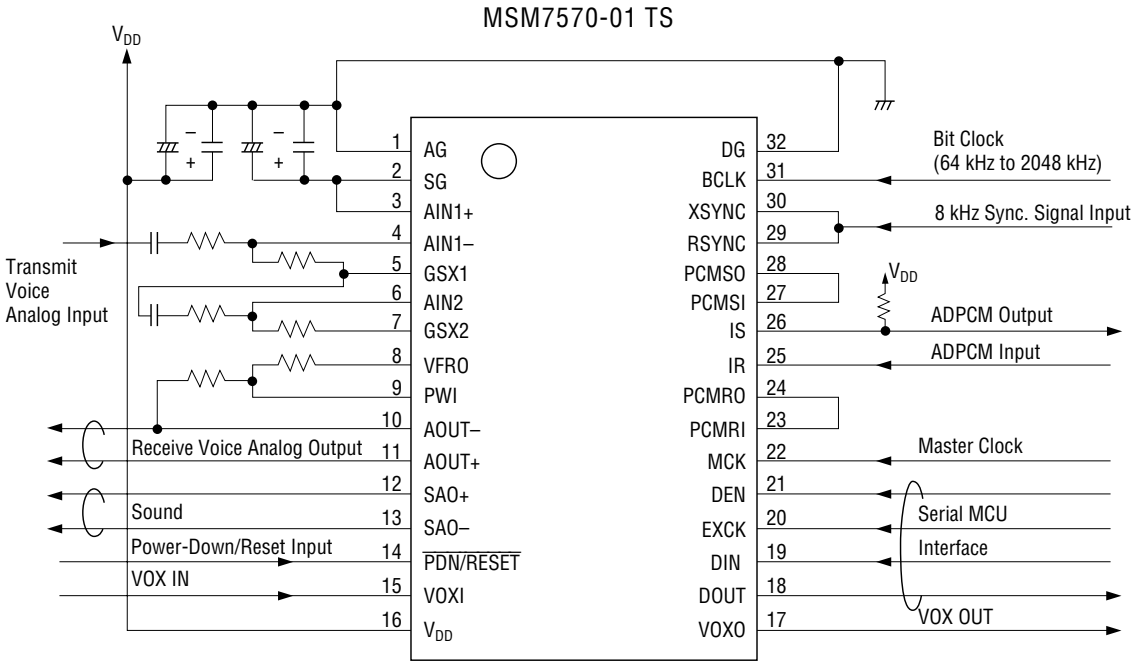
* For IC test

B7 ... Transmit VOX function result; 0/Silence, 1/Voice
B6, B5 ... Transmit silence level (indicator);
(0, 0) : Below –60 dBm0
(0, 1) : –50 to –60 dBm0
(1, 0) : –40 to –50 dBm0
(1, 1) : Above –40 dBm0

Note: These outputs are valid only when the VOX function is enabled by CR6-B7.

B4 ... Not used
B3 ... Not used
B2 ... Not used
B1 ... Not used
B0 ... Not used

APPLICATION CIRCUIT

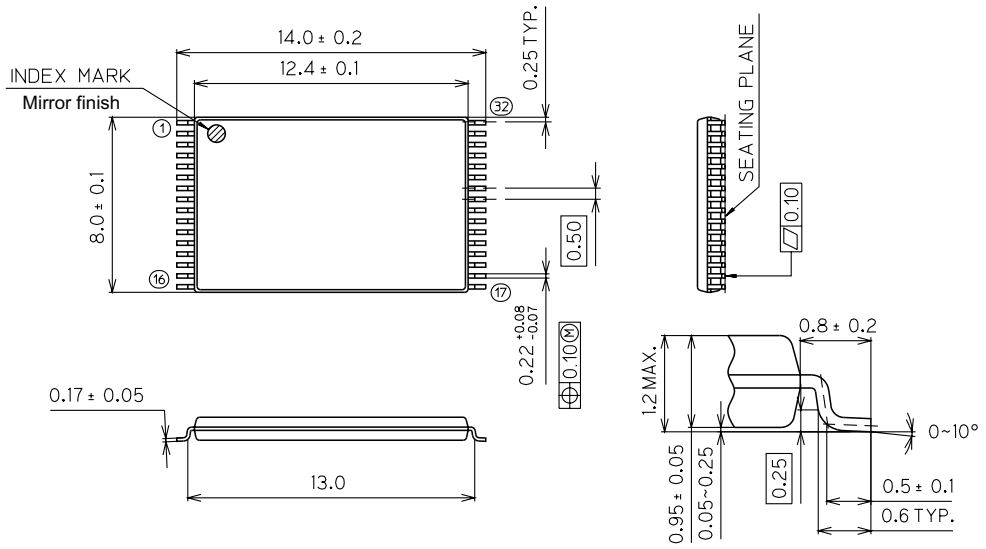


* Single-ended Analog Input Stage Type

PACKAGE DIMENSIONS

(Unit : mm)

TSOP(1)32-P-0814-0.50-1K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5 μm)
Package weight (g)	0.27 TYP.
Rev. No./Last Revised	3/Dec. 10, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
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