E2F0007-18-11

Preliminary

This version: Jan. 1998

OKI Semiconductor

MSM9405

IrDA Communication Controller

GENERAL DESCRIPTION

The MSM9405 is a communication controller conforming to IrDA, the international standard for infrared data communication. The device covers the IrDA physical specifications Ver.1.0 and 1.1.
Since the device performs some of the functions concerning communication protocol control, the load on the software (firmware) for protocol control can be reduced. By combining the device with another microcontroller and an infrared transceiver module, a device provided with IrDA-compliant communication function can be configured.

FEATURES

- Data transfer rates
  - IrDA 1.0 : 2400, 9600 bps; 19.2, 38.4, 57.6, 115.2 kbps
  - IrDA 1.1 : 0.576, 1.152, 4 Mbps

- Detection/removal for beginning of frame and end of frame (IrDA 1.0, 1.1)

  Insertion for beginning of frame and end of frame (IrDA 1.0, 1.1)

- Generation/check for CRC (IrDA 1.0, 1.1)

- Host interface
  - 8-bit data bus : D_0-D_7
  - DMA transfer : DREQ, DACK, $\overline{TC}$
  - Interrupt : $\overline{INTR}$
  - Address : A_0-A_3
  - Control signal : $\overline{CS}$, $\overline{RD}$, $\overline{WR}$

- Infrared module control signal : SD

- Built-in 32-byte transmit-receive FIFOs

- Power down mode

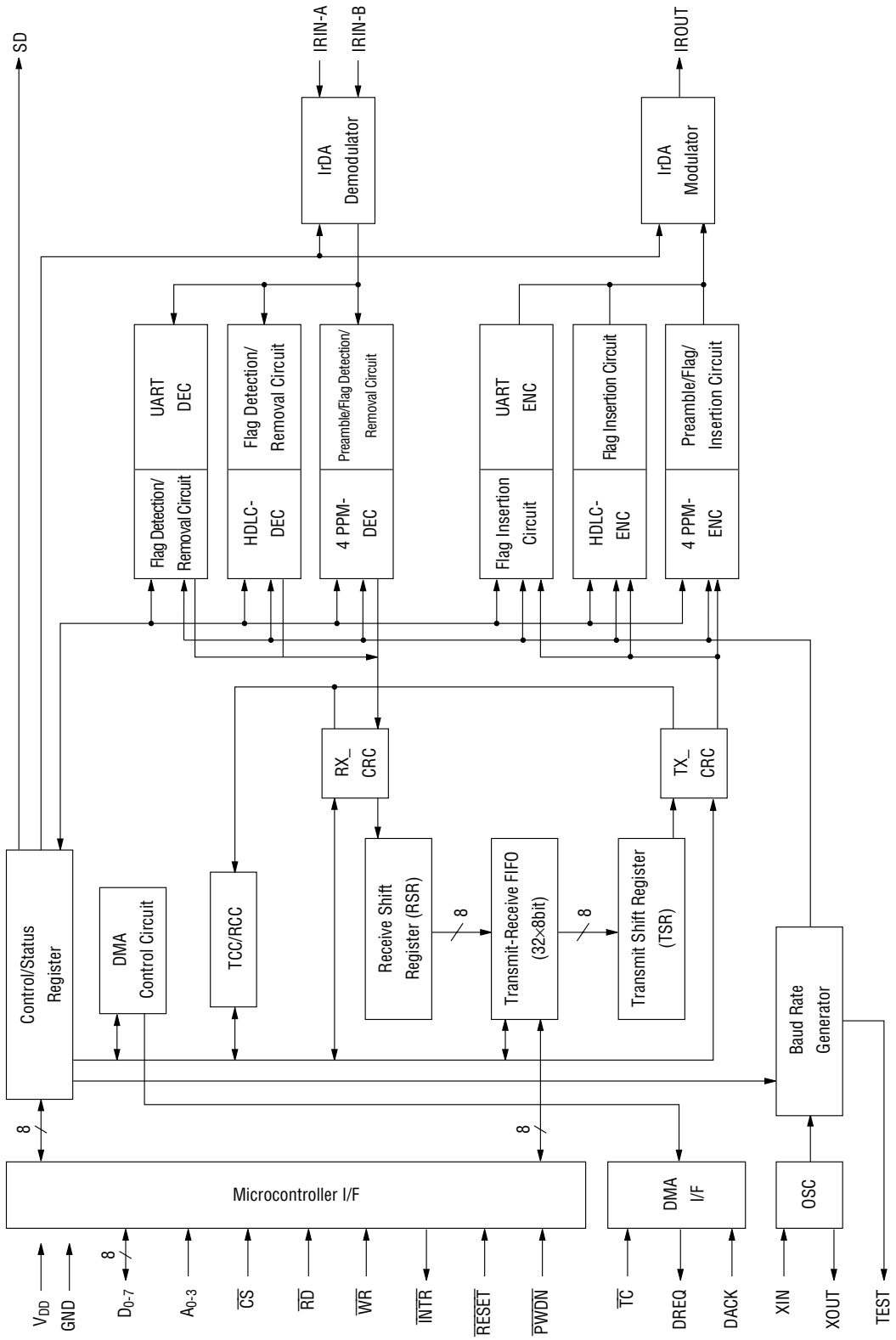
- Built-in oscillator circuit

- Crystal oscillation frequency : 18.432 MHz (other than 4 Mbps data rate)
  : 48 MHz (when 4 Mbps data rate used)

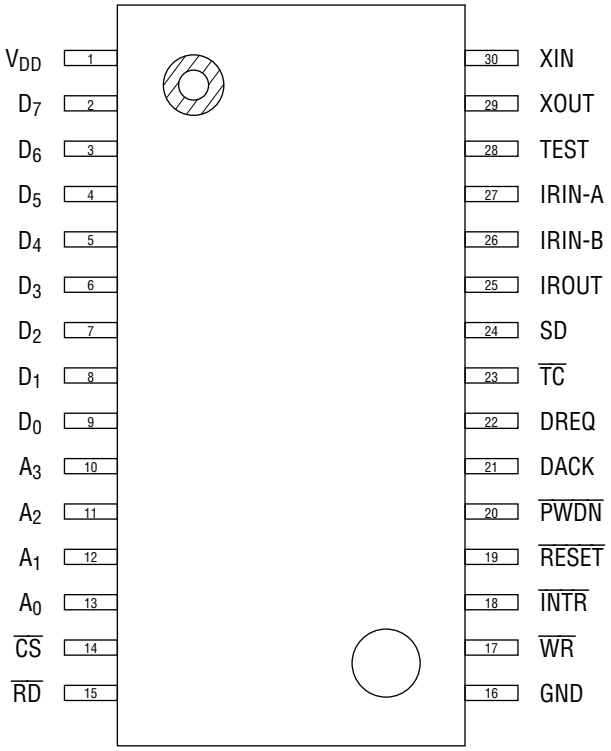
- Operating voltage (V_{DD}) : 2.7 to 3.6 V

- Package:
  30-pin plastic SSOP (SSOP30-P-56-0.65-K) (Product name : MSM9405MB)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



30-Pin Plastic SSOP

PIN DESCRIPTIONS

Function	Pin	Symbol	Type	Description
Transceiver Module Interface	27	IRIN-A	I	Receive signal input A. (2.4 kbps to 4 Mbps) *1
	26	IRIN-B	I	Receive signal input B. (0.576 to 4 Mbps) When connecting this device to a transceiver module, tie this pin high or low if the number of the receive signal output pins that the module has is only one. *1
	25	IROUT	O	Transmit signal output. Active high.
	24	SD	O	Transceiver module control signal output. Becomes active when PWDN is set low. *1 This pin must be left open if connecting this device to a transceiver module having no shutdown pins.
Microcontroller Interface	9-2	D_0-D_7	I/O	Data input-output.
	13-10	A_0-A_3	I	Register address inputs.
	14	$\overline{CS}$	I	Chip select input. Active low. When low, read and write signals are enabled.
	15	$\overline{RD}$	I	Read signal input. Active low.
	17	$\overline{WR}$	I	Write signal input. Active low.
	18	$\overline{INTR}$	O	Interrupt request signal output. Active low.
DMA Controller Interface	22	DREQ	O	DMA Request signal output. *1
	21	DACK	I	DMA acknowledge signal input. *1
	23	$\overline{TC}$	I	DMA transfer end signal input. Active low.
Others	20	$\overline{PWDN}$	I	Power down control. Active low. When set low, oscillation stops and the device enters power down (low supply current) mode.
	19	$\overline{RESET}$	I	System reset input. Active low. When set low, the internal registers are initialized.
	28	TEST	O	Test. Must be left open.
	30	XIN	I	Crystal connect.
	29	XOUT	O	Crystal connect.
	1	V_{DD}	—	Power supply.
	16	GND	—	Ground.

*1 Either active high or active low can be selected depending on the register setting.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	—	–0.5 to +4.0	V
Input Voltage	V_I	—	–0.5 to +6.0	V
Power Dissipation	P_D	—	230	mW
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Supply Voltage	V_{DD}	—	2.7 to 3.6	V
Operating Temperature	T_{op}	—	–20 to +70	°C
Crystal Oscillation Frequency	f_{OSC}	—	18.432 MHz ±200 ppm or 48 MHz ±100 ppm	—

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 2.7 to 3.6 V, Ta = –20 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable Pin
"H" Input Voltage	V_{IH}	—	2.2	—	5.5	V	IRIN-A, IRIN-B, $\overline{PWDN}$
"L" Input Voltage	V_{IL}	—	0	—	0.8*1	V	A_0-A_3, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$,
Input Leakage Current	I_{LI}	$V_I = V_{DD}/0$ V	—	—	±1	µA	$\overline{TC}$, $\overline{RESET}$, DACK
"H" Input Voltage	V_{IH}	—	2.2	—	5.5	V	D_0-D_7
"L" Input Voltage	V_{IL}	—	0	—	0.8*1	V	
Input Leakage Current	I_{LI}	$V_I = V_{DD}/0$ V	—	—	±10	µA	
"H" Output Voltage	V_{OH}	I_O = –4 mA	2.4	—	—	V	
"L" Output Voltage	V_{OL}	I_O = 4 mA	—	—	0.4	V	
"H" Output Voltage	V_{OH}	I_O = –4 mA	2.4	—	—	V	IROUT, $\overline{INTR}$, DREQ
"L" Output Voltage	V_{OL}	I_O = 4 mA	—	—	0.4	V	
Supply Current	I_{DD}	—	—	—	20	mA	V_{DD}
Supply Current (during Power Down)	I_{DPN}	When $\overline{PWDN}$ = "L"	—	—	—	µA	V_{DD}

*1 1.0 V when V_{DD} = 3.0 to 3.6 V

AC Characteristics

(V_{DD} = 2.7 to 3.6 V, Ta = –20 to +70°C)

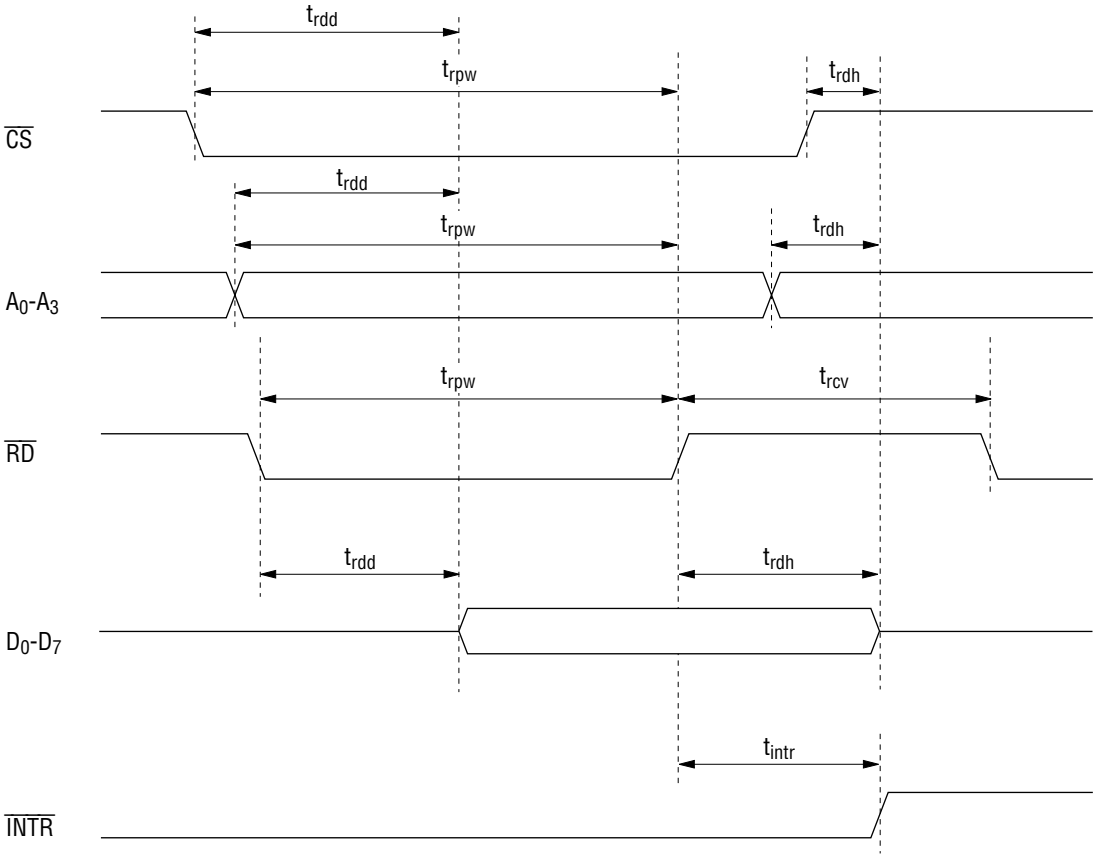
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Read Pulse Width	t_{rpw}	—	120/70	—	—	ns	*1
Read Data Delay Time	t_{rdd}	—	—	—	60	ns	*2
Read Data Hold Time	t_{rdh}	—	0	—	20	ns	*3
Read/Write Recovery Time	t_{rcv}	—	60	—	—	ns	
CS Setup Time	t_{css}	—	60	—	—	ns	
CS Hold Time	t_{csh}	—	0	—	—	ns	
Write Address Hold Time	t_{wah}	—	0	—	—	ns	
Write Pulse Width	t_{wpw}	—	120/70	—	—	ns	*1
Write Data Setup Time	t_{wds}	—	60	—	—	ns	
Write Data Hold Time	t_{wdh}	—	–10	—	—	ns	
Write Address Setup Time	t_{was}	—	–10	—	—	ns	
Interrupt Clear Time	t_{intr}	—	—	—	120/70	ns	*1
DACK Pulse Width	t_{dak}	—	60	—	—	ns	
DACK Setup Time	t_{acs}	—	10	—	—	ns	
DREQ Clear Time	t_{drqr}	—	—	—	120/70	ns	*1
DACK Hold Time (during Read)	t_{achr}	—	–5	—	—	ns	
DACK Hold Time (during Write)	t_{achw}	—	10	—	—	ns	
TC Pulse Width	t_{tcw}	—	50	—	—	ns	
TC Setup Time	t_{tcs}	—	0	—	—	ns	
TC Hold Time	t_{tch}	—	0	—	—	ns	
SIR Pulse Width	t_{spw}	Transmitter	—	1.63	—	µs	
		Receiver	0.9	—	—	µs	
SIR Data Rate Tolerance	SDRT	Transmitter	—	—	±0.87	%	
		Receiver	—	—	±2.0	%	
MIR Pulse width	t_{mpw}	Transmitter	—	218	—	ns	
		Receiver	100	—	—	ns	
MIR Data Rate Tolerance	MDRT	Transmitter	—	—	±0.1	%	
		Receiver	—	—	±0.2	%	
FIR Single Pulse Width	t_{fpw}	Transmitter	—	125	—	ns	
		Receiver	70	—	165	ns	
FIR Data Rate Tolerance	FDRT	Transmitter	—	—	±0.01	%	
		Receiver	—	—	±0.1	%	
FIR Double Pulse Width	t_{fdpw}	Transmitter	—	250	—	ns	
		Receiver	195	—	285	ns	
Reset Pulse Width	t_{rstw}	—	70	—	—	ns	

*1 120 ns when crystal oscillation frequency = 18.432 MHz,
70 ns when crystal oscillation frequency = 48 MHz

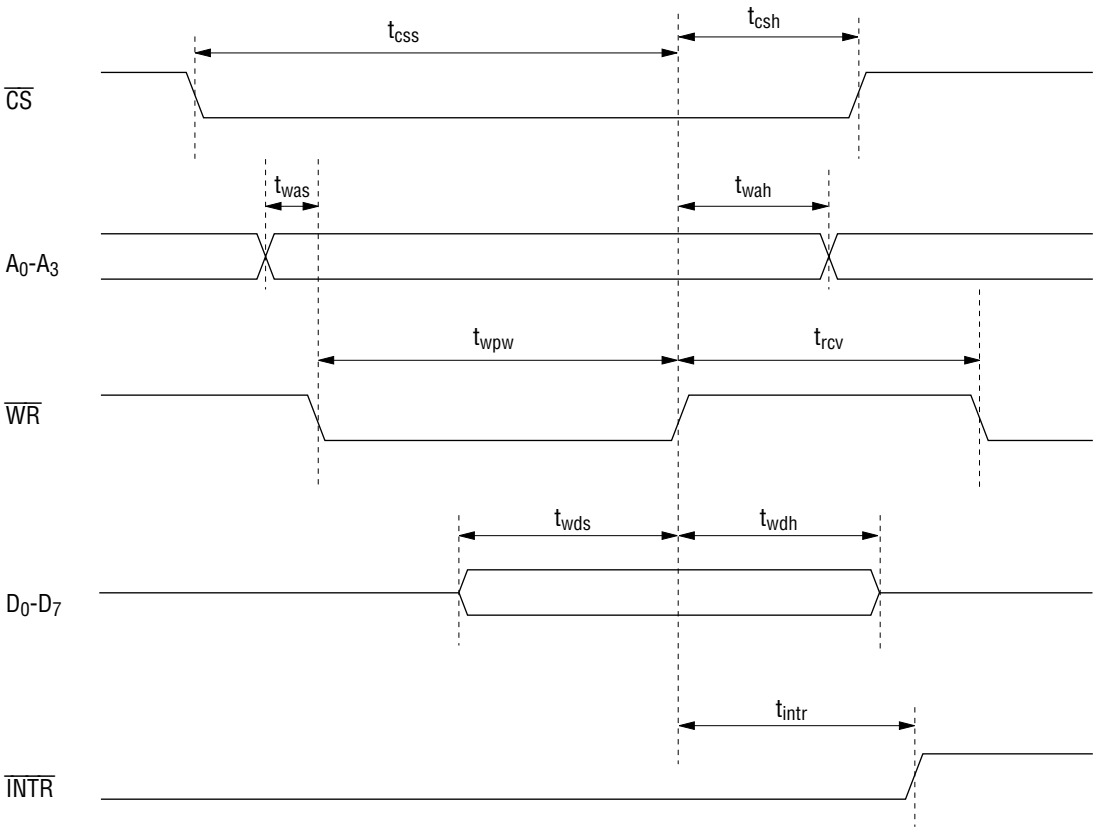
*2 That which occurs latest of the following is to be used for the data delay time (t_{rdd}) : the change of the state of A_0-A_3, the change from $\overline{CS}$ high to low, and the change from $\overline{RD}$ high to low.

*3 That which occurs first of the following is to be used for the read data hold time (t_{rdh}) : the change of the state of A_0-A_3, the change from $\overline{CS}$ low to high, and the change from $\overline{RD}$ low to high.

• Read timing

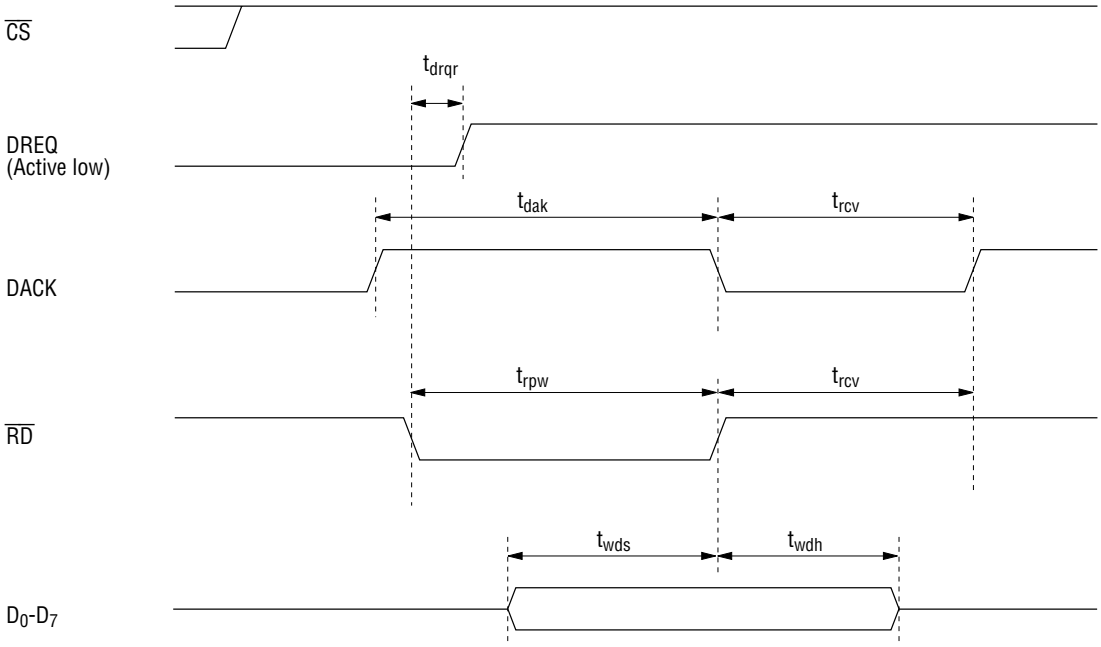


• Write timing

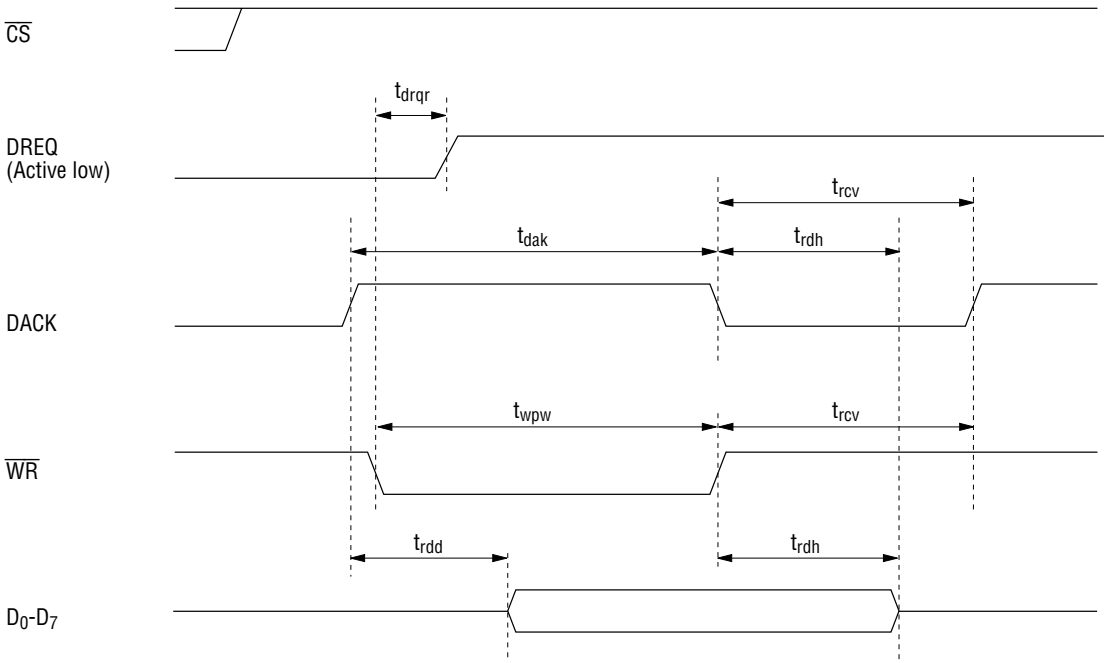


• DMAC access timing 1

DMA_EN = "1", DMA_SL$_1$ = "0", DMA_SL$_0$ = "0"
Memory→M9405



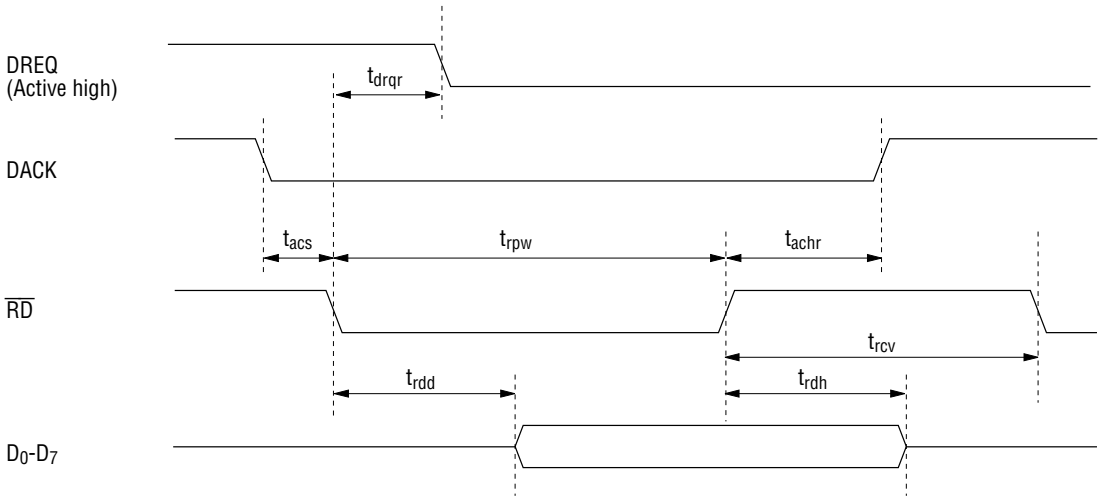
M9405→Memory



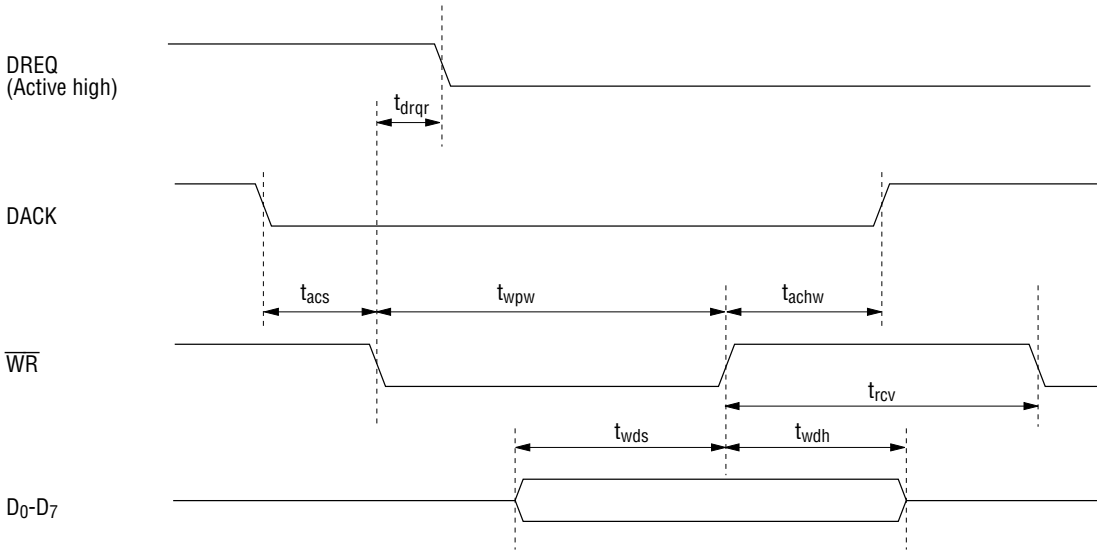
• DMAC access timing 2

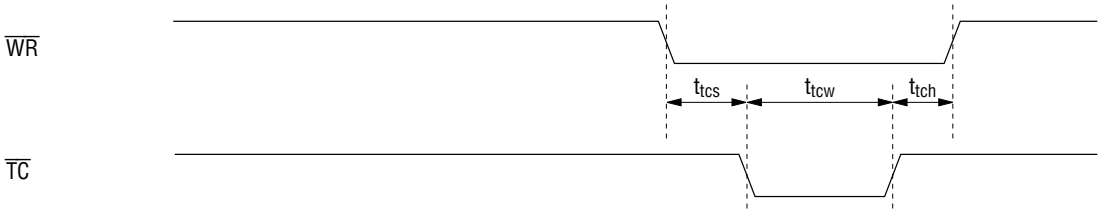
DMA_EN = "1", DMA_SL$_1$ = "0", DMA_SL$_0$ = "1"

M9405→Memory



Memory→M9405

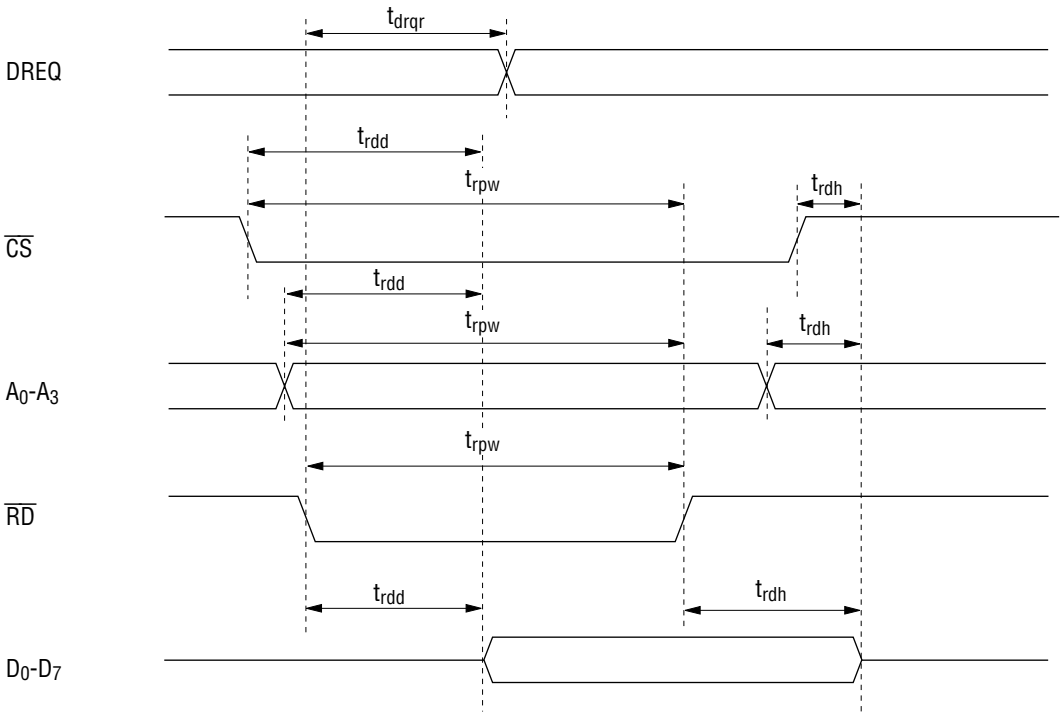




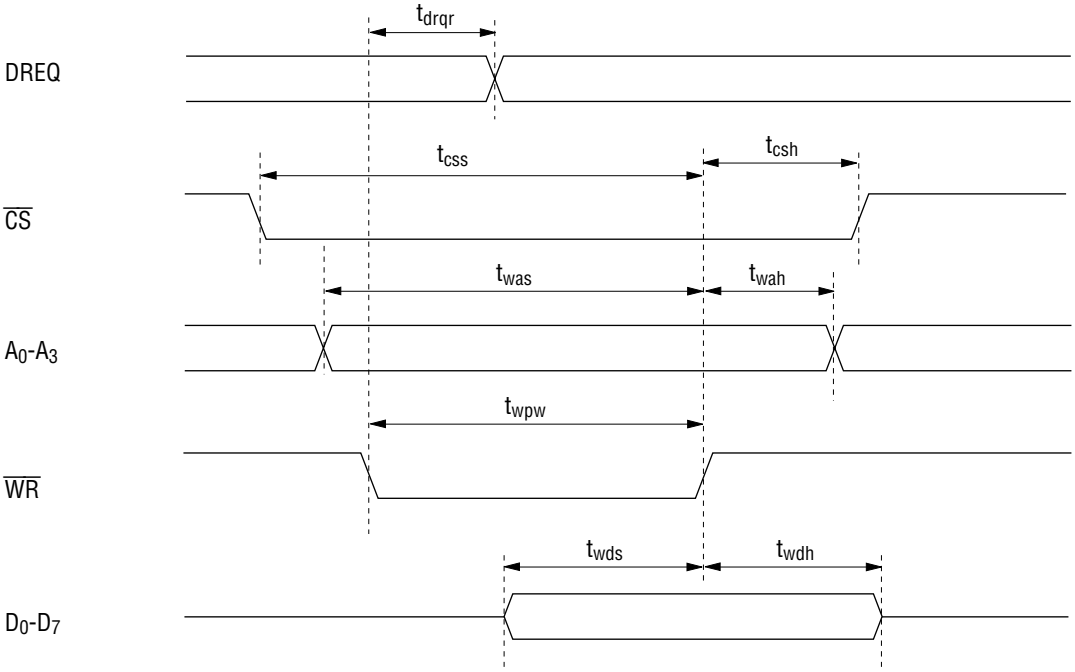
• DMAC access timing 3

DMA_EN = "1", DMA_SL$_1$ = "1", DMA_SL$_0$ = "1" or "0"

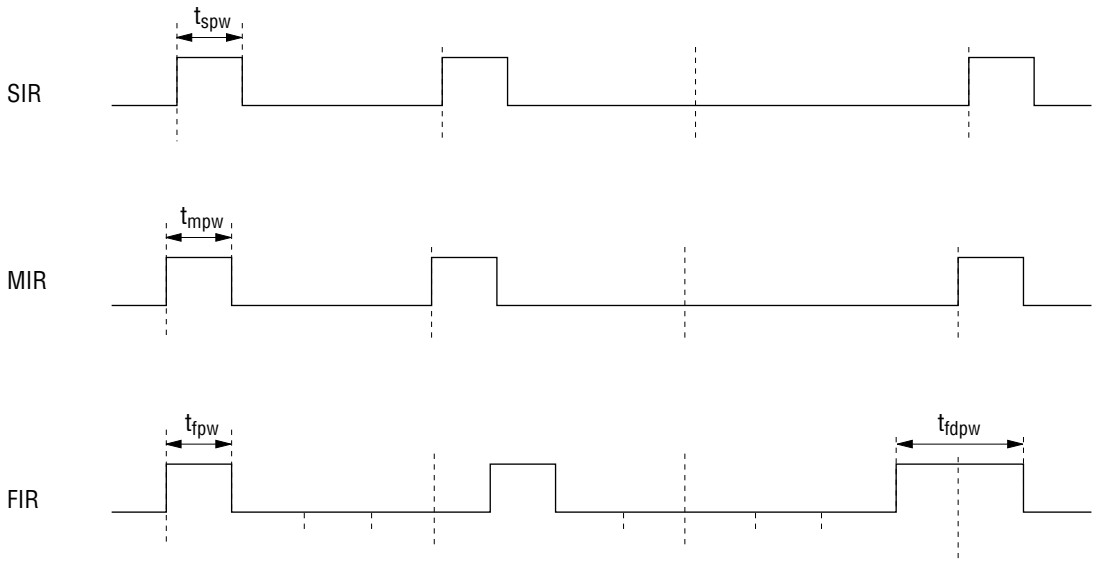
M9405→Memory



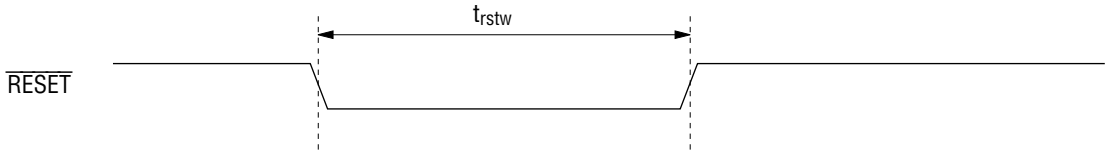
Memory→M9405



• Infrared interface timing



• Reset timing



FUNCTIONAL DESCRIPTION

Modes

There are four modes provided by the MSM9405 for IrDA communication. Communication with IrDA1.0 is in SIR mode or Extended-SIR mode, while communication with IrDA1.1 is in MIR mode or FIR mode. In SIR mode, the MSM9405 has the necessary UART feature for IrDA communication. The Extended-SIR mode is an original feature of the MSM9405. In this mode, BOF/EOF insertion and CRC calculation/check are performed by the MSM9405. Therefore, the burden to the CPU can be reduced compared with IrDA1.0 communication using ordinary UART. Moreover, the Extended-SIR mode allows DMA transfer even in IrDA1.0 communication. In MIR mode, IrDA1.1 communication at up to 1.152 Mbps is possible. The FIR mode supports 4 Mbps transfer for IrDA1.1. Features of each mode are as follows:

MSM9405 Modes Comparison

mode	Transfer rate	BOF	CRC	EOF	CE insertion/ removal	"0" insertion/ removal	Preamble insertion/removal
SIR	2.4 to 115.2 kbps	SW	SW	SW	SW	—	—
Extended-SIR	2.4 to 115.2 kbps	HW	HW	HW	HW	—	—
MIR	0.576, 1.152 Mbps	HW	HW	HW	—	HW	—
FIR	4 Mbps	HW	HW	HW	—	—	HW

CE : Control Escape Byte
SW : Software
HW : Hardware

Sending/Receiving Switching Method

Mode switching between sending and receiving is made using the TX_EN and RX_EN bits in the ICR1 (Infrared Control Register 1). For sending, writing "1" in TX_EN puts the MSM9405 in the sending mode. Writing "1" in RX_EN puts the MSM9405 in the receiving mode. If "0" is written to both TX_EN and RX_EN bits, the MSM9405 does not perform sending/receiving but enters the idle state. Each register can be set even during the idle state. Data to be sent can be written in advance to the FIFO during the idle state.
If "1" is written to both TX_EN and RX_EN, the MSM9405 is put in the receiving mode.

DMA Transfer

The MSM9405 allows DMA transfer. The DMA transfer mode covers the single transfer mode and demand transfer mode, but not the block transfer mode. When a DMA controller with TC output is used for sending, the DMA controller and MSM9405 automatically perform high-speed transfer if the maximum frame length is specified for TFL and the transfer data length for the TC counter of the DMA controller.
The timing when the DREQ signal is asserted is as follows:
During receiving, DREQ is asserted when data in the FIFO is at or above the receiving threshold level or time-out occurs.
If all of the received data in the FIFO is read, DREQ is deasserted.
During sending, DREQ is asserted when data in the FIFO is lower than the sending threshold level. Sent data is written and DREQ is deasserted when the FIFO becomes full or TXE_EV occurs.

Time-out

The MSM9405 outputs an interrupt request or DMA request depending on the register setting when the following time-out occurs even if the received data is below the receiving threshold level:

The condition causing time-out in MIR or FIR mode is:

At least 1-byte data is in the receiving FIFO and 69.5 µs has passed after data is written from the receiving shift register to the FIFO. During this period, the CPU or DMA controller does not read the FIFO data.

The condition causing time-out in SIR or Extended SIR mode is:

At least 1-byte data is in the receiving FIFO and time (Tout) has passed after data is written from the receiving shift register to the FIFO. During this period, the CPU or DMA controller does not read the FIFO data.

Tout = $4 \times 8 \times 1$/baud rate

baud rate: Transfer rate (2.4 to 115.2 kbps)

Register Map

The MSM9405 contains 14 registers, of which 13 are available. Each register can be selected with the register address assigned from 0h through Ch. Various setting options are provided for each register to allow optimum communication.

The registers are listed below. The register table is given on the next page.

A_3-A_0	R/W	Register Name		Description
0h	R	RDR		Receive data register
	W	TDR		Transmit data register
1h	R/W	ENR		Interrupt enable register
2h	R	EIR		Interrupt event and status indication register
3h	R	LSR		Status register
4h	R/W	ICR1		Transmit-receive control register
5h	R/W	ICR2		BOF count setting register
6h	R/W	MSR		Register for setting a transfer mode and a data rate and selecting a crystal to be used
7h	R/W	DSR		DMA mode setting register
8h	R/W	FCR		FIFO threshold setting register
9h	R/W	TFL (L)	*1	Transmit frame-length setting register (low-order byte)
Ah	R/W	TFL (H)	*1	Transmit frame-length setting register (high-order byte)
9h	R	TCC (L)	*1	Transmitter current-count register (low-order byte)
Ah	R	TCC (H)	*1	Transmitter current-count register (high-order byte)
Bh	R/W	MDS (L)	*2	Maximum data size setting register (low-order byte)
0h	R/W	MDS (H)	*2	Maximum data size setting register (high-order byte)
Bh	R	RST (L)	*2	Receiver frame length stack register (low-order byte)
Ch	R	RST (H)	*2	Receiver frame length stack register (high-order byte)
Fh	R/W	TEST		Used for test.

*1 Whether TFL or TCC is read depends on the setting of the CTEST bit in the MSR register.

*2 Whether MDS or RST is read depends on the setting of the CTEST bit in the MSR register.

Register Table

Add	Register name	Mode	R/W	Function of each bit							
				Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	TDR/RDR	all	R/W	TDR_7 /RDR_7	TDR_6 /RDR_6	TDR_5 /RDR_5	TDR_4 /RDR_4	TDR_3 /RDR_3	TDR_2 /RDR_2	TDR_1 /RDR_1	TDR_0 /RDR_0
1	ENR	SIR	R/W	TXE_IE	TXL_IE	RXH/T_IE	*	MLE_IE	*	OE_IE	FE_IE
		Ex-SIR					EOF_IE		CE_IE		
		MIR									AS_IE
		FIR									ECE_IE
2	EIR	SIR	R	TXE_EV	TXL_EV	RXH/T_EV	*	MLE_EV	*	OE_EV	FE_EV
		Ex-SIR					EOF_EV		CE_EV		
		MIR									AS_EV
		FIR									ECE_EV
3	LSR	SIR	R	FLV_5	FLV_4	FLV_3	FLV_2	FLV_1	FLV_0	IR_DET	TOUT
		Ex-SIR									
		MIR									
		FIR									
4	ICR1	SIR	R/W	MS_EN	TCC_EN	*	FCLR	*	*	RX_EN	TX_EN
		Ex-SIR				CRC_INV			S_EOT		
		MIR						IR_PLS			
		FIR									
5	ICR2	SIR	R/W	CTEST	SD_INV	IRIN_SL	RXINV	*	*	*	*
		Ex-SIR						SBF_3	SBF_2	SBF_1	SBF_0
		MIR						MBF_3	MBF_2	MBF_1	MBF_0
		FIR						*	*	*	*
6	MSR	all	R/W	DRS_2	DRS_1	DRS_0	XT_SL	*	*	$IRSL_1$	$IRSL_0$
7	DSR	all	R/W	*	*	*	*	*	DMA_SL_1	DMA_SL_0	DMA_EN
8	FCR	all	R/W	$RXTH_3$	$RXTH_2$	$RXTH_1$	$RXTH_0$	$TXTH_3$	$TXTH_2$	$TXTH_1$	$TXTH_0$
9	TFL (L)	all	R/W	TFL_7	TFL_6	TFL_5	TFL_4	TFL_3	TFL_2	TFL_1	TFL_0
	TCC (L)	all	R	TCC_7	TCC_6	TCC_5	TCC_4	TCC_3	TCC_2	TCC_1	TCC_0
A	TFL (H)	all	R/W	*	*	*	*	TFL_{11}	TFL_{10}	TFL_9	TFL_8
	TCC (H)	all	R	*	*	*	*	TCC_{11}	TCC_{10}	TCC_9	TCC_8
B	MDS (L)	all	R/W	MDS_7	MDS_6	MDS_5	MDS_4	MDS_3	MDS_2	MDS_1	MDS_0
	RST (L)	all	R	RST_7	RST_6	RST_5	RST_4	RST_3	RST_2	RST_1	RST_0
C	MDS (H)	all	R/W	*	*	*	*	MDS_{11}	MDS_{10}	MDS_9	MDS_8
	RST (H)	all	R	*	*	*	*	RST_{11}	RST_{10}	RST_9	RST_8
F	TEST	all	R/W	$TEST_7$	$TEST_6$	$TEST_5$	$TEST_4$	$TEST_3$	$TEST_2$	$TEST_1$	$TEST_0$

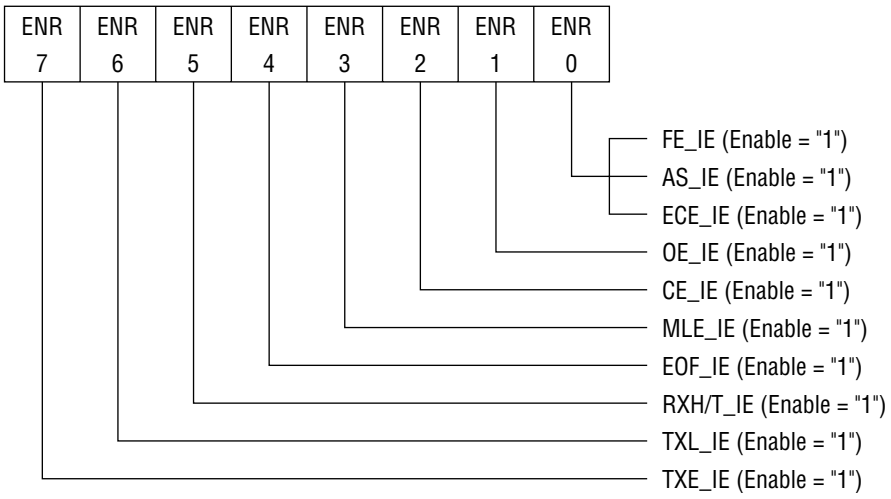
Registers

- TDR: Transmit Data Register (Write Only)
  RDR: Receive Data Register (Read Only) (Address = 0h)

The TDR (Transmit Data Register) and RDR (Receive Data Register) are used to read/write data directly upon receiving/sending the data. The TDR and RDR share the same address. When data is written in the sending mode or during the idle state, the TDR works as the top of the FIFO and 1-byte data can be written to the FIFO. When data is read in the receiving mode, the RDR works as the bottom of the FIFO and 1-byte data in the FIFO can be read. Serial-to-parallel conversion is performed by the RSR. Parallel-to-serial conversion is performed by the TSR. Reading from the TDR or writing to the RDR is invalid. The contents of the FIFO and TDR/RDR are cleard by writing "1" to FCLR in the ICR1 register. The TSR and RSR cannot be cleared.

- ENR: Enable Register (Address = 1h)

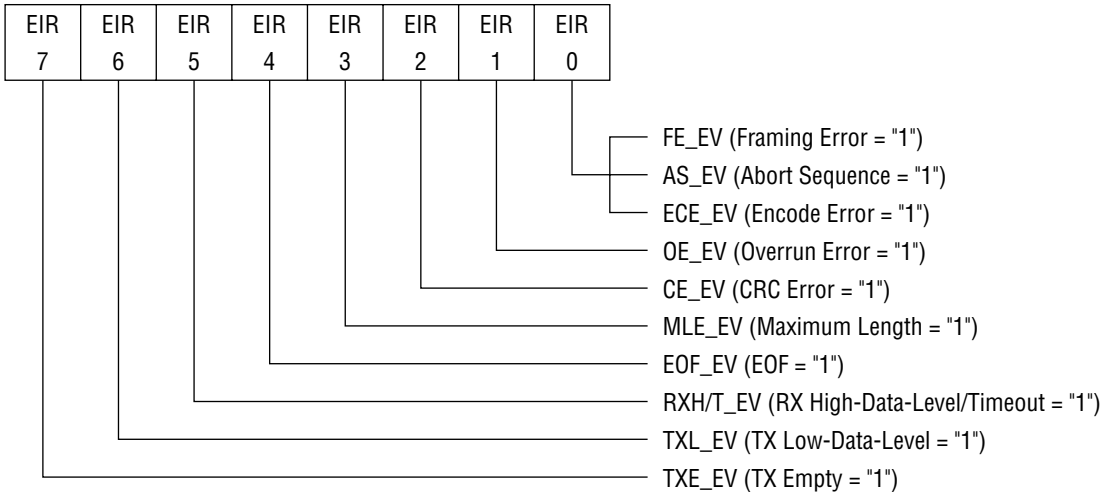
The ENR (Enable Register) is used to control enabling/disabling various interrupts on the MSM9405. Each of eight bits corresponds to each of eight interrupts provided on the MSM9405. Each of eight interrupts can be independently controlled by each bit. When the system is reset, all bits are reset to "0". By writing "1" to the bit corresponding to the desired interrupt, the specified interrupt is enabled.



ENR bit	Table bit
ENR[0]	This bit works as FE_IE in SIR or Extended-SIR mode, as AS_IE in MIR mode, and as ECE_IE in FIR mode. - FE_IE (Framing Error Interrupt Enable) (SIR mode/Extended-SIR mode): This bit enables/disables interrupt when an FE (Framing Error : Stop bit not detected) has occurred. - AS_IE (Abort Sequence Interrupt Enable) (MIR mode): This bit enables/disables interrupt when an abort sequence has been received. - ECE_IE (Encode Error Interrupt Enable) (FIR mode): This bit enables/disables interrupt when an encode error has occurred.
ENR[1]	OE_IE (Overrun Error Interrupt Enable) : This bit enables/disables interrupt when an OE (Overrun error : Error that occurs when the FIFO is full upon receiving and the next character is completely received by the RSR) has occurred.
ENR[2]	CE_IE (CRC Error Interrupt Enable) : This bit enables/disables interrupt when a CE (CRC Error) has occurred. This bit is valid in either Extended-SIR, MIR, or FIR mode. In SIR mode, this bit must be set to "0" (disable).
ENR[3]	MLE_IE (Maximum Length Error Interrupt Enable) : This bit enables/disables interrupt when an MLE (Maximum Length Error: Error that occurs when a frame exceeding the maximum data size set by the MDS is received) has occurred.
ENR[4]	EOF_IE (End Of Frame Interrupt Enable) : This bit enables/disables interrupt when the last byte in the frame's data field has been detected in either Extended-SIR, MIR, or FIR mode. In SIR mode, this bit must be set to "0" (disable).
ENR[5]	RXH/T_IE (Receiver High-Data-Level/Timeout Interrupt Enable) : This bit enables/disables interrupt when the received data is at or above the receiving threshold level or time-out has occurred.
ENR[6]	TXL_IE (Transmitter Low-Data-Level Interrupt Enable) : This bit enables/disables interrupt when the sent data is below the sending threshold level.
ENR[7]	TXE_IE (Transmitter Empty Interrupt Enable) : This bit enables/disables interrupt when both the FIFO and the TSR have become empty upon sending.

• EIR: Event Identification Register (Read Only) (Address = 2h)

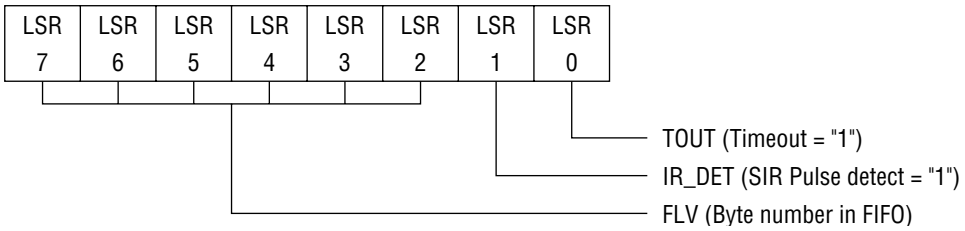
The EIR (Event Identification Register) indicates factors of various interrupts on the MSM9405. Each of eight bits corresponds to each interrupt bit assignment set on the ENR. The EIR works as the status register even if the interrupt is disabled. When an event occurs, each corresponding bit is set to "1". When the system is reset, all bits are reset to "0".



EIR bit	Description
EIR[0]	This bit works as FE_EV in SIR or Extended-SIR mode, as AS_EV in MIR mode, and as ECE_EV in FIR mode. When the CPU reads the EIR contents, this bit is set to "0". - FE_EV (Framing Error Event) (SIR mode/Extended-SIR mode): The bit is set to "1" when FE occurs. - AS_EV (Abort Sequence Event) (MIR mode): The bit is set to "1" when an abort sequence is received. - ECE_EV (Encode Error Event) (FIR mode): The bit is set to "1" when ECE occurs.
EIR[1]	OE_EV (Overrun Error Event): When OE occurs, this bit is set to "1". When the CPU reads the EIR contents, OE_EV is set to "0". The RSR characters are not transferred to the FIFO but overwritten.
EIR[2]	CE_EV (CRC Error Event): When a CRC error occurs, this bit is set to "1". When the CPU reads the EIR, this bit is set to "0". This bit is valid in either Extended-SIR, MIR, or FIR mode. This bit is not used in SIR mode.
EIR[3]	MLE_EV (Maximum Length Error Event): When MLE occurs, this bit is set to "1". When the CPU reads the EIR, this bit is set to "0".
EIR[4]	EOF_EV (End Of Frame Event): This bit is valid in either Extended-SIR, MIR, or FIR mode. When the last byte in the frame's data field reaches the bottom of the FIFO in receiving mode, EOF_EV is set to "1". When the CPU reads the EIR, this bit is set to "0". In SIR mode, this bit is not used.
EIR[5]	RXH/T_EV (Receiver High-Data-Level/Timeout Event): When received data in the FIFO is at or above the receiving threshold level or time-out occurs, RXH/T_EV is set to "1". The condition for setting RXH/T_EV to "0" depends on the following two cases : If received data in the FIFO is at or above the receiving threshold level : Received data is read. When received data in the FIFO is below the threshold level, this bit is set to "0". If time-out occurs : After received data in the FIFO is read, this bit is set to "0".
EIR[6]	TXL_EV (Transmitter Low-Data-Level Event): When sent data in the FIFO is below the sending threshold level, this bit is set to "1". When sent data is written and sent data in the FIFO is at or above the threshold level, this bit is set to "0".
EIR[7]	TXE_EV (Transmitter Empty Event): When both FIFO and TSR are empty in sending mode, this bit is set to "1". When the CPU reads the EIR, this bit is set to "0".

• LSR: Line Status Register (Read Only) (Address = 3h)

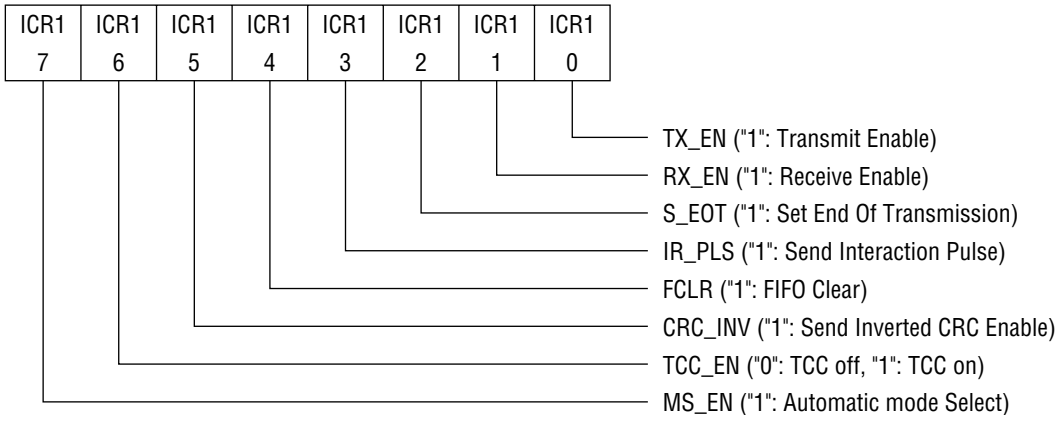
The LSR (Line Status Register) indicates various statuses of the MSM9405 that is running. When the system is reset, all bits of the LSR are set to "0". This register is for read only and cannot be written.



LSR bit	Description
LSR[0]	TOUT (FIFO Timeout): When time-out occurs in the FIFO during receiving, this bit is set to "1". When received data is read from the FIFO, TOUT is set to "0".
LSR[1]	IR_DET (SIR Pulse detect) : This bit is set to "1" when a pulse having a width of t_{spw} (SIR pulse width upon receiving). It is set to "0" when the CPU reads the LSR.
LSR[2-7]	FLV (FIFO Level): These bits indicate the number of data items in the FIFO with a value of 0 to 32.

• ICR1: Infrared Control Register 1 (Address = 4h)

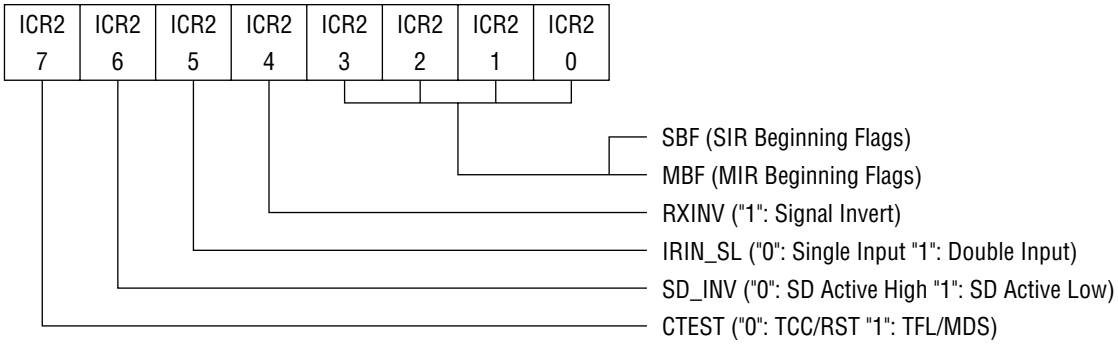
The ICR1 (Infrared Control Register 1) is used to set various environment so that the MSM9405 can perform IrDA communication under proper conditions. When the system is reset, all bits of ICR1 are set to "0".



ICR1 bit	Description
ICR1[0]	TX_EN (Transmit Enable): When "1" is written to this bit, the sending mode is selected. When "0" is written to this bit, sending terminates when data remaining in the FIFO has all been sent. In this case, the TXE interrupt does not occur.
ICR1[1]	RX_EN (Receive Enable): When "1" is written to this bit, the receiving mode is selected. When "0" is written to this bit, the device enters receive end mode.
ICR1[2]	S_EOT (Set End Of Transmission): This bit is valid in Extended-SIR, MIR, or FIR mode. When "1" is written to this bit, the data written to the FIFO next time is recognized as the end of frame, and immediately after it, the data added with CRC and EOF is sent as a frame. After a frame is sent, this bit is automatically set to "0". To use S_EOT, TFL must be set to the maximum value or TCC must be unused with TCC_EN = "0". This bit is not used in SIR mode.
ICR1[3]	IR_PLS (Send Interaction Pulse): This bit is valid in MIR or FIR mode. When "1" is written to this bit, an approximately 2-μs serial infrared interaction pulse is sent immediately after the frame being sent. After a frame is sent, this bit is automatically set to "0". This bit is not used in SIR mode and Extended-SIR mode.
ICR1[4]	FCLR (FIFO Clear): When "1" is written to this bit, the FIFO (including the TDR and RDR) is made empty. The FIFO threshold level does not change. The TSR and RSR are not cleared. When the FIFO is made empty, this bit is automatically set to "0".
ICR1[5]	CRC_INV (Invert Transmitter CRC): This bit is valid in Extended-SIR, MIR, or FIR mode and is not used in SIR mode. When "1" is written to this bit, transmission is interrupted if TXE (Transmitter Empty) occurs. The inverted CRC and EOF are automatically added to the frame that caused TXE, then the frame is sent. Writing "0" to this bit disables this function.
ICR1[6]	TCC_EN (TCC Enable): This bit is valid in Extended-SIR, MIR, or FIR mode. When this bit is set to "1", the TCC is enabled. When TCC_EN is set to "0", the TCC is disabled. To use S_EOT, the TFL must be set to the maximum value or the TCC must be disabled with TCC_EN = "0".
ICR1[7]	MS_EN (Mode Select Enable): When "1" is written to this bit, the MSM9405 performs the following operation depending on the mode. After the operation is completed, this bit is automatically set to "0". If the MSM9405 is in FIR mode: 1. The SD pin is set to "H", and the Tx pin to "H". 2. Approximately 300 ns later, the SD pin is set to "L". 3. Approximately 300 ns later, the Tx pin is set to "L". If the MSM9405 is in SIR, Extended-SIR, or MIR mode: 1. The SD pin is set to "H", and the Tx pin to "L". 2. Approximately 300 ns later, the SD pin is set to "L". 3. The Tx pin is held in the "L" level for approximately 300 ns.

• ICR2: Infrared Control Register 2 (Address = 5h)

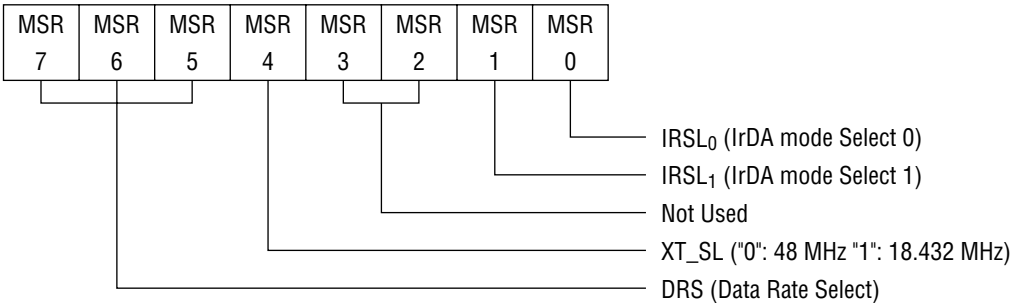
The ICR2 (Infrared Control Register 2) is used to set various environment so that the MSM9405 can perform IrDA communication under proper conditions. When the system is reset, all bits of ICR2 are set to "0".



<table>
<tr><th>IRC2 bit</th><th>Description</th></tr>
<tr><td>ICR2[0-3]</td><td>These bits work as the SBF when Extended-SIR mode is selected, and as the MBF when the MIR mode is selected. This function is disabled in SIR mode and FIR mode.
SBF (SIR beginning Flags): These bits determine the number of BOFs to be added during sending in Extended-SIR mode as shown below.
MBF (MIR Beginning Flags): These bits determine the number of BOFs to be added during sending in MIR mode as shown below.
<table>
<tr><th>Encoding</th><th>SIR BOFs</th><th>MIR BOFs</th></tr>
<tr><td>0000</td><td>1</td><td>2</td></tr>
<tr><td>0001</td><td>2</td><td>3</td></tr>
<tr><td>0010</td><td>3</td><td>4</td></tr>
<tr><td>0011</td><td>4</td><td>5</td></tr>
<tr><td>0100</td><td>5</td><td>8</td></tr>
<tr><td>0101</td><td>7</td><td>12</td></tr>
<tr><td>0110</td><td>9</td><td>16</td></tr>
<tr><td>0111</td><td>13</td><td>24</td></tr>
<tr><td>1000</td><td>17</td><td>24</td></tr>
<tr><td>1001</td><td>25</td><td>24</td></tr>
<tr><td>1010</td><td>49</td><td>24</td></tr>
<tr><td>1011</td><td>49</td><td>24</td></tr>
<tr><td>1100</td><td>49</td><td>24</td></tr>
<tr><td>1101</td><td>49</td><td>24</td></tr>
<tr><td>1110</td><td>49</td><td>24</td></tr>
<tr><td>1111</td><td>49</td><td>24</td></tr>
</table></td></tr>
<tr><td>ICR2[4]</td><td>RXINV (IRIN Signal Invert): This bit is used to select active low or active high of the receive signal.
RXINV = "0": Active low
RXINV = "1": Active high</td></tr>
<tr><td>ICR2[5]</td><td>IRIN_SL (IRIN Select): This bit determines how the receive signal input pin is used.
IRIN_SL = "0": Only the input from the IRIN-A pin (2.4 kbps to 4 Mbps) is accepted.
IRIN_SL = "1": An input from IRIN-A or IRIN-B is automatically selected depending on the transfer rate. (A: 2.4 to 115.2 kbps, B: 0.576 to 4 Mbps)</td></tr>
<tr><td>ICR2[6]</td><td>SD_INV (SD Signal Invert): This bit changes the polarity (active high/low) of the SD pin output on the MSM9405.
SD_INV = "0": Active high ("H" output during shutdown)
SD_INV = "1": Active low ("L" output during shutdown)</td></tr>
<tr><td>ICR2[7]</td><td>CTEST (Counter Test): Normally this bit is set to "0". When TFL/TCC and MDS/RCC are read after "1" is written to this bit, the TFL and MDS values can be obtained.</td></tr>
</table>

• MSR: Mode Select Register (Address = 6h)

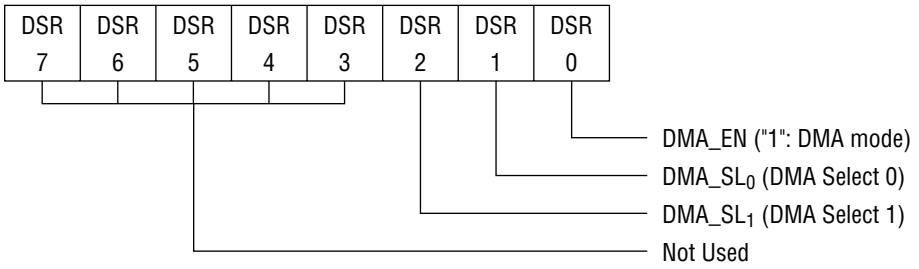
The MSR is used to select various modes of the MSM9405. When the system is reset, each bit is set to the initial value.



<table>
<tr><th>MSR Bit</th><th>Description</th></tr>
<tr><td>MSR[0-1]</td><td>IRSL (Infrared Mode Select): These bits are used to select the transfer mode as shown below. The initial value is set to "00".
<table>
<tr><th>IRSL1</th><th>IRSL0</th><th>mode</th></tr>
<tr><td>0</td><td>0</td><td>SIR</td></tr>
<tr><td>0</td><td>1</td><td>Extended-SIR</td></tr>
<tr><td>1</td><td>0</td><td>MIR</td></tr>
<tr><td>1</td><td>1</td><td>FIR</td></tr>
</table></td></tr>
<tr><td>MSR[2-3]</td><td>These bits are not used.</td></tr>
<tr><td>MSR[4]</td><td>XT_SL (Crystal Select): This bit determines the crystal to be used.
The initial value is set to "0".
XT_SL = "0": 48 MHz crystal is used
XT_SL = "1": 18.432 MHz crystal is used</td></tr>
<tr><td>MSR[5-7]</td><td>DRS (Data Rate Select): These bits determine the transfer rate as shown below. The initial value is set to "001".
<table>
<tr><th>Encoding</th><th>SIR Data Rate</th><th>MIR Data Rate</th><th>FIR Data Rate</th></tr>
<tr><td>000</td><td>2400 bps</td><td>0.576 Mbps</td><td>reserved</td></tr>
<tr><td>001</td><td>9600 bps</td><td>1.152 Mbps</td><td>4 Mbps</td></tr>
<tr><td>010</td><td>19.2 kbps</td><td>reserved</td><td>reserved</td></tr>
<tr><td>011</td><td>38.4 kbps</td><td>reserved</td><td>reserved</td></tr>
<tr><td>100</td><td>57.6 kbps</td><td>reserved</td><td>reserved</td></tr>
<tr><td>101</td><td>115.2 kbps</td><td>reserved</td><td>reserved</td></tr>
<tr><td>110</td><td>reserved</td><td>reserved</td><td>reserved</td></tr>
<tr><td>111</td><td>reserved</td><td>reserved</td><td>reserved</td></tr>
</table></td></tr>
</table>

• DSR: DMA Mode Select Register (Address = 7h)

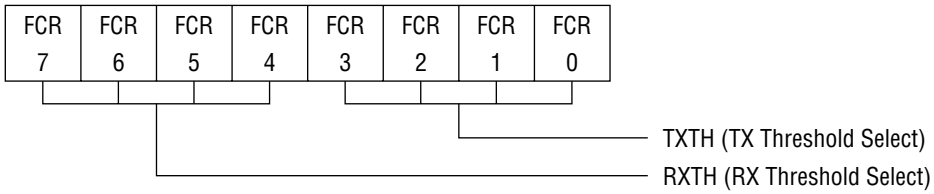
The DSR (DMA Mode Select Register) is used to select the DMA mode for the MSM9405. When the system is reset, all bits of DSR are set to "0".



<table>
<tr><th>DSR Bit</th><th>Description</th></tr>
<tr><td>DSR[0]</td><td>DMA_EN (DMA Mode Enable): This bit determines whether the DMA is to be used. The initial value is set to "0".
When "1" is written to this bit, DSR[1-2] (DMA_SL$_0$, DMA_SL$_1$) setting is enabled and the MSM9405 enters the DMA transfer standby mode. (DREQ is asserted when the DREQ assert condition is met.)
If DMA_EN = "0", DSR[1-2] (DMA_SL$_0$, DMA_SL$_1$) setting is disabled and DMA transfer is not performed. (DREQ is not asserted even if the DREQ assert condition is met.)</td></tr>
<tr><td>DSR[1-2]</td><td>DMA_SL (DMA Select): These bits are used to select the method of interfacing with DMAC.
<table>
<tr><th>DMA_SL$_1$</th><th>DMA_SL$_0$</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>DREQ becomes active low and DACK becomes active high. When the $\overline{RD}$ signal becomes active while DACK is active, the DMA read cycle (Memory→M9405) is selected. When the $\overline{WR}$ signal becomes active while DACK is active, the DMA write cycle (M9405→Memory) is selected. While DACK is being asserted, address "0" (TDR/RDR) is accessed regardless of the status of A$_0$ to A$_3$.</td></tr>
<tr><td>0</td><td>1</td><td>DREQ becomes active high and DACK becomes active low. When the $\overline{WR}$ signal becomes active while DACK is active, the DMA read cycle (Memory→M9405) is selected. When the $\overline{RD}$ signal becomes active while DACK is active, the DMA write cycle (M9405→Memory) is selected. While DACK is being asserted, address "0" (TDR/RDR) is accessed regardless of the status of A$_0$ to A$_3$.</td></tr>
<tr><td>1</td><td>0</td><td>DREQ becomes active low and DACK becomes active high. DACK is disabled.</td></tr>
<tr><td>1</td><td>1</td><td>DREQ becomes active high and DACK becomes active low. DACK is disabled.</td></tr>
</table></td></tr>
<tr><td>DSR[3-7]</td><td>These bits are not used.</td></tr>
</table>

FCR : FIFO Control Register (Address = 8h)

The FCR (FIFO Control Register) is used to set the threshold level of the FIFO to be used by the MSM9405 upon sending/receiving. The FCR setting is applied to both interrupt and DMA. When the system is reset, the FCR is set to the initial value.



FCR bit	Description
FCR[0-3]	TXTH (Transmit Threshold Select): These four bits set the following 16 sending threshold levels. The initial value is set to "0111".

FCR (0-3)	TX Threshold Level (Byte)
0000	01
0001	02
0010	04
0011	06
0100	08
0101	10
0110	12
0111	14
1000	16
1001	18
1010	20
1011	22
1100	24
1101	26
1110	28
1111	30

FCR[4-7]	RXTH (Receive Threshold Select): These four bits set the following 16 receiving threshold levels. The relationship between the FCR (4-7) value and receiveing threshold level is the same as the relationship between the FCR (0-3) and sending threshold level. The initial value is set to "0111".

TFL : (Transmitter Frame Length Register
TCC : Transmitter Current-Count Register (Address = 9, Ah)

The TFL (Transmitter Frame Length) and TCC (Transmitter Current-Count Register) are used to specify the length of the frame to be transferred for sending. The TFL and TCC shares the same address. Bits 0 to 7 of address 9h and bits 0 to 3 of address Ah (totally 12 bits) are used. Bit 0 of address 9h is the LSB.
When the TFL/TCC value is read, the CTEST setting is reflected. If CTEST = "0", the TCC contents can be read. If CTEST = "1", the TFL contents can be read. When the TFL/TCC is written, the TFL value is rewritten. The TCC cannot be written.
To use the TFL/TCC, write "1" to TCC_EN, and set the frame length in the TFL. The frame length to be set does not include the CE, FCS, BOF, and EOF. When "1" is written to TX_EN, the TFL value that has been set as the frame length is loaded to the TCC. When sending is started, the TCC value is decremented by 1 each time 1 byte is sent. When the TCC value becomes "0", the end of frame is assumed and the frame is automatically added with the CRC and EOF and sent. After one frame is sent, the TFL value is loaded again into the TCC when the BOF of the second frame is sent.
The TFL/TCC initial value is set to 800h.

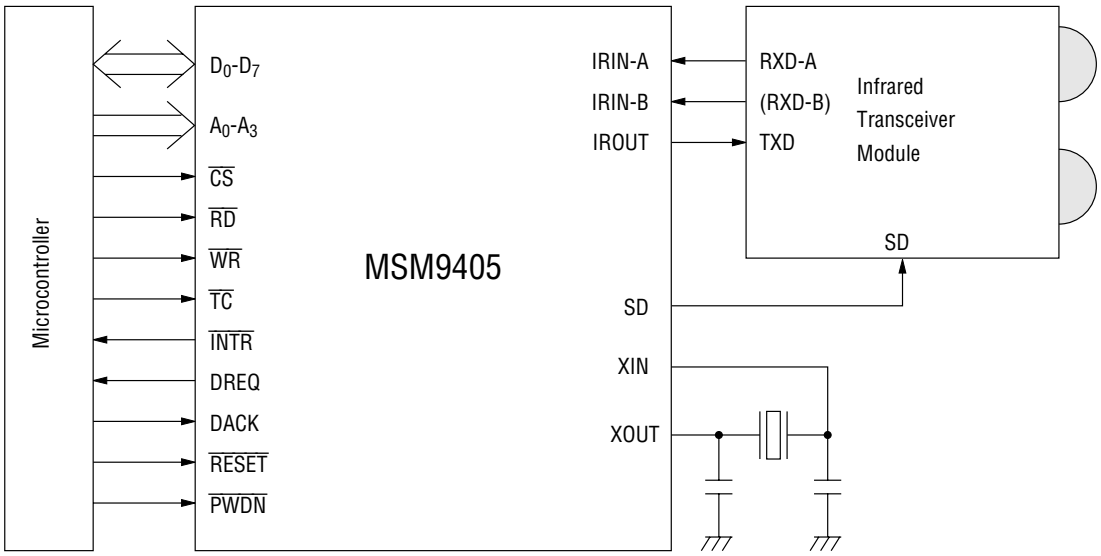
MDS : Maximum Data Size Register
RST : Receiver Frame Length Stack Register (Address = B, Ch)

The MDS (Maximum Data Size Register) is used to set the maximum data size. The RST (Receiver Frame Length Stack Register) is used to stack the received frame length. The MDS and RST share the same address. Bits 0 to 7 of address Bh and bits 0 to 3 of address Ch (totally 12 bits) are used. Bit 0 of address Bh is the LSB.
When the MDS/RST value is read, the CTEST setting is reflected. If CTEST = "0", the RST contents can be read. If CTEST = "1", the MDS contents can be read. When the MDS/RST is written, the MDS value is rewritten. The RST cannot be written.
To use the MDS, set the maximum data size in the MDS in advance. The frame length to be set does not include the CE, FCS, BOF, and EOF in the Extended-SIR, MIR, and FIR modes. (However, it does include them in the SIR mode.) When receiving is started, the internal counter value is incremented by 1 each time one byte is received. If the internal counter value exceeds the MDS value during receiving, MLE occurs. The MDS initial value is set to 800h.
When a frame is fully received and all the data in the received frame is taken out of the FIFO, the received frame length counted by the internal counter is stacked in the RST. This value is stored untill the next frame is fully received. The value stacked in the RST is maintained even if MSM9405 sending/receiving is switched. The RST initial value is set to 0h.

TEST : Test Register (Address = Fh)

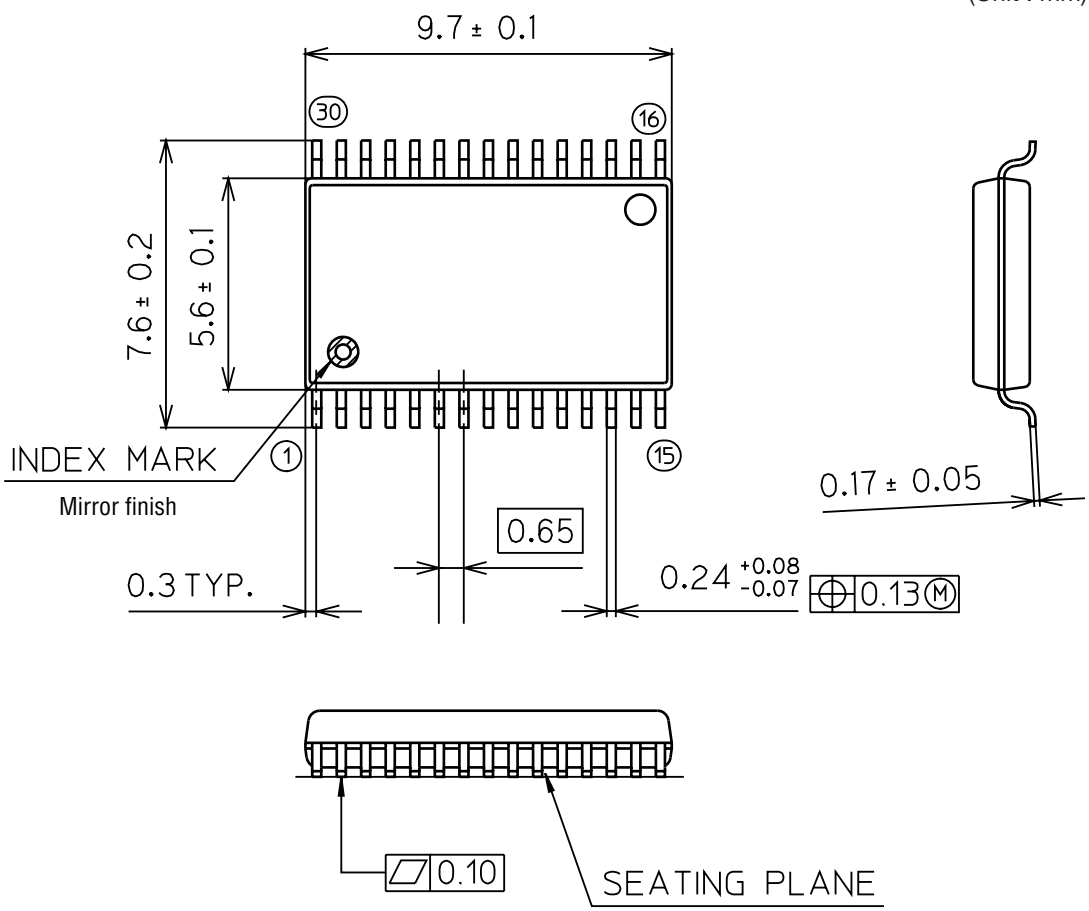
This register is used for testing.

APPLICATION CIRCUIT



PACKAGE OUTLINES AND DIMENSIONS

(Unit : mm)



30-Pin Plastic SSOP