DATA SHEET

O K I A S I C P R O D U C T S

MSM12R/13R/98R
0.5 μm Mixed 3-V/5-V Sea of Gates and Customer Structured Arrays

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Oki Semiconductor

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Oki Semiconductor

MSM12R/13R/98R

0.5μm Mixed 3-V/5-V Sea of Gates and Customer Structured Arrays

DESCRIPTION

OKI's 0.5μm ASIC products, specially designed for mixed 3-V/5-V applications, are now available in both Sea Of Gates (SOG) and Customer Structured Array (CSA) architectures. Both the SOG-based MSM13R Series and the CSA-based MSM98R Series use a three-layer-metal process on 0.5μm drawn (0.4μm L-effective) CMOS technology. The MSM12R SOG series uses two-layer metal process. The semiconductor process is adapted from OKI's production-proven 16-Mbit DRAM manufacturing process.

The MSM12R/13R and MSM98R series feature high speed, low power, and high density logic with either a 5-V or 3-V interface. The MSM12R/13R and MSM98R Series employ a 3-V core and flexible I/O architecture to support both 3-V and 5-V voltage levels.

The MSM12R SOG series is available in 5 sizes with up to 240 I/O pads and over 40k usable gates. The MSM13R SOG Series is available in 10 sizes with up to 624 I/O pads and over 464k gates. The SOG array sizes are designed to fit the most popular quad flat pack (QFP) packages, such as 100-, 144-, 176-, 208-, 240-, and 304-pin QFPs. MSM12R/13R SOG-based designs are therefore ideal for pad-limited circuits that require rapid prototyping turnaround times.

The MSM98R CSA Series is an all-mask-level superset of the SOG series, available in 36 sizes. The CSA offerings combine the SOG architecture's logic flexibility with the higher integration yielded by optimized diffusion for faster and more compact memory blocks. The MSM98R is ideal for core-limited applications or circuits with large and/or multiple memory functions. Customer modification to the structure of any of the 36 predefined masterslices, rather than creation of a new masterslice every time, improves the prototyping turnaround time over cell-based manufacturing techniques.

Each product family is supported by OKI's proprietary MEMGEN tool which quickly and easily generates SOG memories (for the MSM12R/13R) as well as optimized memories for the MSM98R Series. The families also feature floorplanning to control pre-layout timing, clock-skew management software that guarantees worst-case clock skew of 0.5 ns or less, and scan-path design techniques that support ATPG for fault coverage approaching 100%.

FEATURES

- 0.5μm drawn two- and three-layer metal CMOS
- Optimized 3.3-V core with 3-V or 5-V interface
- SOG and CSA architecture availability
- 110-ps typical gate propagation delay (for a 2-input 4x-drive NAND gate, operating at 3.3 V, with a fan-out of 2 and 0 mm of wire)
- Up to 464K usable gates and 624 pads
- User-configurable I/O with V_{SS}, V_{DD}, CMOS, TTL, 3-state, and 2 mA ~ 24 mA options
- Slew-rate-controlled outputs for low-radiated noise
- Clock tree cells with ≤ 0.5-ns clock skew, worst-case (fan-out ≥ 9000 at 75 MHz)
- User-configurable single and dual-port memories
- Specialized 3-V and 5-V macrocells, including phase-locked loop, PCI, and USB cells
- Floorplanning for front-end simulation, back-end layout controls, and links to synthesis
- JTAG boundary scan and scan-path ATPG
- Support for popular CAE systems including Cadence, Exemplar, Model Technology, Inc. (MTI), Zycad, and Synopsys

MSM12R/13R/98R FAMILY LISTING

CSA Part#	CSA Master#	SOG Part#	I/O Pads	Rows [1]	Columns	Raw Gates	Usable Gates [2]
MSM98R020X020	B98RB01	—	80	58	164	9,512	7,610
MSM98R024X024	B98RB02	—	96	72	204	14,688	11,750
—	—	MSM12R0170	104	78	224	17,472	8,387
MSM98R026X026	B98RB03	MSM13R0170	104	78	224	17,472	13,978
MSM98R030X030	B98RB04	—	120	92	264	24,288	19,430
MSM98R032X032	B98RB05	—	128	99	280	27,720	22,176
—	—	MSM12R0350	144	112	320	35,840	17,203
MSM98R036X036	B98RB06	MSM13R0350	144	112	320	35,840	26,880
MSM98R038X038	B98RB07	—	152	119	340	40,460	30,345
MSM98R040X040	B98RB08	—	160	126	360	45,360	34,020
MSM98R042X042	B98RB09	—	168	133	380	50,540	37,905
—	—	MSM12R0560	176	140	400	56,000	25,200
MSM98R044X044	B98RB10	MSM13R0560	176	140	400	56,000	39,200
MSM98R048X048	B98RB11	—	192	153	436	66,708	46,696
MSM98R050X050	B98RB12	—	200	160	456	72,960	51,072
—	—	MSM12R0790	208	167	476	79,492	31,797
MSM98R052X052	B98RB13	MSM13R0790	208	167	476	79,492	55,644
MSM98R056X056	B98RB14	—	224	180	516	92,880	65,016
—	—	MSM12R1070	240	194	552	107,088	40,693
MSM98R060X060	B98RB15	MSM13R1070	240	194	552	107,088	74,962
MSM98R064X064	B98RB16	—	256	208	592	123,136	81,270
MSM98R068X068	B98RB17	—	272	221	632	139,672	92,184
MSM98R072X072	B98RB18	—	288	235	672	157,920	104,227
MSM98R076X076	B98RB19	MSM13R1750	304	248	708	175,584	115,885
MSM98R080X080	B98RB20	—	320	262	748	195,976	125,425
MSM98R084X084	B98RB21	—	336	276	788	217,488	139,192
MSM98R088X088	B98RB22	—	352	289	824	238,136	152,407
MSM98R092X092	B98RB23	—	368	303	864	261,792	167,547
MSM98R096X096	B98RB24	MSM13R2850	384	316	904	285,664	177,112
MSM98R100X100	B98RB25	—	400	330	944	311,520	193,142
MSM98R104X104	B98RB26	—	416	344	980	337,120	209,014
MSM98R108X108	B98RB27	—	432	357	1,020	364,140	225,767
MSM98R112X112	B98RB28	MSM13R3930	448	371	1,060	393,260	235,956
MSM98R118X118	B98RB29	—	472	391	1,116	436,356	261,814
MSM98R122X122	B98RB30	—	488	405	1,156	468,180	280,908
MSM98R126X126	B98RB31	MSM13R4990	504	418	1,196	499,928	299,957
MSM98R132X132	B98RB32	—	528	439	1,252	549,628	329,777
MSM98R138X138	B98RB33	—	552	459	1,312	602,208	361,325
MSM98R144X144	B98RB34	—	576	480	1,368	656,640	393,984
MSM98R150X150	B98RB35	—	600	500	1,428	714,000	428,400
MSM98R156X156	B98RB36	—	624	520	1,488	773,760	464,256

1. Row and column numbers are used to evaluate the number and size of mega macrocells that may be included into each array. For example, a 7,600-gate mega macrocell with a size and aspect ratio of 36 rows by 245 columns can be used on the MSM98R030x030 or any larger array base, but not on the MSM98R026x026.
2. Usable gate count is design dependent and varies based upon the number of fan-outs per net, internal busses, floor plan, RAM/ROM blocks, etc.

ARRAY ARCHITECTURE

The primary components of a 0.5µm MSM12R/13R/98R circuit include:

- I/O base cells
- Configurable I/O pads for V_{DD}, V_{SS}, or I/O (I/O in both 3V and 5V)
- V_{DD} and V_{SS} pads dedicated to wafer probing
- Separate power bus for output buffers
- Separate power bus for internal core logic and input buffers
- Core base cells containing N-channel and P-channel pairs, arranged in column of gates
- Isolated gate structure for reduced input capacitance and increased routing flexibility

Each array has 24 dedicated corner pads for power and ground use during wafer probing, with four pads per corner. The arrays also have separate power rings for the internal core functions (V_{DDC} and V_{SSC}) and output drive transistors (V_{DDO} and V_{SSO}).

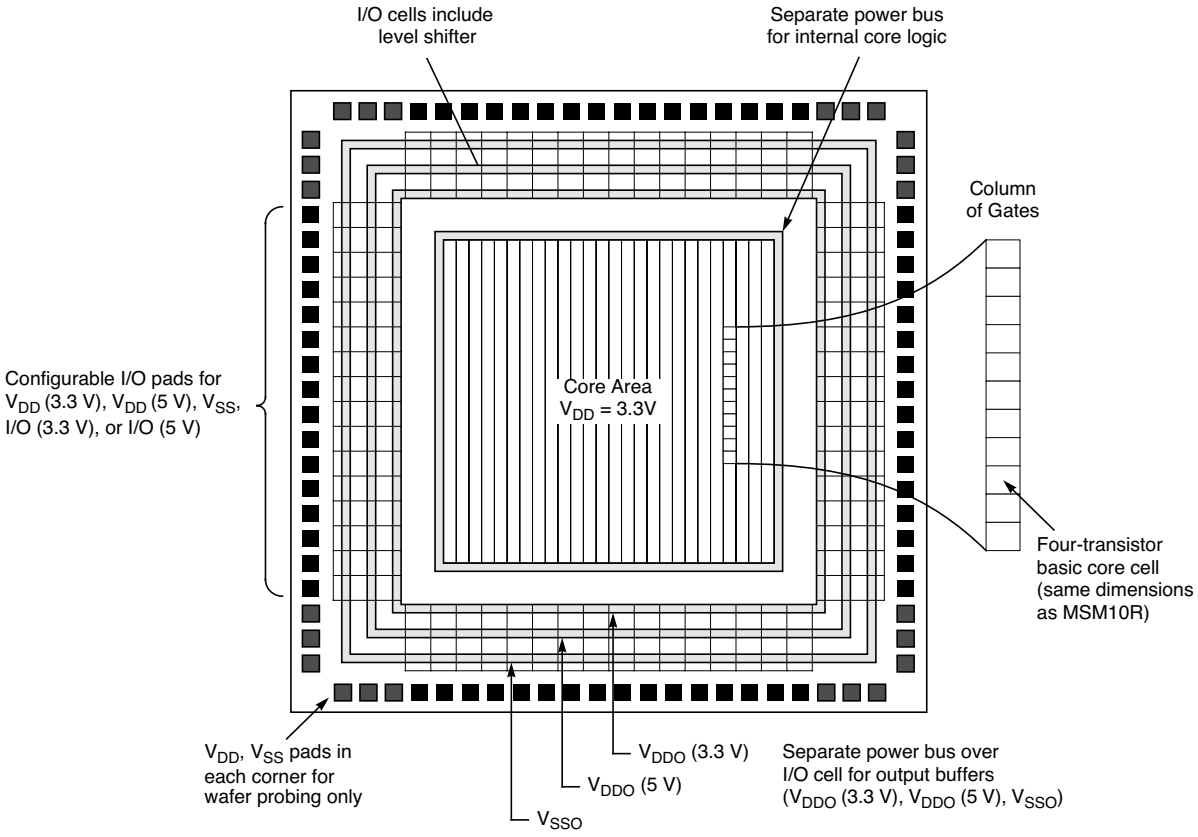


Figure 7. MSM13R0000 Array Architecture

MSM98R000 CSA Layout Methodology

The procedure to design, place, and route a CSA follows.

1. Select suitable base array frame from the available predefined sizes. To select an array size:
    - Identify the macrocell functions required and the minimum array size to hold the macrocell functions.
    - Add together all the area occupied by the required random logic and macrocells and select the optimum array.
2. Make a floor plan for the design's megacells.
    - OKI Design Center engineers verify the master slice and review simulation.
    - OKI Design Center engineers floorplan the array using OKI's proprietary floorplanner and customer performance specifications.
    - Using OKI CAD software, Design Center engineers remove the SOG transistors and replace them with diffused memory macrocells to the customer's specifications.

Figure 8 shows an array base after placement of the optimized memory macrocells.

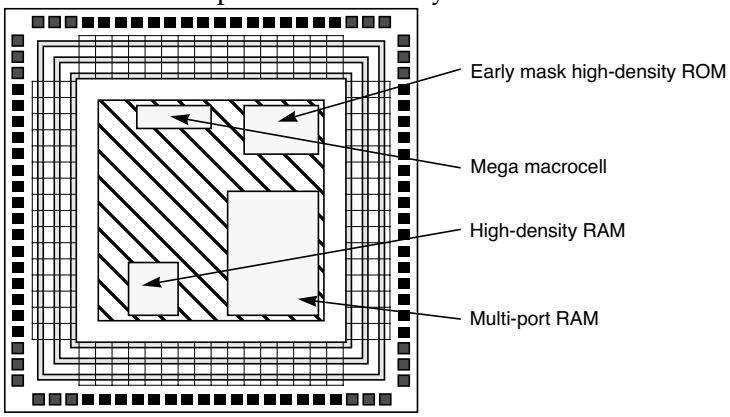


Figure 8. Optimized Memory Macrocell Floor Plan

3. Place and route logic into the array transistors.
    - OKI Design Center engineers use layout software and customer performance specifications to connect the random logic and optimized memory macrocells.

Figure 9 marks the area in which placement and routing is performed with light shading.

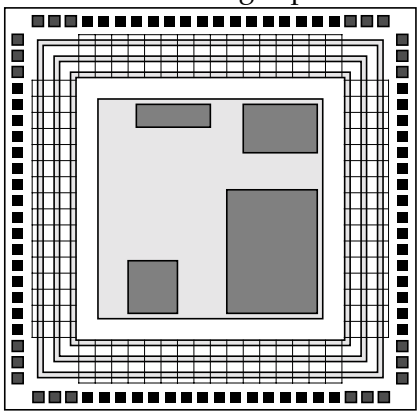


Figure 9. Random Logic Place and Route

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (V_{SS} = 0 V, T_j = 25° C) [1]

Parameter		Symbol	Conditions	Rated Value	Unit
Power supply voltage	Core and 3.3V I/O	$V_{DD}A$	-	-0.3 ~ +4.6	V
	5.0V I/O	$V_{DD}B$	-	-0.5 ~ +6.5	
Input voltage	3.3V buffer	V_I	-	-0.3 ~ $V_{DD}A$+0.3	
	5.0V buffer		-	-0.5 ~ $V_{DD}B$+0.3	
Output voltage	Normal Buffer	V_O	-	-0.3 ~ $V_{DD}A$+0.3	
	5V Tolerant Buffer		-	-0.5 ~ $V_{DD}B$+0.3	
Input current	Normal Buffer	I_I	-	-10 ~ + 10	mA
Output current	1mA buffer	I_O	-	-5 ~ + 5	
	2mA buffer		-	-10 ~ + 10	
	4mA buffer		-	-20 ~ + 20	
	6mA buffer		-	-25 ~ + 25	
	8mA buffer		-	-25 ~ + 25	
	12mA buffer		-	-32 ~ + 32	
	24mA buffer		-	-48 ~ + 48	
	48mA buffer		-	-100 ~ + 100	
Storage temperature		Tj	-	-65 ~ +150	˚C

1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in other parts of this chapter. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions (V_{SS} = 0 V)

Parameter		Symbol	Rated Value			Unit
			Min	Typ	Max	
Power supply voltage	Core	$V_{DD}A$	+3.0	+3.3	+3.6	V
		$V_{DD}A$	+2.7	+3.0	+3.3	
	I/O	$V_{DD}B$	+4.5	+5.0	+5.5	
Junction temperature		Tj	-40	-	+85	˚C
Input rise time/fall time		tr, tf	-	2	20	ns

DC Characteristics (V_{DD} = 3.0 V ± 0.3 V, V_{SS} = 0 V, T_j = -40° C ~ +85° C)

Parameter	Symbol	Conditions	Rated Value			Unit
			Min	Typ [1]	Max	
High-level input voltage	V_{IH}	TTL level input	1.8	-	V_{DD}+0.3	V
		CMOS level input	0.7*V_{DD}	-	V_{DD}+0.3	
Low-level input voltage	V_{IL}	TTL level input	-0.3	-	0.6	
		CMOS level input	-0.3	-	0.3*V_{DD}	
TTL-level Schmitt Trigger threshold voltage Normal buffer	Vt+	-	-	-	1.8	
	Vt-		0.6	-	-	
	ΔVt	Vt+ - Vt-	0.1	-	-	
TTL-level Schmitt Trigger threshold voltage	Vt+	-	-	-	0.76*V_{DD}	
	Vt-		0.24*V_{DD}	-	-	
	ΔVt	Vt+ - Vt-	0.1*V_{DD}	-	-	
High-level output voltage	V_{OH}	I_{OH} = -100μA	V_{DD}-0.2	-	-	
		I_{OH} = -1, -2, -4, -6, -8, -12 mA	2.2	-	-	
Low-level output voltage	V_{OL}	I_{OL}= 100μA	-	-	0.2	
		I_{OL} = 1, 2, 4, 6, 8 mA	-	-	0.4	
		I_{OL} = 12, 24 mA	-	-	0.5	
High-level input current	I_{IH}	V_{IH} = V_{DD}	-	-	1	μA
		V_{IH} = V_{DDIO} (75 kΩ pull down)	10	45	160	
Low-level input current Normal buffer	I_{IL}	V_{IL} = V_{SS}	-1	-	-	
		V_{IL} = V_{SS} (75 kΩ pull up)	-160	-45	-10	
		V_{IL} = V_{SS} (4.5 kΩ pull up)	-2.66	-0.76	-0.16	mA
3-state output leakage current Normal buffer	I_{OZH}	V_{OH} = V_{DDIO}	-	-	1	μA
		V_{OH} = V_{DDIO} (75kΩ pull down)	10	45	160	
	I_{OZL}	V_{OL} = V_{SS}	-1	-	-	
		V_{OL} = V_{SS} (75kΩ pull up)	-160	-45	-10	
		V_{OL} = V_{SS} (4.5kΩ pull up)	-2.66	-0.76	-0.16	mA

DC Characteristics (V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, T_j = -40° C ~ +85° C)

Parameter	Symbol	Conditions	Rated Value			Unit
			Min	Typ [1]	Max	
High-level input voltage	V_{IH}	TTL level input	2.0	-	V_{DD}+0.3	V
		CMOS level input	0.7*V_{DD}	-	V_{DD}+0.3	
Low-level input voltage	V_{IL}	TTL level input	-0.3	-	0.8	
		CMOS level input	-0.3	-	0.3*V_{DD}	
TTL-level Schmitt Trigger threshold voltage Normal buffer	Vt+	-	-	-	2.0	
	Vt-		0.8	-	-	
	ΔVt	Vt+ - Vt-	0.1	-	-	
TTL-level Schmitt Trigger threshold voltage	Vt+	-	-	-	0.76*V_{DD}	
	Vt-		0.24*V_{DD}	-	-	
	ΔVt	Vt+ - Vt-	0.1*V_{DD}	-	-	
High-level output voltage	V_{OH}	I_{OH} = -100μA	V_{DD}-0.2	-	-	
		I_{OH} = -1, -2, -4, -6, -8, -12 mA	2.4	-	-	
Low-level output voltage	V_{OL}	I_{OL}= 100μA	-	-	0.2	
		I_{OL} = 1, 2, 4, 6, 8 mA	-	-	0.4	
		I_{OL} = 12, 24 mA	-	-	0.5	
High-level input current	I_{IH}	V_{IH} = V_{DD}	-	-	1	μA
		V_{IH} = V_{DDIO} (75 kΩ pull down)	10	45	160	
Low-level input current Normal buffer	I_{IL}	V_{IL} = V_{SS}	-1	-	-	
		V_{IL} = V_{SS} (75 kΩ pull up)	-160	-45	-10	
		V_{IL} = V_{SS} (4.5 kΩ pull up)	-2.66	-0.76	-0.16	mA
3-state output leakage current Normal buffer	I_{OZH}	V_{OH} = V_{DDIO}	-	-	1	μA
		V_{OH} = V_{DDIO} (75kΩ pull down)	10	45	160	
	I_{OZL}	V_{OL} = V_{SS}	-1	-	-	
		V_{OL} = V_{SS} (75kΩ pull up)	-160	-45	-10	
		V_{OL} = V_{SS} (4.5kΩ pull up)	-2.66	-0.76	-0.16	mA

DC Characteristics (V_{DD} = 5.0 V ± 0.5 V, V_{SS} = 0 V, T_j = -40° C ~ +85° C)

Parameter	Symbol	Conditions	Rated Value			Unit
			Min	Typ [1]	Max	
High-level input voltage	V_{IH}	TTL level input	2.2	-	V_{DD}+0.5	V
		CMOS level input	0.7*V_{DD}	-	V_{DD}+0.5	
Low-level input voltage	V_{IL}	TTL level input	-0.5	-	0.8	
		CMOS level input	-0.5	-	0.3*V_{DD}	
TTL-level Schmitt Trigger threshold voltage Normal buffer	Vt+	-	-	-	2.2	
	Vt-		0.8	-	-	
	ΔVt	Vt+ - Vt-	0.2	-	-	
TTL-level Schmitt Trigger threshold voltage	Vt+	-	-	-	0.76*V_{DD}	
	Vt-		0.24*V_{DD}	-	-	
	ΔVt	Vt+ - Vt-	0.4	-	-	
High-level output voltage	V_{OH}	I_{OH} = -100μA	V_{DD}-0.2	-	-	
		I_{OH} = -1, -2, -4, -6, -8, -12 mA	3.7	-	-	
Low-level output voltage	V_{OL}	I_{OL}= 100μA	-	-	0.2	
		I_{OL} = 1, 2, 4, 6, 8 mA	-	-	0.4	
		I_{OL} = 12, 24 mA	-	-	0.5	
High-level input current	I_{IH}	V_{IH} = V_{DD}	-	-	10	μA
		V_{IH} = V_{DDIO} (50 kΩ pull down)	20	100	250	
Low-level input current Normal buffer	I_{IL}	V_{IL} = V_{SS}	-10	-	-	
		V_{IL} = V_{SS} (50 kΩ pull up)	-250	-100	-20	
		V_{IL} = V_{SS} (3 kΩ pull up)	-5	-1.6	-0.5	mA
3-state output leakage current Normal buffer	I_{OZH}	V_{OH} = V_{DDIO}	-	-	10	μA
		V_{OH} = V_{DDIO} (75kΩ pull down)	20	100	250	
	I_{OZL}	V_{OL} = V_{SS}	-10	-	-	
		V_{OL} = V_{SS} (75kΩ pull up)	-250	-100	-20	
		V_{OL} = V_{SS} (4.5kΩ pull up)	-5	-1.6	-0.5	mA

AC Characteristics (V_{DD} = 3.3 V, V_{SS} = 0 V, T_j = 25° C)

Parameter		Driving Type	Conditions [1] [2]	Rated Value [3]	Unit
Internal gate propagation delay	Inverter	1X	F/O = 2, L = 0mm	0.11	ns
		2X		0.09	
		4X		0.07	
	2-input NAND	1X		0.16	
		2X		0.12	
		4X		0.11	
	Inverter	1X	F/O = 2 standard wire length	0.33	
		2X		0.24	
		4X		0.15	
	2-input NAND	1X		0.43	
		2X		0.26	
		4X		0.17	
Toggle frequency [4]			F/O = 1, L = 0mm	720	MHz
Input buffer propagation delay	TTL level normal input buffer		F/O = 2, standard wire length	0.42	ns
	TTL level 5V tolerant input buffer			0.38	
Output buffer propagation delay	Push-pull Normal output buffer	4 mA	CL = 20pF	2.22	
		8 mA	CL = 50pF	2.73	
		12 mA	CL = 100pF	3.77	
		24 mA	CL = 150pF	3.39	
Output buffer transition times[1]	Push-pull Normal output buffer	24 mA	CL = 150pF	6.12 (r) 3.72 (f)	

1. Input transition time is 0.18 ns for 3.3V (TTL) and 0.3 ns for 5.0V (CMOS)
2. Typical condition is $V_{DD}A$ = 3.3V, $V_{DD}B$ = 5.0V, and Tj = 25°C
3. Rated value is calculated as an average of the L-H and H-L delay times for each macro type on a typical process.
4. Output rise and fall times are both specified over a 10% to 90% range.

MACRO LIBRARY

Oki Semiconductor supports a wide range of macrocells and macrofunctions, ranging from simple hard macrocells for basic Boolean operations to large, user-parameterizable macrofunctions. The following figure illustrates the main classes of macrocells and macrofunctions available.

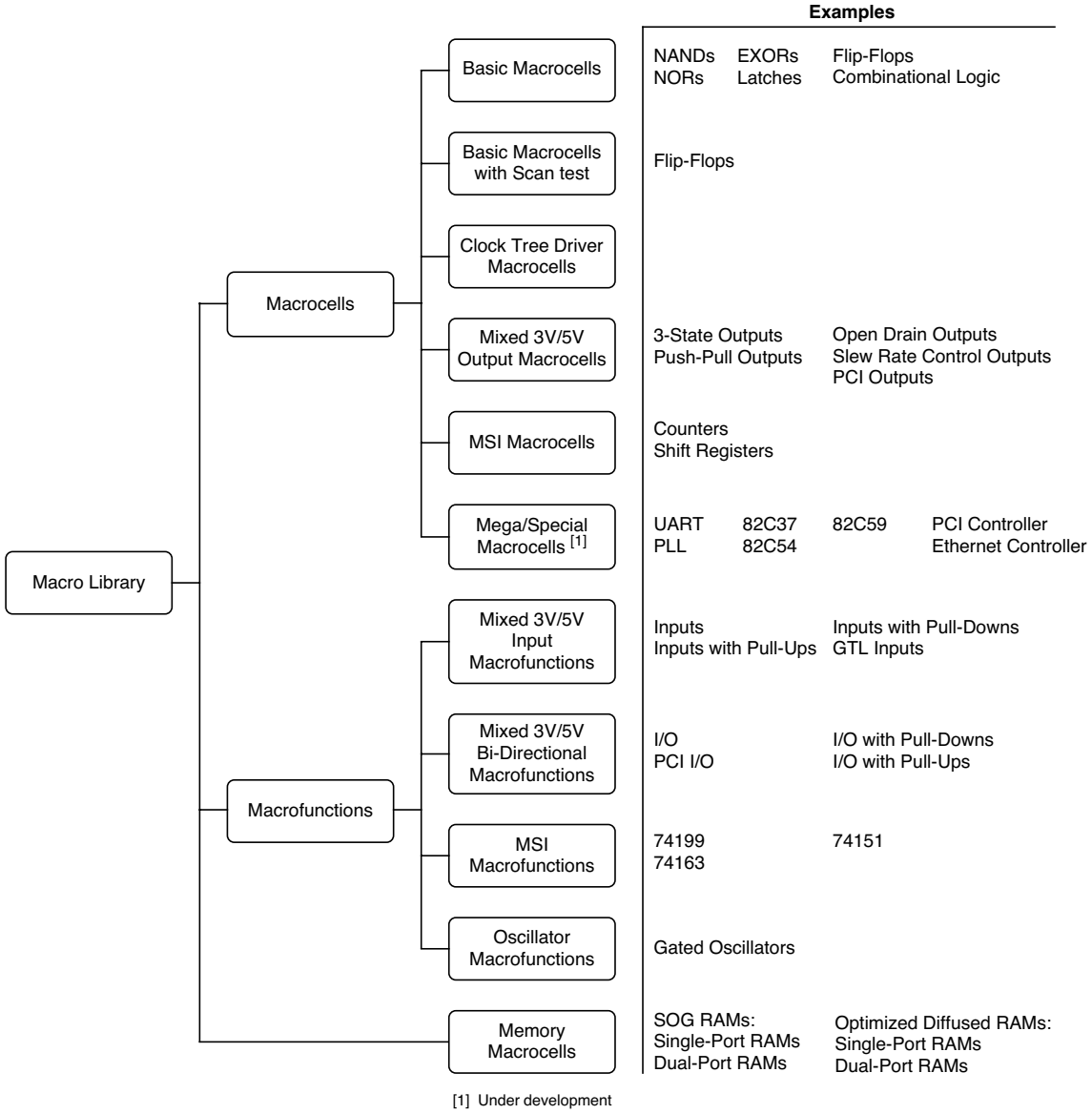


Figure 10. Oki Macrocell and Macrofunction Library

Macrocells for Driving Clock Trees

Oki offers clock-tree drivers that guarantee a skew time of less than 0.5 ns. The advanced layout software uses dynamic driver placement and sub-trunk allocation to optimize the clock-tree implementation for a particular circuit. Features of the clock-tree driver-macrocells include:

- Clock skew ≤ 0.5 ns
- Automatic fan-out balancing
- Dynamic sub-trunk allocation
- Single clock tree driver logic symbol
- Single-level clock drivers
- Automatic branch length minimization
- Dynamic driver placement
- Up to four clock trunks

The clock-skew management scheme is described in detail in Oki's *0.5µm Technology Clock Skew Management Application Note*.

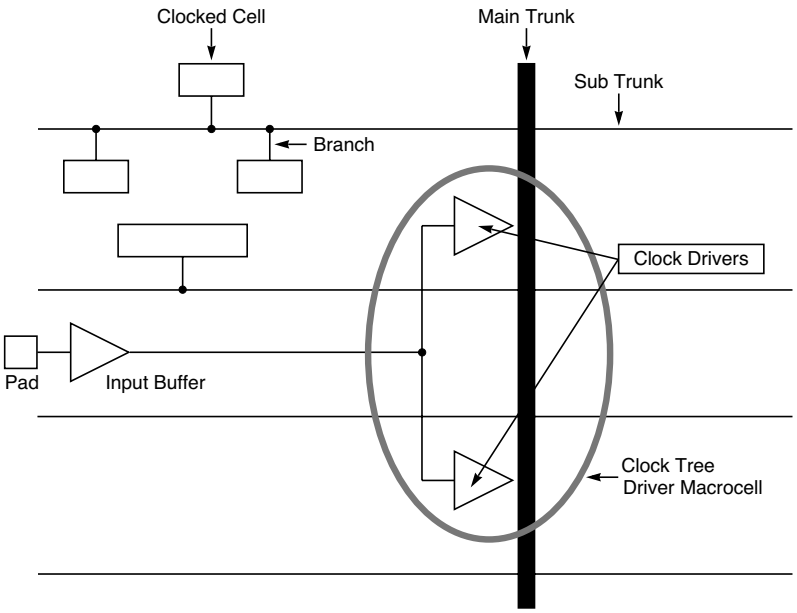


Figure 11. Clock Tree Structure

OKI ADVANCED DESIGN CENTER CAD TOOLS

Oki's advanced design center CAD tools include support for the following:

- Floorplanning for front-end simulation and back-end layout control
- Clock tree structures improve first-time silicon success by eliminating clock skew problems
- JTAG Boundary scan support
- Power calculation which predicts circuit power under simulation conditions to accurately model package requirements

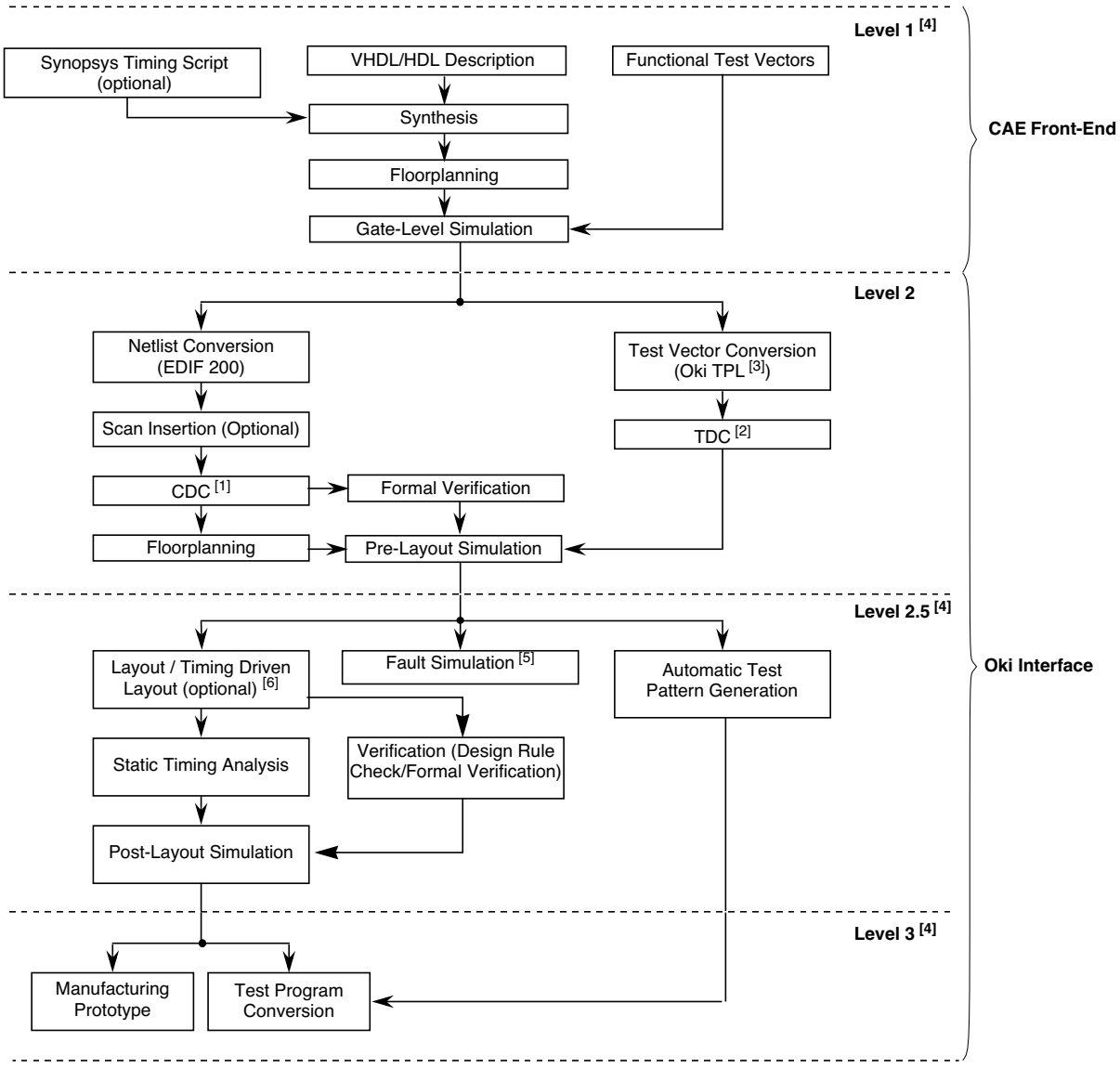
Oki Design Kit Availability

Vendor	Platform	Operating System [1]	Vendor Software/Revision [1]	Description
Cadence	Sun® [2]	Solaris	Ambit Buildgates NC-Verilog™ Verilog XL	Design Synthesis Design Simulation Design Simulation
Syntest	Sun® [2]	Solaris	Turbo Fault	Fault Simulation
Synopsys	Sun® [2]	Solaris	Design Compiler Ultra + Tetramax/ATPG Primetime DFT Compiler/Test Compiler RTL Analyzer VCS	Design synthesis Test Synthesis Static Timing Analysis (STA) Test synthesis RTL check Design Simulation
Model Technology Inc. (MTI)	Sun® [2] NT	Solaris WinNT4.0	MTI-VHDL MTI-Verilog	Design Simulation Design Simulation
Oki	Sun® [2]	Solaris	Floorplanner	Floor planning
Verplex	Sun® [2]	Solaris	Conformal	Formal Verification

1. Contact Oki Application Engineering for current software versions.
2. Sun or Sun-compatible.

Design Process

The following figure illustrates the overall IC design process, also indicating the three main interface points between external design houses and Oki ASIC Application Engineering.



[1] Oki's Circuit Data Check program (CDC) verifies logic design rules
[2] Oki's Test Data Check program (TDC) verifies test vector rules
[3] Oki's Test Pattern Language (TPL)
[4] Alternate Customer-Oki design interfaces available in addition to standard level 2
[5] Standard design process includes fault simulation
[6] Requires Synopsys timing script for Oki timing driven layout

Figure 12. Oki's Design Process

Automatic Test Pattern Generation

Oki's 0.5µm ASIC technologies support Automatic Test Pattern Generation (ATPG) using full scan-path design techniques, including the following:

- Increases fault coverage ≥ 95%
- Uses Synopsys Test Compiler
- Automatically inserts scan structures
- Connects scan chains
- Traces and reports scan chains
- Checks for rule violations
- Generates complete fault reports
- Allows multiple scan chains
- Supports vector compaction

ATPG methodology is described in detail in Oki's *0.5µm Scan Path Application Note*.

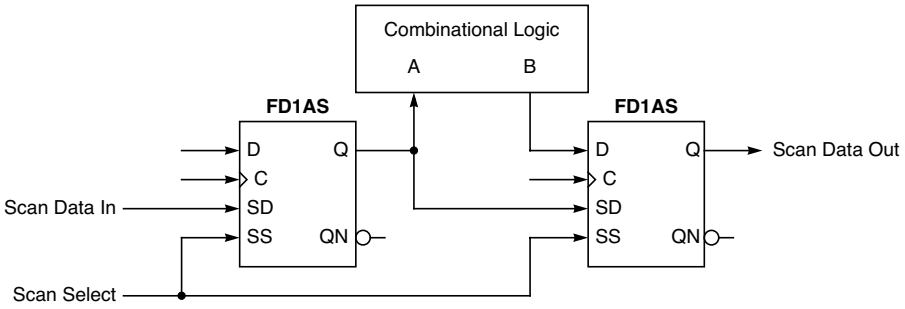


Figure 13. Full Scan Path Configuration

Floorplanning Design Flow

Oki's floorplanner can be classified as both a front-end floorplanner and a back-end floorplanner. During front-end floorplanning, logic designers use the floorplanner to generate two files: a capacitance file for pre-layout simulation, and a floorplanner interface file for layout.

During back-end floorplanning, the layout engineer transfers the floorplanner interface file to Oki's proprietary layout software, code-named Pegasus. The floorplanner interface file contains information about the placement of blocks and groups of blocks. The back-end floorplanner is automated and is transparent to logic designers.

Figure 14 shows a diagram of front-end floorplanning. *Figure 15* shows a diagram of back-end floorplanning.

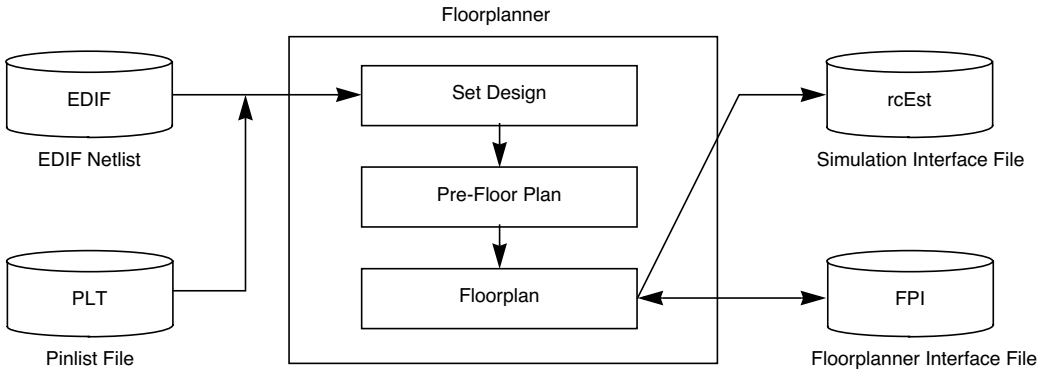


Figure 14. Front-End Floorplanning

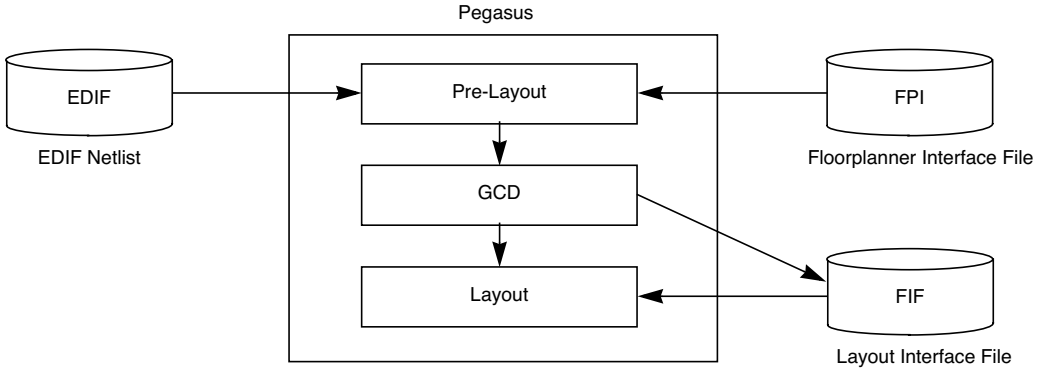


Figure 15. Back-End Floorplanning

IEEE JTAG Boundary Scan Support

Boundary scan offers efficient board-level and chip-level testing capabilities. Benefits resulting from incorporating boundary-scan logic into a design include:

- Improved chip-level and board-level testing and failure diagnostic capabilities
- Support for testing of components with limited probe access
- Easy-to-maintain testability and system self-test capability with on-board software
- Capability to fully isolate and test components on the scan path
- Built-in test logic that can be activated and monitored
- An optional Boundary Scan Identification (ID) Register

Oki's boundary scan methodology meets the JTAG Boundary Scan standard, IEEE 1149.1-1990. Oki supports boundary scan on both Sea of Gates (SOG) and Customer Structured Array (CSA) ASIC technologies. Either the customer or Oki can perform boundary-scan insertion. More information is available in Oki's *JTAG Boundary Scan Application Note.* Contact the Oki Application Engineering Department for interface options.

PACKAGE OPTIONS

MSM12R/13R/98R Package Menu

SOG Base	Prod Name MSM98R	I/O Pads [1]	QFP									TQFP					TQFP			PBGA		
			44	64	80	100	128	160	208	240	304	44	64	80	100	128	144	176	208	256	352	420
	MSM98RB0	80		●	❍	❍						●										
	MSM98RB0	96	❍	●	❍	❍						●		●								
MSM12R0170		104	●	●	●	●						●	●	●	●							
MSM13R0170	MSM98RB0	104	●	●	●	●						●	●	●	●							
	MSM98RB0	120	❍	●	❍	❍						●	●	●	●							
	MSM98RB0	128	❍	●	❍	❍						●	●	●	●	●						
MSM12R0350		144	❍	●	●	●						●	●	●	●	●	●					
MSM13R0350	MSM98RB0	144	❍	●	●	●						●	●	●	●	●	●					
	MSM98RB0	152	❍	●	❍	❍						●	●	●	●	●	●					
	MSM98RB0	160	❍	●	❍	❍						●	●	●	●	●	●					
	MSM98RB0	168	❍	●	❍	❍		❍				●	●	●	●	●	●	❍		●		
MSM12R0560		176	●	●	●	●	●	●				●	●	●	●	●	●	●		●		
MSM13R0560	MSM98RB1	176	●	●	●	●	●	●				●	●	●	●	●	●	●		●		
	MSM98RB1	192		●	❍	❍	●	●				❍	●	●	●	●	●	●		●		
	MSM98RB1	200	●	●	❍	❍	●	●	❍			❍	●	●	●		●	●		●		
MSM12R0790		208	●	●	●	●	●	●	●			●	●	●	●		●	●	●	●		
MSM13R0790	MSM98RB1	208	●	●	●	●	●	●	●			●	●	●	●		●	●	●	●		
	MSM98RB1	224		●	❍	❍	●	●	●					●	●		●	●	●	●		
MSM12R1070		240		●	●	●	●	●	●	●				●	●		●	●	●	●		
MSM13R1070	MSM98RB1	240		●	●	●	●	●	●	●				●	●		●	●	●	●		
	MSM98RB1	256		●	❍	❍	●	●	●	●				●	●		●	❍	●	●		
	MSM98RB1	272		●	❍	❍	●	●	●					●	●		●	●	●	●	●	
	MSM98RB1	288		●	❍	❍	●	●	●					●	●		●	●	●	●	●	
MSM13R1750	MSM98RB1	304		●	●	●	●	●	●	●	●				●		●	●	●	●	●	
	MSM98RB2	320		●	❍	❍	●	●	●	❍	●				●		●	●	●	●	●	●
	MSM98RB2	336		●	❍	❍	●	●	●	●	●				●		●	●	●	●	●	●
	MSM98RB2	352			❍	❍	●	●	●	●							●	●	●	●	●	●
	MSM98RB2	368					●	●	●	●							●	●	●	●	●	●
MSM13R2850	MSM98RB2	384					●	●	●	●	●						●	●	●	●	●	●
	MSM98RB2	400					●	●	●	●	●						●	●	●	●	●	●
	MSM98RB2	416					●	●	●	●							●	●	●		●	●
	MSM98RB2	432						●	●	●							●	●	●		●	●
MSM13R3930	MSM98RB2	448						●	●	●	●						●	●	●		●	
	MSM98RB2	472					❍	●	●									●	●		●	
	MSM98RB3	488					❍	●	❍									●	●		●	
MSM13R4990	MSM98RB3	504					●	●	●	❍	●							●	●		●	
	MSM98RB3	528						●	●	●	●							●	●			
	MSM98RB3	552																				
	MSM98RB3	576																				
	MSM98RB3	600																				
	MSM98RB3	624																				
Body Size (mm)			9x10	14x14	14x20	14x20	28x28	28x28	28x28	32x32	40x40	10x10	10x10	12x12	14x14	14x14	20x20	24x24	28x28	27x27	35x35	35x35
Lead Pitch (mm)			0.8	0.8	0.8	0.65	0.8	0.65	0.5	0.5	0.5	0.8	0.5	0.5	0.5	0.5	0.5	0.5	0.5	1.27	1.27	1.27
Ball Count																				256	352	420
Signal I/O																				231	304	352
Power Balls																				12	16	32
Ground Balls																				13	32	36

1. I/O Pads can be used for input, output, bi-directional, power, or ground.
l = Available now; m = In development

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