E2D0020-39-93

New

OKI Semiconductor

This version: Sep. 1999
Previous version: May 1997

MSM9810

8-channel Mixing OKI ADPCM Type Voice Synthesis LSI

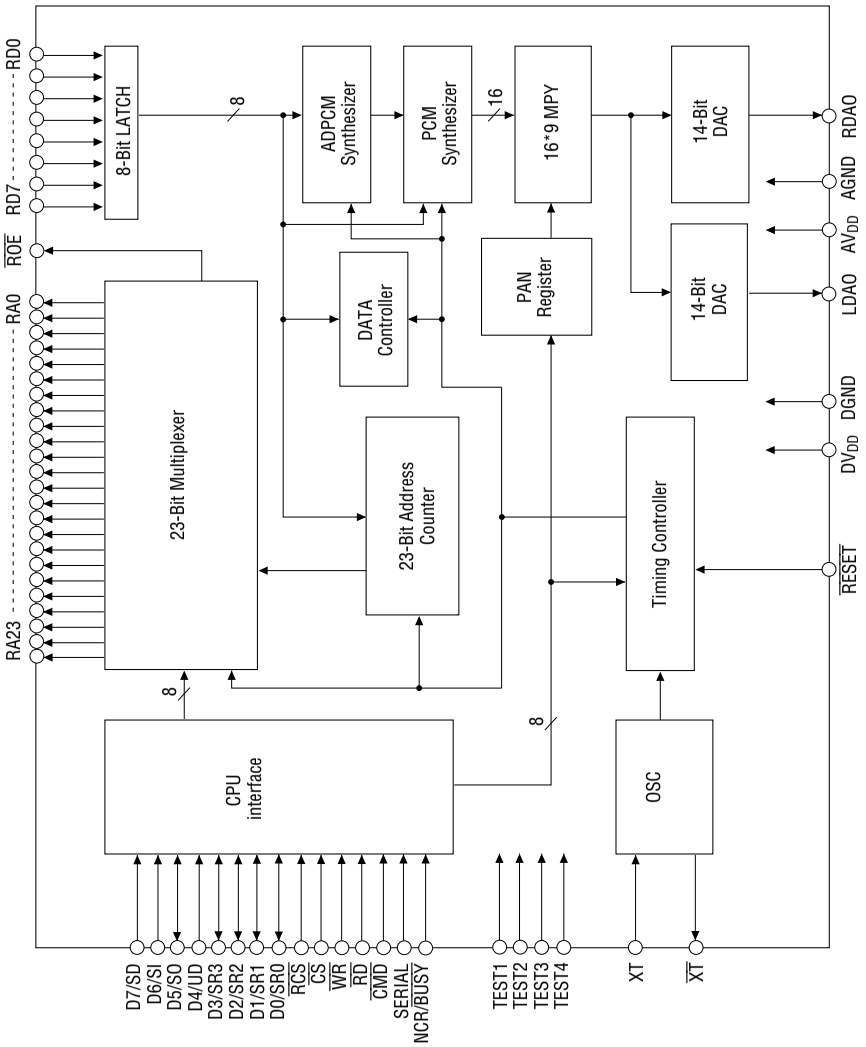
GENERAL DESCRIPTION

The MSM9810 is an 8-channel mixing voice synthesis IC, to which up to 128 Mbits of ROM and/or EPROM storing voice data can directly be connected externally.
The device is straight 8-bit PCM playback, non-linear 8-bit PCM playback, 4-bit ADPCM playback, and 4-bit ADPCM2 playback selectable and provides 2-channel stereo output and volume control. The MSM9810 contains a 14-bit D/A converter and LPF.
The MSM9810 can easily configure a system by connecting voice data storage memory, power amplifier, and CPU externally.

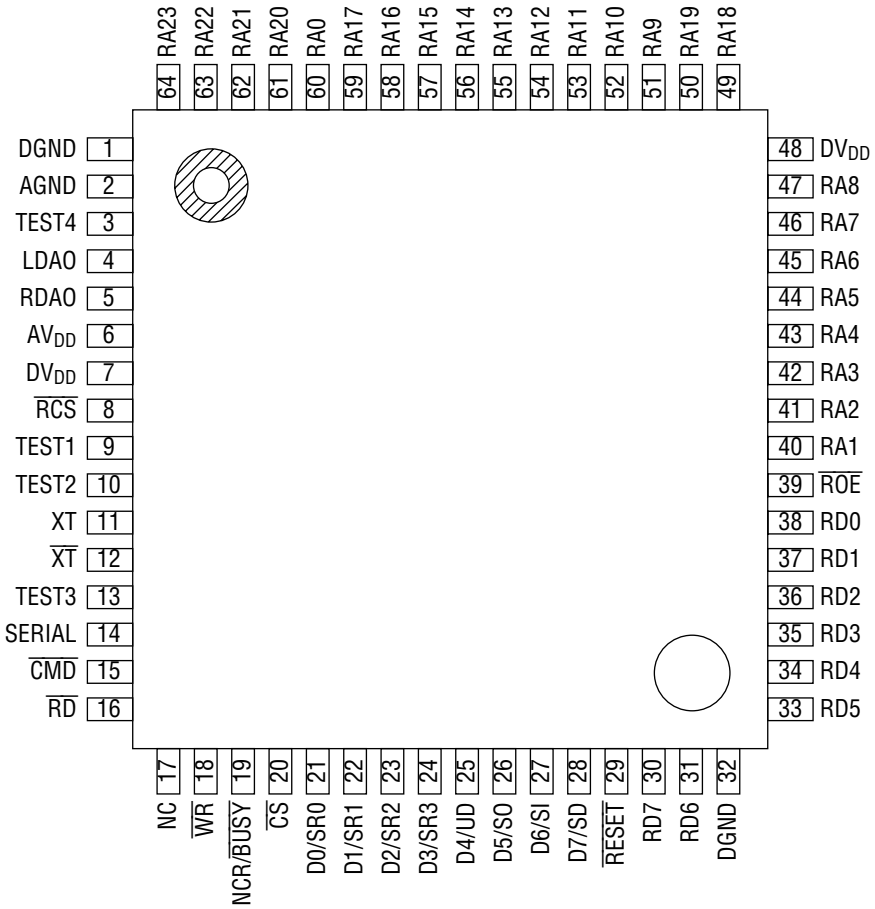
FEATURES

- Non-linear 8-bit PCM / straight 8-bit PCM / 4-bit ADPCM / 4-bit ADPCM2
- Serial input or parallel input selectable
- Phrase Control Table function
- 8-channel mixing function
- Master clock frequency : 4.096 MHz
- Sampling frequency : 4.0 kHz, 5.3 kHz, 6.4 kHz, 8.0 kHz, 10.6 kHz, 12.8 kHz, 16.0 kHz, 21.2 kHz, 25.6kHz, 32.0kHz
- Maximum number of phrases : 256
- Output channel : L/R 2 channels
- Built-in volume control function (for each output channel)
- Built-in 14-bit D/A converter
- Built–in low–pass filter : Digital filter
- Package :
  64-pin plastic QFP(QFP64-P-1414-0.80-BK)(Product name : MSM9810GS-BK)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC: No connection

64-pin Plastic QFP

PIN DESCRIPTIONS

Pin	Symbol	Type	Description
40-47, 49-64	RA23-RA0	O	Address pins for external memory. These pins become high impedance when $\overline{RCS}$ pin is "H".
30, 31, 33-38	RD7-RD0	I	Data pin for external memory. Pull-down resistors are internally connected to these pins. These pull-down resistors become valid when the $\overline{RCS}$ pin is "H", and become invalid when the $\overline{RCS}$ pin is "L".
39	$\overline{ROE}$	O	Output enable pin for external memory.
8	$\overline{RCS}$	I	When this pin is "L", RA23 to RA0 and $\overline{ROE}$ pins output address data and output enable signal. When this pin is "H", RA23 to RA0 and $\overline{ROE}$ pins become high impedance.
15	$\overline{CMD}$	I	Select pin for Command data or Subcommand data. When this pin is "H", subcommand input is selected. When this pin is "L", command input is selected. A pull-up resistor is internally connected to this pin.
16	$\overline{RD}$	I	Read pin for CPU interface. A pull-up resistor is internally connected to this pin.
18	$\overline{WR}$	I	Write pin for CPU interface. A pull-up resistor is internally connected to this pin.
20	$\overline{CS}$	I	Chip select pin for CPU interface. When $\overline{CS}$ is "H", $\overline{WR}$ signal is not entered in this IC. A pull-up resistor is internally connected to this pin.
14	SERIAL	I	CPU interface select pin. When SERIAL is "H", serial input interface is selected. When it is "L", parallel input interface is selected.
28	D7/SD	I/O	Data bus pin for CPU interface when parallel input interface is selected. When $\overline{WR}$ is "L", this pin serves as data input pin. When $\overline{RD}$ is "L", this pin serves as channel status data output pin. When serial input interface is selected, this pin serves as serial data input pin.
27	D6/SI	I/O	Data bus pin for CPU interface when parallel input interface is selected. When $\overline{WR}$ is "L", this pin serves as data input pin. When $\overline{RD}$ is "L", this pin serves as channel status output pin. When serial input interface is selected, this pin serves as serial clock input pin.
26	D5/SO	I/O	Data bus pin for CPU interface when parallel input interface is selected. When $\overline{WR}$ is "L", this pin serves as data input pin. When $\overline{RD}$ is "L", this pin serves as channel status output pin. When serial input interface is selected, this pin serves as channel status output pin.

Pin	Symbol	Type	Description
25	D4/UD	I/O	Data bus pin for CPU interface when parallel input interface is selected. When $\overline{WR}$ is "L", this pin serves as data input pin. When $\overline{RD}$ is "L", this pin serves as channel status output pin. When serial input interface is selected, this pin serves as channel status selecter pin. When UD is "H", channels 8 thru 5 are output to SR3 thru SR0, respectively. When UD is "L", channels 4 thru 1 are output to SR3 thru SR0, respectively.
24	D3/SR3	I/O	Data bus pin for CPU interface when parallel input interface is selected. When $\overline{WR}$ is "L", this pin serves as data input pin. When $\overline{RD}$ is "L", this pin serves as channel status output pin. When serial input interface is selected, this pin serves as channel status output pin. When UD is "H", channels 8 thru 5 are output to SR3 thru SR0, respectively. When UD is "L", channels 4 thru 1 are output to SR3 thru SR0, respectively.
23	D2/SR2		
22	D1/SR1		
21	D0/SR0		
4	LDA0	O	LEFT side D/A output pin.
5	RDA0	O	RIGHT side D/A output pin.
11	XT	I	Crystal or ceramic oscillator connection pin. A feedback resistor of about 1MΩ is connected between XT and $\overline{XT}$. If necessary, enter external clocks into this pin.
12	$\overline{XT}$	O	Crystal or ceramic oscillator connection pin. When external clocks are used, leave this pin open.
29	$\overline{RESET}$	I	When this pin is "L" level, the LSI is initialized. At that time, oscillation stopsand D/A outputs go to GND level.
19	NCR/$\overline{BUSY}$	I	Channel status select pin. When this pin is "H", NCR signal is output. When it is "L", $\overline{BUSY}$ signal is output.
9	TEST1	I	Pins for IC testing. Apply "L" level to these pins. Pull-down resistors are internally connected to these pins.
10	TEST2		
13	TEST3		
3	TEST4	I	Pins for IC testing. Apply "L" level to these pins.
7, 48	DV_{DD}	—	Power supply pin.
6	AV_{DD}		
1, 32	DGND	—	GND pin.
2	AGND		

ABSOLUTE MAXIMUM RATINGS

(GND=0 V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta=25°C	–0.3 to +7.0	V
Input Voltage	V_{IN}		–0.3 to V_{DD}+0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(GND=0 V)

Parameter	Symbol	Condition	Range			Unit
Power Supply Voltage	V_{DD}	—	3.5 to 5.5			V
Operating Temperature	T_{op}	—	–40 to +85			°C
Master Clock Frequency	f_{OSC}	—	**Min.**	**Typ.**	**Max.**	MHz
			3.5	4.096	4.5	

ELECTRICAL CHARACTERISTICS

DC Characteristics

(DV_{DD}=AV_{DD}=4.5 to 5.5 V, DGND=AGND=0 V, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High-level Input Voltage	V_{IH}	—	0.84×V_{DD}	—	—	V
Low-level Input Voltage	V_{IL}	—	—	—	0.16×V_{DD}	V
High-level Output Voltage	V_{OH}	I_{OH} = –1mA	V_{DD}–0.4	—	—	V
Low-level Output Voltage	V_{OL}	I_{OL} = 2mA	—	—	0.4	V
High-level Input Current 1	I_{IH1}	V_{IH} = V_{DD}	—	—	10	µA
High-level Input Current 2	I_{IH2}	Applied to pins with internal pull-down resistor	30	—	300	µA
Low-level Input Current 1	I_{IL1}	V_{IL} = GND	–10	—	—	µA
Low-level Input Current 2	I_{IL2}	Applied to pins with internal pull-up resistor	–300	—	–30	µA
Output Leakage Current	I_{LO}	$0 \le V_{OUT} \le V_{DD}$	–10	—	+10	µA
Operating Current	I_{DD}	—	—	6	15	mA
Standby Current	I_{DS}	Ta = –40°C to +70°C	—	—	15	µA
		Ta = –40°C to +85°C	—	—	50	µA

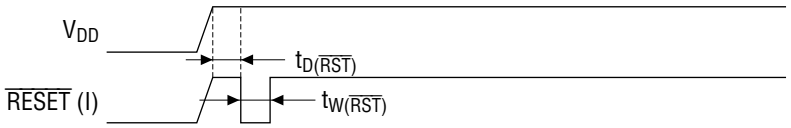
AC Characteristics

(V_{DD}=3.5 to 5.5V, GND=0 V, Ta=–40 to +85°C)

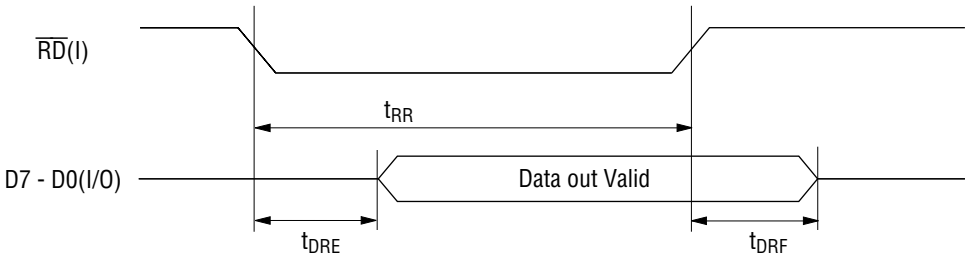
Parameter	Symbol	Min.	Typ.	Max.	Unit
Master Clock Duty Cycle	f_{duty}	40	50	60	%
$\overline{\text{RESET}}$ Input Pulse Width	$t_{w(\overline{RST})}$	1	—	—	µs
$\overline{\text{RESET}}$ Delay Time From Raising of Power Supply	$t_{D(\overline{RST})}$	0	—	—	µs
Set up and Hold Time of $\overline{\text{CS}}$ for $\overline{\text{RD}}$, at serial input I/F	t_{CR}	30	—	—	ns
$\overline{\text{RD}}$ Pulse Width	t_{RR}	200	—	—	ns
Output Data Valid Time after Fall of $\overline{\text{RD}}$	t_{DRE}	—	—	100	ns
Data Float Time after Rise of $\overline{\text{RD}}$	t_{DRF}	—	10	50	ns
Setup and Hold Time of $\overline{\text{CMD}}$ for $\overline{\text{WR}}$	t_{DW}	50	—	—	ns
Setup and Hold Time of $\overline{\text{CS}}$ for $\overline{\text{WR}}$	t_{CW}	30	—	—	ns
$\overline{\text{WR}}$ Pulse Width	t_{WW}	200	—	—	ns
Data Setup Time before Rise of $\overline{\text{WR}}$	t_{DWS}	100	—	—	ns
Data Hold Time after Rise of $\overline{\text{WR}}$	t_{DWH}	30	—	—	ns
$\overline{\text{WR}}$-$\overline{\text{WR}}$ Pulse Interval	t_{WWS}	160	—	—	ns
$\overline{\text{CS}}$-$\overline{\text{CS}}$ Pulse Interval	t_{CC}	100	—	—	ns
Serial Data Setup Time	t_{SDS}	30	—	—	ns
Serial Data Hold Time	t_{SSD}	30	—	—	ns
Serial Clock Pulse Width	$t_{W(SCK)}$	200	—	—	ns

TIMING DIAGRAMS

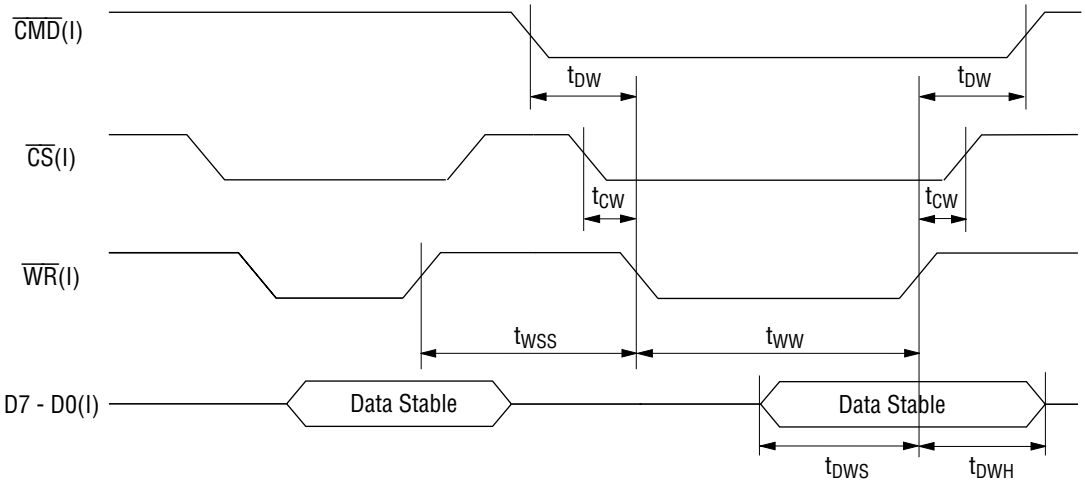
Power-On Timing



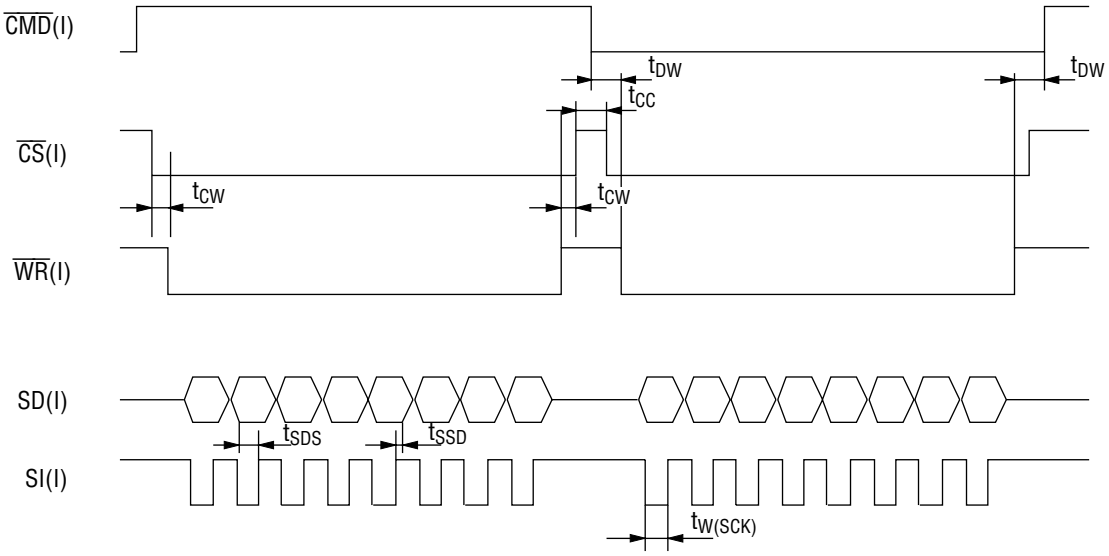
Data Read Timing, Parallel Input



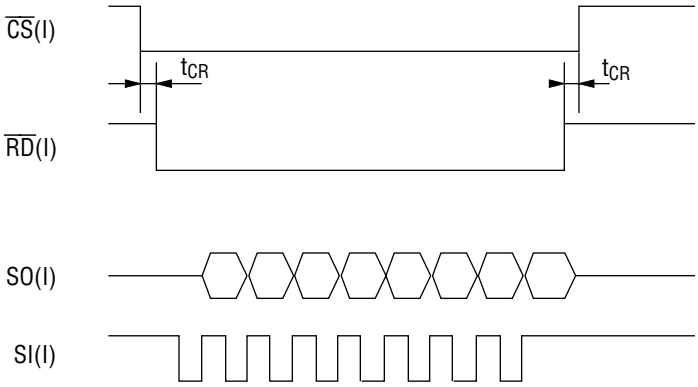
Data Write Timing, Parallel Input



Data Write Timing, Serial Input

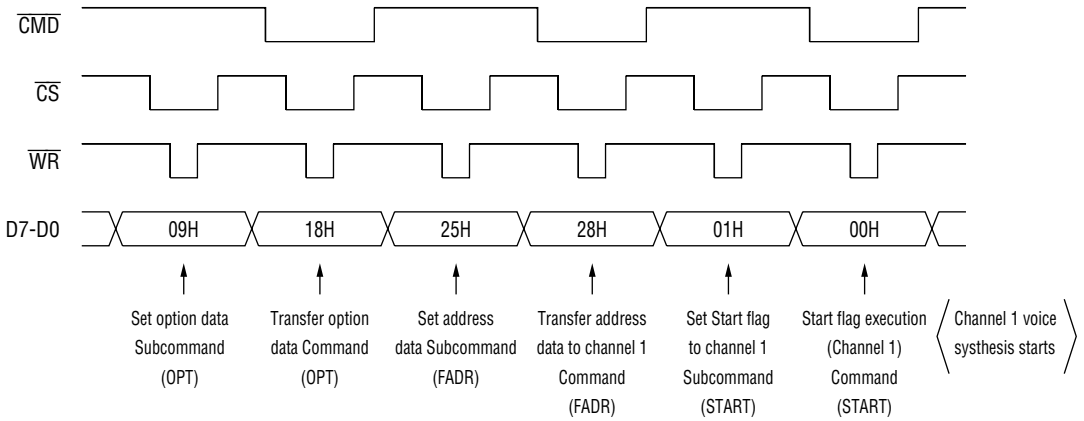


Data Read Timing, Serial Input



Command input timing in parallel input interface

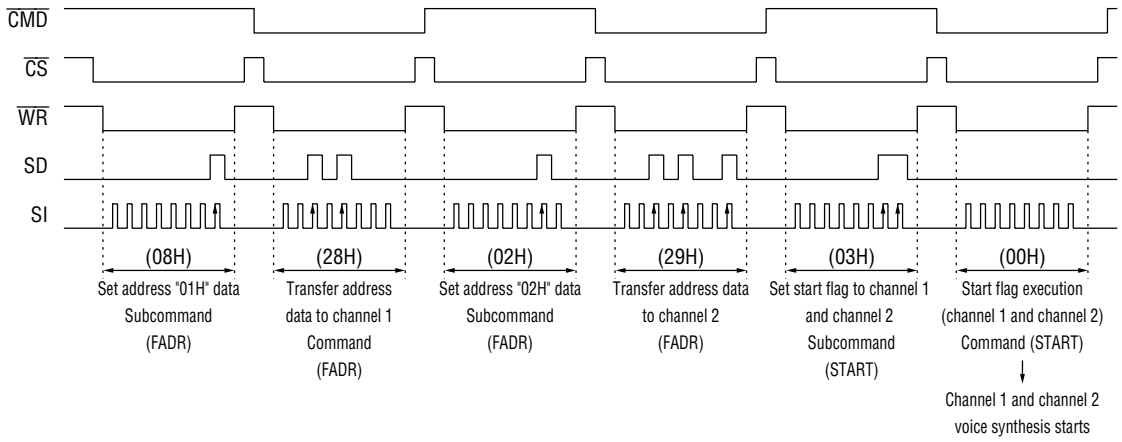
- The phrase address "25H" data is played back via channel 1
- The command options selected are 1/2 V_{DD} (P-P) sound volume for all channels, use of an internal low pass filter, secondary digital filter processing, and voltage follower output.



See 9. "Command Data and Subcommand Data" for further information on commands and subcommands.

Command input timing in serial input interface

- Phrase address "08H" to channel 1 data and Phrase address "02H" to channel 2 data are played back simultaneously.
- The command option is default setting.



See 3-1 "Channel Synthesis" for further information on channel synthesis.

FUNCTIONAL DESCRIPTION

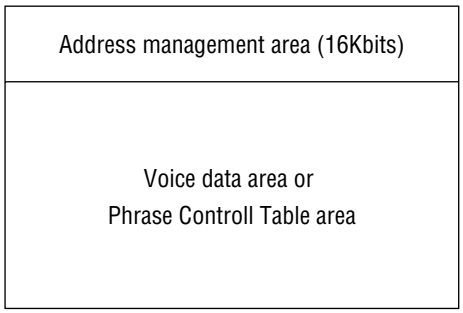
1. User Specification Phrase

A maximum of 256 phrases can be selected with user specification phrases. User specification phrases are stored in the voice management area of external ROM. Merely by selecting a phrase, sampling frequency and the start and stop address of voice are controlled.
The MSM9810 can directly specify a start address or stop address externally without using user specification phrases. Only channels 1 to 4 can be used for directly specifying a start address or stop address externally.

2. Playback Time and Memory Capacity

Table 2.1 shows the configuration of external ROM. The capacity of an actual voice data ROM is different from the indicated ROM capacity.

Table 2.1 ROM Configuration



Playback time depends on external memory capacity, sampling frequency, and the playback system. The relationship is shown below.

$$\text{Playback time} = \frac{1.024 \times (\text{memory capacity} - 16)\ (\text{Kbits})}{\text{Sampling frequency (kHz)} \times \text{bit length}}\ \text{(Seconds)}$$

(Bit length is ADPCM, ADPCM2...4bits, PCM...8bits)

For example, when one 8 Mbits ROM is used with a 16 kHz sampling frequency in a 4-bit ADPCM type, the playback time becomes as follows.

$$\text{Playback time} = \frac{1.024 \times (8192 - 16)\ \text{Kbits}}{16\ (\text{kHz}) \times 4\ (\text{bit})} \fallingdotseq 131\ \text{seconds}$$

In the above equation, the playback time when the Phrase Controll Table function is not used is shown.

3. Sampling Frequency

Sampling frequency can be specified for each phrase in the address management area of external ROM. For the sampling frequency, the following ten types can be selected when voice data is created.

4.0 kHz, 8.0 kHz, 16.0 kHz, 32.0 kHz	(Group 1)
5.3 kHz, 10.6 kHz, 21.3 kHz	(Group 2)
6.4 kHz, 12.8 kHz, 25.6 kHz	(Group 3)

3-1 Channel Synthesis

When the internal LPFs are used, use of a different sampling frequency than the selected sampling frequency GroupX is not permitted for channel synthesis.
The internal LPF can be used by selecting "use of internal LPF" with the OPT command (see 9-4 "OPT Command").
When the internal LPFs are not used, channel synthesis can be made using a different sampling frequency as shown below.

When channels are synthesized, the sampling frequency Group of the first vocalizing channel (one of the above Group 1 to 3) is selected. If the sampling frequency Group other than the selected Group is used for channel synthesis, playback becomes fast or slow. Figure 3.1 and Figure 3.2 show examples.

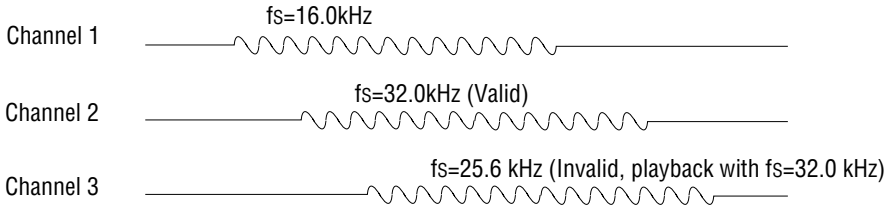


Figure 3.1 When channel 3 is played back using a different sampling frequency while channel 1 and 2 are being played back.

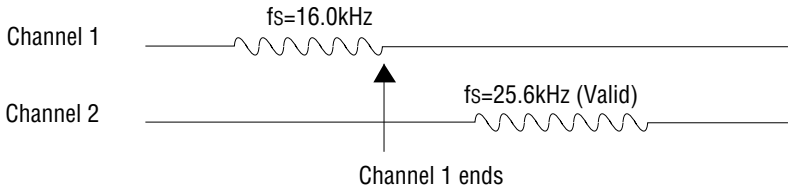


Figure 3.2 Channel 2 is played back using different sampling frequency after channel 1 was played back

When multiple channels are played back simultaneously, the sampling frequency Group of the smallest channel has priority.

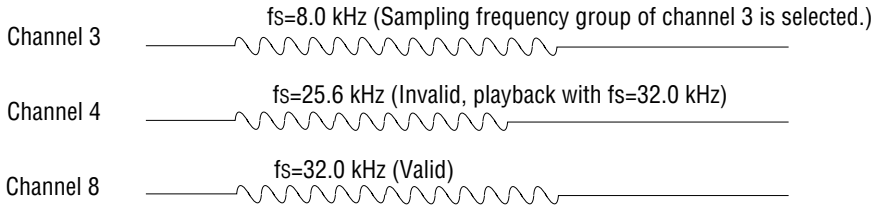


Figure 3.3 When channel 3, 4 and 8 are played back simultaneously.

4. Reset Function

When "L" level is input to the $\overline{\text{RESET}}$ pin, LSI enters power down state, stopping oscillation and minimizing current consumption. At the same time, the control circuit is reset and initialized. Power down status is as follows.

(1) Oscillation stops and all internal circuits stop operation.
(2) Current consumption is minimized. When an external clock is in use, input "L" level to the XT pin in power down status, so that current does not flow into the oscillation circuit.
(3) When a crystal oscillator is in use, "L" level is output to the $\overline{\text{XT}}$ pin.
(4) GND level is output to the D/A output pin (LDAO, RDAO).

Be certain to input "L" level to the $\overline{\text{RESET}}$ pin when power is turned on.

5. Playback System

This LSI has four types of playback systems to support various voices: 4-bit ADPCM, 4-bit ADPCM2, 8-bit straight PCM, and 8-bit non-linear PCM.

5-1 4-bit ADPCM

ADPCM (Adaptive Differential Pulse Code Modulation) system adaptively changes the quantization width and encodes 4-bit data for each sampling, so that the follow up to a voice waveform improves.
ADPCM data is converted by using an analysis tool.
For a human voice, animal voice and natural sounds, it is better to use the ADPCM system because the voice data capacity decreases.

5-2 4-bit ADPCM2

In 4-bit ADPCM 2, the follow-up characteristics to a voice waveform is even better than the 4-bit ADPCM. This system is compatible only with MSM9841/MSM9842.
ADPCM2 data is converted by using an analysis tool.

5-3 8-bit Straight PCM

The follow-up characteristics to a voice waveform to all voice areas is the best of all four types. This system is suitable for sound effects, where waveforms change rapidly, and for pulse shape waveforms.

5-4 8-bit Non-linear PCM

This system plays back the center of a waveform to be a voice quality equivalent to 10 bits. This system is to improve the voice quality of low volume sounds.
8-bit non-linear PCM data is converted by using an analysis tool.

6. Voice Output

The voice is output as 14-bit D/A converter output in stereo (LDAO, RDAO), with L/R in phase. The output amplitude from the D/A converter has a maximum (16383/16384) × V_{DD}, and the output waveform has a step waveform synchronized with sampling frequency.
The command option has been set for voice output. D/A converter output and voltage follower output can be selected by option.

7. Microcomputer Interface

There are two types of interface with microcomputer; one is parallel input interface and the other is serial input interface. Either of the two interfaces can be selected with the SERIAL pin. The parallel input interface is selected when SERIAL is at a "L" level.
The serial input interface is selected when SERIAL is at "H" level.
When the parallel input interface is selected, the MSM9810 is controlled by nine different commands using D7 to D0 (data buses) and control pins $\overline{CMD}$, $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$. The internal status register is used to check the status of the LSI.
When the serial input interface is selected, the MSM9810 is controlled by nine different commands using serial data input pin SD and serial clock input pin SI, and control pins $\overline{CMD}$, $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$.
The SO, SR3, SR2, SR1 and SR0 pins are used to check the status of the LSI.
The pins 21 to 28 function differently according to whether the parallel input interface is selected or the serial input interface is selected.
The table 7-1 shows the pin names. See "PIN DESCRIPTIONS" for their functions.

Table 7-1 Difference between parallel input and serial input pins

Pin number	21	22	23	24	25	26	27	28
Parallel input	D7	D6	D5	D4	D3	D2	D1	D0
Serial input	SD	SI	SO	UD	SR3	SR2	SR1	SR0

7-1 Parallel Input Interface

In the parallel input interface, the microcomputer controls the LSI via 13 pins of $\overline{\text{RESET}}$, $\overline{\text{CMD}}$, $\overline{\text{CS}}$, $\overline{\text{WR}}$, $\overline{\text{RD}}$ and D7-D0.
Command and subcommand data are input from D7-D0 by control of $\overline{\text{CMD}}$, $\overline{\text{CS}}$ and $\overline{\text{WR}}$, as shown in Figure 7-1, and the status is output from D7-D0 by control of $\overline{\text{RD}}$, as shown in Figure 7-2.

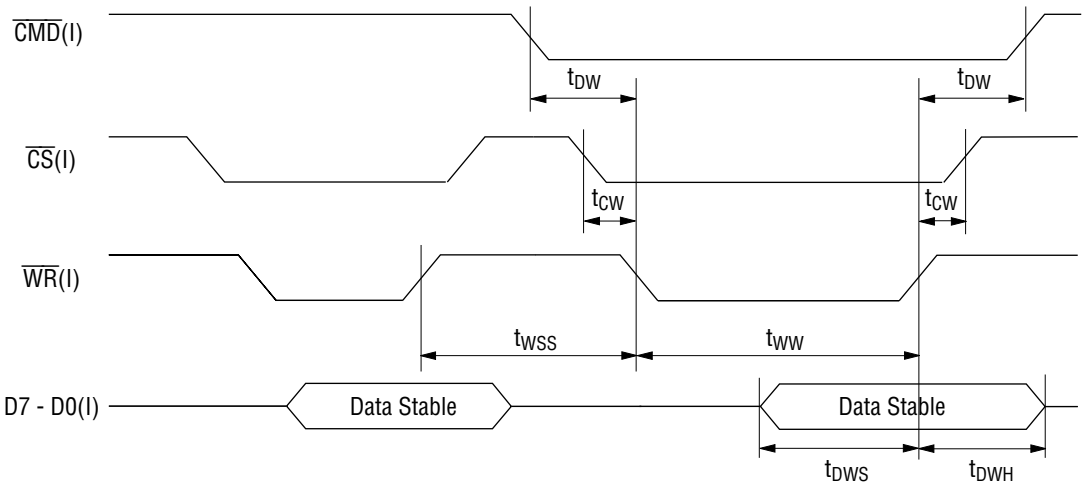


Figure 7-1 Parallel input write cycle timing

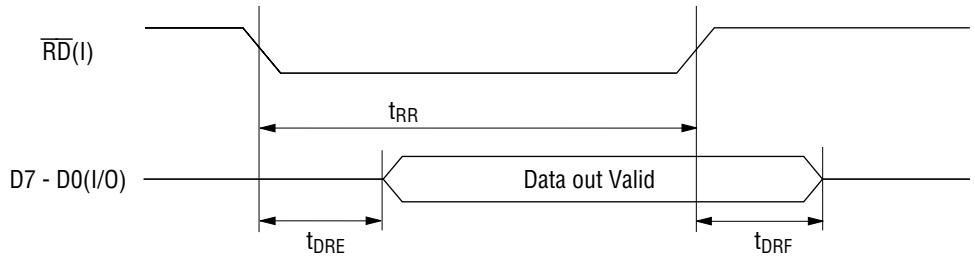


Figure 7-2 Parallel input read cycle timing

7-2 Serial Input Interface

In the serial input interface, the microcomputer controls the LSI via 8 pins of $\overline{\text{RESET}}$, $\overline{\text{CMD}}$, $\overline{\text{CS}}$, $\overline{\text{WR}}$, $\overline{\text{RD}}$, SD, SI and SO. In parallel input, data is output from D7-D0, but in serial input, data for D7-D0 is input in serial from MSB using SD and SI.

Figure 7-3 shows the command and subcommand input timing, and Figure 7-4 shows read timing.

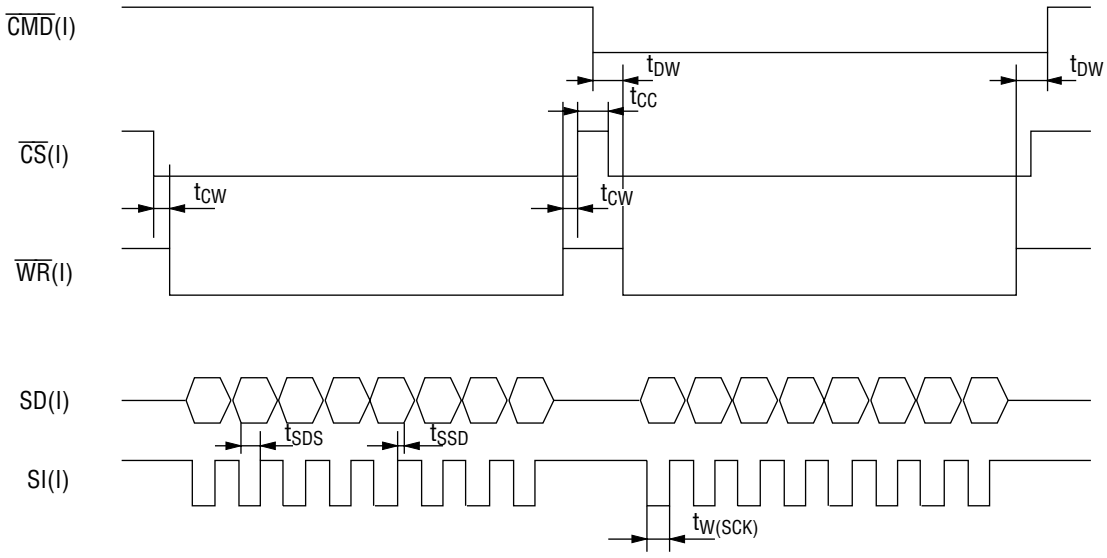


Figure 7-3 Serial input write cycle timing

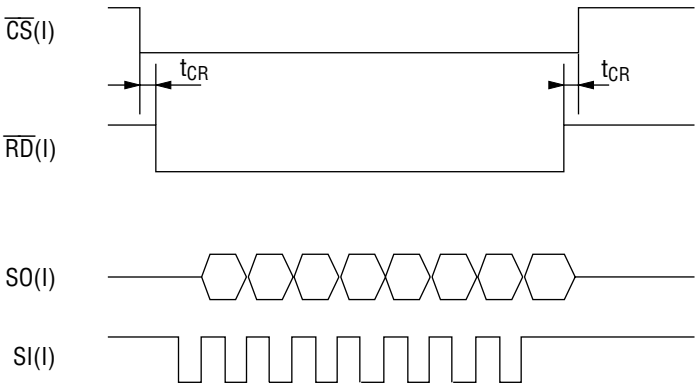


Figure 7-4 Serial input read cycle timing

8. Channel Status

The channel status is output from D7-D0.
There are two types of signals to be output as channel status: $\overline{BUSY}$n (n = 1-8) signals and NCRn signals. These two types are selected by the NCR/$\overline{BUSY}$ pin. When the NCR/$\overline{BUSY}$ pin is at "H" level, NCR is output, and when at "L" level, $\overline{BUSY}$ is output.
The NCR signal is the command and subcommand input status signal (Next Command Request) of each channel, and the $\overline{WR}$ signal input is enabled at "H" level.
The $\overline{BUSY}$ signal outputs "L" level while each channel is executing voice synthesis.
Each channel status signal is output from D7-D0 pins in parallel input interface, and from D5/S0 pins and D3/SR3-D0/SR0 pins in serial input interface by control of $\overline{RD}$. Table 8-1 shows the relationship between D7-D0 and channels, and Figure 8-1 shows read timing in the parallel input interface.

Table 8-1 Correspondence between D7-D0 and channels

Data bus	D7	D6	D5	D4	D3	D2	D1	D0
Corresponding channel	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

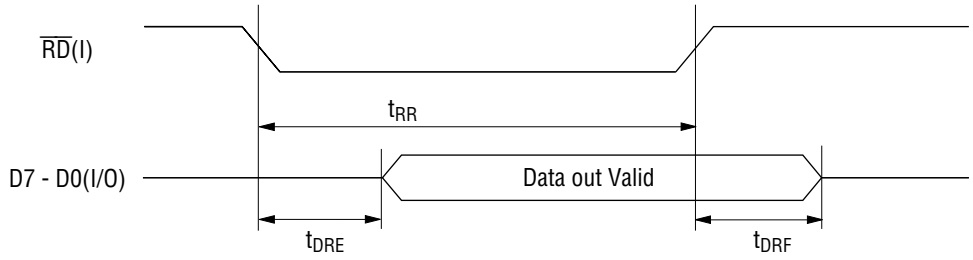


Figure 8-1 Read timing in parallel input interface

In serial input interface, serial output from D5/SO pins by control of $\overline{CS}$ and $\overline{RD}$, and D3/SR3-D0/SR0 parallel output (constantly output) can be selected.

For serial output from D5/SO pin, D7-D0, shown in Table 8-1, are output from MSB in serial at the rise of the SI pin when the $\overline{RD}$ pin is at "L" level.
Figure 8-2 shows this timing.

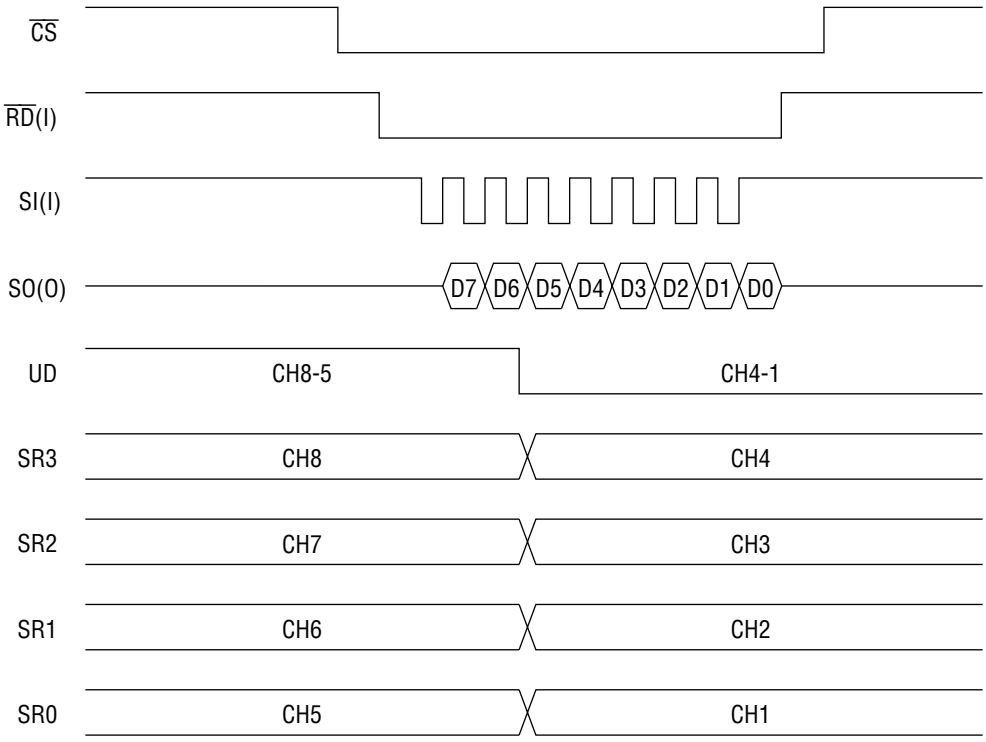


Figure 8-2 Read timing in serial input interface

In serial input interface, status signals are constantly output from D3/SR3 to D0/SR0 pins. Selection of NCR and $\overline{\text{BUSY}}$ is controlled by the NCR/$\overline{\text{BUSY}}$ pin. Since there are only four D3/SR3 to D0/SR0 pins, 8 channels of status signals are selected by control of the D4/UD pin. Table 8-2 shows the relationship between D4/UD pin and D3/SR3 to D0/SR0 pins.

Table 8-2 Correspondence between D4/UD and D3/SR3 to D0/SR0

	D4/UD="L"	D4/UD="H"
D3/SR3	Channel 4	Channel 8
D2/SR2	Channel 3	Channel 7
D1/SR1	Channel 2	Channel 6
D0/SR0	Channel 1	Channel 5

9. Command Data and Subcommand Data

In parallel input, command data and subcommand data are controlled by the data bus of D7-D0 pins and by $\overline{CMD}$, $\overline{CS}$ and $\overline{WR}$ control pins. In serial input, command data and subcommand data are controlled by data input/output of SD, SI and SO pins and by $\overline{CMD}$, $\overline{CS}$ and $\overline{WR}$ control pins.

This LSI reads data to the internal register (TMP register) by executing the subcommand, and transfers data of the TMP register to the register of each command function and executes data by executing the command.

A subcommand and command are distinguished by the level of the $\overline{CMD}$ pin. "H" level indicates a subcommand, and "L" level indicates a command.

Table 9-1 shows the command data list, Table 9-2 shows details of C2-C0 of Table 9-1 (channel specification), and Table 9-3 shows subcommand data list corresponding to command data.

Table 9-1 Command Data List

		D7	D6	D5	D4	D3	D2	D1	D0	Function
1	START	0	0	0	0	0	X	X	X	Starts playback of the channel for which data stored in the register is "H"
2	STOP	0	0	0	0	1	X	X	X	Stops playback of channel for which data stored in the register is "H".
3	LOOP	0	0	0	1	0	X	X	X	Repeats playback of channel for which data stored in the regiter is "H".
4	OPT	0	0	0	1	1	X	X	X	Changes option by command.
5	MUON	0	0	1	0	0	C2	C1	C0	Inserts silence corresponding to the length of data stored in the register.
6	FADR	0	0	1	0	1	C2	C1	C0	Transfers phrase address stored in the register to the phrase register of the specified channel.
7	DADR	0	0	1	1	0	C2	C1	C0	This command internally transfers the 7-byte start and stop address, the value of sampling frequency and playback algorithm which are stored in the TMP register.
8	CVOL	0	0	1	1	1	C2	C1	C0	Changes volume of the specified channel to the volume of data stored in the register.
9	PAN	0	1	0	0	0	C2	C1	C0	Changes volume of the right and left D/A converter to volume of data stored in the register.

(X - - - don't care. For C1, C2 and C0, see Table 9-2.)

Table 9-2 Channel Specification List

C2	C1	C0	Channel control
0	0	0	Channel 1
0	0	1	Channel 2
0	1	0	Channel 3
0	1	1	Channel 4
1	0	0	Channel 5
1	0	1	Channel 6
1	1	0	Channel 7
1	1	1	Channel 8

Table 9-3 Subcommand Data List

Command	D7	D6	D5	D4	D3	D2	D1	D0	Subcommand funciton
START	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	Channel setting
STOP	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	Channel setting
LOOP	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	Channel setting
OPT	0	0	0	O4	O3	O2	O1	O0	Option setting
MUON	M7	M6	M5	M4	M3	M2	M1	M0	Silence time setting
FADR	FA7	FA6	FA5	FA4	FA3	FA2	FA1	FA0	Phrase address setting
DADR	SA23	SA22	SA21	SA20	SA19	SA18	SA17	SA16	(1st byte) address setting
	SA15	SA14	SA13	SA12	SA11	SA10	SA9	SA8	(2nd byte)
	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0	(3nd byte)
	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16	(4nd byte)
	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	(5nd byte)
	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	(6nd byte)
	S3	S2	S1	S0	P1	P0	X	X	(7nd byte)
CVOL	X	X	X	X	V3	V2	V1	V0	Volume setting
PAN	L3	L2	L1	L0	R3	R2	R1	R0	Volume setting

(X - - - don't care.)

9-1 START Command

The START command starts voice synthesis of the channel corresponding to the data stored in the TMP register. Table 9-4 shows the correspondence between data input (D7-D0) and channels. For serial input, the sequence of D7-D0 and serial input data is shown in Figure 8-2.

Table 9-4 Correspondence between D7-D0 and Channels

Data bus	D7	D6	D5	D4	D3	D2	D1	D0
Corresponding channel	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

When the START command is input, data stored in the TMP register is set at the start register, and voice synthesis processing starts. For example, when all " 1" is written from the data bus to the TMP register and the START command is input, all channels start voice synthesis simultaneously.
Input the START command when the status signal (NCR or $\overline{BUSY}$) of the channel to be started is at "H". When NCR is "L", input is disabled.
Figure 9-1 shows the flowchart when the START command is input.

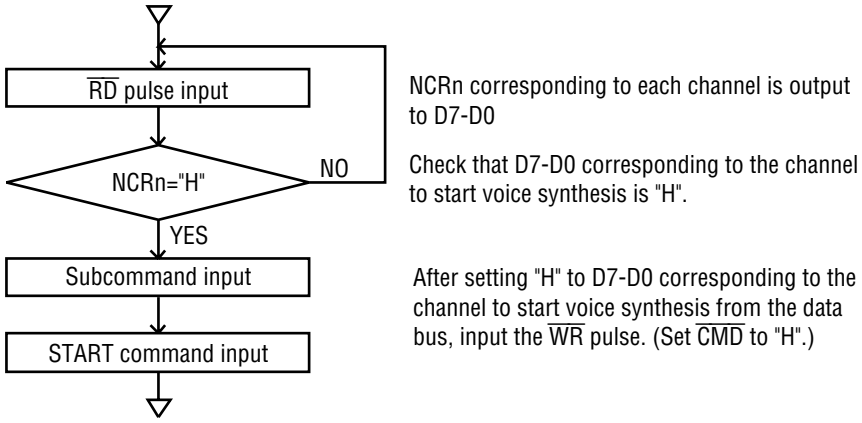


Figure 9-1 START Command Input Flow

9-2 STOP Command

The STOP command stops voice synthesis processing of the channel corresponding to data stored in the TMP register. Table 9-5 shows the correspondence between data input (D7-D0) and channels.

Table 9-5 Correspondence between D7-D0 and channels

Data bus	D7	D6	D5	D4	D3	D2	D1	D0
Corresponding channel	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

When the STOP command is input, the LSI stops processing of voice synthesis of the corresponding channel at the rise of the $\overline{WR}$ pulse. When voice synthesis stops, the PCM value of that channel is cleared to 1/2 V_{DD}, and the NCR and $\overline{BUSY}$ channel status signals become "H".

When "H" has been set at the START register, the START register is cleared to "L".

9-3 LOOP Command

The LOOP command repeats a playback of voice synthesis of the channel corresponding to data stored in the TMP registers. Table 9-6 shows the correspondence between data input (D7-D0) and channels.

Table 9-6 Correspondence between D7-D0 and channels

Data bus	D7	D6	D5	D4	D3	D2	D1	D0
Corresponding channel	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

When the LOOP command is input, the LSI writes data of the TMP register to the LOOP register at rise of $\overline{WR}$ pulse, and repeats a playback of the channel where "H" is set. Once "H" is set at the LOOP register, playback continues until "L" is set from the outside. If the phrase controll table function has been used for a phrase address, the edited voice is repeatedly played back.
To end a repeating playback, set the register of the channel to end the repeat to "L" using the LOOP command again. When the register is set to "L", repeating ends with the current playback phrase. If the START register has been set to continue the playback of another phrase, another phrase is played back continuously after repeating ends.
Figure 9-2 shows an example.

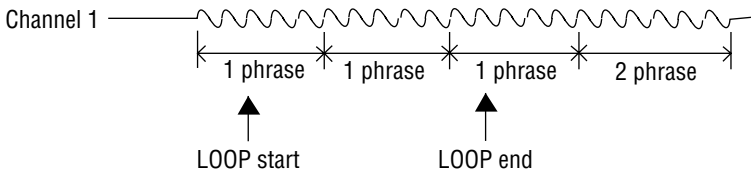


Figure 9-2 LOOP Command Execution Example

9-4 OPT Command

The OPT command changes the setting inside the LSI according to data stored in the TMP register. Table 9-7 shows the correspondence between data input (D7 to D0) and options.

Table 9-7 Correspondence between D7-D0 and options

D4	D3	Option
0	0	Sets volume of all channels to $V_{DD(P-P)}$.
0	1	Sets volume of all channels to $1/2V_{DD(P-P)}$.
1	0	Sets volume of all channels to $1/4V_{DD(P-P)}$.
1	1	Sets volume of all channels to $1/8V_{DD(P-P)}$.

D2	Option
0	Uses internal LPF.
1	Does not use internal LPF.

D1	Option
0	Executes 2nd digital filter processing.
1	Executes 1st digital filter processing.

D0	Option
0	Outputs directly from the D/A converter.
1	Outputs via a voltage follower.

(Input "L" to D7-D5.)

When the OPT command is input, the LSI changes the option at the rising edge of the $\overline{WR}$ pulse. When power is turned on, or when the $\overline{RESET}$ pulse is input, the registers corresponding to D3-D0 have been set to "L".
If the option is changed when voice synthesis is in execution, voice quality may change. Oki recommends to set the option after power is turned on or after $\overline{RESET}$ is input.

1) Volume Option
Volume can be set by the CVOL command and PAN command, but a waveform may be clamped when channel synthesis is executed.
If the CVOL command and PAN command are used to prevent a waveform from being clamped, the number of steps used for actual volume decreases, and effective voice synthesis may not be performed.
If it is known that a waveform will be clamped, this option can set the volume of all channels to low, so that the number of steps of the volume can be utilized to the maximum level.
2) Digital Filter Processing
This LSI has a built-in oversampling circuit for digital filter processing. This oversampling system evenly generates four times more points of sampling frequencies.
When power is turned on or if the $\overline{RESET}$ pulse is input, those pulses have been set to pass through the oversampling circuit. If digital filter processing is unnecessary, change this setting by the OPT command.

3) Analog Output
When power is turned on, it has been set that the output of the D/A converter is output via the voltage follower. To change this setting, use the OPT command.
The output impedance of analog signals being output via the voltage follower is about 500Ω.
The output impedance of analog signals directly output from the D/A converter is about 30kΩ.

9-5 MUON Command

The MUON command inserts silence into the specified channel at the rise of the $\overline{WR}$ pulse. The length of silence is according to the size of data stored in the TMP register.
The length of silence data is input in advance, before executing the MUON command. Silence length can be set for 255 steps, 4 ms to 1020 ms, in 4 ms intervals. Silence time can be set as follows.

$t_{mu} = (2^7 \times (D7) + 2^6 \times (D6) + 2^5 \times (D5) + 2^4 \times (D4) + 2^3 \times (D3) + 2^2 \times (D2) + 2^1 \times (D1) + 2^0 \times (D0) \times 4.096$ ms

The operation of the MUON command is similar to the START command to start voice synthesis. When the MUON command is input, "H" is set to the START register, and NCR and $\overline{BUSY}$ signals becomes "L".
If the MUON command is input when voice synthesis is in execution, silence time is inserted after voice synthesis ends.
Input the MUON command when the status signal (NCR or $\overline{BUSY}$) of the channel to start voice synthesis is at "H". When NCR is "L", input is disabled.

Figure 9-3 shows a flow chart example when the MUON command is input.

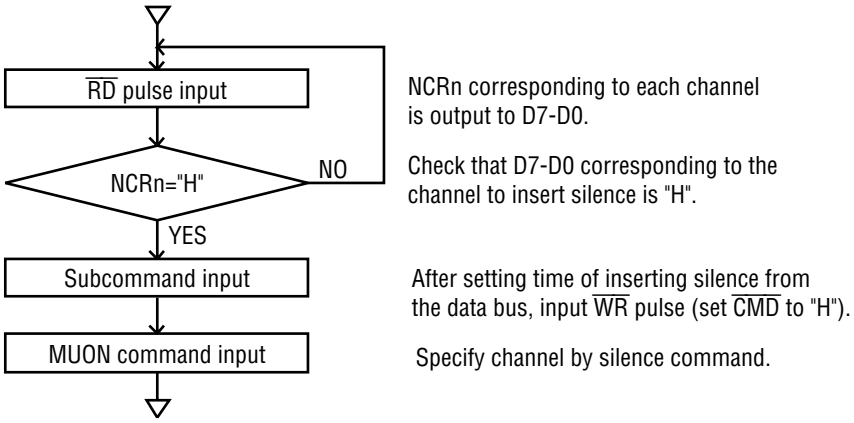


Figure 9-3 MUON Command Input Flow

9-6 FADR Command

The FADR command transfers data stored in the TMP register to the phrase address register of the corresponding channel at the rise of the $\overline{WR}$ pulse.

For the phrase address, the user specification phrases have been set by an analysis tool, and the playback system, sampling frequency and start and stop address of voice data have been registered to the address management area.
When the phrase address is set and the START command is input, the LSI reads data of the address management area, and starts voice synthesis.
Since the phrase address is set by D7-D0, a maximum of 256 phrases can be set. The edit function can be used for phrase addresses, so not only one phrase but combinations with other phrases are possible.

9-7 DADR Command

The DADR command transfers data stored in the TMP (1-7) register to the start and stop address register of the corresponding channel at the rise of the $\overline{WR}$ pulse.
For the direct address, the playback system, sampling frequency, and start and stop address of voice data is directly input from the microcomputer without using the address management area.
Direct address playback system is available with channel 1 to 4, and not available with channel 5 to 8.
Since the phrases that can be set at a phrase address is a maximum of 256, if voice data exceeds 256 phrases, use this command. Data on the playback system, sampling frequency, and start and stop address of voice data is displayed when an analysis tool is used.
Data on the playback system, sampling frequency, and start and stop address of voice data is input to the TMP1 to TMP7 registers divided in 7 steps, unlike the data input of other commands.
Figure 9-4 shows the input method.

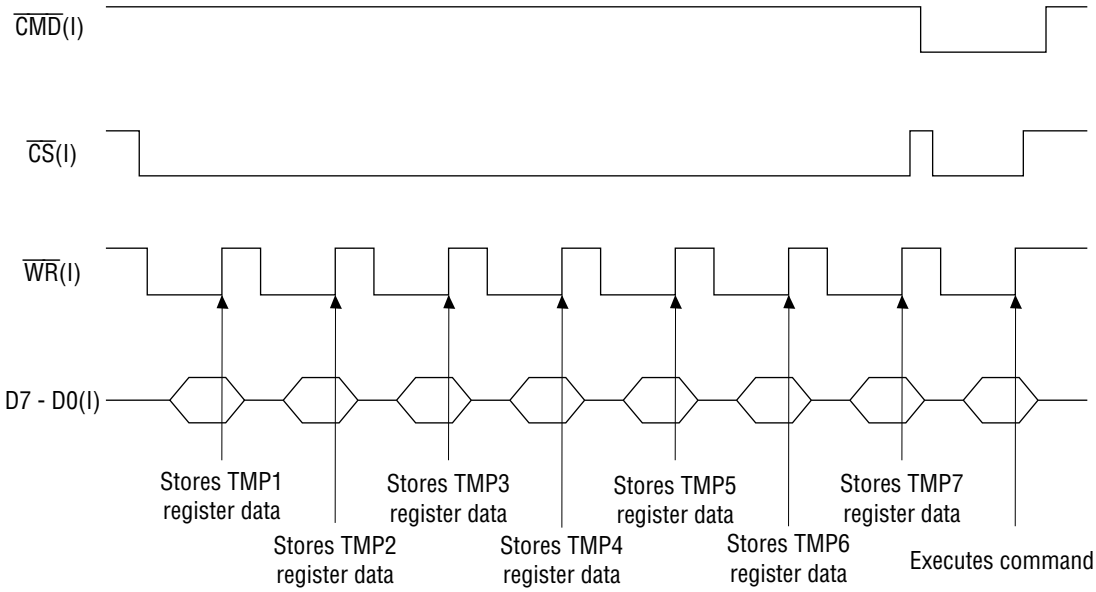


Figure 9-4 DADR Input Timing

As Figure 9-4 shows, $\overline{CS}$ and $\overline{WR}$ pulses are input 7 times when $\overline{CMD}$ is in "H" status, to input data to the TMP1 to TMP7 registers. The LSI increments the registers at the rise of the $\overline{WR}$ pulse when $\overline{CMD}$ is "H". $\overline{CMD}$ must not be "L" while inputting data. When $\overline{CMD}$ becomes "L" while inputting data, the increment of registers is cleared.

Table 9-8 shows the configuration of data to be input to TMP1 to TMP7 registers.

Table 9-8 TMP Register Data Configuration

	D7	D6	D5	D4	D3	D2	D1	D0
TMP1 register	A23	A22	A21	A20	A19	A18	A17	A16
TMP2 register	A15	A14	A13	A12	A11	A10	A9	A8
TMP3 register	A7	A6	A5	A4	A3	A2	A1	A0
TMP4 register	T23	T22	T21	T20	T19	T18	T17	T16
TMP5 register	T15	T14	T13	T12	T11	T10	T9	T8
TMP6 register	T7	T6	T5	T4	T3	T2	T1	T0
TMP7 register	S3	S2	S1	S0	P1	P0	0	0

Input the start address of voice data to TMP1 to TMP3 registers. Input the stop address of voice data to TMP4 to TMP6 registers.

Input the playback system and sampling frequency to the TMP7 register. Table 9-9 shows the input data configuration of the playback system and sampling frequency.

Table 9-9 Data Configuration of Playback System and Sampling Frequency

S3	S2	S1	S0	
0	0	0	0	Sampling frequency 4.0kHz
0	0	0	1	Sampling frequency 8.0kHz
0	0	1	0	Sampling frequency 16.0kHz
0	0	1	1	Sampling frequency 32.0kHz
0	1	0	1	Sampling frequency 6.4kHz
0	1	1	0	Sampling frequency 12.8kHz
0	1	1	1	Sampling frequency 25.6kHz
1	0	0	1	Sampling frequency 5.3kHz
1	0	1	0	Sampling frequency 10.6kHz
1	0	1	1	Sampling frequency 21.3kHz

P1	P0	
0	0	Playback system: 4-bit ADPCM
0	1	Playback system: 4-bit ADPCM2
1	0	Playback system: 8-bit non-linearPCM
1	1	Playback system: 8-bit straight PCM

9-8 CVOL Command

The CVOL command adjusts the volume of the specified channel to the volume which corresponds to the size of data stored in the TMP register at the rise of the $\overline{WR}$ pulse.

Volume can be set in 16 steps up to -30 dB in -2dB step units. Set data as shown in Table 9-10.

Table 9-10 Volume Setting Data Configuration

D3	D2	D1	D0	Volume (dB)
0	0	0	0	0dB
0	0	0	1	–2dB
0	0	1	0	–4dB
0	0	1	1	–6dB
0	1	0	0	–8dB
0	1	0	1	–10dB
0	1	1	0	–12dB
0	1	1	1	–14dB
1	0	0	0	–16dB
1	0	0	1	–18dB
1	0	1	0	–20dB
1	0	1	1	–22dB
1	1	0	0	–24dB
1	1	0	1	–26dB
1	1	1	0	–28dB
1	1	1	1	–30dB

(D7-D4 : Don't care)

When power is turned on and the $\overline{RESET}$ pulse is input, all channels are set to 0dB.

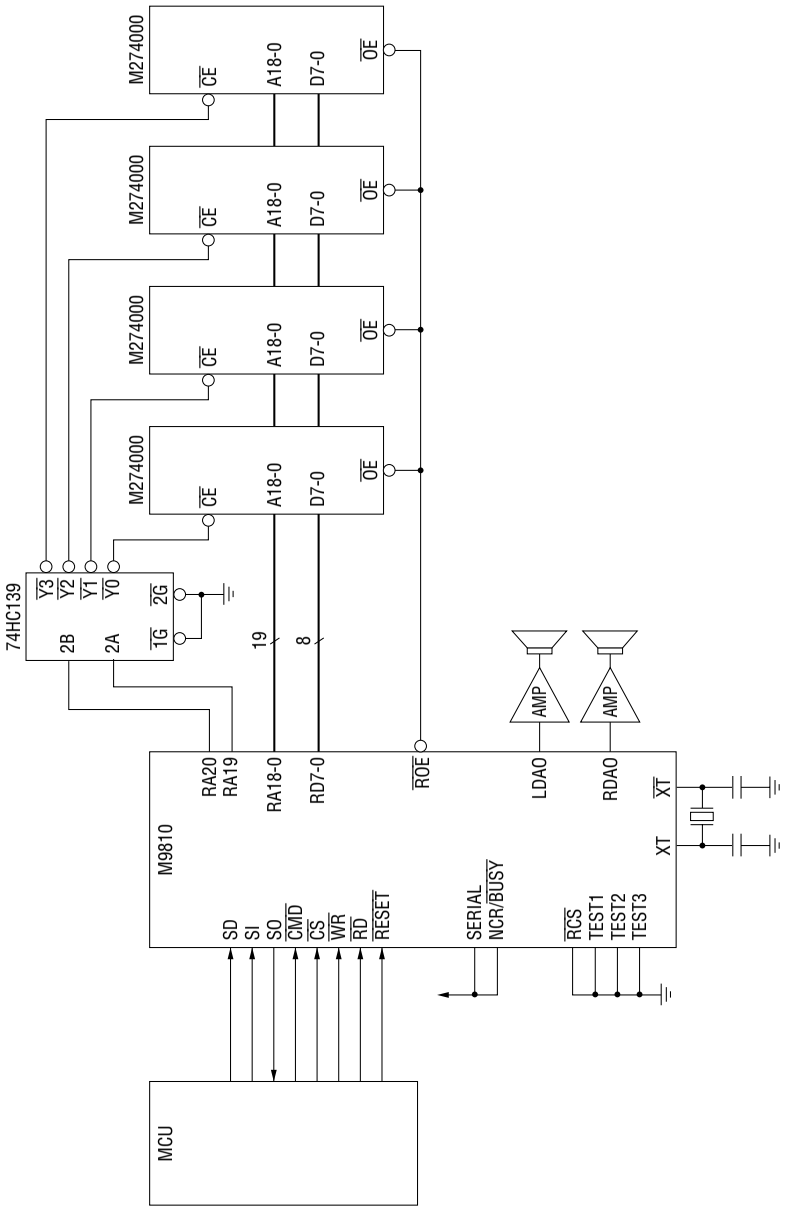
9-9 PAN Command

The PAN command adjusts the volume of the specified channel for the left and right respectively, to the volume which corresponds to the size of data stored in the TMP register at the rise of the $\overline{WR}$ pulse.
This command enables stereo output.
When volume is controlled by the OPT command and CVOL command, volume to be output is the volume stored in ROM multiplied by volume set by the OPT command, CVOL command, and PAN command respectively. This volume is output from LDAO and RDAO.
Volume can be set in 16 steps up to –30 dB in –2 dB step units. Set data as shown in Table 9-11.

Table 9-11 PAN Data Configuration

D7	D6	D5	D4	Volume at left side
D3	D2	D1	D0	Volume at right side
0	0	0	0	0dB
0	0	0	1	–2dB
0	0	1	0	–4dB
0	0	1	1	–6dB
0	1	0	0	–8dB
0	1	0	1	–10dB
0	1	1	0	–12dB
0	1	1	1	–14dB
1	0	0	0	–16dB
1	0	0	1	–18dB
1	0	1	0	–20dB
1	0	1	1	–22dB
1	1	0	0	–24dB
1	1	0	1	–26dB
1	1	1	0	–28dB
1	1	1	1	–30dB

APPLICATION CIRCUITS

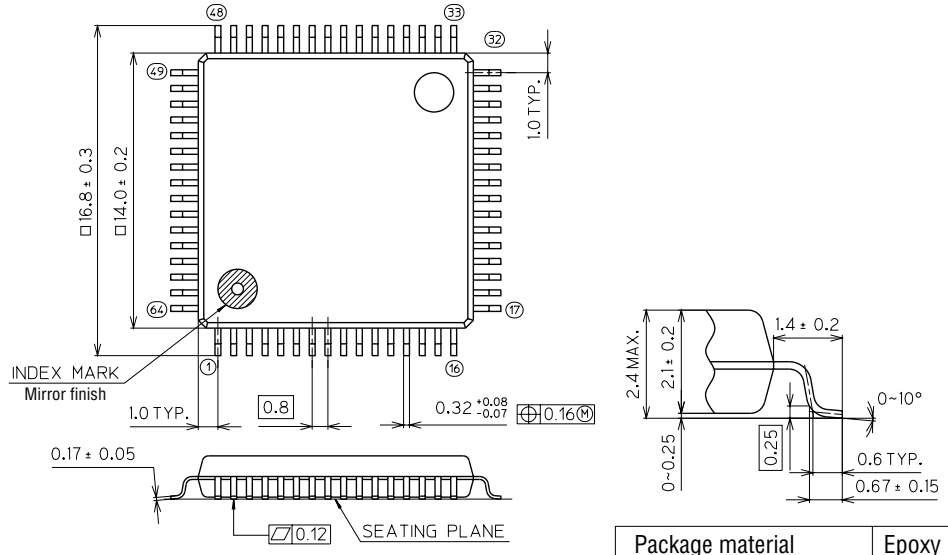


Application circuit example when four 4Mbit EPROMs are connected (serial interface)

PACKAGE DIMENSIONS

(Unit : mm)

QFP64-P-1414-0.80-BK



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 µm or more
Package weight (g)	0.87 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
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