OKI Semiconductor

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# MSM9841

**Recording and Playback LSI with Built-in FIFO**

This document contains minimum specifications. For full specifications, please contact your nearest Oki office or representative.

## GENERAL DESCRIPTION

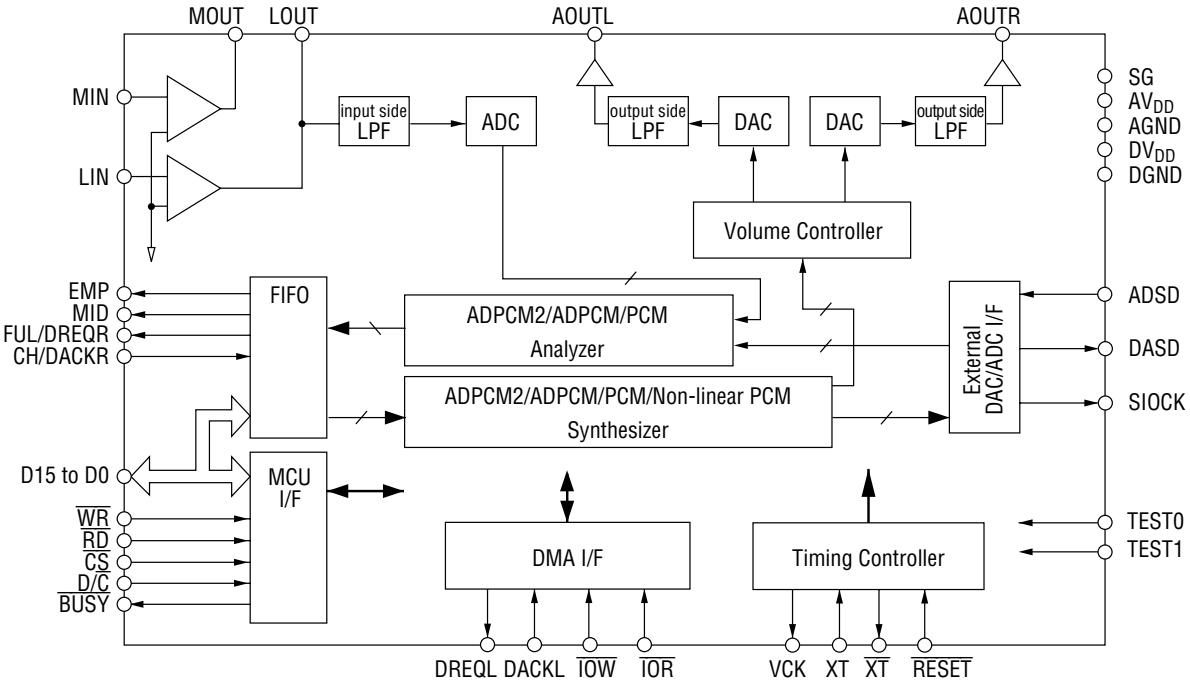
The MSM9841 is a mono/stereo record and playback LSI with a built-in 1K bit FIFO for easy interface with external systems or non-semiconductor memory. It utilizes multiple record and playback modes, including the new ADPCM2 algorithm, which allows for even higher quality sound reproduction. The record and playback functions of the MSM9841 is controlled by an MCU via 8/16-bit bus interface.

## FEATURES

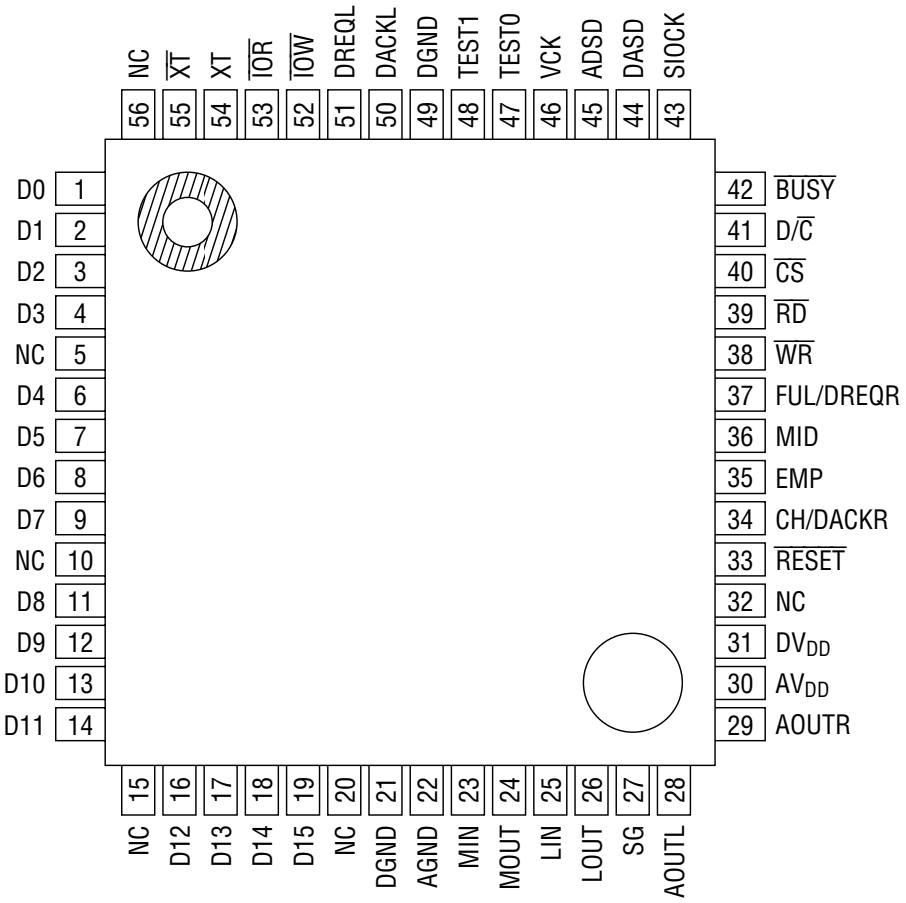
- 16/8-bit bus interface support
- FIFO capacity: User-definable (256/512/1024 bits)
  (buffering time of 32 ms when using 8 kHz sampling frequency, 4-bit ADPCM2/ADPCM, and in monaural playback)
- Supports four compression algorithms for record and playback:
  4, 5, 6, 7, 8-bit ADPCM2; 4-bit ADPCM; 8; 16-bit PCM; and 8-bit Nonlinear PCM
- Sampling frequency: 4.0 kHz, 6.4 kHz, 8.0 kHz, 12.8 kHz, 16.0 kHz, 32.0 kHz* (fosc=4.096 MHz)
- Sampling frequency: 22.05 kHz*, 44.1 kHz* (fosc=5.6448 MHz)
- For the built-in ADC, set the sampling frequency at 16 kHz or less.
- DMA interface support
- Volume control (8 steps: 0 dB to –21 dB)
- Built-in 14-bit A/D converter
- Built-in 14-bit D/A converter
- Built-in low pass filter (LPF) : (input side: analog LPF)
  : (output side: digital LPF)
- Power supply voltage: 2.7 V to 5.5 V
- Package:
  56-pin plastic QFP (QFP56-P-910-0.65-2K) (Product name: MSM9841GS-2K)

*note 32 kHz, 22.05 kHz and 44.1 kHz are available only for playback.

## BLOCK DIAGRAM



## PIN CONFIGURATION (TOP VIEW)




NC : No Connection

**56-pin plastic QFP**

## PIN DESCRIPTIONS

| Symbol | Type | Description |
|---|---|---|
| D15-D8 | I/O | For 8-bit bus interface, the command allows these pins to be configured to be inputs or outputs to input or output data to and from an external memory. Otherwise, these pins are configured to be inputs only.<br>For 16-bit interface, these pins are a bidirectional data bus to input or output data to and from an external microcontroller and memory. |
| D7-D0 | I/O | Birirectional data bus to input or output data and output status to and from an external microcontroller and memory. |
| $\overline{WR}$ | I | Write pulse input pin. This pin pulses "L" when command or voice data is input to D15-D0 pins. |
| $\overline{RD}$ | I | Read pulse input pin. This pin pulses "L" when status or voice data is output to D15-D0 pins. |
| $\overline{CS}$ | I | Accepts write pulse and read pulse when this pin is "L". Does not accept write pulse and read pulse when this pin is "H". |
| D/$\overline{C}$ | I | Voice data is input or output to and from D15-D0 pins when this pin is "H". Command is input to and status is output from D7-D0 pins when this pin is "L". |
| $\overline{BUSY}$ | O | This pin outputs a "L" level during RECORDING, PLAYBACK or PAUSE. |
| EMP | O | "H" level indicates that there is no data in FIFO memory. Active "H" can be changed to active "L" by command input. |
| MID | O | "H" level indicates that more than half of the FIFO memory space is filled with data.<br>During playback, voice synthesis starts when MID changes to "H" level. Active "H" can be changed to active "L" by command input. This pin outputs a synchro signal for voice data input/output when non-use of FIFO is selected. |
| FUL/DREQR | O | "H" level indicates that FIFO memory is full of data. During playback, this pin is "H" and data cannot be written in FIFO memory. Active "H" can be changed to active "L" by command input.<br>When DMA transfer and stereo playback are selected, "H" level DREQR outputs a signal to request a DMA transfer. Active "H" can be changed to active "L" by command input. |
| CH/DACKR | I | When stereo playback is selected and CH is "H", the EMP, MID or FUL pin outputs the status of right FIFO memory. When CH is "L", the EMP, MID or FUL pin outputs the status of left FIFO memory. Set this pin to "L" during recording and monophonic playback. When DMA transfer and stereo playback are selected, DACKR is selected. In this case, input a DMA transfer acknowledge signal to DACKR. When DACKR is "L", the $\overline{IOW}$ signal is accepted. Active "L" can be changed to active "H" by command input. |
| DREQL | O | When DMA transfer is selected, "H" level DREQL outputs a signal to request a DMA transfer.<br>When stereo playback is selected, "H" level DREQL outputs a signal to request a DMA transfer. Active "H" can be changed to active "L" by command input. |
| DACKL | I | Input to DACKL a signal when DMA transfer is permitted by the DMA controller. When DACKL is "L", $\overline{IOR}$ and $\overline{IOW}$ signals are accepted. When stereo playback is selected, input to DACKL a DMA transfer acknowledge signal for left FIFO memory. Active "L" can be changed to active "H" by command input. If DMA transfer is not used, set this pin to "H" level. |

## PIN DESCRIPTIONS

| Symbol | Type | Description |
|---|---|---|
| $\overline{IOW}$ | I | Write pulse input pin to write external memory data to MSM9841 during DMA transfer. If DMA transfer is not used, set this pin to "H" level. |
| $\overline{IOR}$ | I | Read pulse input pin to read data of MSM9841 during DMA transfer. If DMA transfer is not used, set this pin to "H" level. |
| ADSD | I | 16-bit serial data input pin when external ADC is used. If external ADC is not used, set this pin to "L" level. |
| DASD | O | 16-bit serial data output pin when external DAC is used. |
| SIOCK | O | Synchronizing clock for 16-bit serial data input/output when external ADC or DAC is used. |
| XT<br>$\overline{XT}$ | I<br>O | Oscillator connection pins. When external clock is used, input clock into XT pin and leave $\overline{XT}$ pin open. |
| VCK | O | Outputs sampling frequency selected at recording or playback. VCK pin is used as a synchronizing signal when external ADC or DAC is used. |
| $\overline{RESET}$ | I | When this pin is "L" level input, the LSI is initialized. |
| TEST0<br>TEST1 | I | Pins for testing. Set the pins to "L". |
| SG | O | Analog circuit signal ground output pin. |
| MIN<br>LIN | I | Inverting input pin for built-in OP amplifier. Noninverting input pin is connected to SG (Signal Ground) internally. |
| MOUT<br>LOUT | O | MOUT is the output of internal OP amplifier to MIN, and LOUT is to LIN. |
| AOUTL | O | Left analog output pin from built-in LPF. This is the output pin of playback wavefroms, and is connected to the amplifier for driving speakers. |
| AOUTR | O | Right analog output pin from built-in LPF. This is the output pin of playback wavefroms, and is connected to the amplifier for driving speakers. |
| $DV_{DD}$ | — | Digital power supply pin. Insert a minimum 0.1 μF bypass capacitor between this pin and DGND pin. |
| DGND | — | Digital GND pin. |
| $AV_{DD}$ | — | Analog power supply pin. Insert a minimum 0.1 μF bypass capacitor between this pin and AGND pin. |
| AGND | — | Analog GND pin. |

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Power Supply Voltage | $V_{DD}$ | Ta=25°C | –0.3 to +7.0 | V |
| Input Voltage | $V_{IN}$ | Ta=25°C | –0.3 to $V_{DD}$+0.3 | V |
| Storage Temperature | $T_{STG}$ | — | –55 to +155 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Condition | Range | | | Unit |
|---|---|---|---|---|---|---|
| Power Supply Voltage | $V_{DD}$ | DGND=AGND=0V | 2.7 to 5.5 | | | V |
| Operating Temperature | $T_{OP}$ | — | –40 to +85 | | | °C |
| Master Clock Frequency | $f_{OSC}$ | — | Min. | Typ. | Max. | MHz |
| | | | 4.0 | 4.096 | 6.0 | |

## ELECTRICAL CHARACTERISTICS

### DC Characteristics

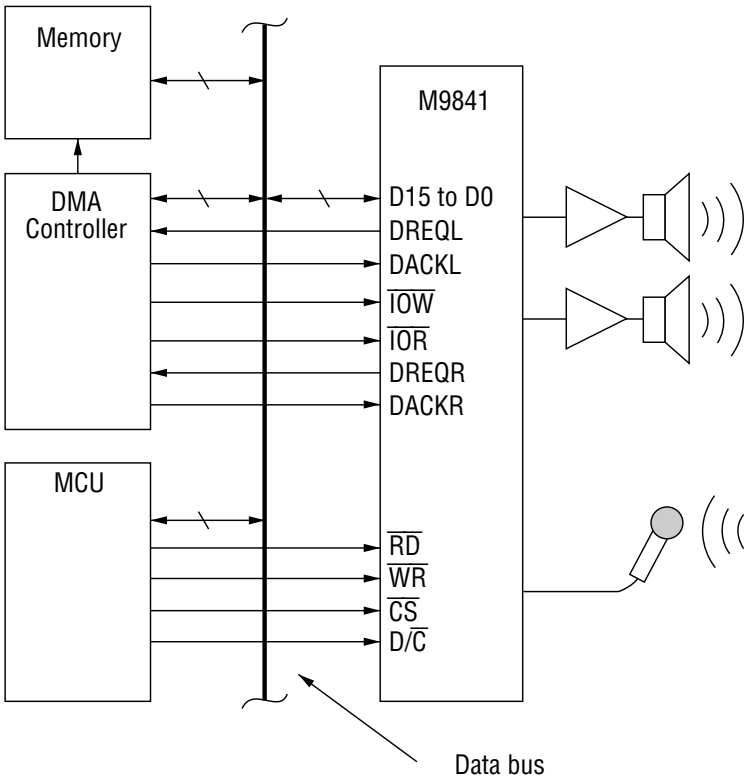
$DV_{DD}$=$AV_{DD}$=2.7 to 5.5V, DGND=AGND=0V, Ta=–40 to +85°C

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| High-level Input Voltage | $V_{IH}$ | — | $V_{DD}$×0.85 | — | — | V |
| Low-level Input Voltage | $V_{IL}$ | — | — | — | $V_{DD}$×0.2 | V |
| High-level output Voltage | $V_{OH}$ | $I_{OH}$=–40 µA | $V_{DD}$–0.3 | — | — | V |
| Low-level output Voltage | $V_{OL}$ | $I_{OL}$=2 mA | — | — | 0.45 | V |
| High-level Input Current (*1) | $I_{IH1}$ | $V_{IH}$=$V_{DD}$ | — | — | 10 | µA |
| High-level Input Current (*2) | $I_{IH2}$ | $V_{IH}$=$V_{DD}$ | — | — | 20 | µA |
| High-level Input Current (*3) | $I_{IH3}$ | $DV_{DD}$=$AV_{DD}$=4.5 to 5.5 V, $V_{IH}$=$V_{DD}$ | 30 | 150 | 300 | µA |
| | | $DV_{DD}$=$AV_{DD}$=2.7 to 3.6 V, $V_{IH}$=$V_{DD}$ | 10 | 50 | 100 | µA |
| Low-level Input Current (*1) | $I_{IL1}$ | $V_{IL}$=GND | –10 | — | — | µA |
| Low-level Input Current (*2) | $I_{IL2}$ | $V_{IL}$=GND | –20 | — | — | µA |
| Operating Current consumption | $I_{DD}$ | $DV_{DD}$=$AV_{DD}$=4.5 to 5.5 V, fosc=4.096 MHz, whithout load | — | 15 | 30 | mA |
| | | $DV_{DD}$=$AV_{DD}$=2.7 to 3.6 V, fosc=4.096 MHz, whithout load | — | 10 | 20 | mA |
| Stanby Current consumption | $I_{DDS}$ | At power down, without load Ta=–40 to +70°C | — | — | 10 | µA |
| | | At power down, without load Ta=–40 to +85°C | — | — | 50 | µA |

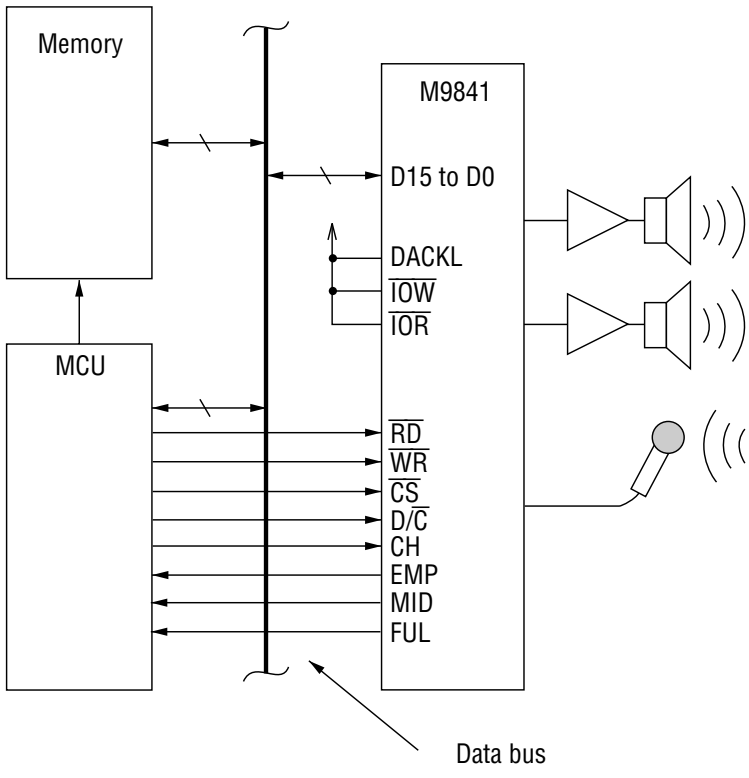
*1 Applicable to input pins excluding XT pin.
*2 Applicable to XT pin.
*3 Applicable to TEST0 pin and TEST1 pin.

## CPU INTERFACE EXAMPLES

1) Interface when DMA controler is used (16-bit bus)



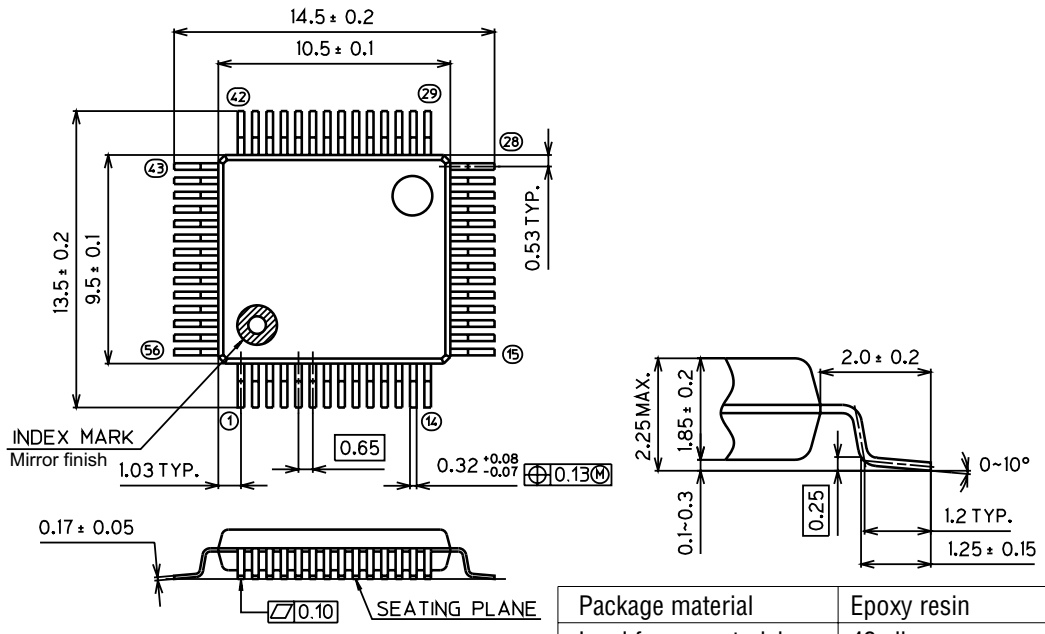

2) MCU & external memory interface (16-bit bus)



## PACKAGE DIMENSIONS

(Unit : mm)

QFP56-P-910-0.65-2K




| | |
|---|---|
| Package material | Epoxy resin |
| Lead frame material | 42 alloy |
| Pin treatment | Solder plating (≥5 μm) |
| Package weight (g) | 0.43 TYP. |
| Rev. No./Last Revised | 4/Nov. 28, 1996 |

**Oki Electric Industry Co., Ltd.**

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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