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**MSM9225B**

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**CAN (Controller Area Network) Controller**

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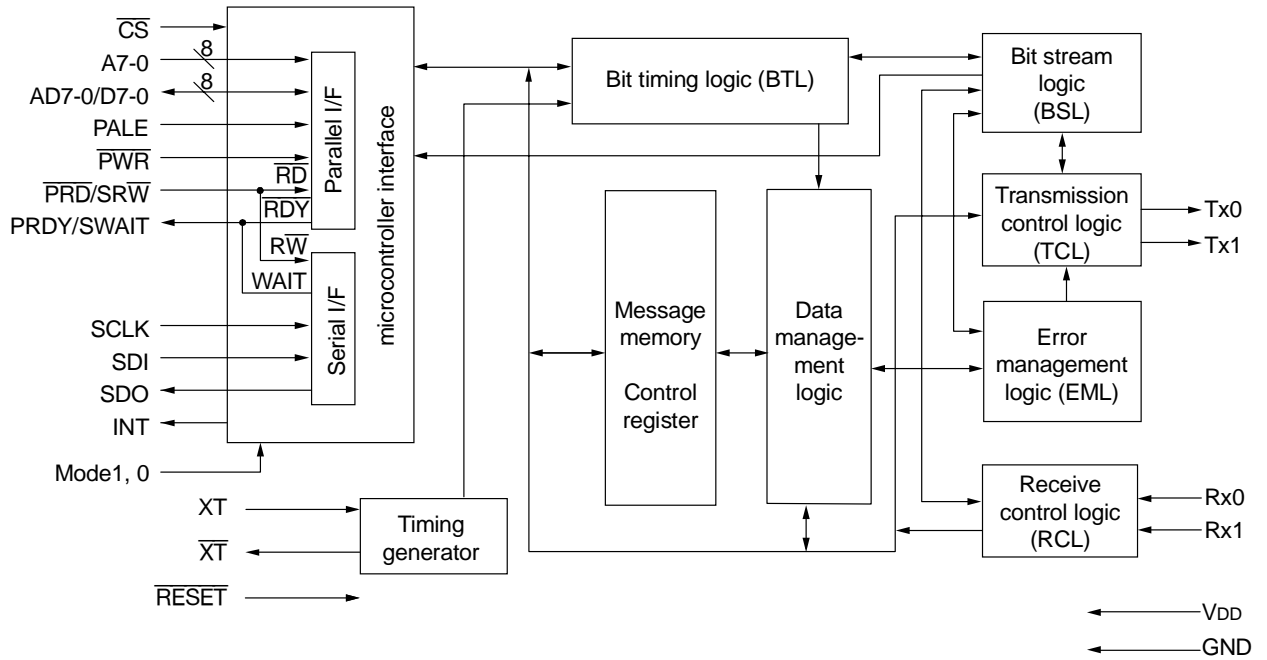
**GENERAL DESCRIPTION**

The MSM9225B is a microcontroller peripheral LSI which conforms to the CAN protocol for high-speed LANs in automobiles.

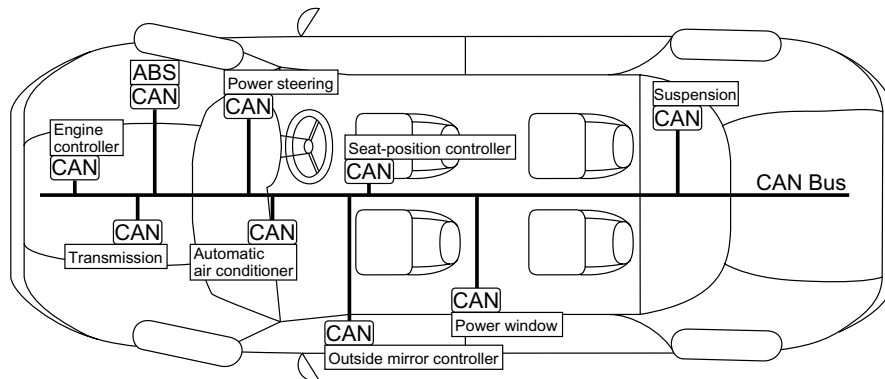
**FEATURES**

- Conforms to CAN protocol specification (Bosch, V2.0 part B/Active)
- Maximum of 1 Mbps bit rate
- Communication method:
  - Transmission line is bi-directional, two-wire serial communication
  - NRZ (Non-Return to Zero) system using bit stuff function
  - Multi-master system
  - Broadcast system
- Message boxes:
  - Up to 16 message boxes can be used, and messages up to 8 bytes long can be transmitted or received for each message box.
  - Number of received messages can be extended by group message function (up to 2 groups can be set)
  - Overwrite flag is provided
- Priority control by identifier
  - 2032 types in standard format,  $2032 \times 2^{18}$  types in extended format
- Microcontroller interface
  - Corresponding to both parallel and serial interface
    - Parallel interface: Separate address/data bus type (with address latch signal/no address latch signal) and multiplexed address/data bus type
    - Serial interface: Synchronous communication type
  - Three interrupt sources: Transmission/receive/error
- Error control:
  - Bit error/stuff error/CRC error/form error/acknowledgment error detection functions
  - Retransmission/error status monitoring function when error occurs
  - Bit error flag/stuff error flag/CRC error flag/form error flag/acknowledge error flag are provided
- Communication control by remote data request function
- Sleep/Stop mode function
- Supply voltage:  $5\text{ V} \pm 10\%$
- Operating temperature:  $-40$  to  $+125^\circ\text{C}$
- Package: 44-pin plastic QFP (QFP44-P-910-0.80-2K) (Product name: MSM9225BGA-2K)

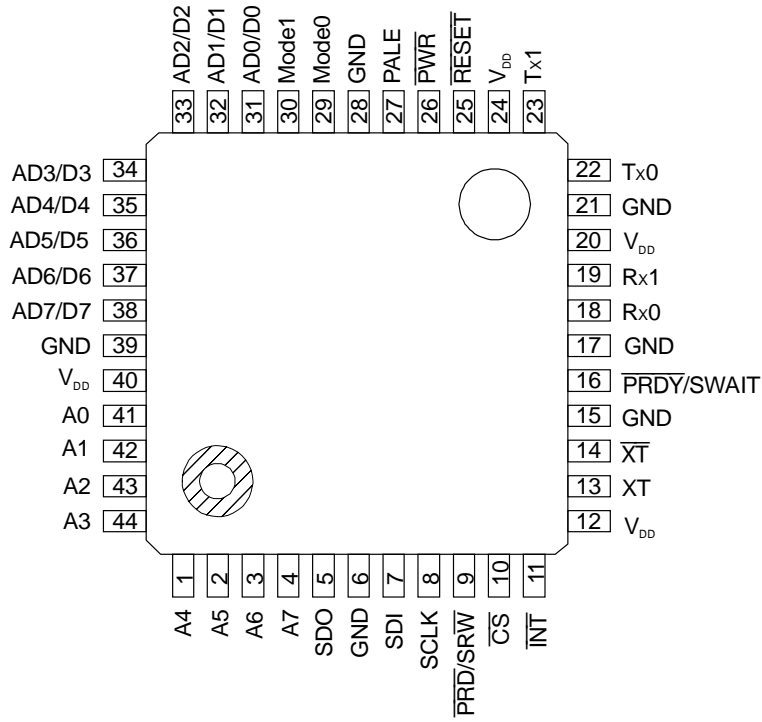
**BLOCK DIAGRAM**



**CONFIGURATION EXAMPLE**



**PIN CONFIGURATION**



**44-Pin Plastic QFP (Top View)**

## PIN DESCRIPTIONS

Symbol	Pin	Type	Description									
$\overline{CS}$	10	I	Chip select pin. When "L", PALE, $\overline{PWR}$ , $\overline{PRD/SRW}$ , SCLK and SDO pins (microcontroller interface pins) are valid. When "H", these pins are invalid.									
A7-0	41-44, 1-4	I	Address bus pins (when using separate buses). If used with a multiplexed bus or if used in the serial mode, fix these pins at "H" or "L" levels.									
AD7-0/ D7-0	31-38	I/O	Multiplexed bus: Address/data pins (AD7-0) Separate buses: Data pins (D7-0) If used in the serial mode, fix these pins at a "L" levels.									
$\overline{PWR}$	26	I	Write input pin if used in the parallel mode. Data is captured when this pin is at a "L" level. If used in the serial mode, fix this pin at a "L" level.									
$\overline{PRD}/$ $SRW$	9	I	Parallel mode: Read signal pin ( $\overline{PRD}$ ) When at a "L" level, data is output from the data pins. Serial mode: Read/write signal pin (SRW) When at a "H" level, data is output from the SDO pin. When at a "L" level, the SDO pin is at high impedance, and data is captured beginning with the second byte of data input from the SDI pin.									
PALE	27	I	Address latch signal pin When at a "H" level, addresses are captured. If used in the parallel mode and the address latch signal is unnecessary or in the serial mode, fix this pin at a "H" or "L" level.									
SDI	7	I	Serial data input pin Addresses (1st byte) and data (beginning from the 2nd byte) are input to this pin, LSB first. If used in the parallel mode, fix this pin at a "H" or "L" level.									
SDO	5	O	Serial data output pin When the $\overline{CS}$ pin is at a "H" level, this pin is at high impedance. When $\overline{CS}$ is at a "L" level, data is output from this pin, LSB first. If used in the parallel mode, fix this pin at a "H" or "L" level.									
SCLK	8	I	Shift clock input pin for serial data At the rising edge of the shift clock, SDI pin data is captured. At the falling edge, data is output from the SDO pin.									
$\overline{PRDY}/$ SWAIT	16	O	Ready output pin When required by the MSM9225B, a signal may be output to extend the bus cycle until the internal access is completed. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th></th> <th>Internal access in progress</th> <th>After completion of access</th> </tr> </thead> <tbody> <tr> <td>Parallel mode (<math>\overline{PRDY}</math>)</td> <td>"L" level output</td> <td>High impedance output</td> </tr> <tr> <td>Serial mode (SWAIT)</td> <td>"H" level output</td> <td>"L" level output</td> </tr> </tbody> </table>		Internal access in progress	After completion of access	Parallel mode ( $\overline{PRDY}$ )	"L" level output	High impedance output	Serial mode (SWAIT)	"H" level output	"L" level output
	Internal access in progress	After completion of access										
Parallel mode ( $\overline{PRDY}$ )	"L" level output	High impedance output										
Serial mode (SWAIT)	"H" level output	"L" level output										

Symbol	Pin	Type	Description																		
Mode1, 0	29, 30	I	Microcontroller interface select pins																		
			<table border="1"> <thead> <tr> <th>Mode1</th> <th>Mode0</th> <th colspan="2">Interface</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td rowspan="2">Parallel mode</td> <td>Separate buses</td> </tr> <tr> <td>0</td> <td>1</td> <td>No address latch signal</td> </tr> <tr> <td>1</td> <td>0</td> <td rowspan="2">Serial mode</td> <td>With address latch signal</td> </tr> <tr> <td>1</td> <td>1</td> <td>Multiplexed buses</td> </tr> </tbody> </table>	Mode1	Mode0	Interface		0	0	Parallel mode	Separate buses	0	1	No address latch signal	1	0	Serial mode	With address latch signal	1	1	Multiplexed buses
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$\overline{\text{INT}}$	11	O	Interrupt request output pin When an interrupt request occurs, a "L" level is output. This pin automatically outputs a "H" level after 32 Ts (T = 1/fosc). Three types of interrupts share this pin: transmission complete, reception complete, and error.																		
$\overline{\text{RESET}}$	25	I	Reset pin System is reset when this pin is at a "L" level.																		
XT	13	I	Clock pins. If internal oscillator is used, connect a crystal (ceramic resonator).																		
$\overline{\text{XT}}$	14	O	If external clock is used, input clock via XT pin. The $\overline{\text{XT}}$ pin should be left open.																		
Rx0, Rx1	18, 19	I	Receive input pin. Differential amplifier included.																		
Tx0, Tx1	22, 23	O	Transmission output pin																		
V <sub>DD</sub>	12, 20, 24, 40	—	Power supply pin																		
GND	6, 15, 17, 21, 28, 39	—	GND pin																		

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	$V_{DD}$	$T_a = 25^\circ\text{C}$	-0.3 to +7.0	V
Input Voltage	$V_I$	—	-0.3 to $V_{DD} + 3.0$	V
Output Voltage	$V_O$	—	-0.3 to $V_{DD} + 3.0$	V
Power Dissipation	$P_D$	$T_a \leq 25^\circ\text{C}$	615	mW
Operating Temperature	$T_{OP}$	—	-40 to +125	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	—	-65 to +150	$^\circ\text{C}$

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	$V_{DD}$	$V_{DD} = AV_{DD}$	4.5	5.0	5.5	V
Operating Temperature	$T_{OP}$	—	-40	+25	+125	$^\circ\text{C}$

## ELECTRICAL CHARACTERISTICS

## DC Characteristics

 $(V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, T_a = -40 \text{ to } +125^\circ\text{C})$ 

Parameter	Symbol	Applicable pin	Condition	Min.	Max.	Unit
"H" Input Voltage	$V_{IH}$	Applies to all inputs	—	$0.8V_{DD}$	$V_{DD} + 0.3$	V
"L" Input Voltage	$V_{IL}$	Applies to all inputs	—	-0.3	$+0.2 V_{DD}$	V
"H" Input Current	$I_{IH1}$	XT	$V_I = V_{DD}$	3	25	$\mu\text{A}$
	$I_{IH2}$	Other inputs		-1.0	+1.0	$\mu\text{A}$
"L" Input Current	$I_{IL1}$	XT	$V_I = 0\text{V}$	-25	-3	$\mu\text{A}$
	$I_{IL2}$	Other input		-1.0	+1.0	$\mu\text{A}$
"H" Output Voltage	$V_{OH1}$	$\overline{\text{INT}}$ , $\overline{\text{PRDY/SWAIT}}$	$I_{OH1} = -80 \mu\text{A}$	$V_{DD} - 1.0$	—	V
	$V_{OH2}$	AD7-0/D7-0	$I_{OH2} = -400 \mu\text{A}$	$V_{DD} - 1.0$	—	V
"L" Output Voltage	$V_{OL1}$	$\overline{\text{INT}}$ , $\overline{\text{PRDY/SWAIT}}$	$I_{OL1} = 1.6 \text{ mA}$	—	0.4	V
	$V_{OL2}$	AD7-0/D7-0	$I_{OL2} = 3.2 \text{ mA}$	—	0.4	V
Output Leakage Current	$I_{IH1}$	$\overline{\text{PRDY/SWAIT}}$ AD7-0/D7-0	$V_I = V_{DD}/0 \text{ V}$	-1.0	+1.0	$\mu\text{A}$
Dynamic Supply Current	$I_{DD}$	—	$f_{\text{OSC}} = 16 \text{ MHz}$ , No Load	—	9	mA
Static Supply Current	$I_{DDs}$	—	SLEEP Mode	—	400	$\mu\text{A}$
		—	STOP Mode	—	100	$\mu\text{A}$

## Rx0, Rx1 Characteristics

Differential input mode

 $(V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, T_a = -40 \text{ to } +125^\circ\text{C})$ 

Parameter	Symbol	Applicable pin	Condition	Min.	Max.	Unit
'dominant' Input Voltage	$VR_{x0} (d)$	Rx0	$VR_{x1} = 0.4 V_{DD}$ to $0.6 V_{DD}$	-0.3	$VR_{x1} - 0.4$	V
'recessive' Input Voltage	$VR_{x0} (r)$	Rx0		$VR_{x1} + 0.4$	$V_{DD} + 3$	V
Input Leakage Current	$I_{LK}$	Rx0, Rx1	$VR_{x1} = V_{DD}/0 \text{ V}$	-1	+1	$\mu\text{A}$

## Tx0, Tx1 Characteristics

 $(V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, T_a = -40 \text{ to } +125^\circ\text{C})$ 

Parameter	Symbol	Condition	Min.	Max.	Unit
"H" Output Voltage	$V_{OH}$	$I_{OH} = -3.0 \text{ mA}$	$V_{DD} - 0.4$	—	V
"L" Output Voltage	$V_{OL}$	$I_{OL} = 10.0 \text{ mA}$	—	0.4	V

## AC Characteristics

Parallel mode

 $(V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, T_a = -40 \text{ to } +125^\circ\text{C}, f_{OSC} = 16 \text{ MHz})$ 

Parameter	Symbol	Condition	Min.	Max.	Unit
ALE Address Setup Time	$t_{AS}$	—	10	—	ns
ALE Address Hold Time	$t_{AH}$	—	10	—	ns
PRD Output Data Delay Time	$t_{RDLY}$	—	—	$60^{*1}$	ns
PRD Output Data Hold Time	$t_{RDH}$	—	5	—	ns
ALE "H" Level Width	$t_{WALFH}$	—	16.5	—	ns
Access Cycle	$t_{cyc}$	—	4T	—	ns
			7T	—	ns
Address Hold Time from PRD	$t_{RAH}$	—	0	—	ns
ALE Delay Time from PRD	$t_{HRA}$	—	27	—	ns
PRD "H" Level Width	$t_{WRDH}$	—	27	—	ns
PRDY "L" Delay Time	$t_{ARLDLY}$	—	—	35	ns
PRDY "L" Level Width	$t_{WRDYL}$	—	0	2.5T	ns
Data Output Delay Time from PRDY	$t_{ARDDLY}$	—	—	35	ns
PWR Hold Time from PRDY	$t_{ARWDLY}$	—	10	—	ns
Input Data Setup Time	$t_{WDS}$	—	30	—	ns
Input Data Hold Time	$t_{WDH}$	—	4	—	ns
PRD Delay Time	$t_{RS}$	—	10	—	ns
PWR Delay Time	$t_{WS}$	—	10	—	ns
Address Hold Time from PWR	$t_{WAH}$	—	10	—	ns
ALE Delay Time from PWR	$t_{HWA}$	—	27	—	ns
PWR "H" Level Width	$t_{WRH}$	—	40	—	ns
PWR "L" Level Width	$t_{WRL}$	—	$20^{*1}$	—	ns
CS Delay Time from PRD	$t_{HRC}$	—	0	—	ns
CS Delay Time from PWR	$t_{HWC}$	—	0	—	ns

 $T = 1/f_{OSC}$ 

The values with \*1 indicate those when  $\overline{\text{PRDY}}$  is not generated.

The values with \*1 when  $\overline{\text{PRDY}}$  is generated are defined by "Data Output Delay Time from  $\overline{\text{PRDY}}$ "  $t_{ARDDLY}$  and "PWR Hold Time from  $\overline{\text{PRDY}}$ "  $t_{ARWDLY}$ .



## Serial mode

(V<sub>DD</sub> = 4.5 to 5.5 V, Ta = -40 to +125°C, f<sub>OSC</sub> = 16 MHz)

Parameter	Symbol	Condition	Min.	Max.	Unit
$\overline{\text{CS}}$ Setup Time	t <sub>CS</sub>	—	10	—	ns
$\overline{\text{CS}}$ Hold Time	t <sub>CH</sub>	—	8T	—	ns
SCLK Cycle	t <sub>CP</sub>	—	167	—	ns
SCLK Pulse Width	t <sub>CW</sub>	—	83	—	ns
SDI Setup Time	t <sub>DS</sub>	—	30	—	ns
SDI Hold Time	t <sub>DH</sub>	—	5	—	ns
SDO Output Enable Time	t <sub>CSODLY</sub>	—	—	30	ns
SDO Output Disable Time	t <sub>CSZDLY</sub>	—	—	30	ns
SDO Output Delay Time	t <sub>PD</sub>	—	—	30	ns
SR $\overline{\text{W}}$ Setup Time	t <sub>RS</sub>	—	10	—	ns
SR $\overline{\text{W}}$ Hold Time	t <sub>RH</sub>	—	0	—	ns
SWAIT Output Delay Time	t <sub>SRDLY</sub>	—	—	2T	ns
SWAIT "H" Level Width	t <sub>WRDY</sub>	—	—	6T	ns
Byte Delay	t <sub>WAIT</sub>	—	8T	—	ns

T = 1/f<sub>OSC</sub>

## Other timing characteristics

(V<sub>DD</sub> = 4.5 to 5.5 V, Ta = -40 to +125°C)

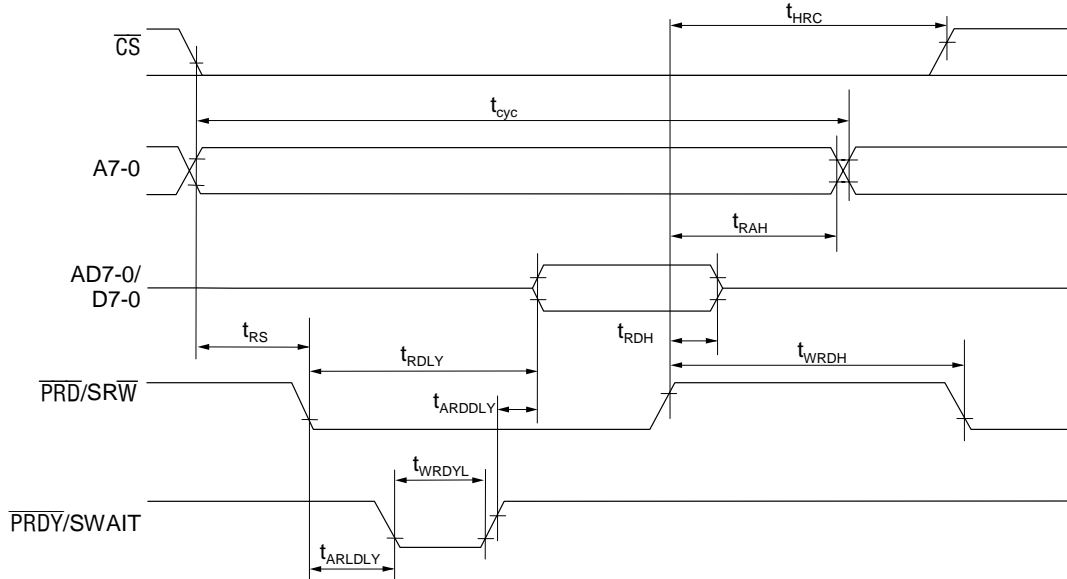
Parameter	Symbol	Condition	Min.	Max.	Unit
System Clock Cycle	t <sub>clkcy</sub>	—	62	—	ns
$\overline{\text{RESET}}$ "H" Level Input Width	t <sub>WRSTH</sub>	—	5	—	μs
$\overline{\text{RESET}}$ "L" Level Input Width	t <sub>WRSTL</sub>	—	5	—	μs
$\overline{\text{INT}}$ "L" Level Output Width	t <sub>WINTL</sub>	—	32T	—	ns

T = 1/f<sub>OSC</sub>

**TIMING DIAGRAMS**

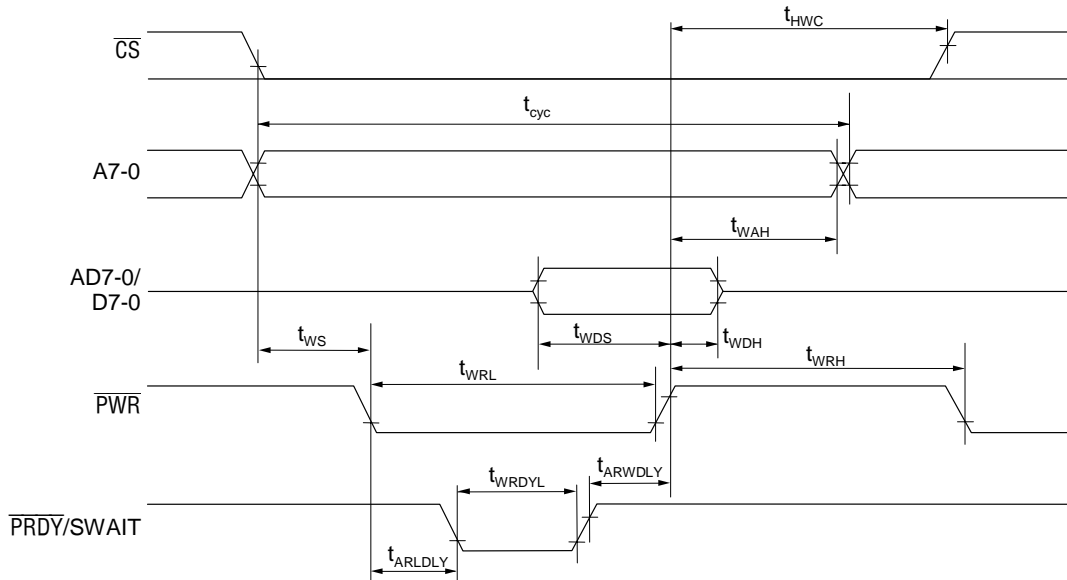
**Separate Bus Mode**

Read access timing



Note: The  $\overline{PRDY}$  signal may be output depending on the internal state of the MSM9225B.

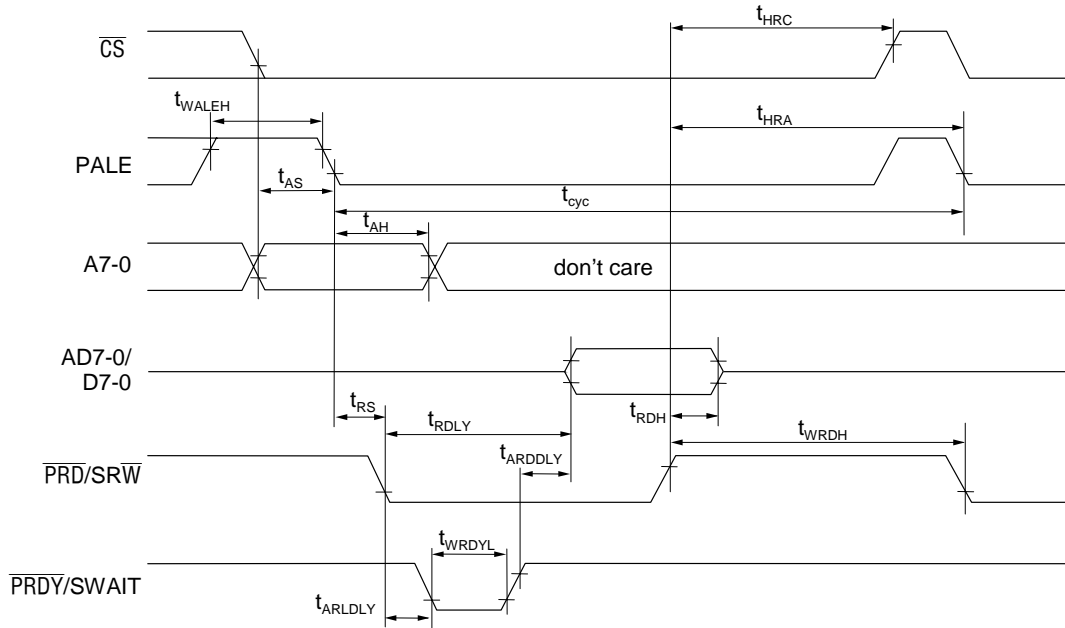
Write access timing



Note: The  $\overline{PRDY}$  signal may be output depending on the internal state of the MSM9225B.

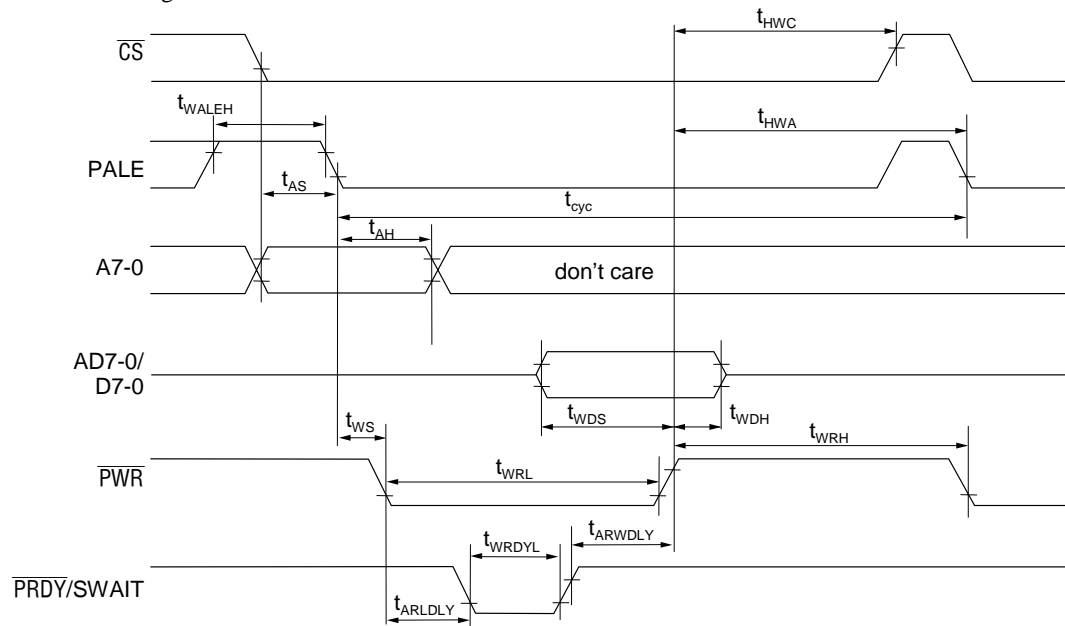
**Separate Bus/Address Latch Mode**

Read access timing



Note: The  $\overline{PRDY}$  signal may be output depending on the internal state of the MSM9225B.

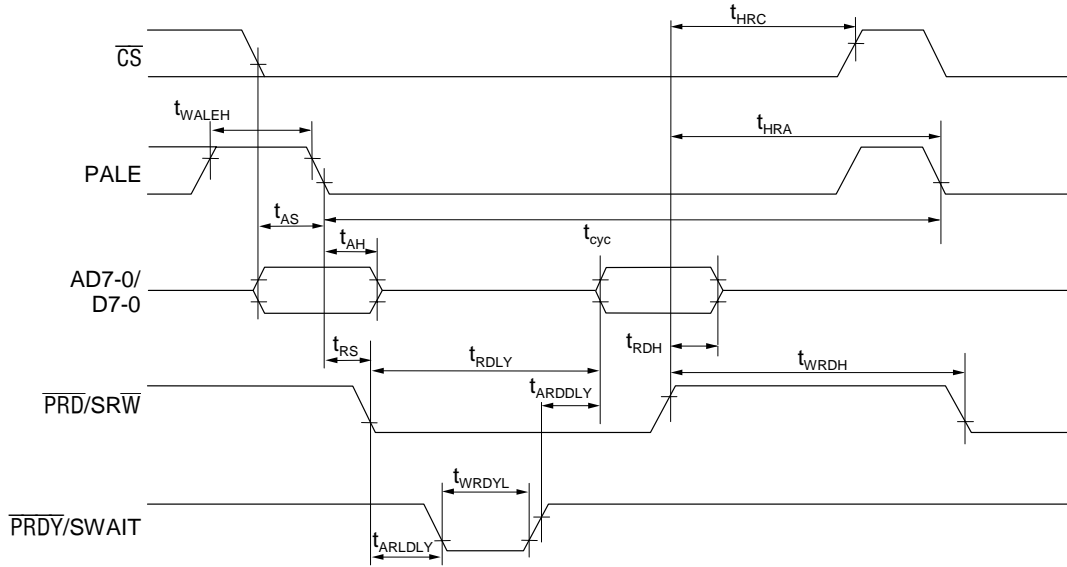
Write access timing



Note: The  $\overline{PRDY}$  signal may be output depending on the internal state of the MSM9225B.

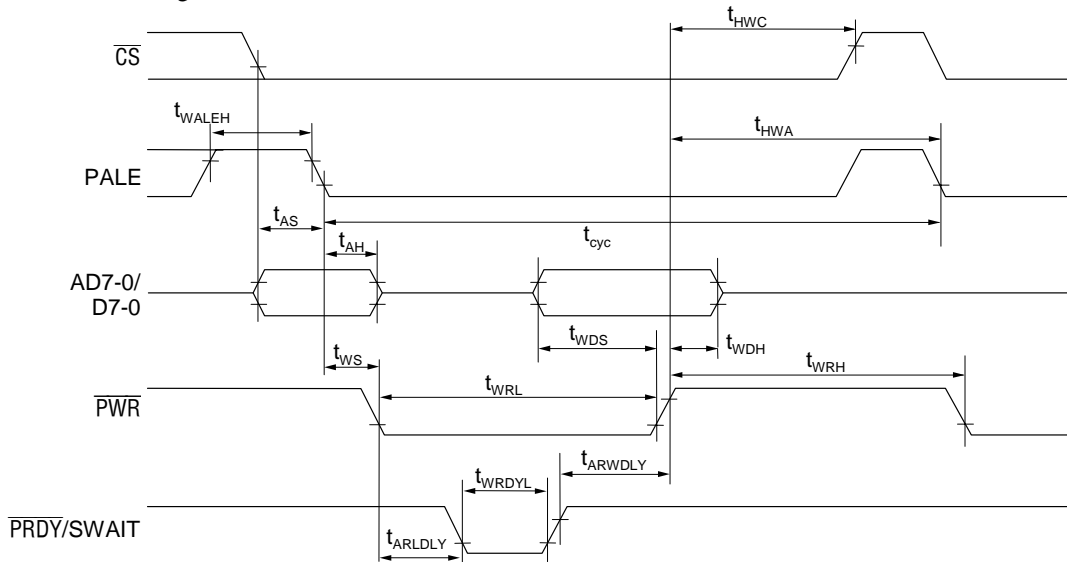
**Multiplexed Bus Mode**

Read access timing



Note: The  $\overline{PRDY}$  signal may be output depending on the internal state of the MSM9225B.

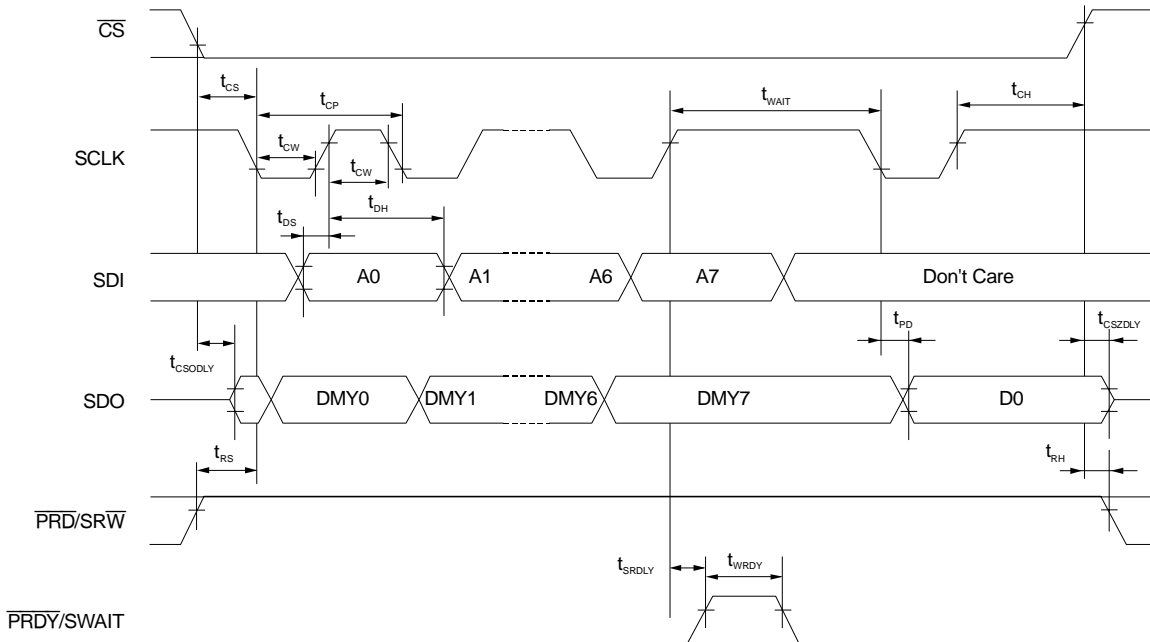
Write access timing



Note: The  $\overline{PRDY}$  signal may be output depending on the internal state of the MSM9225B.

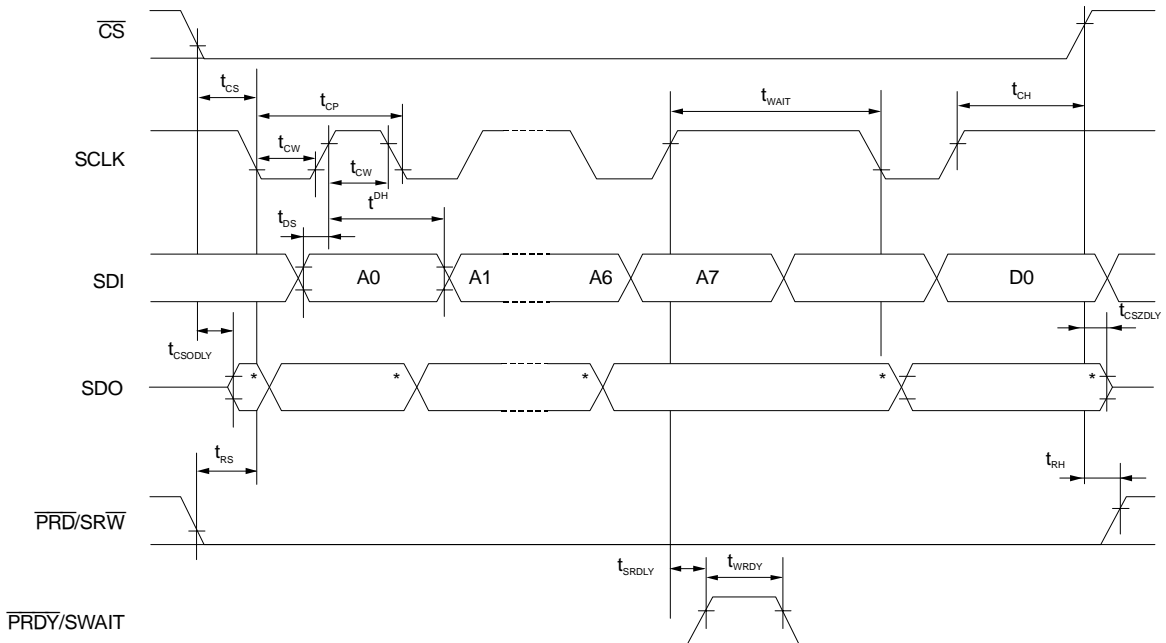
**Serial Mode**

Read access timing



Note: The SWAIT signal will be output during the interval between address and data transfers.

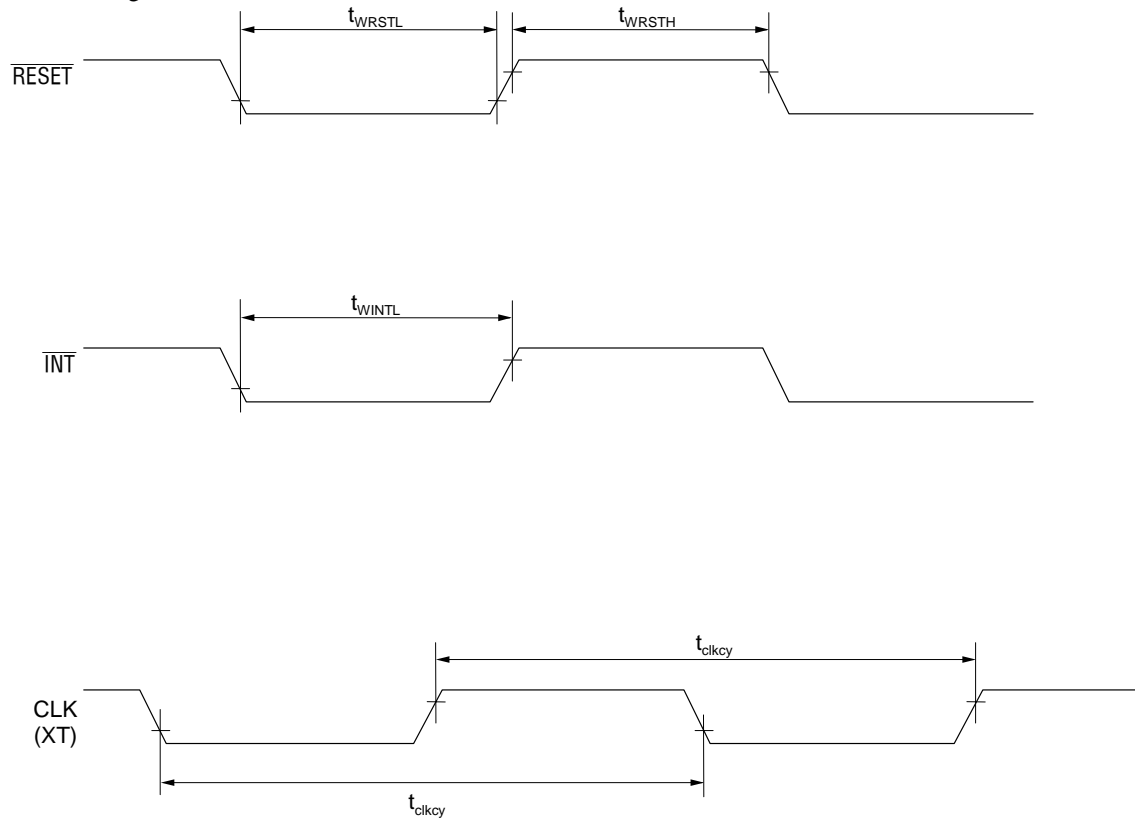
Write access timing



Note: The SWAIT signal will be output during the interval between address and data transfers.

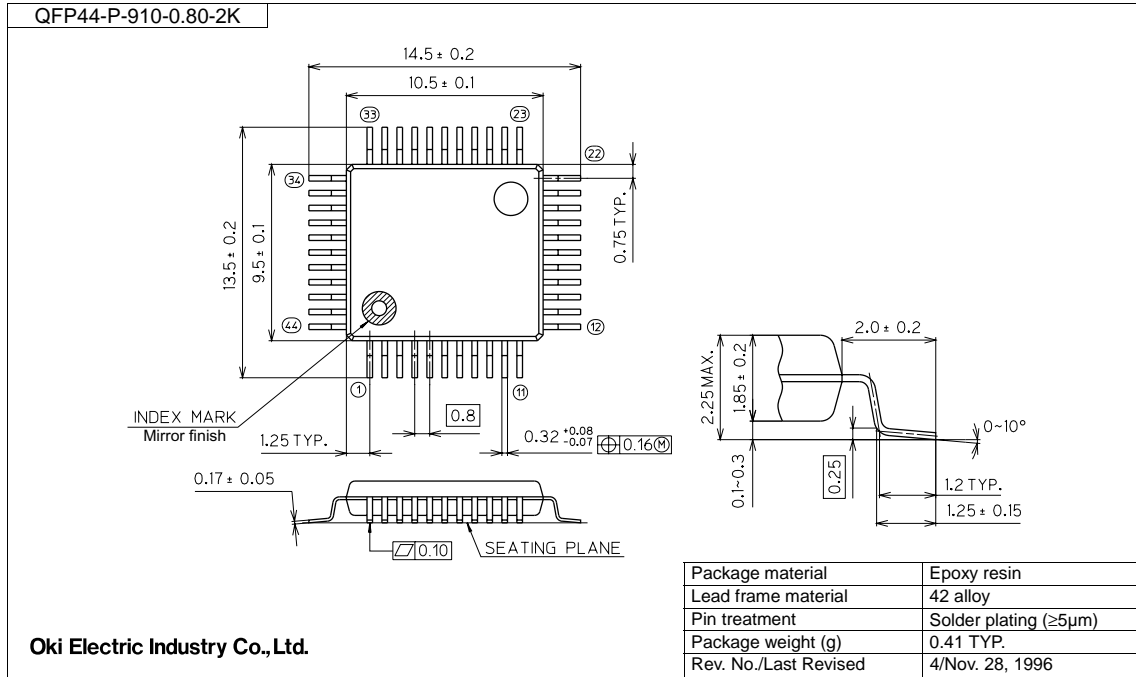
\* : don't care

## Other Timing



**PACKAGE DIMENSIONS**

(Unit: mm)



**Notes for Mounting the Surface Mount Type Package**

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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