FEDL7224-001FULL-01
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OKI Semiconductor

ML7224-001TC

4ch VoIP CODEC

GENERAL DESCRIPTION

The ML7224-001 is a VoIP codec that has speech codecs with four channels. These speech codecs support the PLC (Packet Loss Concealment) function, with the coding format selectable between G.711 (μ-law) and G.711 (A-law). The ML7224-001 is equipped with an echo canceller that supports a delay of 32 ms for each channel; it also has functions such as FSK generation, DTMF detection/generation, and tone detection/generation. The ML7224-001 is an LSI device best suited to add multichannel VoIP capability to a TA, router and others.
Note that because this LSI device employs the method of downloading the DSP firmware from outside of the LSI to a built-in memory, it is capable of supporting functional expansion by changing the DSP firmware.

FEATURES

- Speech codecs (with 4 channels):
  - Selectable between ITU-T G.711 (64 kbps) μ-law and A-law
  - Supports ITU-T G.711 Appendix I compliant PLC (Packet Loss Concealment) function
- Interface for transferring speech CODEC transmit/receive data:
  - Selectable between FIFO buffer interface and PCM interface[*1]
- FIFO buffer interface:
  - Number of interfaces : 2 (one for CH0a/CH1a and the other for CH0b/CH1b)
  - FIFO buffer size : CH0a/CH1a: 640 bytes, CH0b/CH1b: 640 bytes
  - Frame/DMA (slave) interface can be selected
- PCM interface
  - Number of interfaces : 2 (one for CH0a/CH1a and the other for CH0b/CH1b)
  - Serial transmission rate : 128 kHz to 2.048 MHz (fixed at 2.048 MHz during output)
  - 1-time-slot bit width : Fixed to 16 bits
  - Time slot assignment : A maximum of 16 slots can be assigned (when BCLK = 2.048 MHz)
  - Input time slot selection : Arbitrary 4 slots maximum can be selected (for each block)
  - Output time slot selection : Arbitrary 2 slots maximum can be selected (for each block)
- Front-end interface
  - Selectable between analog interface and PCM interface[*1]

(Note) When a PCM interface is selected, data is input or output by multiplexing time slots on the PCM interface above. ITU-T G.711 (64 kbps) μ-law or A-law can be selected as the coding format for this purpose.

- Analog interface[*1]
  - Number of interfaces : 4 with one input amplifier and one output amplifier incorporated for each channel (10 kΩ driving)
- Echo canceller for 32 ms delay (One block installed per channel.)
- DTMF detection function (One block installed per channel.)
- DTMF generation function (One block installed per channel[*2]. The DTMF signal can be generated by the tone generation function.)
- 2100 Hz single tone/phase inversion detection function (Two blocks installed per channel[*3].)
- Tone detection function (400Hz. Detecting frequency can be changed. Two blocks installed per channel[*3].)
- Tone generation function (One block installed per channel[*2].)
- FSK generation function (One block installed per channel[*2].)
- Meody generation function (One block installed for every two channels[*4].)
- Dial pulse detection function (One block installed per channel.): Secondary function of a general-purpose input/output port

- Dial pulse transmission function (One block installed per channel[*2].): Secondary function of a general-purpose input/output port
- 16-bit timer (One block installed for every two channels.)
- Equipped with an interface for serial control
- Allows downloading of DSP firmware
- General-purpose input/output port:
  28 ports (some of them have a secondary function)
- Power supply voltage:
  Digital power supply voltage (DVDD0, 1, 2, 3, 4, 5, 6) : 3.0 to 3.6V
  Analog power supply voltage (AVDD0,1) : 3.0 to 3.6V
- Master clock frequency:
  12.288 MHz (crystal resonator/external input)
- Power down control by hardware or software
- Package:
  176-pin plastic LQFP (LQFP176-P-2424-0.50-ZK)

*1:
Selecting an analog interface is prohibited in the ML7224-001. Also, selecting a PCM interface as a speech codec interface is not supported.

*2:
Only one of the FSK generation function, tone generation function (DTMF generation function) and dial pulse transmission function can be used at a time per channel. Note that using more than one generation function at the same time is not used.

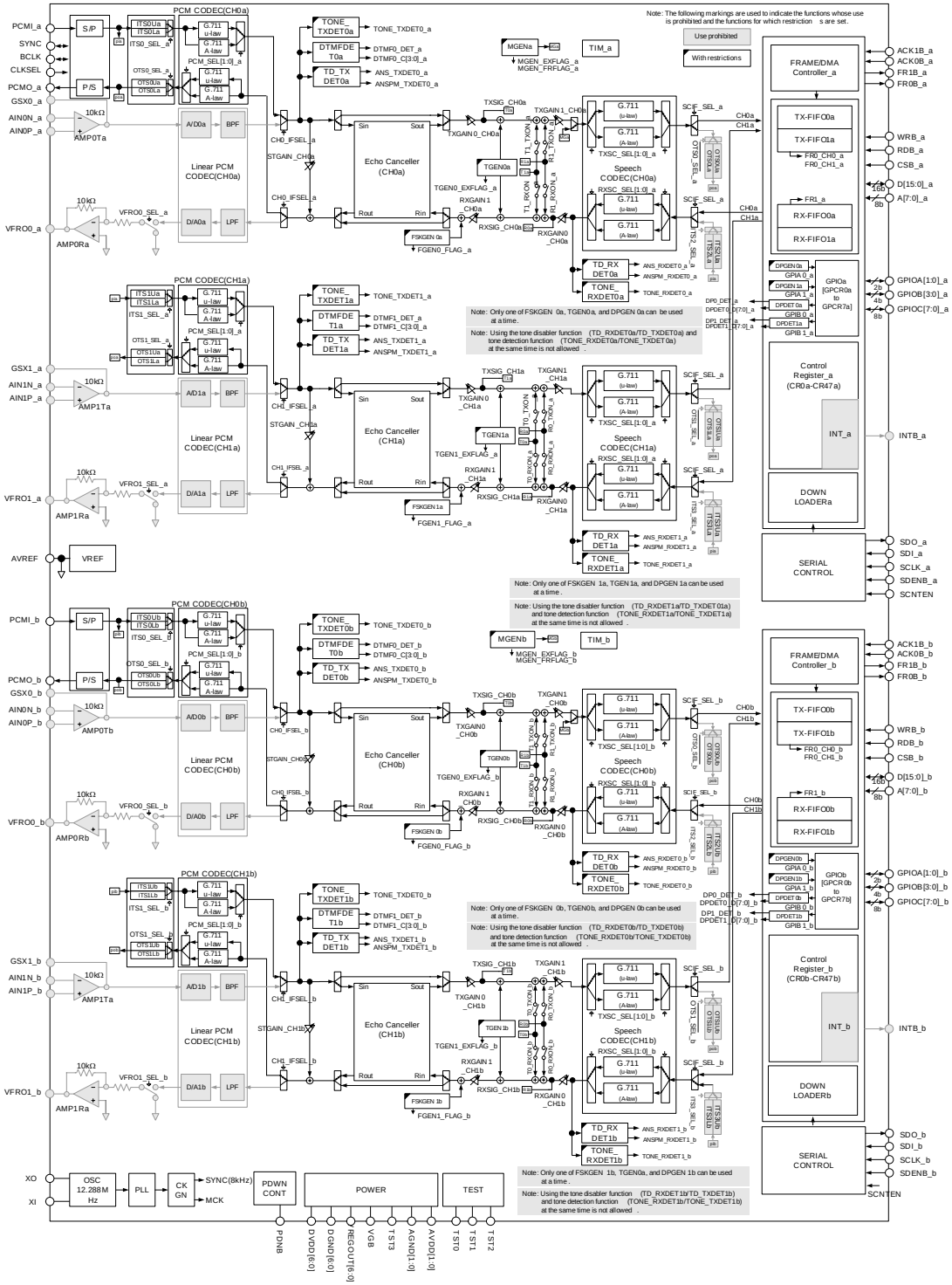
*3:
Using the 2100 Hz single tone /phase inversion detection function and the tone detection function for each channel at the same time is not allowed.

*4:
If the melody generation function is used, stop all the functions described below on the DSP side that generates melodies.
In addition, when starting a speech codec, do not start it on the channel 1 side (SC_CH1EN = 1).

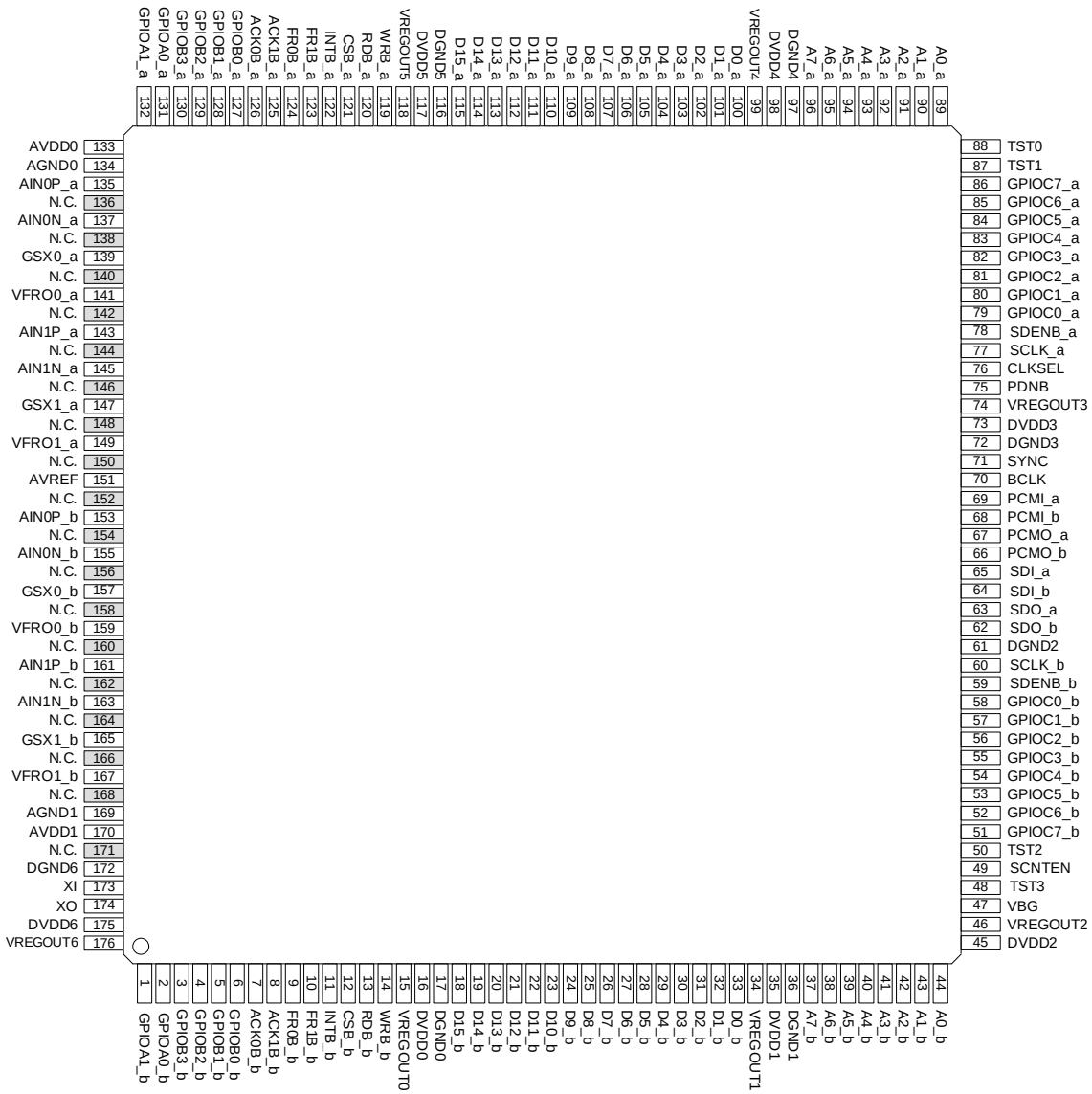
- Tone generation function (TGEN0/TGEN1)
- Tone detection function (TONE_RXDET0/TONE_TXDET0, TONE_RXDET1/TONE_TXDET1)
- FSK generation function (FSKGEN0/FSKGEN1)
- Tone disabler detection function (TD_RXDET0/TD_TXDET0, TD_RXDET1/TD_TXDET1)
- DTMF detection function (DTMF_DET0/DTMF_DET1)
- Echo canceller (EC0/EC1)
- Dial pulse detection function (DPDET0/DPDET1)
- Dial pulse transmission function (DPGEN0/DPGEN1)
- Timer (TIMER)

(Additional note)
This LSI incorporates two DSPs. One DSP performs processing for two channels.
This document distinguishes these two DSPs as the DSP_A side and the DSP_B side, and _a or _b is affixed to the names of related pins, control registers and others.

BLOCK DIAGRAM



PIN ASSIGNMENT (TOP VIEW)



176-Pin Plastic LQFP

PIN DESCRIPTIONS

MCU Interface

Pin No.	Symbol	I/O	When PDNB = "0"	Description
100	D0_a	I/O	I	Data input/output for CH0a/CH1a
101	D1_a	I/O	I	Data input/output for CH0a/CH1a
102	D2_a	I/O	I	Data input/output for CH0a/CH1a
103	D3_a	I/O	I	Data input/output for CH0a/CH1a
104	D4_a	I/O	I	Data input/output for CH0a/CH1a
105	D5_a	I/O	I	Data input/output for CH0a/CH1a
106	D6_a	I/O	I	Data input/output for CH0a/CH1a
107	D7_a	I/O	I	Data input/output for CH0a/CH1a
108	D8_a	I/O	I	Data input/output for CH0a/CH1a. Fix the input level when using in 8-bit bus access (BW_SELa = "1").
109	D9_a	I/O	I	Data input/output for CH0a/CH1a. Fix the input level when using in 8-bit bus access (BW_SELa = "1").
110	D10_a	I/O	I	Data input/output for CH0a/CH1a. Fix the input level when using in 8-bit bus access (BW_SELa = "1").
111	D11_a	I/O	I	Data input/output for CH0a/CH1a. Fix the input level when using in 8-bit bus access (BW_SELa = "1").
112	D12_a	I/O	I	Data input/output for CH0a/CH1a. Fix the input level when using in 8-bit bus access (BW_SELa = "1").
113	D13_a	I/O	I	Data input/output for CH0a/CH1a. Fix the input level when using in 8-bit bus access (BW_SELa = "1").
114	D14_a	I/O	I	Data input/output for CH0a/CH1a. Fix the input level when using in 8-bit bus access (BW_SELa = "1").
115	D15_a	I/O	I	Data input/output for CH0a/CH1a. Fix the input level when using in 8-bit bus access (BW_SELa = "1").
89	A0_a	I	I	Address input for CH0a/CH1a
90	A1_a	I	I	Address input for CH0a/CH1a
91	A2_a	I	I	Address input for CH0a/CH1a
92	A3_a	I	I	Address input for CH0a/CH1a
93	A4_a	I	I	Address input for CH0a/CH1a
94	A5_a	I	I	Address input for CH0a/CH1a
95	A6_a	I	I	Address input for CH0a/CH1a
96	A7_a	I	I	Address input for CH0a/CH1a
121	CSB_a	I	I	Chip select input for CH0a/CH1a
120	RDB_a	I	I	Read enable input for CH0a/CH1a
119	WRB_a	I	I	Write enable input for CH0a/CH1a

MCU Interface (continued)

Pin No.	Symbol	I/O	When PDNB = "0"	Description
33	D0_b	I/O	I	Data input/output for CH0b/CH1b
32	D1_b	I/O	I	Data input/output for CH0b/CH1b
31	D2_b	I/O	I	Data input/output for CH0b/CH1b
30	D3_b	I/O	I	Data input/output for CH0b/CH1b
29	D4_b	I/O	I	Data input/output for CH0b/CH1b
28	D5_b	I/O	I	Data input/output for CH0b/CH1b
27	D6_b	I/O	I	Data input/output for CH0b/CH1b
26	D7_b	I/O	I	Data input/output for CH0b/CH1b
25	D8_b	I/O	I	Data input/output for CH0b/CH1b. Fix the input level when using in 8-bit bus access (BW_SELb = "1").
24	D9_b	I/O	I	Data input/output for CH0b/CH1b. Fix the input level when using in 8-bit bus access (BW_SELb = "1").
23	D10_b	I/O	I	Data input/output for CH0b/CH1b. Fix the input level when using in 8-bit bus access (BW_SELb = "1").
22	D11_b	I/O	I	Data input/output for CH0b/CH1b. Fix the input level when using in 8-bit bus access (BW_SELb = "1").
21	D12_b	I/O	I	Data input/output for CH0b/CH1b. Fix the input level when using in 8-bit bus access (BW_SELb = "1").
20	D13_b	I/O	I	Data input/output for CH0b/CH1b. Fix the input level when using in 8-bit bus access (BW_SELb = "1").
19	D14_b	I/O	I	Data input/output for CH0b/CH1b. Fix the input level when using in 8-bit bus access (BW_SELb = "1").
18	D15_b	I/O	I	Data input/output for CH0b/CH1b. Fix the input level when using in 8-bit bus access (BW_SELb = "1").
44	A0_b	I	I	Address input for CH0b/CH1b
43	A1_b	I	I	Address input for CH0b/CH1b
42	A2_b	I	I	Address input for CH0b/CH1b
41	A3_b	I	I	Address input for CH0b/CH1b
40	A4_b	I	I	Address input for CH0b/CH1b
39	A5_b	I	I	Address input for CH0b/CH1b
38	A6_b	I	I	Address input for CH0b/CH1b
37	A7_b	I	I	Address input for CH0b/CH1b
12	CSB_b	I	I	Chip select input for CH0b/CH1b
13	RDB_b	I	I	Read enable input for CH0b/CH1b
14	WRB_b	I	I	Write enable input for CH0b/CH1b

FRAM/DMA Interface

Pin No.	Symbol	I/O	When PDNB = "0"	Description
126	ACK0B_a	I	I	Transmit buffer DMA access acknowledge signal input for CH0a/CH1a
125	ACK1B_a	I	I	Receive buffer DMA access acknowledge signal input for CH0a/CH1a
124	FR0B_a (DMARQ0B_a)	O	"H"	FR0B:(FD_SEL = "0") Transmit buffer frame signal output for CH0a/CH1a DMARQ0B: (FD_SEL = "1") Transmit buffer DMA access request signal output for CH0a/CH1a
123	FR1B_a (DMARQ1B_a)	O	"H"	FR1B: (FD_SEL = "0") Receive buffer frame signal output for CH0a/CH1a DMARQ1B: (FD_SEL = "1") Receive buffer DMA access request signal output for CH0a/CH1a
7	ACK0B_b	I	I	Transmit buffer DMA access acknowledge signal input for CH0b/CH1b
8	ACK1B_b	I	I	Receive buffer DMA access acknowledge signal input for CH0b/CH1b
9	FR0B_b (DMARQ0B_b)	O	"H"	FR0B: (FD_SEL = "0") Transmit buffer frame signal output for CH0b/CH1b DMARQ0B: (FD_SEL = "1") Transmit buffer DMA access request signal output for CH0b/CH1b
10	FR1B_b (DMARQ1B_b)	O	"H"	FR1B: (FD_SEL = "0") Receive buffer frame signal output for CH0b/CH1b DMARQ1B: (FD_SEL = "1") Receive buffer DMA access request signal output for CH0b/CH1b

Interrupt

Pin No.	Symbol	I/O	When PDNB = "0"	Description
122	INTB_a	O	"H"	Interrupt request output for CH0a/CH1a (Not supported in this code. Use it open.)
11	INTB_b	O	"H"	Interrupt request output for CH0b/CH1b (Not supported in this code. Use it open.)

Analog Interface

Pin No.	Symbol	I/O	When PDNB = "0"	Description
135	AIN0P_a	I	I	Transmit amplifier non-inverting input for CH0a
137	AIN0N_a	I	I	Transmit amplifier inverting input for CH0a
139	GSX0_a	O	"Hi-Z"	Transmit amplifier output for CH0a (10 kΩ drive)
141	VFRO0_a	O	"Hi-Z"	Receive amplifier output for CH0a (10 kΩ drive)
143	AIN1P_a	I	I	Transmit amplifier non-inverting input for CH1a
145	AIN1N_a	I	I	Transmit amplifier inverting input for CH1a
147	GSX1_a	O	"Hi-Z"	Transmit amplifier output for CH1a (10 kΩ drive)
149	VFRO1_a	O	"Hi-Z"	Receive amplifier output for CH1a (10 kΩ drive)
153	AIN0P_b	I	I	Transmit amplifier non-inverting input for CH0b
155	AIN0N_b	I	I	Transmit amplifier inverting input for CH0b
157	GSX0_b	O	"Hi-Z"	Transmit amplifier output for CH0b (10 kΩ drive)
159	VFRO0_b	O	"Hi-Z"	Receive amplifier output for CH0b (10 kΩ drive)
161	AIN1P_b	I	I	Transmit amplifier non-inverting input for CH1b
163	AIN1N_b	I	I	Transmit amplifier inverting input for CH1b
165	GSX1_b	O	"Hi-Z"	Transmit amplifier output for CH1b (10 kΩ drive)
167	VFRO1_b	O	"Hi-Z"	Receive amplifier output for CH1b (10 kΩ drive)
151	AVREF	O	"L"	Analog signal ground electric potential output (approx. 1.4 V)

Oscillator Circuit

Pin No.	Symbol	I/O	When PDNB = "0"	Description
173	XI	I	I	For 12.288 MHz crystal oscillator or 12.288 MHz clock input
174	XO	O	"H"	For 12.288 MHz crystal oscillator

Power Down Control

Pin No.	Symbol	I/O	When PDNB = "0"	Description
75	PDNB	I	"0"	Power down control input "0": Power down reset "1": Normal operation

PCM Interface

Pin No.	Symbol	I/O	When PDNB = "0"	Description
67	PCMO_a	O	"Hi-Z"	PCM signal output for CH0a/CH1a [open drain output pin]
69	PCMI_a	I	I	PCM signal input for CH0a/CH1a
66	PCMO_b	O	"Hi-Z"	PCM signal output for CH0b/CH1b [open drain output pin]
68	PCMI_b	I	I	PCM signal input for CH0b/CH1b
70	BCLK	I/O	I	CLKSEL = "0": PCM shift clock input
			"L"	CLKSEL = "1": PCM shift clock output
71	SYNC	I/O	I	CLKSEL = "0": PCM synchronous signal 8 kHz input
			"L"	CLKSEL = "1": PCM synchronous signal 8kHz output
76	CLKSEL	I	I	SYNC and BCLK I/O control input "0": SYNC and BCLK become inputs "1": SYNC and BCLK become outputs

Serial Control Interface

Pin No.	Symbol	I/O	When PDNB = "0"	Description
63	SDO_a	O	"Hi-Z"	Serial control output for CH0a/CH1a [open drain output pin]
65	SDI_a	I	I	Serial control input for CH0a/CH1a
77	SCLK_a	I	I	Serial control clock input for CH0a/CH1a
78	SDENB_a	I	I	Serial control data enable input for CH0a/CH1a
62	SDO_b	O	"Hi-Z"	Serial control output for CH0b/CH1b [open drain output pin]
64	SDI_b	I	I	Serial control input for CH0b/CH1b
60	SCLK_b	I	I	Serial control clock input for CH0b/CH1b
59	SDENB_b	I	I	Serial control data enable input for CH0b/CH1b
49	SCNTEN	I	I	Serial control enable setting

General-Purpose Input/Output Ports

Pin No.	Symbol	I/O	When PDNB = "0"	Description
131	GPIOA0_a	I/O	I	General-purpose input/output port A0 for CH0a/CH1a [5 V tolerant pin]
132	GPIOA1_a	I/O	I	General-purpose input/output port A1 for CH0a/CH1a [5 V tolerant pin]
127	GPIOB0_a	I/O	I	General-purpose input/output port B0 for CH0a/CH1a [5 V tolerant pin]
128	GPIOB1_a	I/O	I	General-purpose input/output port B1 for CH0a/CH1a [5 V tolerant pin]
129	GPIOB2_a	I/O	I	General-purpose input/output port B2 for CH0a/CH1a [5 V tolerant pin]
130	GPIOB3_a	I/O	I	General-purpose input/output port B3 for CH0a/CH1a [5 V tolerant pin]
79	GPIOC0_a	I/O	I	General-purpose input/output port C0 for CH0a/CH1a
80	GPIOC1_a	I/O	I	General-purpose input/output port C1 for CH0a/CH1a
81	GPIOC2_a	I/O	I	General-purpose input/output port C2 for CH0a/CH1a
82	GPIOC3_a	I/O	I	General-purpose input/output port C3 for CH0a/CH1a
83	GPIOC4_a	I/O	I	General-purpose input/output port C4 for CH0a/CH1a
84	GPIOC5_a	I/O	I	General-purpose input/output port C5 for CH0a/CH1a
85	GPIOC6_a	I/O	I	General-purpose input/output port C6 for CH0a/CH1a
86	GPIOC7_a	I/O	I	General-purpose input/output port C7 for CH0a/CH1a
2	GPIOA0_b	I/O	I	General-purpose input/output port A0 for CH0b/CH1b [5 V tolerant pin]
1	GPIOA1_b	I/O	I	General-purpose input/output port A1 for CH0b/CH1b [5 V tolerant pin]
6	GPIOB0_b	I/O	I	General-purpose input/output port B0 for CH0b/CH1b [5 V tolerant pin]
5	GPIOB1_b	I/O	I	General-purpose input/output port B1 for CH0b/CH1b [5 V tolerant pin]
4	GPIOB2_b	I/O	I	General-purpose input/output port B2 for CH0b/CH1b [5V tolerant pin]
3	GPIOB3_b	I/O	I	General-purpose input/output port B3 for CH0b/CH1b [5V tolerant pin]
58	GPIOC0_b	I/O	I	General-purpose input/output port C0 for CH0b/CH1b
57	GPIOC1_b	I/O	I	General-purpose input/output port C1 for CH0b/CH1b
56	GPIOC2_b	I/O	I	General-purpose input/output port C2 for CH0b/CH1b
55	GPIOC3_b	I/O	I	General-purpose input/output port C3 for CH0b/CH1b
54	GPIOC4_b	I/O	I	General-purpose input/output port C4 for CH0b/CH1b
53	GPIOC5_b	I/O	I	General-purpose input/output port C5 for CH0b/CH1b
52	GPIOC6_b	I/O	I	General-purpose input/output port C6 for CH0b/CH1b
51	GPIOC7_b	I/O	I	General-purpose input/output port C7 for CH0b/CH1b

Analog Power Supply Pins

Pin No.	Symbol	I/O	When PDNB = "0"	Description
133	AVDD0	—	—	Analog power supply 0
170	AVDD1	—	—	Analog power supply 1
134	AGND0	—	—	Analog ground 0
169	AGND1	—	—	Analog ground 1

Digital Power Supply Pins

Pin No.	Symbol	I/O	When PDNB = "0"	Description
16	DVDD0	—	—	Digital power supply 0
35	DVDD1	—	—	Digital power supply 1
45	DVDD2	—	—	Digital power supply 2
73	DVDD3	—	—	Digital power supply 3
98	DVDD4	—	—	Digital power supply 4
117	DVDD5	—	—	Digital power supply 5
175	DVDD6	—	—	Digital power supply 6
17	DGND0	—	—	Digital ground 0
36	DGND1	—	—	Digital ground 1
61	DGND2	—	—	Digital ground 2
72	DGND3	—	—	Digital ground 3
97	DGND4	—	—	Digital ground 4
116	DGND5	—	—	Digital ground 5
172	DGND6	—	—	Digital ground 6
15	VREGOUT0	—	—	Internal regulator voltage output pin 0 (approx. 2.5 V)
34	VREGOUT1	—	—	Internal regulator voltage output pin 1 (approx. 2.5 V)
46	VREGOUT2	—	—	Internal regulator voltage output pin 2 (approx. 2.5V)
74	VREGOUT3	—	—	Internal regulator voltage output pin 3 (approx. 2.5 V)
99	VREGOUT4	—	—	Internal regulator voltage output pin 4 (approx. 2.5 V)
118	VREGOUT5	—	—	Internal regulator voltage output pin 5 (approx. 2.5V)
176	VREGOUT6	—	—	Internal regulator voltage output pin 6 (approx. 2.5V)
47	VBG	—	—	Internal regulator reference voltage output pin

Test Pins

Pin No.	Symbol	I/O	When PDNB = "0"	Description
88	TST0	I	"0"	Input pin 0 for testing. Normally input "0".
87	TST1	I	"0"	Input pin 1 for testing. Normally input "0".
50	TST2	I	"0"	Input pin 2 for testing. Normally input "0".
48	TST3	I	"0"	Input pin 3 for testing. Normally input "0".

N.C. Pins

Pin No.	Symbol	I/O	When PDNB = "0"	Description
136	N.C.	—	—	"No Connect" pin. Leave it open.
138	N.C.	—	—	"No Connect" pin. Leave it open.
140	N.C.	—	—	"No Connect" pin. Leave it open.
142	N.C.	—	—	"No Connect" pin. Leave it open.
144	N.C.	—	—	"No Connect" pin. Leave it open.
146	N.C.	—	—	"No Connect" pin. Leave it open.
148	N.C.	—	—	"No Connect" pin. Leave it open.
150	N.C.	—	—	"No Connect" pin. Leave it open.
152	N.C.	—	—	"No Connect" pin. Leave it open.
154	N.C.	—	—	"No Connect" pin. Leave it open.
156	N.C.	—	—	"No Connect" pin. Leave it open.
158	N.C.	—	—	"No Connect" pin. Leave it open.
160	N.C.	—	—	"No Connect" pin. Leave it open.
162	N.C.	—	—	"No Connect" pin. Leave it open.
164	N.C.	—	—	"No Connect" pin. Leave it open.
166	N.C.	—	—	"No Connect" pin. Leave it open.
168	N.C.	—	—	"No Connect" pin. Leave it open.
171	N.C.	—	—	"No Connect" pin. Leave it open.

Explanation of pin status when PDNB = "0"
"I" : Input a high or low level signal to the pin.
"0" : Input a low level signal to the pin.
"H" : A high level signal is output from the pin.
"L" : A low level signal is output from the pin.
"Hi-Z" : The pin is placed in a Hi-Z state.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions		Rating	Unit
Analog power supply voltage	AVDD	—		–0.3 to +4.6	V
Digital power supply voltage	DVDD	—		–0.3 to +4.6	V
Analog input voltage	VAIN	Analog pins		–0.3 to AVDD + 0.3	V
Digital input voltage	VDIN1	Normal digital pins		–0.3 to DVDD + 0.3	V
	VDIN2	5 V tolerant pins	DVDD = 3.0 to 3.6 V	–0.3 to +6.0	V
			DVDD < 3.0 V	–0.3 to DVDD+0.3	V
Output current	IO	—		–20 to +20	mA
Power dissipation	PD	Ta = 60°C, per package		700	mW
Storage temperature range	Tstg	—		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS **Preliminary**

(Unless otherwise specified, AVDD = 3.0 to 3.6 V, DVDD = 3.0 to 3.6 V, AGND = DGND = 0.0 V, Ta = –20 to +60°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Analog power supply voltage	AVDD	—	3.0	3.3	3.6	V
Digital power supply voltage	DVDD	—	3.0	3.3	3.6	V
Operating temperature range	Ta	—	–20	—	+60	°C
Digital high level input voltage	VIH1	Normal digital pins	0.75 × DVDD	—	DVDD+ 0.3	V
	VIH2	5 V tolerant pins	0.75 × DVDD	—	5.5	V
Digital low level input voltage	VIL	Digital pins	–0.3	—	0.19 × DVDD	V
Digital input rise time	tIR	Digital pins	—	2	20	ns
Digital input fall time	tIF	Digital pins	—	2	20	ns
Digital output load capacitance	CDL	Digital pins	—	—	50	pF
Digital output load resistance	RDL	Open drain pins. Pull-up resisor.	500	—	—	Ω
Capacitance of bypass capacitor for AVREF	Cvref	Between AVREF and AGND	2.2+0.1	—	4.7+0.1	µF
Capacitance of bypass capacitor for VREGOUT	Cvout1	Between VREGOUT2 and DGND	—	10+0.1	—	µF
	Cvout2	Between VREGOUT[6:3,1:0] and DGND	—	0.1	—	µF
Capacitance of bypass capacitor for VBG	CVBG	Between VBG and DGND	—	150	—	pF
Master clock frequency	Fmck	MCK	–0.01%	12.288	+0.01%	MHz
PCM shift clock frequency	Fbclk	BCLK (at input)	128	—	2048	kHz
PCM sync signal frequency	Fsync	SYNC (at input)	—	8.0	—	kHz
Clock duty ratio	DRCLK	MCK, BCLK (at input)	40	50	60	%
PCM sync timing	tBS	BCLK to SYNC (at input)	100	—	—	ns
	tSB	SYNC to BCLK (at input)	100	—	—	ns
PCM sync signal width	tWS	SYNC (at input)	1BCLK	—	100	µs

Note: It is recommended that power be applied at the same time to the analog power supply voltage (AVDD) and digital power supply voltage (DVDD) that are to be supplied to this LSI. However, if it is difficult to do so due to the configuration of the power supply circuit, applying power to DVDD first and AVDD next is recommneded. Also, as for the power-off sequence, it is recommended that power be turned off in the reverse order of power on.

ELECTRICAL CHARACTERISTICS

Preliminary

DC Characteristics

(Unless otherwise specified, AVDD = 3.0 to 3.6 V, DVDD = 3.0 to 3.6 V, AGND = DGND = 0.0 V, Ta = –20 to +60°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply current	ISS	Standby state (PDNB = "0", DVDD = AVDD = 3.3 V, Ta = 25°C)	—	TBD	TBD	μA
	IDD	Operating state, Speech CODEC (4CH) being activated/ PCM interface used; analog interface not used A 12.288 MHz crystal oscillator connected to XI and XO	—	TBD	TBD	mA
Digital input pin input leakage current	IIH	Vin = DVDD	—	0.01	10	μA
	IIL	Vin = DGND	–10	–0.01	—	μA
Digital I/O pin output leakage current	IOZH	Vout = DVDD	—	0.01	10	μA
	IOZL	Vout = DGND	–10	—	—	μA
High level output voltage	VOH	Digital output pins, input/output pins IOH = 4.0 mA IOH = 0.5 mA (XO pin)	0.78× DVDD	—	—	V
Low level output voltage	VOL1	Digital output pins, input/output pins IOL = –4.0 mA IOL = –0.5 mA (XO pin)	—	—	0.4	V
	VOL2	Open drain output pins IOL = –12.0 mA	—	—	0.4	V
Input capacitance*1	CIN1	Input pins	—	6	—	pF
	CIN2	Input/output pins	—	10	—	pF

*1 Guaranteed design value

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AC Characteristics

Gain Setting (Speech CODEC = G.711 (μ-law))

(Unless otherwise specified, AVDD = 3.0 to 3.6 V, DVDD = 3.0 to 3.6 V, AGND = DGND = 0.0 V, Ta = –20 to +60°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Transmit and receive gain setting accuracy	GAC	Relative to set gain	–1.0	—	+1.0	dB

Tone Output (Speech CODEC = G.711 (μ-law))

(Unless otherwise specified, AVDD = 3.0 to 3.6 V, DVDD = 3.0 to 3.6 V, AGND = DGND = 0.0 V, Ta = –20 to +60°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Frequency deviation	fDFT	Relative to set frequency	–1.5	—	+1.5	%
Output level	oLEV	Relative to set gain	–2.0	—	+2.0	dB

DTMF Detector, Other Detectors (Speech CODEC = G.711 (μ-law))

(Unless otherwise specified, AVDD = 3.0 to 3.6 V, DVDD = 3.0 to 3.6 V, AGND = DGND = 0.0 V, Ta = –20 to +60°C)

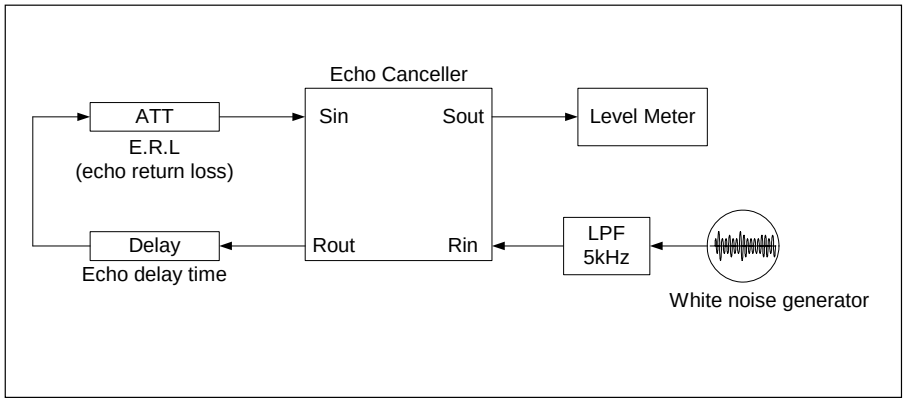
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Detect level accuracy	dLAC	Relative to set detect level	–2.5	—	+2.5	dB

Echo Canceller

(Unless otherwise specified, AVDD = 3.0 to 3.6 V, DVDD = 3.0 to 3.6 V, AGND = DGND = 0.0 V, Ta = –20 to +60°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Echo attenuation	eRES	—	—	35	—	dB
Erasable echo delay time	tECT	—	—	—	32	ms

Measurement method



PDNB, XO, AVREF Timings

(Unless otherwise specified, AVDD = 3.0 to 3.6 V, DVDD = 3.0 to 3.6 V, AGND = DGND = 0.0 V, Ta = –20 to +60°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power down signal pulse width	tPDNB	PDNB pin	250	—	—	µs
AVDD supply delay time	tAVDDON	—	0	—	—	ns
Oscillation start-up time	txtal	—	—	—	10	ms
AVREF rise time	tAVREF	AVREF =1.4 (90%) 4.7 µF+0.1 µF	—	—	600	ms
		AVREF = 1.4 (90%) 2.2 µF+0.1 µF	—	—	300	ms

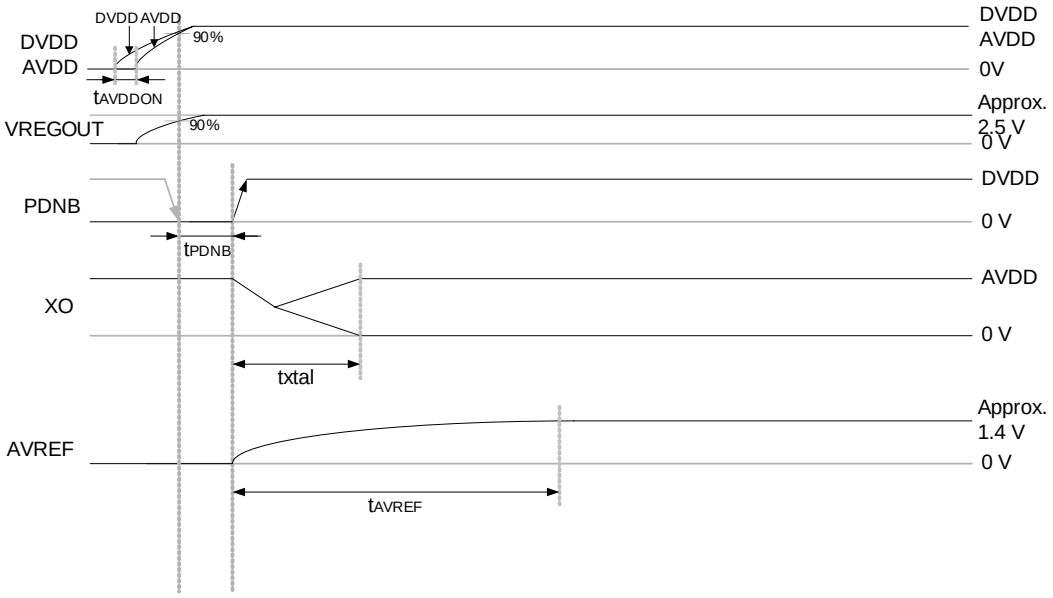


Figure 1 PDNB, XO, and AVREF Timings

Note:

The capacitance of the capacitor for AVREF affects the AVREF rise time and analog characteristics. To place more importance on analog characteristics, set the capacitance to 4.7 µF; to place more importance on the AVREF rise time, set it to 2.2 µF. Since the use of an analog interface is prohibited in this code, connect a capacitor of 2.2 µF or 4.7 µF.

PCM Interface

(Unless otherwise specified, AVDD = 3.0 to 3.6 V, DVDD = 3.0 to 3.6 V, AGND = DGND = 0.0 V, Ta = –20 to +60°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Bit clock frequency	fBCLK	CDL = 20 pF (at output)	–0.1%	2.048	+0.1%	MHz
Bit clock duty ratio	dBCLK	CDL = 20 pF (at output)	45	50	55	%
Sync signal frequency	fSYNC	CDL = 20 pF (at output)	–0.1%	8	+0.1%	kHz
Sync signal duty ratio	dSYNC1	CDL = 20 pF (at output) BCLK = At 2.048 MHz output	45	50	55	%
Transmit/receive signal sync timing	tBS	BCLK to SYNC (at output)	100	—	—	ns
	tSB	SYNC to BCLK (at output)	100	—	—	ns
Input setup time	tDS	PCMI pin	50	—	—	ns
Input hold time	tDH		50	—	—	ns
Digital output delay time	tSDX	PCMO pin Pull-up resistor RDL = 500Ω CDL = 50 pF	—	—	100	ns
	tXD1		—	—	100	ns
Digital output hold time	tXD2		—	—	100	ns
	tXD3		—	—	100	ns

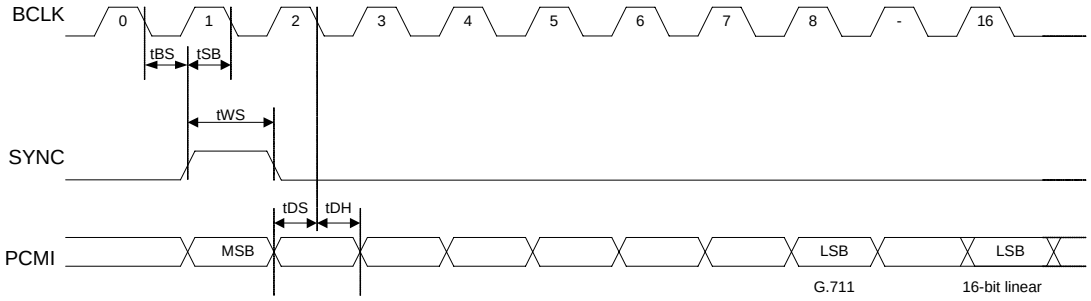


Figure 2 PCM Interface Input Timing (Long Frame)

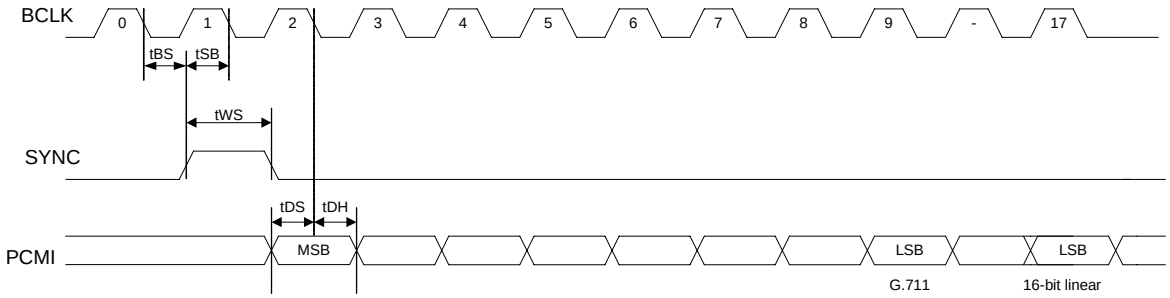


Figure 3 PCM Interface Input Timing (Short Frame)

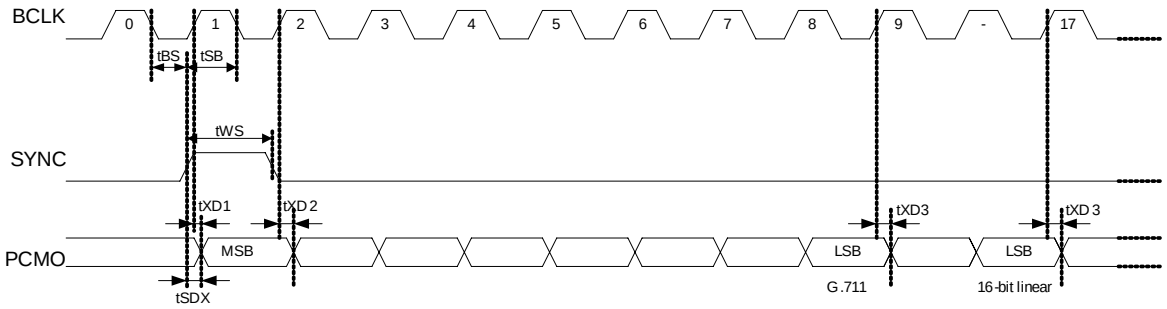


Figure 4 PCM Interface Output Timing (Long Frame)

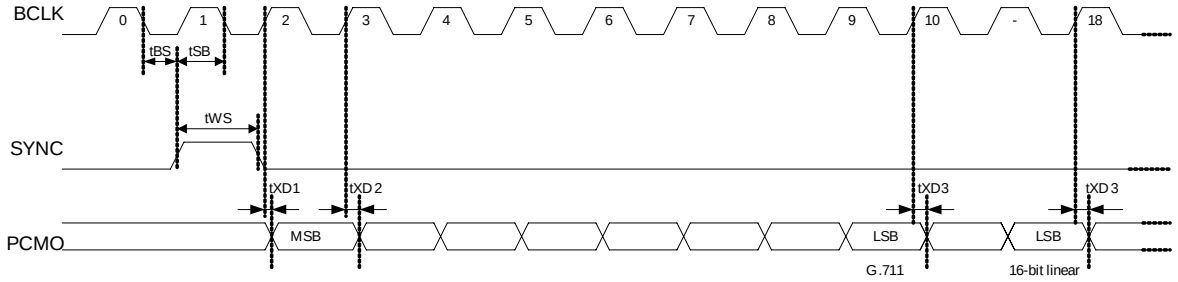


Figure 5 PCM Interface Output Timing (Short Frame)

Control Register Interface

(Unless otherwise specified, AVDD = 3.0 to 3.6 V, DVDD = 3.0 to 3.6 V, AGND = DGND = 0.0 V, Ta = –20 to +60°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Address setup time (during read)	tRAS	CL = 50pF	10	—	—	ns
Address hold time (during read)	tRAH		0	—	—	ns
Address setup time (during write)	tWAS		10	—	—	ns
Address hold time (during write)	tWAH		10	—	—	ns
Write data setup time	tWDS		20	—	—	ns
Write data hold time	tWDH		10	—	—	ns
CSB setup time (during read)	tRCS		10	—	—	ns
CSB hold time (during read)	tRCH		0	—	—	ns
CSB setup time (during write)	tWCS		10	—	—	ns
CSB hold time (during write)	tWCH		10	—	—	ns
WRB pulse width	tWW		10	—	—	ns
Read data output delay time	tRDD		—	—	20	ns
Read data output hold time	tRDH		3	—	—	ns
RDB pulse width	tRW		25	—	—	ns
CSB disable time	tCD	CL = 50 pF When in any mode other than download mode	10	—	—	ns
		CL = 50 pF During download mode	350	—	—	ns

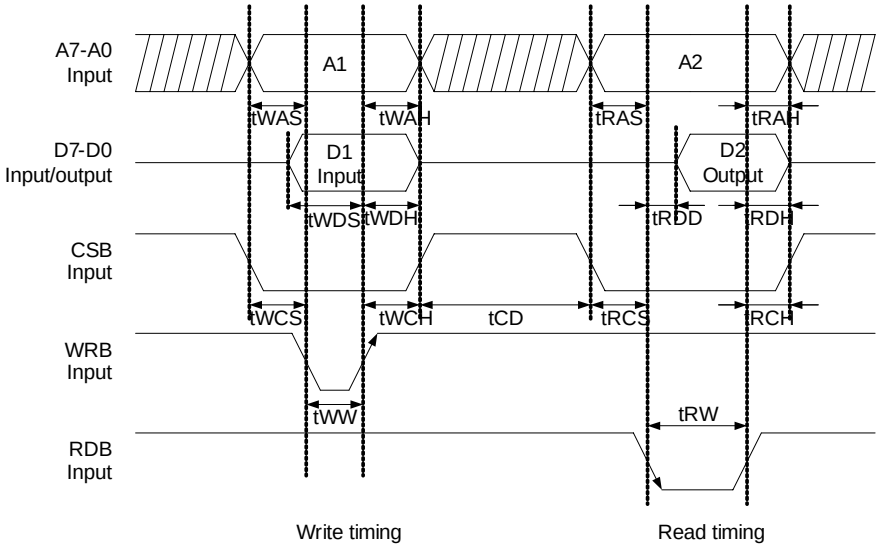


Figure 6 Control Register Interface

Transmit and Receive Buffer Interface (in Frame Mode)

(Unless otherwise specified, AVDD = 3.0 to 3.6 V, DVDD = 3.0 to 3.6 V, AGND = DGND = 0.0 V, Ta = –20 to +60°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
FR1B setup time	tF1S	CL = 50 pF	3	—	—	ns
FR1B output delay time	tF1D		—	—	20	ns
Address setup time (during read)	tRAS		10	—	—	ns
Address hold time (during read)	tRAH		0	—	—	ns
Address setup time (during write)	tWAS		10	—	—	ns
Address hold time (during write)	tWAH		10	—	—	ns
Write data setup time	tWDS		20	—	—	ns
Write data hold time	tWDH		10	—	—	ns
CSB setup time (during read)	tRCS		10	—	—	ns
CSB hold time (during read)	tRCH		0	—	—	ns
CSB setup time (during write)	tWCS		10	—	—	ns
CSB hold time (during write)	tWCH		10	—	—	ns
WRB pulse width	tWW		10	—	—	ns
FR0B setup time	tF0S		3	—	—	ns
FR0B output delay time	tF0D		—	—	20	ns
Read data output delay time	tRDD		—	—	30	ns
Read data output hold time	tRDH		3	—	—	ns
RDB pulse width	tRW		35	—	—	ns
CSB disable time	tCD		10	—	—	ns

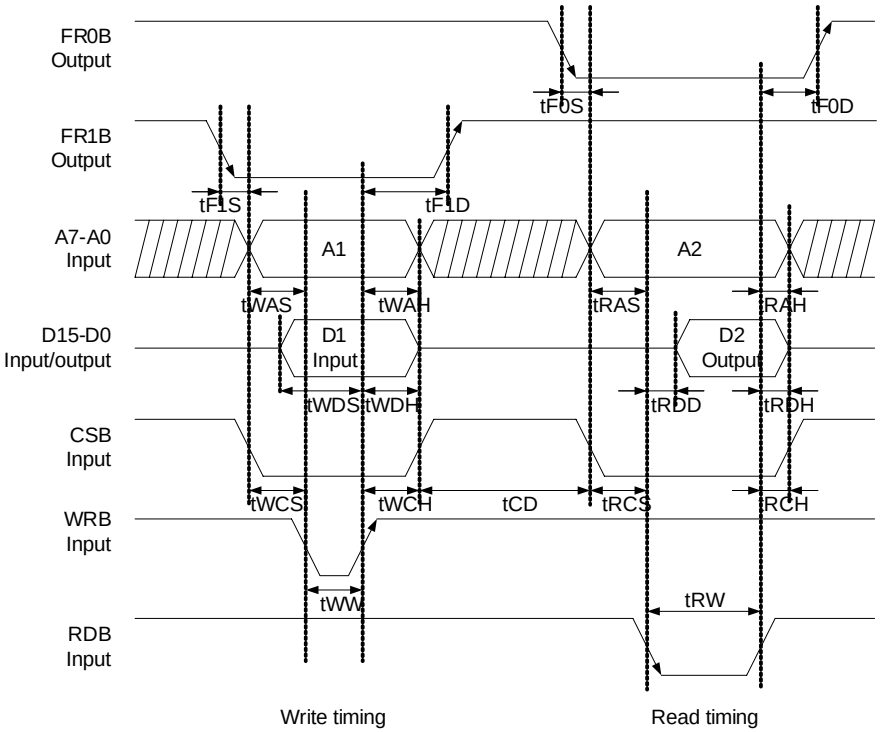


Figure 7 Transmit and Receive Buffer Interface (in Frame Mode)

Transmit and Receive Buffer Interface (in DMA Mode)

(Unless otherwise specified, AVDD = 3.0 to 3.6 V, DVDD = 3.0 to 3.6 V, AGND = DGND = 0.0 V, Ta = –20 to +60°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
DMARQ1B setup time	tDR1S	CL = 50 pF	3	—	—	ns
DMARQ1B output delay time	tDR1RD		—	—	30	ns
	tDR1FD		—	—	30	ns
Address setup time (during read)	tRAS		10	—	—	ns
Address hold time (during read)	tRAH		0	—	—	ns
Address setup time (during write)	tWAS		10	—	—	ns
Address hold time (during write)	tWAH		10	—	—	ns
Write data setup time	tWDS		20	—	—	ns
Write data hold time	tWDH		10	—	—	ns
ACK0B setup time	tAK0S		10	—	—	ns
ACK0B hold time	tAK0H		0	—	—	ns
ACK1B setup time	tAK1S		10	—	—	ns
ACK1B hold time	tAK1H		10	—	—	ns
WRB pulse width	tWW		10	—	—	ns
DMARQ0B setup time	tDR0S		3	—	—	ns
DMARQ0B output delay time	tDR0RD		—	—	30	ns
	tDR0FD		—	—	30	ns
Read data output delay time	tRDD		—	—	30	ns
Read data output hold time	tRDH		3	—	—	ns
RDB pulse width	tRW		35	—	—	ns
ACKB disable time	tAD		10	—	—	ns

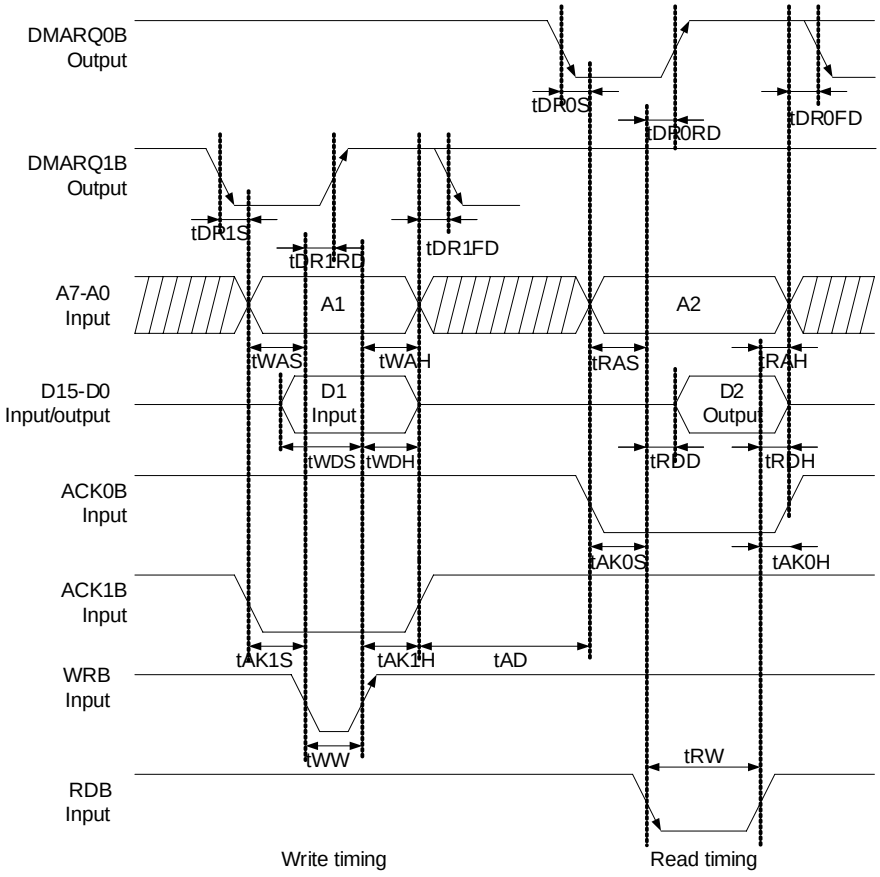


Figure 8 Transmit and Receive Buffer Interface (in DMA Mode)

Serial Control Interface

(Unless otherwise specified, AVDD = 3.0 to 3.6 V, DVDD = 3.0 to 3.6 V, AGND = DGND = 0.0 V, Ta = –20 to +60°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Serial control interface timing	ts1	CDL = 20 pF	150	—	—	ns
	ts2		50	—	—	ns
	ts3		250	—	—	ns
	ts4		500	—	—	ns
	ts5		250	—	—	ns
	ts6		250	—	—	ns
	ts7	RDL = 500Ω, CDL = 50 pF	—	—	200	ns
	ts8		0	—	—	ns
	ts9	CDL = 20 pF	400	—	—	ns
	ts10	RDL = 500Ω, CDL = 50 pF	—	—	100	ns
	ts11	CDL = 20 pF	500	—	—	ns

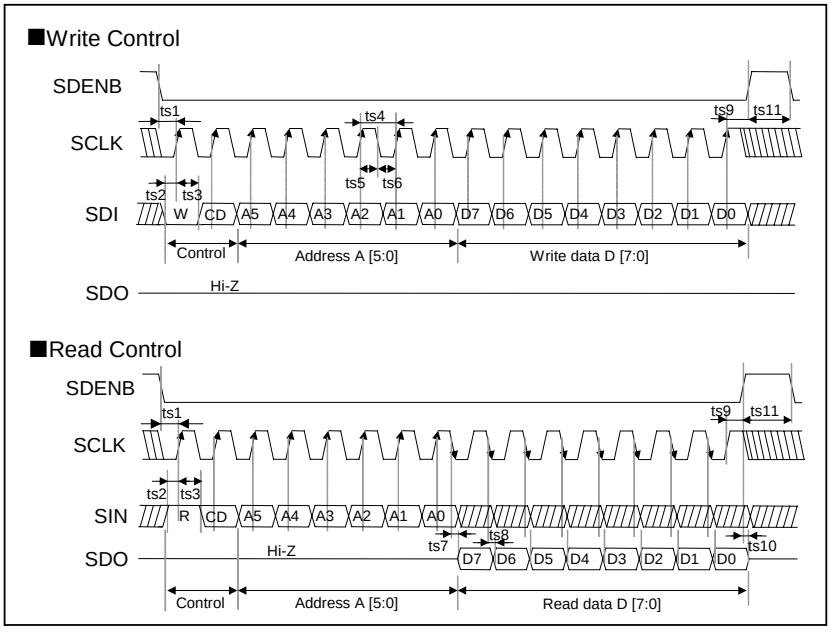


Figure 9 Serial Control Interface Timing

PIN FUNCTIONAL DESCRIPTIONS

D0_a–D15_a
Data input/output pins for accessing the frames/DMA/control registers for CH0a/CH1a. Since these are input/output pins, connect a pull-up resistor. If 8-bit bus access is selected with the MCU interface data width selection register (BW_SELa), D0–D7 will be enabled. If they are used for 8-bit bus access (BW_SELa = "1"), upper D8–D15 will always be placed in an input state; therefore, fix the inputs to "0" or "1".

A0_a–A7_a
Address input pins for accessing the frames/DMA/control registers for CH0a/CH1a. Each address is as follows:

Transmit buffer (TX Buffer)	A7_a–A0_a = 80h
Receive buffer (RX Buffer)	A7_a–A0_a = 81h
Control registers (CR,GPCR,DLCR)	For addresses, see the Control Register List.

CSB_a
Chip select input pin for accessing the frames/control registers for CH0a/CH1a.

RDB_a
Read enable input pin for accessing the frames/DMA/control registers for CH0a/CH1a.

WRB_a
Write enable input pin for accessing the frames/DMA/control registers for CH0a/CH1a.

D0_b–D15_b
Data input/output pins for accessing the frames/DMA/control registers for CH0b/CH1b. Since these are input/output pins, connect a pull-up resistor. If 8-bit bus access is selected with the MCU interface data width selection register (BW_SELb), D0–D7 will be enabled. If they are used for 8-bit bus access (BW_SELb = "1"), upper D8–D15 will always be placed in an input state; therefore, fix the inputs to "0" or "1".

A0_b–A7_b
Address input pins for accessing the frames/DMA/control register for CH0b/CH1b. Each address is as shown below:

Transmit buffer (TX Buffer)	A7_b–A0_b = 80h
Receive buffer (RX Buffer)	A7_b–A0_b = 81h
Control registers (CR,GPCR,DLCR)	For addresses, see the Control Register List.

CSB_b
Chip select input pin for accessing the frames/control registers for CH0b/CH1b.

RDB_b
Read enable input pin for accessing the frames/DMA/control register for CH0b/CH1b.

WRB_b
Write enable input pin for accessing the frames/DMA/control registers for CH0b/CH1b.

ACK0B_a
This is the DMA acknowledge input pin for the DMARQ0B_a signal during DMA access of the transmit buffer of CH0a/CH1a and becomes valid in the DMA mode (FD_SELa = "1").
Tie this pin to "1" when using this LSI in the frame mode (FD_SELa = "0").

ACK1B_a
This is the DMA acknowledge input pin for the DMARQ1B_a signal during DMA access of the receive buffer of CH0a/CH1a and becomes valid in the DMA mode (FD_SELa = "1").
Tie this pin to "1" when using this LSI in the frame mode (FD_SELa = "0").

FR0B_a (DMARQ0B_a)
- FR0B_a (In frame mode (the FRAME/DMA selection register FD_SELa = "0"))
  This is the transmit frame output pin which outputs the signal when the transmit buffer is full during frame access at CH0a/CH1a. This pin outputs a "L" level when the transmit buffer becomes full, and maintains that "L" level output until a specific number of words are read out from the MCU.

- DMARQ0B_a (In DMA mode (the FRAME/DMA selection register FD_SELa = "1"))
  This is the DMA request output pin which outputs the signal when the transmit buffer is full during DMA access at CH0a/CH1a. This output becomes "L" when the transmit buffer becomes full, and returns to the "H" level automatically on the falling edge of the read enable signal (RDB_a = "1" → "0") when there is an acknowledge signal (ACK0B_a = "0") from the MCU. This relationship is repeated until a specific number of words are read out from the MCU.

FR1B_a (DMARQ1B_a)
- FR1B_a (In frame mode (the FRAME/DMA selection register FD_SELa = "0"))
  This is the receive frame output pin which outputs the signal when the receive buffer is empty during frame access at CH0a/CH1a. This pin outputs a "L" level when the receive buffer becomes empty, and maintains that "L" level output until a specific number of words are written from the MCU.

- DMARQ1B_a (In DMA mode (the FRAME/DMA selection register FD_SELa = "1"))
  This is the DMA request output pin which outputs the signal when the receive buffer is full during DMA access at CH0a/CH1a. This output becomes "L" when the receive buffer becomes empty, and returns to the "H" level automatically on the falling edge of the write enable signal (WRB_a = "1" → "0") when there is an acknowledge signal (ACK1B_a = "0") from the MCU. This relationship is repeated until a specific number of words are written from the MCU.

ACK0B_b
This is the DMA acknowledge input pin for the DMARQ0B_b signal during DMA access of the transmit buffer of CH0b/CH1b and becomes valid in the DMA mode (FD_SELb = "1").
Tie this pin to "1" when using this LSI in the frame mode (FD_SELb = "0").

ACK1B_b
This is the DMA acknowledge input pin for the DMARQ1B_b signal during DMA access of the receive buffer of CH0b/CH1b and becomes valid in the DMA mode (FD_SELb = "1").
Tie this pin to "1" when using this LSI in the frame mode (FD_SELb = "0").

FR0B_b (DMARQ0B_b)
- FR0B_b (In frame mode (the FRAME/DMA selection register FD_SELb = "0"))
  This is the transmit frame output pin which outputs the signal when the transmit buffer is full during frame access at CH0b/CH1b. This pin outputs a "L" level when the transmit buffer becomes full, and maintains that "L" level output until a specific number of words are read out from the MCU.

- DMARQ0B_b (In DMA mode (the FRAME/DMA selection register FD_SELb = "1"))
  This is the DMA request output pin which outputs the signal when the transmit buffer is full during DMA access at CH0b/CH1b. This output becomes "L" when the transmit buffer becomes full, and returns to the "H" level automatically on the falling edge of the read enable signal (RDB_b = "1" → "0") when there is an acknowledge signal (ACK0B_b = "0") from the MCU. This relationship is repeated until a specific number of words are read out from the MCU.

FR1B_b (DMARQ1B_b)
- FR1B_b (In frame mode (the FRAME/DMA selection register FD_SELb = "0"))
  This is the receive frame output pin which outputs the signal when the receive buffer is empty during frame access at CH0b/CH1b. This pin outputs a "L" level when the receive buffer becomes empty, and maintains that "L" level output until a specific number of words are written from the MCU.

- DMARQ1B_b (In DMA mode (the FRAME/DMA selection register FD_SELb = "1"))
  This is the DMA request output pin which outputs the signal when the receive buffer is empty during DMA access at CH0b/CH1b. This output becomes "L" when the receive buffer becomes empty, and returns to the "H" level automatically on the falling edge of the write enable signal (WRB_b = "1" → "0") when there is an acknowledge signal (ACK1B_b = "0") from the MCU. This relationship is repeated until a specific number of words are written from the MCU.

INTB_a
Interrupt request output pin for CH0a/CH1a. Since the interrupt notification function is not supported in this code, this pin will always output "1". Leave it open.

INTB_b
Interrupt request output pin for CH0b/CH1b. Since the interrupt notification function is not supported in this code, this pin will always output "1". Leave it open.

AIN0N_a, AIN0P_a, GSX0_a
Transmission analog input and transmission level adjustment pins for CH0a. AIN0N_a is connected to the inverting input pin of the internal transmit amplifier, and AIN0P_a is connected to the non-inverting input pin. GSX0_a is conneced to the output pin of the internal transmit amplifier. For more information about level adjustment, see Figure 10.
At hardware power down (PDNB = "0"), or in a reset state on the DSP_A side (DSP_RESET_a = "1"), the output of GSX0_a will be placed in a high impedance state. Since the use of an analog interface is prohibited in this code, short GSX0_a and AIN0N_a, and connect AIN0P_a with AVREF.

VFRO0_a
Reception analog output pin for CH0a. VFRO0_a is connected to the output pin of the internal receive amplifier. For the output signal of VFRO0_a, output can be selected with the VFRO0 selection register_a (VFRO0_SEL_a). When selected ("1"), a reception signal is output; when unselected ("0"), AVREF (approximately 1.4 V) is output. At hardware power down (PDNB = "0"), or in a reset state on the DSP_A side (DSP_RESET_a = "1"), the output of this pin will be placed in a high impedance state. It is recommended to use the output signal via a capacitor for DC coupling.
Because the use of an analog interface is prohibited in this code, leave this pin open.

Note:
If output selection is changed during a call, minor noise will be generated. Therefore, it is recommended to select an output before starting a call, and then start a call after output selection. When canceling a reset or resetting, it is recommended to do so with the output of VFRO0_a selected to the AVREF output side.

AIN1N_a, AIN1P_a, GSX1_a
Transmission analog input and transmission level adjustment pins for CH1a. AIN1N_a is connected to the inverting input pin of the internal transmit amplifier, and AIN1P_a is connected to the non-inverting input pin. GSX1_a is conneced to the output pin of the internal transmit amplifier. For more information about level adjustment, see Figure 10.
At hardware power down (PDNB = "0"), or in a reset state on the DSP_A side (DSP_RESET_a = "1"), the output of GSX1_a will be placed in a high impedance state. Since the use of an analog interface is prohibited in this code, short GSX1_a and AIN1N_a, and connect AIN1P_a with AVREF.

VFRO1_a
Reception analog output pin for CH1a. VFRO1_a is connected to the output pin of the internal receive amplifier. For the output signal of VFRO1_a, output can be selected with the VFRO1 selection register_a (VFRO1_SEL_a). When selected ("1"), a reception signal is output; when unselected ("0"), AVREF (approximately 1.4 V) is output. At hardware power down (PDNB = "0"), or in a reset state on the DSP_A side (DSP_RESET_a = "1"), the output of this pin will be placed in a high impedance state. It is recommended to use the output signal via a capacitor for DC coupling.
Because the use of an analog interface is prohibited in this code, leave this pin open.

Note:
If output selection is changed during a call, minor noise will be generated. Therefore, it is recommended to select an output before starting a call. When canceling a reset or resetting, it is recommended to do so with the output of VFRO1_a selected to the AVREF output side.

AIN0N_b, AIN0P_b, GSX0_b
Transmission analog input and transmission level adjustment pins for CH0b. AIN0N_b is connected to the inverting input pin of the internal transmit amplifier, and AIN0P_b is connected to the non-inverting input pin. GSX0_b is conneced to the output pin of the internal transmit amplifier. For more information about level adjustment, see Figure 10.
At hardware power down (PDNB = "0"), or in a reset state on the DSP_B side (DSP_RESET_b = "1"), the output of GSX0_b will be placed in a high impedance state. Since the use of an analog interface is prohibited in this code, short GSX0_b and AIN0N_b, and connect AIN0P_b with AVREF.

VFRO0_b
Reception analog output pin for CH0b. VFRO0_b is connected to the output pin of the internal receive amplifier. For the output signal of VFRO0_b, output can be selected with the VFRO0 selection register_b (VFRO0_SEL_b). When selected ("1"), a reception signal is output; when unselected ("0"), AVREF (approximately 1.4 V) is output. At hardware power down (PDNB = "0"), or in a reset state on the DSP_B side (DSP_RESET_b = "1"), the output of this pin will be placed in a high impedance state. It is recommended to use the output signal via a capacitor for DC coupling.
Because the use of an analog interface is prohibited in this code, leave this pin open.

Note:
If output selection is changed during a call, minor noise will be generated. Therefore, it is recommended to select an output before starting a call, and then start a call after output selection. When canceling a reset or resetting, it is recommended to do so with the output of VFRO0_b selected to the AVREF output side.

AIN1N_b, AIN1P_b, GSX1_b
Transmission analog input and transmission level adjustment pins for CH1b. AIN1N_b is connected to the inverting input pin of the internal transmit amplifier, and AIN1P_b is connected to the non-inverting input pin. GSX1_b is conneced to the output pin of the internal transmit amplifier. For more information about level adjustment, see Figure 10.
At hardware power down (PDNB = "0"), or in a reset state on the DSP_B side (DSP_RESET_b = "1"), the output of GSX1_b will be placed in a high impedance state. Since the use of an analog interface is prohibited in this code, short GSX1_b and AIN1N_b, and connect AIN1P_b with AVREF.

VFRO1_b
Reception analog output pin for CH1b. VFRO1_b is connected to the output pin of the internal receive amplifier. For the output signal of VFRO1_b, output can be selected with the VFRO1 selection register_b (VFRO1_SEL_b). When selected ("1"), a reception signal is output; when unselected ("0"), AVREF (approximately 1.4 V) is output. At hardware power down (PDNB = "0"), or in a reset state on the DSP_B side (DSP_RESET_b = "1"), the output of this pin will be placed in a high impedance state. It is recommended to use the output signal via a capacitor for DC coupling.
Because the use of an analog interface is prohibited in this code, leave this pin open.

Note:
If output selection is changed during a call, minor noise will be generated. Therefore, it is recommended to select an output before starting a call, and then start a call after output selection. When canceling a reset or resetting, it is recommended to do so with the output of VFRO1_b selected to the AVREF output side.

AVREF
This is the output pin for the analog signal ground potential. The output potential at this pin will be about 1.4 V. Connect a 2.2 to 4.7 μF (aluminum electrolytic type) capacitor and a 0.1 μF (ceramic type) capacitor in parallel between this pin and the GND pin as bypass capacitors. The output at the AVREF pin goes to 0.0 V in the hardware power-down state. The voltage starts rising after the hardwdare power-down state is released (PDNB = "1"). Also, if the output of the AVREF pin is used externally, use it via a buffer.

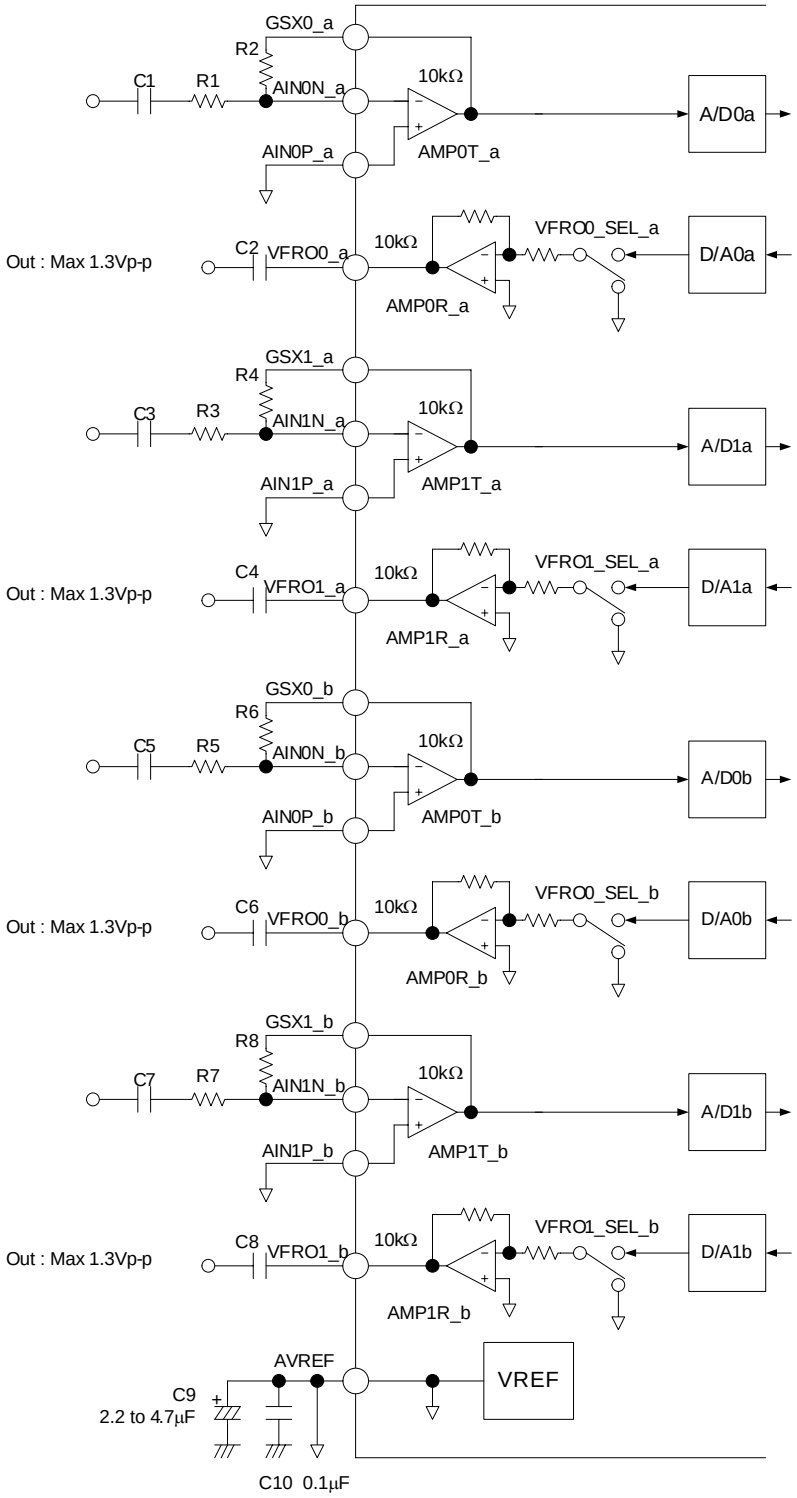


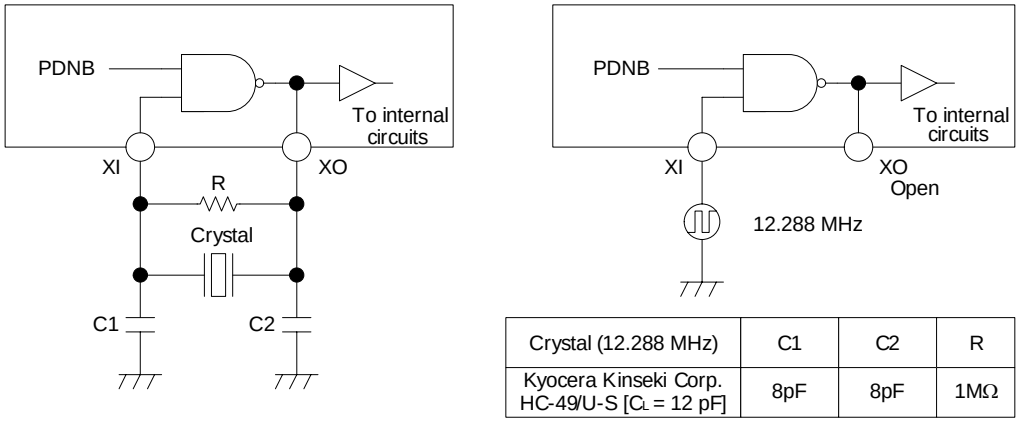
Figure 10 Analog Interface

XI, XO

These are the pins for either connecting the crystal oscillator for the master clock or for inputting an external master clock signal.

The oscillations of the master clock oscillator will be stopped during a power down due to the PDNB signal. The oscillations start when the power down condition is released, and the internal clock supply of the LSI will be started after counting up the oscillation stabilization period (of about 10 ms), and the DSP firmware can then be downloaded.

Examples of crystal oscillator connection and external master clock input are shown in Figure. 11.



Crystal (12.288 MHz)	C1	C2	R
Kyocera Kinseki Corp. HC-49/U-S [C_L = 12 pF]	8pF	8pF	1MΩ

Figure 11 Examples of Oscillator Circuit and Clock Input

PDNB

This is the power down control input pin. The power down stateis entered when this pin goes to "0". In addition, this pin also has the function of resetting the LSI. In order to prevent wrong operation of the LSI, carry out the initial power-down reset after switching on the power using this PDNB pin. Also, keep the PDNB pin at "0" level for 250 μs or more to initiate the power down state.

See Figure 1 for the timings of PDNB, AVREF, and XO.

Note:

At the time of turning on the power, start from the power down state using PDNB.

Also, if used by inputting a master clock to the XI pin, maintain a power down state (PDNB = 0) until the digital power (DVDD[6:0]) and analog power (AVDD[1:0]) are supplied (90% or more), as well as until a master clock is completely input to the XI pin, and then cancel the power down state (PDNB = 0→1). Even in this case, fix PDNB at "0" for at least 250 μsec.

PCMO_a
PCM signal output pin for CH0a/CH1a. It outputs a PCM signal in synchronization with the rise of BCLK or SYNC. Regarding output from PCMO_a, data will be output only in the applicable time slot segment according to the setting of the selected time slot position, and the output will be in a high impedance state in any other segments. Note that if the PCM interface of CH0a/CH1a is not used, PCMO_a will be placed in a high impedance state.

Note:
Because the PCMO_a pin is an open drain output pin, be sure to connect a pull-up resistor externally.
Also, do not use a pull-up voltage larger than the digital power supply voltage (DVDD).

PCMI_a
PCM signal input pin for CH0a/CH1a. It is shifted by a fall of BCLK, and input from the MSB.
If the PCM interface of CH0a/CH1a is not used, fix input at either "0" or "1".

PCMO_b
PCM signal output pin for CH0b/CH1b. It outputs a PCM signal in synchronization with the rise of BCLK or SYNC. Regarding output from PCMO_b, data will be output only in the applicable time slot segment according to the setting of the selected time slot position, and the output will be in a high impedance state in any other segments. Note that if the PCM interface of CH0b/CH1b is not used, PCMO_b will be placed in a high impedance state.

Note:
Because the PCMO_b pin is an open drain output pin, be sure to connect a pull-up resistor externally.
Also, do not use a pull-up voltage larger than the digital power supply voltage (DVDD).

PCMI_b
PCM signal input pin for CH0b/CH1b. It is shifted by a fall of BCLK, and input from the MSB.
If the PCM interface of CH0b/CH1b is not used, fix input at either "0" or "1".

BCLK
This is the shift clock input/output pin for the PCM signal that is common to CH0a/CH1a/CH0b/CH1b.
When CLKSEL is "0", it is necessary to input to this pin a clock signal synchronized with SYNC. Input a 128 kHz to 2.048 MHz clock. When CLKSEL is "1", this pin outputs a 2.048 MHz clock that is synchronous with SYNC.

SYNC
This is the 8 kHz sync signal input/output pin of PCM signals that is common to CH0a/CH1a/CH0b/CH1b. When CLKSEL is "0", constantly input an 8 kHz clock synchronized with BCLK. Further, when CLKSEL is "1", this pin outputs an 8 kHz clock synchronous with BCLK. Long frame synchronization is used when the SYNC frame contorl register (SYNC_SEL) is "0" and short frame synchronization is used when it is "1".

Note: The input/output control and frequencies of the above SYNC and BLCK signals will be as shown in Table 1 below.

Table 1 Input/Output Control of SYNC and BCLK

CLKSEL	SYNC	BCLK	Remarks
"0"	Input (8 kHz)	Input (128 kHz to 2.048 MHz)	Input a clock constantly after starting the power supply. Input a 128 kHz to 2.048 MHz clock.
"1"	Output (8 kHz)	Output (2.048 MHz)	A "L" level is output during the power down state.

CLKSEL
Input/output control input pin of SYNC and BCLK. When set to “0”, this pin is configured as input, and when set to “1”, it is configured as output.

SDO_a
Serial control output pin for CH0a/CH1a. If the serial control function of CH0a/CH1a is not used (SCNTEN = “0”), SDO_a will be placed in a high impedance state.

Note:
Because the SDO_a pin is an open drain output pin, be sure to connect a pull-up resistor externally.
Also, do not use a pull-up voltage larger than the digital power supply voltage (DVDD).

SDI_a
Serial control data input pin for CH0a/CH1a. If the serial control function of CH0a/CH1a is not used (SCNTEN = “0”), fix input at either “0” or “1”.

SDO_b
Serial control output pin for CH0b/CH1b. If the serial control function of CH0b/CH1b is not used (SCNTEN = “0”), SDO_b will be placed in a high impedance state.

Note:
Because the SDO_b pin is an open drain output pin, be sure to connect a pull-up resistor externally.
Also, do not use a pull-up voltage larger than the digital power supply voltage (DVDD).

SDI_b
Serial control input pin for CH0b/CH1b. If the serial control function of CH0b/CH1b is not used (SCNTEN = “0”), fix input at either “0” or “1”.

SCLK_a
Serial control clock input pin for CH0a/CH1a. If the serial control function of CH0a/CH1a is not used (SCNTEN = “0”), fix input at either “0” or “1”.

SCLK_b
Serial control clock input pin for CH0b/CH1b. If the serial control function of CH0b/CH1b is not used (SCNTEN = “0”), fix input at either “0” or “1”.

SDENB_a
Serial control data enable input pin for CH0a/CH1a. If the serial control function of CH0a/CH1a is not used, fix input at either “0” or “1”.

SDENB_b
Serial control data enable input pin for CH0b/CH1b. If the serial control function of CH0b/CH1b is not used, fix input at either “0” or “1”.

SCNTEN
Pin for enabling serial control interfaces. To use the serial control interfaces, set this pin to “1”. If the serial control interfaces will not be used, fix this pin at “0”.

GPIOA[1:0]_a
General-purpose input/output port A[1:0] for CH0a/CH1a. As the secondary functions of GPIOA[1:0]_a, the dial pulse output pin for CH1a (DPO1a) and the dial pulse output pin for CH0a (DPO0a) are assigned. For unused general-purpose input/output ports, fix inputs at either “0” or “1”.

GPIOB[3:0]_a
General-purpose input/output port B[3:0] for CH0a/CH1a. If the dial pulse detector is activated, GPIOB[1:0]_a is used as the dial pulse inpt pin for CH1a (DPI1a) or the dial pulse inpt pin for CH0a (DPI0a). For unused general-purpose input/output ports, fix inputs at either “0” or “1”.

GPIOC[7:0]_a
General-purpose input/output port C[7:0] for CH0a/CH1a. For unused general-purpose input/output ports, fix inputs at either “0” or “1”.

GPIOA[1:0]_b
General-purpose input/output port A[1:0] for CH0b/CH1b. As the secondary functions of GPIOA[1:0]_b, the dial pulse output pin for CH1b (DPO1b) and the dial pulse output pin for CH0b (DPO0b) are assigned. For unused general-purpose input/output ports, fix inputs at either “0” or “1”.

GPIOB[3:0]_b
General-purpose input/output port B[3:0] for CH0b/CH1b. If the dial pulse detector is activated, GPIOB[1:0]_b is used as the dial pulse input pin for CH1b (DPI1b) or the dial pulse input pin for CH0b (DPI0b). For unused general-purpose input/output ports, fix inputs at either “0” or “1”.

GPIOC[7:0]_b
General-purpose input/output port C[7:0] for CH0b/CH1b. For unused general-purpose input/output ports, fix inputs at either “0” or “1”.

DVDD[6:0], AVDD[1:0]
These are power supply pins. DVDD[6:0] is the power supply pin for the digital circuits and AVDD[1:0] is the power supply pin for the analog circuits of the LSI. Connect these pins together in the neighborhood of the LSI and connect as bypass capacitors a 10 μF electrolytic capacitor and a 0.1 μF ceramic capacitor in parallel between the DGND and AGND pins.

DGND[6:0], AGND[1:0]
These are ground pins. DGND[6:0] is the ground pin for the digital circuits and AGND[1:0] is the ground pin for the analog circuits of the LSI. Connect these pins together in the neighborhood of the LSI.

VREGOUT[6:0]
Internal regulator voltage (approximately 2.5 V) output pin.
Connect a ceramic capacitor of about 0.1 μF in parrael to a ceramic tantalum capacitor of about 10 μF between the VREGOUT2 pin and the ground pin. Connect a ceramic capacitor of about 0.1 μF between each of the VREGOUT pins other than the VREGOUT2 pin, and the ground pin.

VBG
Reference voltage output pin for the internal regulator.
Connect a multilayer ceramic capacitor of about 150 pF between this pin and the ground pin.

TST[3:0]
Input pin for testing. Keep the inputs to these pins at the “0” level during normal use conditions.

FUNCTIONAL DESCRIPTION

MCU Interfaces

(1) Overview
This LSI has two MCU interfaces: one for CH0a/CH1a and the other for CH0b/CH1b.
Each MCU interface consists of control registers, transmit and receive buffers, frame and DMA controllers that control access to the transmit and receive buffers, and a DSP firmware downloader.

(2) Control Registers
A. Overview
This LSI has the following control registers:
- CR0a–CR47a control registers for performing various controls, status notification and others of CH0a/CH1a
- GPCR0a–GPCR8a control registers for general–purpose input/output ports
- DLCR0a–DLCR5a control registers for DSP firmware downloading
- CR0b–CR47b control registers for performing various controls, status notification and others of CH0b/CH1b
- GPCR0b–GPCR8b control registers for general–purpose input/output ports
- DLCR0b–DLCR5b control registers for DSP firmware downlaoding

For more information about addresses and descriptions of control registers, see the Control Register List and each section on control register description described later.

B. Access method
The control registers can be accessed via a parallel bus interface or via the serial control interfaces described later. The data width when accessing the control registers via a parallel bus interface must be 8-bit width of D7–D0. If a FIFO is accessed in 16-bit access mode, the inputs/outputs of D15–D8 depend on the write and read controls to the control registers. Either “1” or “0” is input to D15–D8 when writing, and “1” is read when reading. Figure 12 shows the control method of the control registers.
For information about the method of accessing the control registers via serial control interfaces, see the section on serial control interfaces described later.

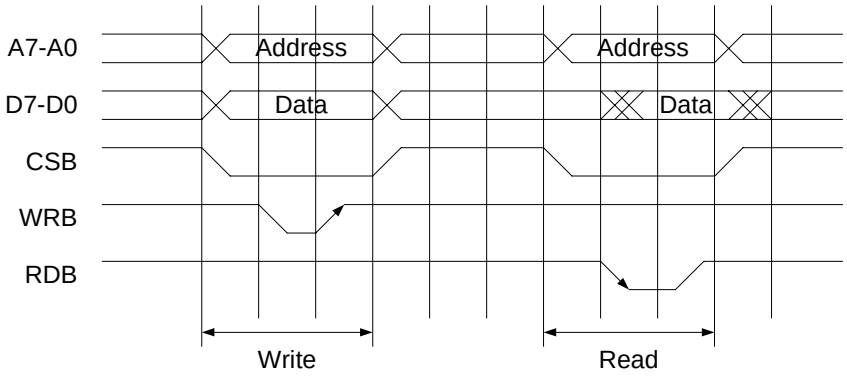


Figure 12 Method of Controlling The Control Registers

(3) Transmit and Receive Buffers

A. Number of embedded transmit and receive buffers

This LSI is embedded with two systems of transmit and receive buffers: TX-FIFOa/RX-FIFOa for CH0a/CH1a, and TX-FIFOb/RX-FIFOb for CH0b/CH1b.

B. Control parameters of transmit and receive buffers

Table 2 lists the controllable parameters of the transmit and receive buffers.

The control parameters listed below can be set individually for TX-FIFOa/RX-FIFOa (transmit and receive buffers for CH0a/CH1a) and TX-FIFOb/RX-FIFOb (transmit and receive buffers for CH0b/CH1b).

Table 2 Controllable Parameters of Transmit and Receive Buffers

Item		Changeable parameter	Initial value	Remarks
Buffering time	Tx	10 ms / 20 ms	10 ms	The number of transmit buffer words is automatically changed by the setting of the buffering time on the transmitter side.
	Rx	10 ms / 20 ms	10 ms	The number of receive buffer words is automatically changed by the setting of the buffering time on the receiver side.
Access method		Frame / DMA	Frame	
FIFO data width		16 bits / 8 bits	16 bits	The number of words is automatically changed by the data width.

C. Transmit and Receive Buffer Sizes

The transmit and receive buffers have a double buffer configuration of the FIFO (First In First Out) type, and one buffer can buffer 10 or 20 milliseconds' worth of data.

As shown in Table 3, the number of FIFO words is automatically changed by the settings of the FIFO data width and buffering time.

Table 3 Buffer Size and Number of Words of Transmit and Receive Buffers

Speech CODEC	10 ms mode			20 ms mode		
	Buffer size	16-bit	8-bit	Buffer size	16-bit	8-bit
G.711 (64 kbps)	80 bytes	40 words	80 words	160 bytes	80 words	160 words

D. Structure of Transmit and Receive Buffers

Examples of timings of accessing the transmit and receive buffers are shown in Figure 13.
Although both the transmit and the receive buffers have a double buffer structure, the buffer to be accessed from the MCU side is automatically switched at every buffering time or by the completion of reading or writing of the specified number of words. Therefore, when accessing from the MCU side, the transmit or receive buffer can be accessed as one buffer.

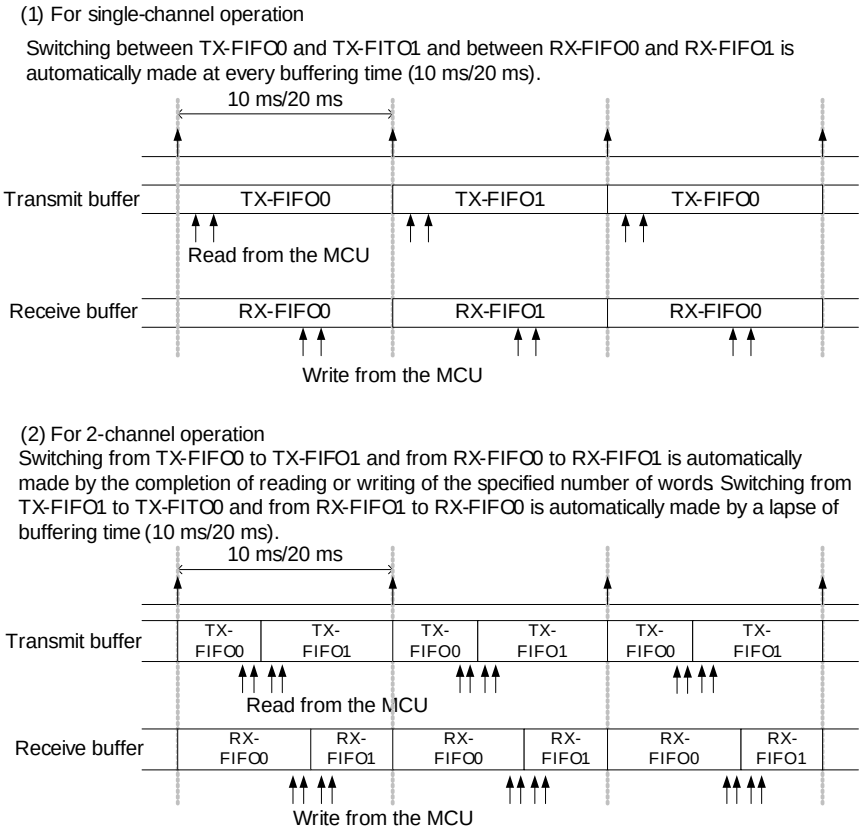


Figure 13 Timings of Accessing the Transmit and Receive Buffers (Example)

E. Data Width Selection (16-Bit Mode, 8-Bit Mode)

As for the data width used to access the transmit and receive buffers, either 16 bits or 8 bits can be selected. Select the data width used to access the transmit and receive buffers for CH0a/CH1a (TX-FIFOa/RX-FIFOa) with the MCU interface data width selection register_a (BW_SELa), and the transmit/receive buffer for CH0b/CH1b (TX-FIFOb/RX-FIFOb) with the MCU interface data width selection register_b (BW_SELb).
During the 16-bit mode, the access is made with a data width of 16 bits and the data bits D15 to D0 are accessed. In the 8-bit mode, the transmit and receive data are input or output to D7 to D0. During the 8-bit access mode, the bits D15 to D8 will always be in the input state.

F. Data Storage Format

The data storage formats for the transmit and receive buffers are shown in Figure 14.

1) G.711 (64 kbps)

G.711 (64 kbps, μ-law/A-law)
8 bits/125 μs
Buffer configuration
80 samples/10 ms
160 samples/20 ms

PCM coding configuration

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0

Word configuration

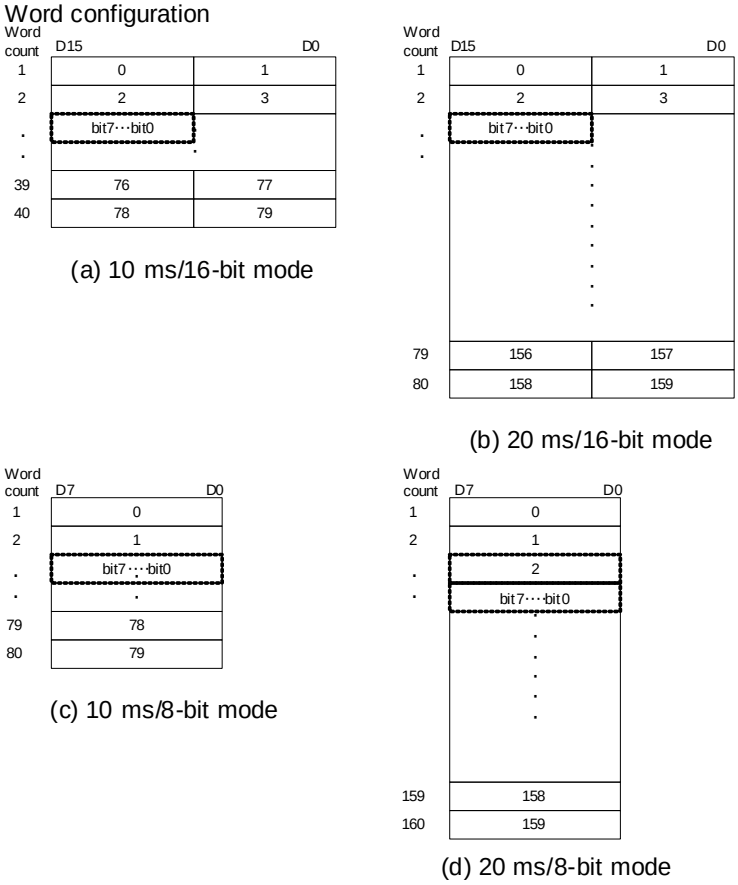


Figure 14 G.711 Data Format

(4) Frame/DMA Access

As for access to the transmit and receive buffers, either the frame mode or DMA mode can be selected.
Select access to the transmit and receive buffers for CH0a/CH1a (TX-FIFOa/RX-FIFOa) with the FRAME/DMA selection register_a (FD_SELa), and the transmit/receive buffer for CH0b/CH1b (TX-FIFOb/RX-FIFOb) with the FRAME/DMA selection register_b (FD_SELb).
The following describes the access methods in both the frame mode and DMA mode using access to the transmit and receive buffers for CH0a/CH1a as an example.

Note:
Access to the transmit and receive buffers can only be made via a parallel bus interface. Note that access via a serial control interface cannot be made.

A. When in the Frame Mode (FRAME/DMA selection register_a (FD_SELa) = “0”)
The control timing of the transmit buffer and the method of accessing it during the frame mode are shown in Figure 15.
When the transmit buffer, which stores the compressed speech data of the transmitting side (the speech compressing side), becomes full, FR0Ba goes to a “L” level from “H”, so that a read request is issued to the MCU. Read the data in the transmit buffer during the following timing. The read address of the transmit buffer is “80h.”
Also, FR0Ba holds a “L” level until either all data in the transmit buffer have been read or the valid read period corresponding to the buffering time selected by the transmit buffering time selection register (TXBUF_TIM_a) is complete.

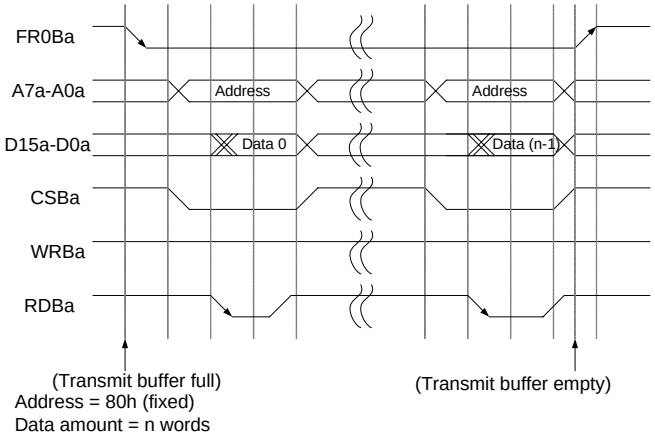


Figure 15 Transmit Buffer Control Timing

The receive buffer control timing during the frame mode is shown in Figure 16.
When the receive buffer, which stores the compressed speech data of the receiving side (the speech expanding side), becomes empty, FR1Ba goes to a “L” level from “H”, so that a write request is issued to the MCU. Write data into the receive buffer during the following timing. The write address of the receive buffer is “81h.” FR1Ba holds a “L” level until either the receive buffer has been written to its full capacity or the valid write period corresponding to the buffering time selected by the receive buffering time selection register (RXBUF_TIM_a) is complete.

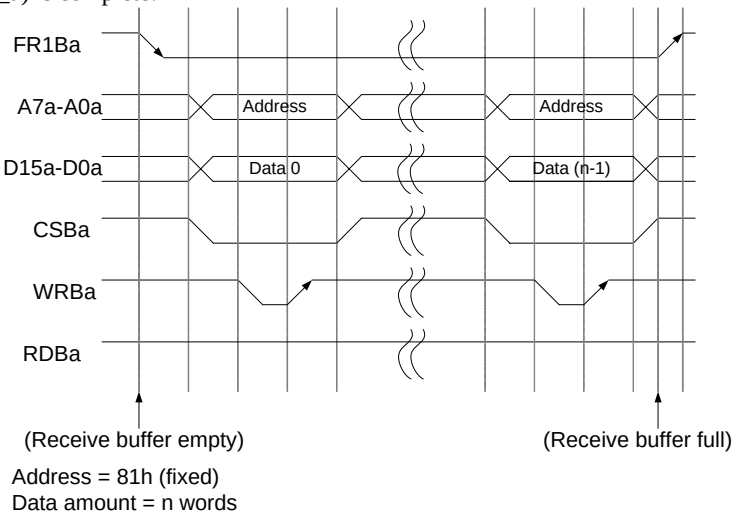


Figure 16 Receive Buffer Control Timing

B. When in the DMA mode (FRAME/DMA selection register_a (FD_SELa) = "1")
The transmit buffer control timing during the DMA mode is shown in Figure 17. When the transmit buffer, which stores the compressed speech data of the transmitting side (the speech compressing side), becomes full, DMARQ0Ba goes to a "L" level from "H", so that a DMA request is issued to the MCU. After the DMA request is made, an acknowledge is input when DMAACK0Ba goes to the "0" state from "1", and also, this DMARQ0Ba will be cleared automatically ("L" → "H") when a falling edge of the read enable signal is accepted (RDBa = "1" → "0"). Read the data in the transmit buffer at the following timing simultaneously with the acknowledgement input. DMARQ0Ba repeats a DMA request until either all data in the transmit buffer have been read or the valid read period corresponding to the buffering time selected by the transmit buffering time selection register (TXBUF_TIM_a) is complete.

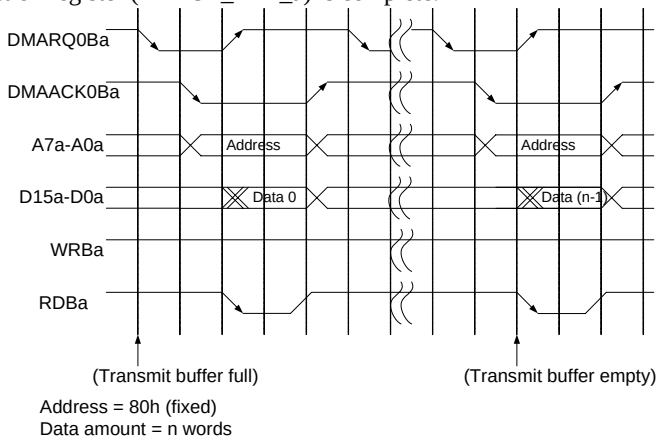


Figure 17 Transmit Buffer Control Timing during DMA Mode

The receive buffer control timing during the DMA mode is shown in Figure 18. When the receive buffer, which stores the compressed speech data of the receiving side (the speech compressing side), becomes empty, DMARQ1Ba goes to a "L" level from "H", so that a DMA request is issued to the MCU. After the DMA request is made, an acknowledge is input when DMAACK1Ba goes to the "0" state from "1", and also, this DMARQ1Ba will be cleared automatically ("L" → "H") when a falling edge of the write enable signal is accepted (WRBa = "1" → "0"). Write data into the receive buffer at the following timing simultaneously with the acknowledgement input. DMARQ1Ba repeats a DMA request until either all data in the receive buffer have been read or the valid read period corresponding to the buffering time selected by the receive buffering time selection register (TXBUF_TIM_a) is complete.

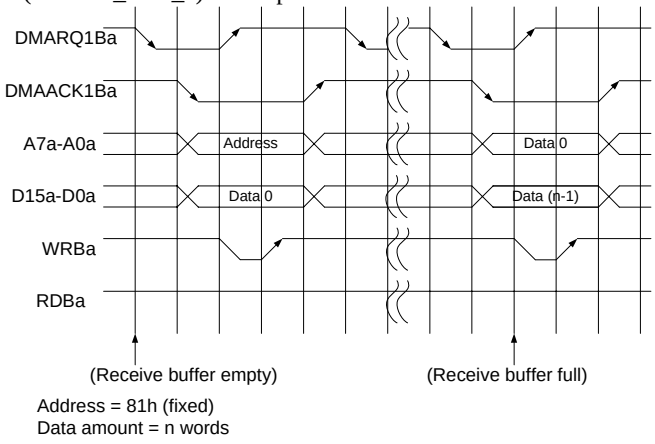


Figure 18 Receive Buffer Control Timing during DMA Mode

(5) DSP Firmware Download Function

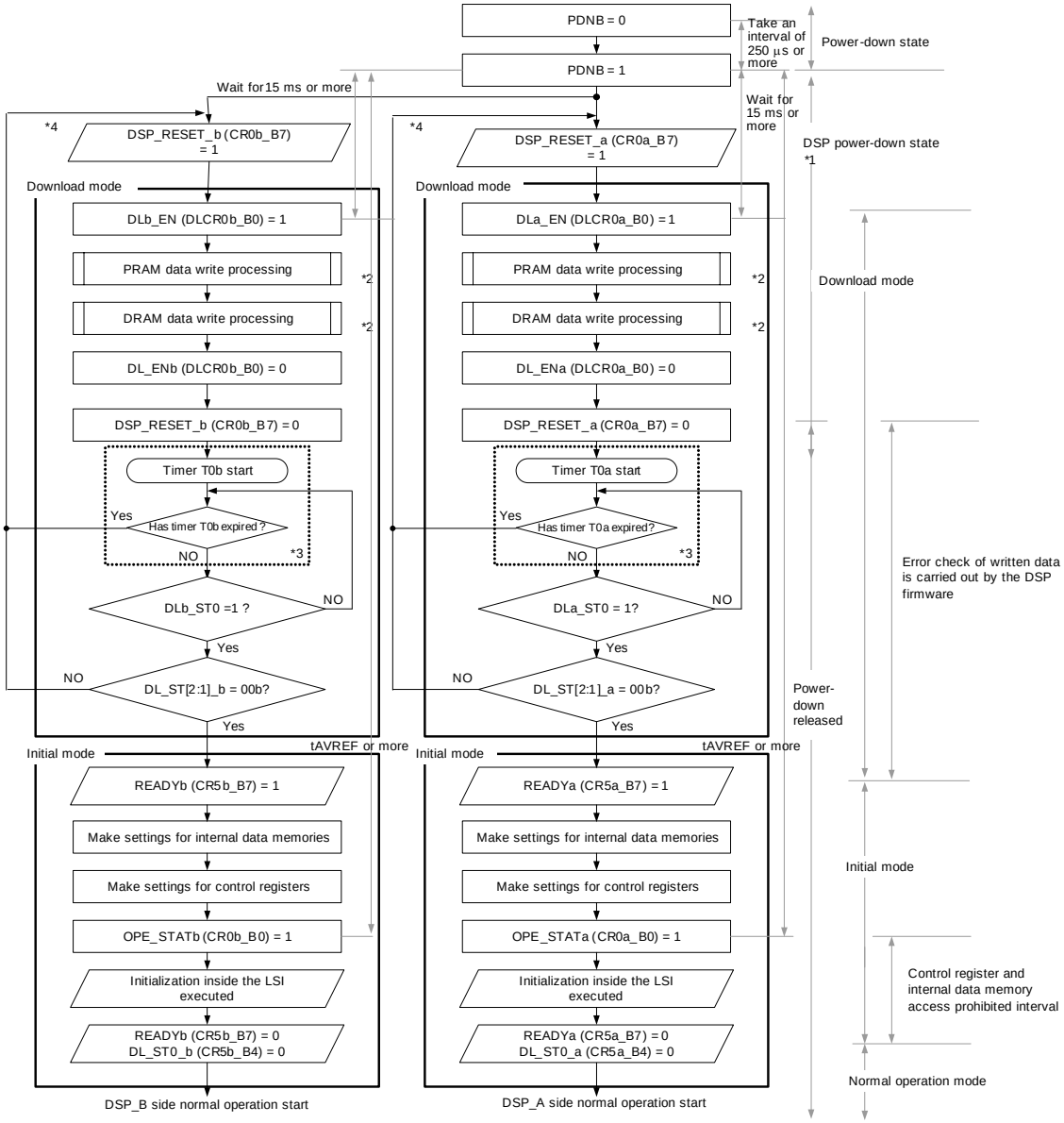
A. Overview
This LSI has internal registers for downloading the DSP firmware: DLCR0a–DLCR5a on the DSP_A side, and DLCR0b–DLCR5b on the DSP_B side. Download the DSP firmware by accessing these registers via a parallel bus interface or serial control interfaces.

B. Control Registers for Download
See the section describing control registers.

C. Download Control Flow
Figures 19 and 20 show control flows for downloading the DSP firmware.
Note that it is necessary to download the DSP firmware (write to PRAM/DRAM) for each of the DSP_A side and DSP_B side.

If hardware power down is canceled (PDNB = "0"→"1"), this LSI is activated in the DSP power-down state (DSP_RESET_a = 1, DSP_RESET_b = 1). Activate the download circuit in this state, write data to PRAM, and write to DRAM. Once writing is complete, stop the download circuit, and cancel the DSP power down state (DSP_RESET_a = 0, DSP_RESET_b = 0).
Succeedingly, the DSP firmware performs error check of written data, and the check result is stored in DL_ST[2:0]a (CR5a-B[6:4]) and DL_ST[2:0]b (CR5b-B[6:4]). However, if the DSP firmware has not been written normally, it is possible that the error check of written data itself may not finish. Therefore, monitor a certain time period (1 sec) or longer from the cancellation of a DSP power down state outside the LSI. If the result of an error check is not posted after a certail time period has elapsed, set to DSP power down state, and write the DSP firmware again.

If the DSP firmware has been written normally, after the completion of an error check, both the initial mode display register_a (READYa) and initial mode display register_b (READYb) are set to "1", thus a initial mode state is entered. Make various settings to the internal data memories and control regisers when in the initial mode, and set both the operation start control register_a (OPE_STATa) and operation start control register_b (OPE_STATb) to "1". Once initialization inside the LSI is complete, both the initial mode display register_a (READYa) and initial mode display register_ b (READYb) are cleared to "0", thus, transitioning to the normal operation mode



*1: In the power-down state, the circuits are placed in a reset state except for the following blocks OSC, VREF, PLL downloader circuit, and serial control circuit

*2: For PRAM data write processing and DRAM data write processing see Figure 20, "PRAM/DRAM Write Control Flow".

*3: Timer T0 is used to monitor normal termination of write error checking performed by the DSP firmware Specify 1 second or longer as the timer value.

*4: If a write error occurs, reset the DSP of the error side by writing DSPa_RESET (CR0a_B7) = 1 and DSPb_RESET (CR0b_B7) = 1 from the CPU side

Figure 19 DSP Firmware Write Control Flow

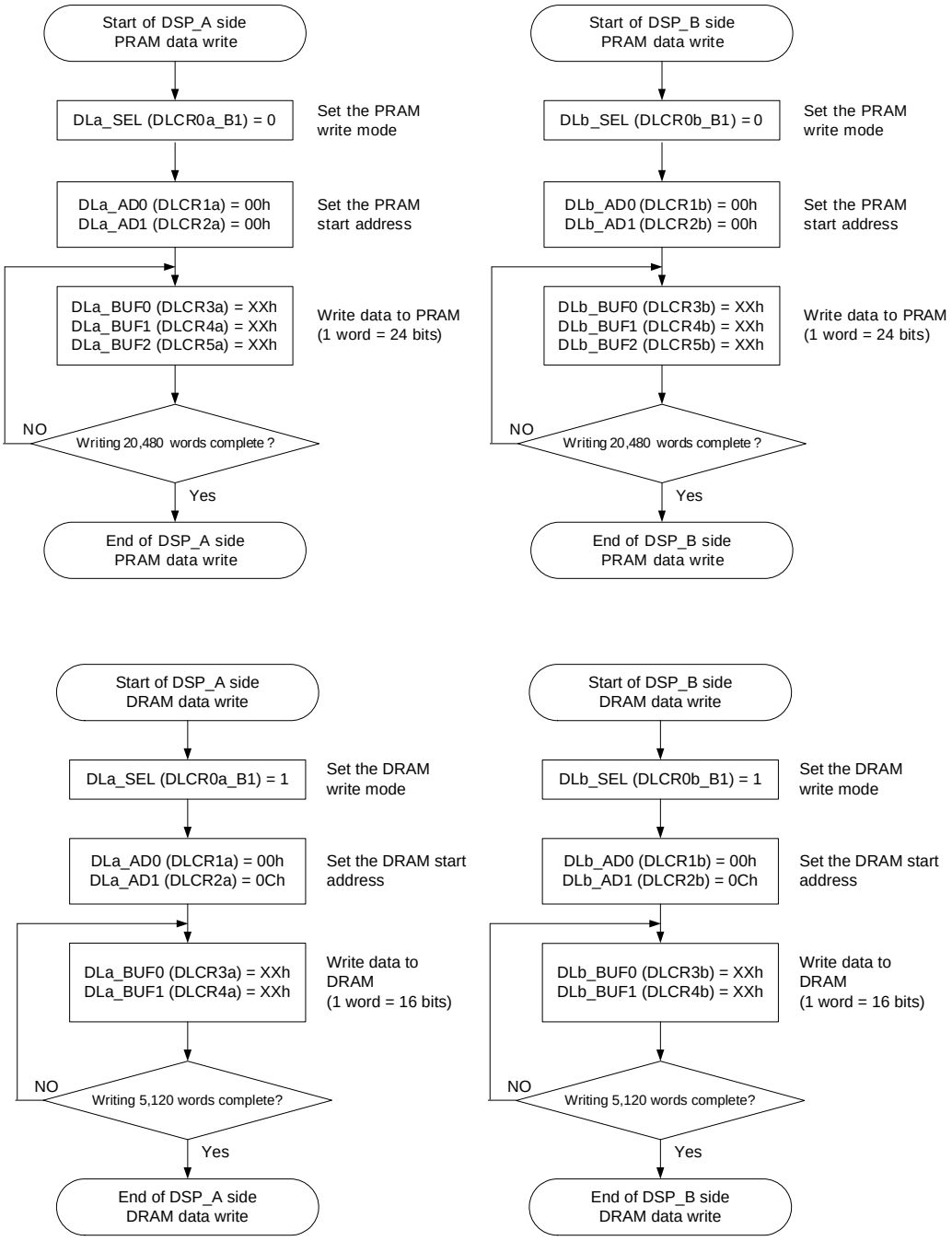


Figure 20 PRAM/DRAM Write Control Flow

Control Methods of Transmit and Receive Buffers

There are four operating states of a speech codec, depending on the settings in the following two registers:

- Speech codec-CH0 control register (SC_CH0EN)
- Speech codec-CH1 control register (SC_CH1EN)

The four oparting states are “stop state,” “single-channel operating state-CH0,” “single-channel operating state-CH1,” and “2-channel operating state CH0&CH1.” Figure 21 is the transition diagram of the operation status of a speech codec.

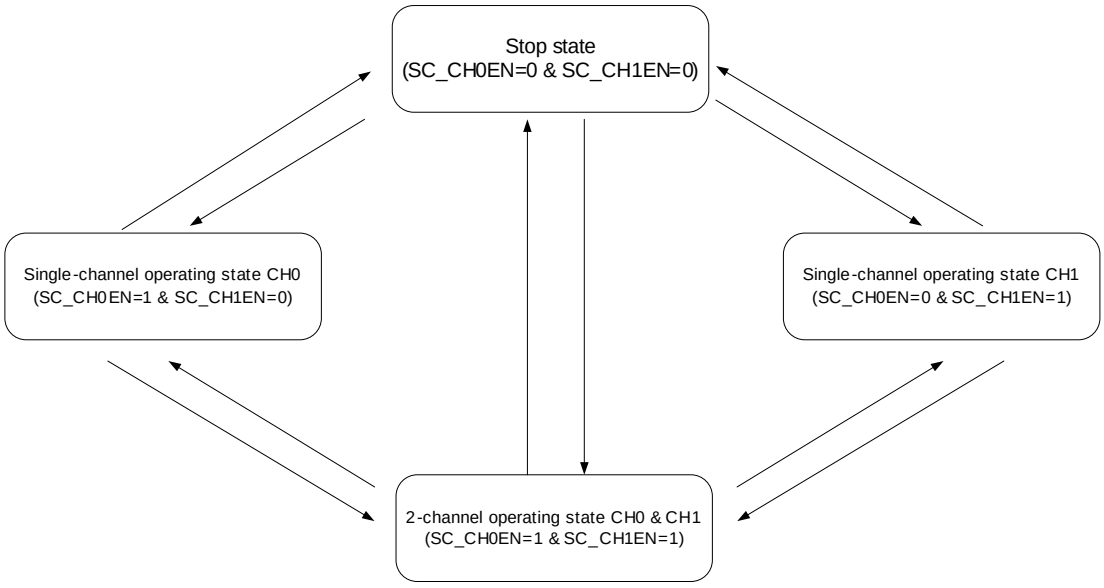


Figure 21 Speech Codec Operation Status Transition Diagram

(1) G.711 (μ-law/A-law) 10 ms mode: single-channel operation (CH0)

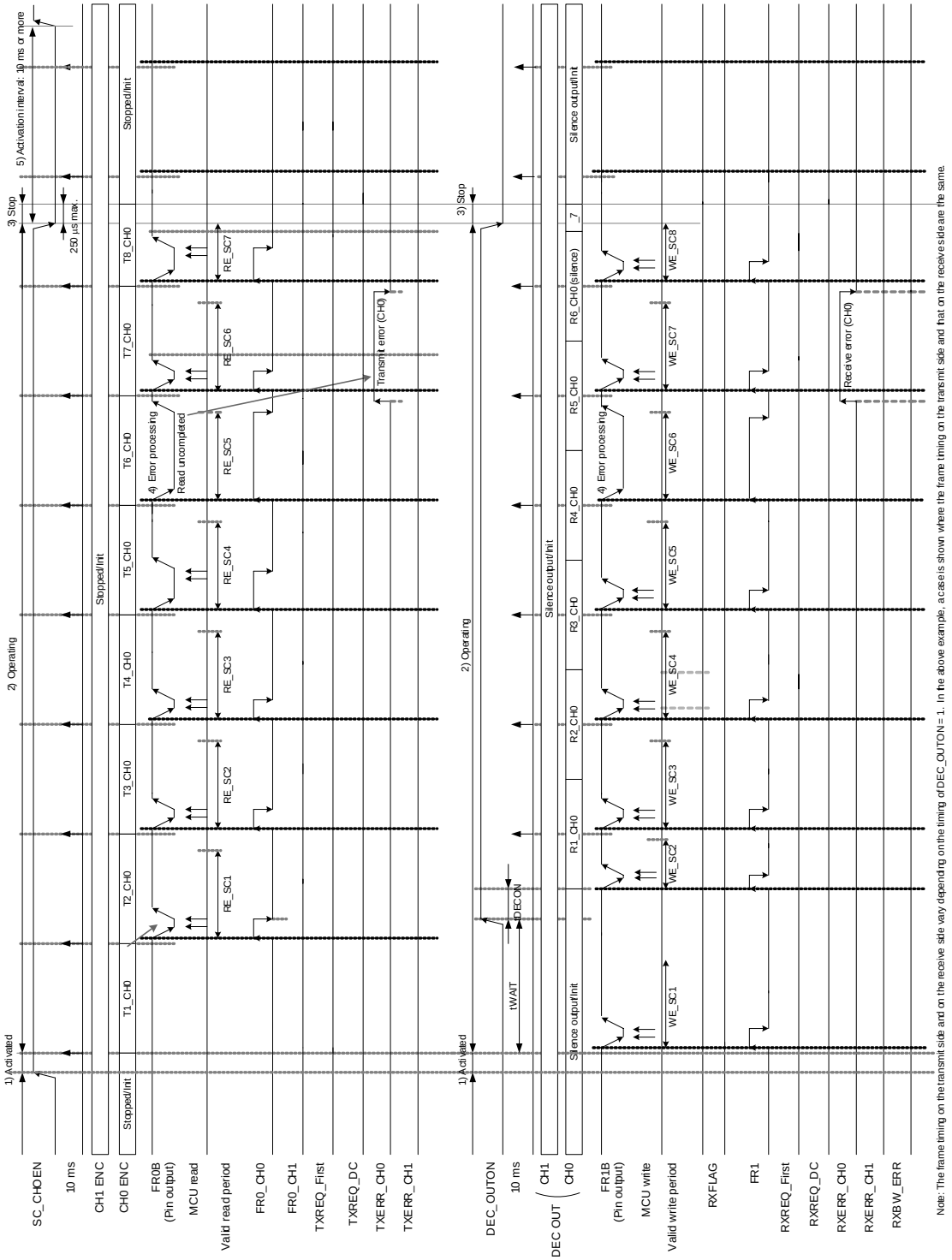


Figure 22 G.711 (μ-law/A-law) 10 ms Mode: Control Timing of Single-Channel Operation (CH0)

Operational Description

[Transmitting side]
1) Activated
Set DEC_OUTON to “0” and SC_CH0EN “0” → “1”
The speech codec is activated within a maximum of 250 μs after SC_CH0EN has been set to "1".
The encoder is activated in the already initialized condition and starts encoding the CH0 transmit data immediately after the speech codec is activated.

2) Operating
The data encoded in the encoding segment Tn_CH0 is read out within the valid read period RE_SCn by the MCU. This operation is repeated until stopping. (n = 1, 2, 3, 4, ...)

3) Stop
Set SC_CH0EN “1” → “0” and DEC_OUTON “1” → “0”.
Encoding after stop is invalid.
Within a maximum of 250 μs after SC_CH0EN has been set to "0", the encoder stops writing data into the transmit buffer.

4) Error processing (transmit error)
An example of transmit error occurrence is shown in valid read period RE_SC5.
If reading of data is not finished within the valid read period, TXERR_CH0 becomes "1".
The state of TXERR_CH0 is maintained during and after the next valid read period until immediately before the frame during which data is normally read from the transmit buffer is terminated.
Even when the data read-out is not finished, the data in the transmit buffer will be updated as usual.

5) Activation interval
An interval of 10.0 ms or more is necessary after the speech codec has stopped before it is activated again.

Valid read period:
Complete the data read-out from the transmit buffer within 9.0 ms from the falling edge of FR0B or after FR_CH0 changes from “0” to “1”.

[Receiving side]
1) Activated
Set DEC_OUTON to “0” and SC_CH0EN “0” → “1”
The speech codec is activated within a maximum of 250 μs after SC_CH0EN has been set to "1".
The decoder performs initialization and outputs silence data after a speech codec is started.
If the first receive data has been written and the tWAIT wait time has elapsed, the decoder can set the decode output control register (DEC_OUTON) to “1”(tWAIT = 2.0 ms).
After setting DEC_OUTON to “1”, the decoder outputs silence data for about 3.75 (+tDECON) ms, and then starts decode output.
However, if the PLC function has been disabled, the decoder starts decode output tDECON ms after setting DEC_OUTON to “1”. Note that by setting in the internal data memory for controlling the decode output start offset time (DEC_ONTIM), the decode output start offset time (tDECON) can be adjusted between 0.0 and 32 ms.
(tDECON: initial value = 0 ms; unit of setting: 125 μs; allowable range of setting : 0.0 to 32 ms)

Note:
To set DEC_OUTON to “1” simultaneously with SC_CH0EN = “1” (starting a speech codec), set in advance so that the internal data memory for controlling the decode output start offset time (DEC_ONTIM) is between 0010h (2.0 ms) and 0100h (32 ms). Upon completion of writing the first receive data and a lapse of the above offset time after starting a speech codec, the decoder starts decode output.

2) Operating

The data written by the MCU in the valid write period WE_SCn is output in decode output segment Rn_CH0. This operation is repeated until stopping. (n = 1, 2, 3, 4, ...)

3) Stop

Set SC_CH0EN "1" → "0" and DEC_OUTON "1" → "0".
Decoding after stop is invalid.
Within a maximum of 250 μs after SC_CH0EN has been set to "0", the decoder stops and outputs silence data.

4) Error processing (receive error)

An example of receive error occurrence is shown in the valid write period WE_SC6.
If writing of data is not finished within the valid write period, RXERR_CH0 becomes "1".
The state of RXERR_CH0 is maintained during and after the next valid write period until immediately before the frame during which data is normally written to the receive buffer is terminated.
If an error has occurred in the valid write period WE_SC6, generated data is output according to the PLC (Packet Loss Concealment) algorithm defined in G.711 Appendix I in the decode output segment R6_CH0. However, silence data is output if the G.711 PLC function is disabled.

5) Activation interval

An interval of 10.0 ms or more is necessary after the speech codec has stopped before it is activated again.

Valid write period

There is no time limit for the first valid write period WE_SC1 after starting a speech codec.
In the valid write period WE_SC2, finish a write to the receive buffer within 2.0 ms from a fall of FR1B, or after FR1 changes from "0" to "1".
In the valid write period WE_SC3 and succeeding segments, finish a write to the receive buffer within 9.0 ms from a fall of FR1B, or after FR1 changes from "0" to "1".

Note:
This operational description is pertaining to the case of the 10 ms mode; in the 20 ms mode, the valid read period and valid write period are as follows:
Valid read period:

Finish a read from the transmit buffer within 18.0 ms from a fall of FR0B, or after FR0_CH0 changes from "0" to "1".

Valid write period:

There is no time limit for the first valid write period WE_SC1 after starting a speech codec.
In the valid write period WE_SC2, finish a write to the receive buffer within 12.0 ms from a fall of FR1B, or after FR1 changes from "0" to "1".
In the valid write period WE_SC3 and succeeding segments, finish a write to the receive buffer within 18.0 ms from a fall of FR1B, or after FR1 changes from "0" to "1".

(2) G.711 (μ-law/A-law) 10 ms mode: single-channel operation (CH1)

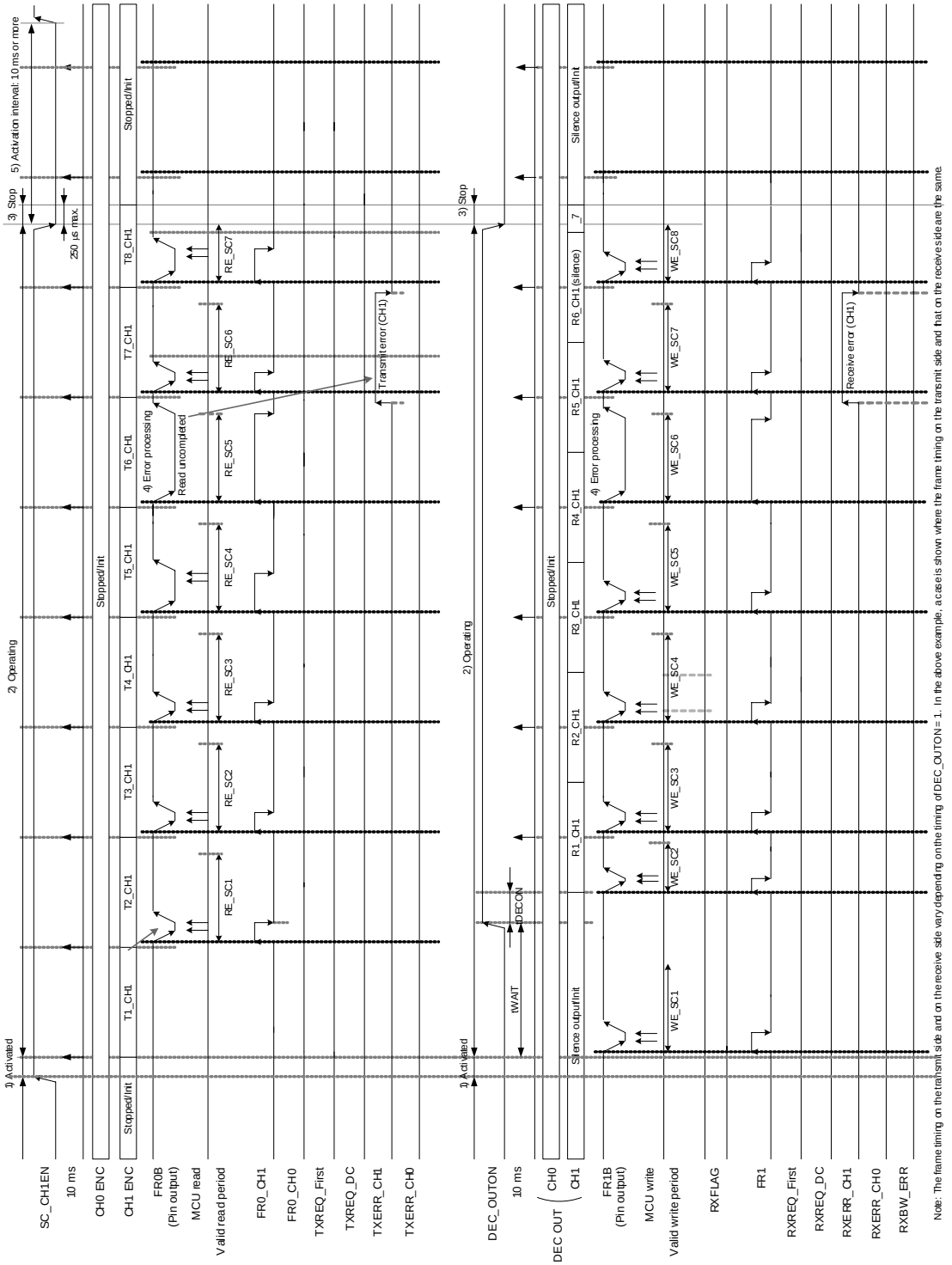


Figure 23 G.711 (μ-law/A-law) 10 ms Mode: Control Timing of Single-Channel Operation (CH1)

Operational Description

[Transmitting side]
1) Activated
DEC_OUTON “0”, SC_CH1EN “0” → “1”
The speech codec is activated within a maximum of 250 μs after SC_CH1EN has been set to "1".
The encoder is activated in the already initialized condition and starts encoding the CH1 transmit data immediately after the speech codec is activated.

2) Operating
The data encoded in the encoding segment Tn_CH1 is read out within the valid read period RE_SCn by the MCU. This operation is repeated until stopping. (n = 1, 2, 3, 4, ...)

3) Stop
Set SC_CH1EN “1” → “0”, DEC_OUTON “1” → “0”.
Encoding after stop is invalid.
Within a maximum of 250 μs after SC_CH1EN has been set to "0", the encoder stops writing data into the transmit buffer.

4) Error processing (transmit error)
An example of transmit error occurrence is shown in valid read period RE_SC5.
If reading of data is not finished within the valid read period, TXERR_CH1 becomes "1".
The state of TXERR_CH1 is maintained during and after the next valid read period until immediately before the frame during which data is normally read from the transmit buffer is terminated.
Even when the data read-out is not finished, the data in the transmit buffer will be updated as usual.

5) Activation interval
An interval of 10.0 ms or more is necessary after the speech codec has stopped before it is activated again.

Valid read period:
Complete the data read-out from the transmit buffer within 9.0 ms from the falling edge of FR0B or after FR_CH1 changes from “0” to “1”.

[Receiving side]
1) Activated
DEC_OUTON “0”, SC_CH1EN “0” → “1”
The speech codec is activated within a maximum of 250 μs after SC_CH1EN has been set to "1".
The decoder performs initialization and outputs silence data after a speech codec is started.
If the first receive data has been written and the tWAIT wait time has elapsed, the decoder can set the decode output control register (DEC_OUTON) to “1”(tWAIT = 2.0 ms).
After setting DEC_OUTON to “1”, the decoder outputs silence data for about 3.75 (+tDECON) ms, and then starts decode output.
However, if the PLC function has been disabled, the decoder starts decode output tDECON ms after setting DEC_OUTON to “1”. Note that by setting in the internal data memory for controlling the decode output start offset time (DEC_ONTIM), the decode output start offset time (tDECON) can be adjusted between 0.0 and 32 ms.
(tDECON: initial value = 0 ms; unit of setting: 125 μs; allowable range of setting : 0.0 to 32 ms)

Note:
To set DEC_OUTON to “1” simultaneously with SC_CH1EN = “1” (starting a speech codec), set in advance so that the internal data memory for controlling the decode output start offset time (DEC_ONTIM) is between 0010h (2.0 ms) and 0100h (32 ms). Upon completion of writing the first receive data and a lapse of the above offset time after starting a speech codec, the decoder starts decode output.

2) Operating

The data written by the MCU in the valid write period WE_SCn is output in decode output segment Rn_CH1. This operation is repeated until stopping. (n = 1, 2, 3, 4, ...)

3) Stop

Set SC_CH1EN "1" → "0", DEC_OUTON "1" → "0".
Decoding after stop is invalid.
Within a maximum of 250 μs after SC_CH1EN has been set to "0", the decoder stops and outputs silence data.

4) Error processing (receive error)

An example of receive error occurrence is shown in the valid write period WE_SC6.
If writing of data is not finished within the valid write period, RXERR_CH1 becomes "1".
The state of RXERR_CH1 is maintained during and after the next valid write period until immediately before the frame during which data is normally written to the receive buffer is terminated.
If an error has occurred in the valid write period WE_SC6, generated data is output according to the PLC (Packet Loss Concealment) algorithm defined in G.711 Appendix I in the decode output segment R6_CH1.
However, silence data is output if the G.711 PLC function is disabled.

5) Activation interval

An interval of 10.0 ms or more is necessary after the speech codec has stopped before it is activated again.

Valid write period

There is no time limit for the first valid write period WE_SC1 after starting a speech codec.
In the valid write period WE_SC2, finish a write to the receive buffer within 2.0 ms from a fall of FR1B, or after FR1 changes from "0" to "1".
In the valid write period WE_SC3 and succeeding segments, finish a write to the receive buffer within 9.0 ms from a fall of FR1B, or after FR1 changes from "0" to "1".

Note:
This operational description is pertaining to the case of the 10 ms mode; in the 20 ms mode, the valid read period and valid write period are as follows:
Valid read period:

Finish a read from the transmit buffer within 18.0 ms from a fall of FR0B, or after FR0_CH1 changes from "0" to "1".

Valid write period:

There is no time limit for the first valid write period WE_SC1 after starting a speech codec.
In the valid write period WE_SC2, finish a write to the receive buffer within 12.0 ms from a fall of FR1B, or after FR1 changes from "0" to "1".
In the valid write period WE_SC3 and succeeding segments, finish a write to the receive buffer within 18.0 ms from a fall of FR1B, or after FR1 changes from "0" to "1".

(3) G.711 (μ-law/A-law) 10 ms mode: 2-channel processing upon and after activation

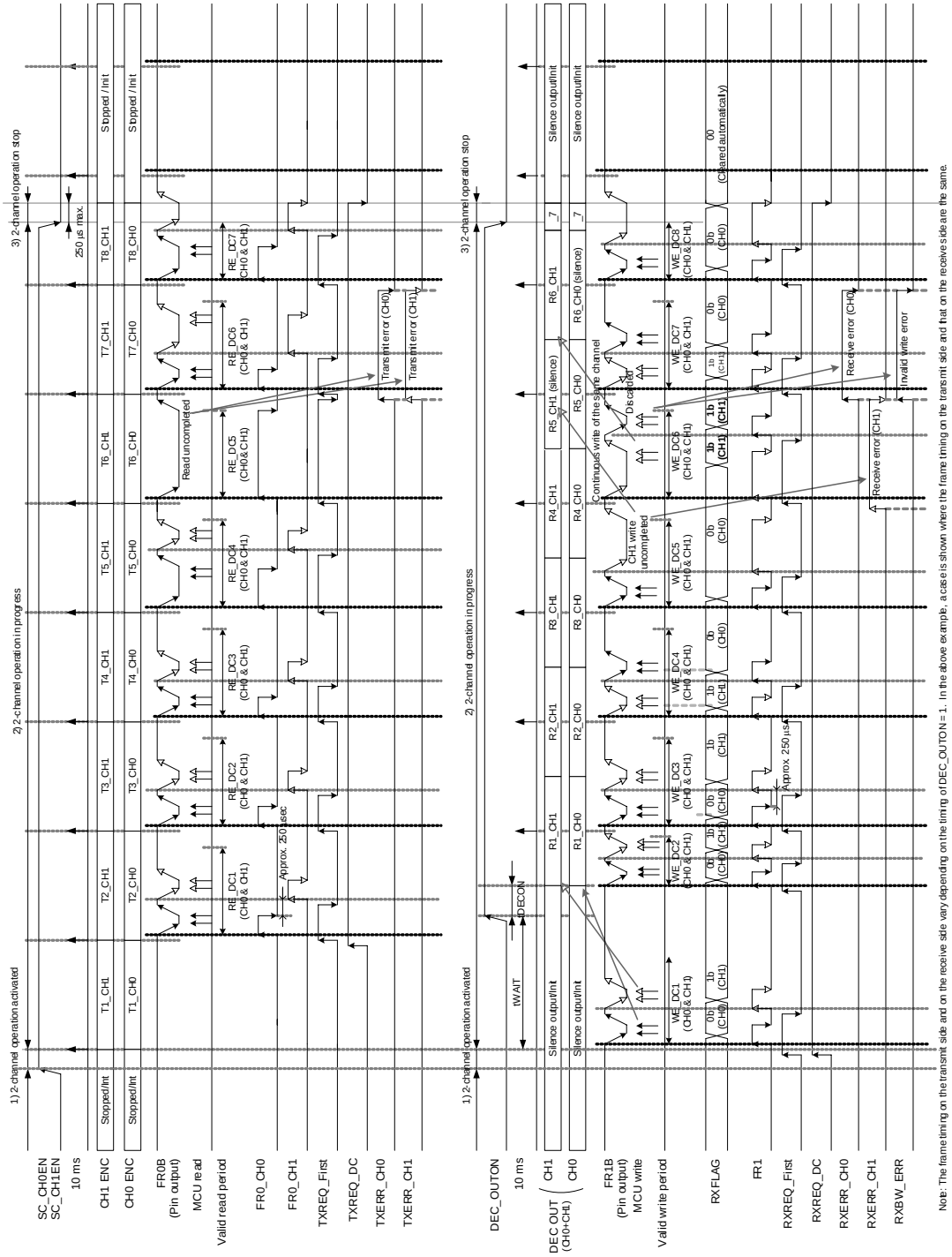


Figure 24 G.711 (μ-law/A-law) 10 ms Mode: Control Timing of 2-Channel Processing upon and after Activation

Operational Description

1) 2-channel operation activated

To activate a 2-channel operation from the stop state of a speech codec, set both SC_CH0EN and SC_CH1EN to “1” at the same time.

Encoder:

Starts encoding transmit data of CH0 and CH1 within a maximum of 250 μsec after SC_CH0EN and SC_CH1EN are set to “1”.

Decoder:

Makes a request to write receive data within a maximum of 250 μsec after SC_CH0EN and SC_CH1EN are set to “1”.

2) 2-channel operation in progress

■ Transmission

- 2-channel transmit request status notification register (TXREQ_DC)

  While a request to read transmit data is being made twice in one frame, the 2-channel transmit request status notification register (TXREQ_DC) is set to “1”.

- Order of channels to read

  Two requests to read transmit data are made in the order of CH0 and then CH1 within one frame. However, if a read from the MCU side does not finish for a CH0 transmit data read request, a request to read CH1 transmit data will not be generated.

- Reading procedure

  Once the encoding processing for one frame of each of the CH0 and CH1 signals is finished, a CH0 transmit data read request will be made as FR0_CH0 = 1 (FR0B = 0). Read CH0 transmit data (80 bytes) by a read request. Once the reading of the CH0 transmit data is finished, a CH1 transmit data read request will be made as FR0_CH1 = 1 (FR0B = 0). Read CH1 transmit data (80 bytes) by a read request.

- Valid read period RE_DCn(CH0 & CH1)

  Complete the CH0 and CH1 transmit data read-out within 9.0 ms after a CH0 transmit data read request is generated (FR0_CH1=0).

- Transmit error processing

  If a read from the MCU side is not finished within the valid read period, the transmit error of the applicable channel (CH0: TXERR_CH0, CH1: TXERR_CH1) will be set to “1”. The transmit error will be held until immediately before the frame during which the transmit data of the applicable channel has normally been read is terminated in the succeeding valid read periods. Even if a data read-out has not been finished, the data in the transmit buffer will be updated as usual.

■ Reception

- 2-channel receive request status notification register (RXREQ_DC)

  In this operating state, the 2-channel receive request status notification register (RXREQ_DC) is set to “1”, and two requests to write receive data in one frame are notified to the MCU side.

- Order of channels to write

  There is no specification as to the order of channles to write, so write receive data in either the order of CH0 to CH1, or CH1 to CH0 within one frame.

  Note:

  Do not write the receive data of the same channel within one frame, such as CH0 to CH0, or CH1 to CH1. In case the receive data of the same channel is written within one frame, the receive data written by the first receive request will be decoded, but the receive data written by the second receive requst will be discarded, setting the invalid-write-on-the-receive-side error (RXBW_ERR) to “1”.

- Writing procedure

The following describes the operation when receive data is written in the order of CH0 to CH1.
Write CH0 receive data (80 bytes) by the first receive data write request (FR1 = 1&RXREQ_First = 1).
Also, before starting to write CH0 receive data, by setting the receive data write channel notification register (RXFLAG) to "0", notify this LSI that CH0 receive data will be written. Once the writing of the CH0 receive data is finished, the second receive data write request (FR1 = 1 & RXREQ_First = 0) will be made.
Write CH1 receive data (80 bytes) by the second write request. Also in this case, before starting to write CH1 receive data, by setting the receive data write channel notification register (RXFLAG) to "1", notify this LSI that CH1 receive data will be written. Note that, regardless of the first or second time, FR1 is set to "1" when a receive data write request is made.

• Valid write period WE_DCn (CH10& CH1)

WE_DC1 (CH0 & CH1)

There is no time limit for the first valid write period after starting a speech codec (CH0 & CH1).
If only the tWAIT wait time has elapsed after completion of writing received data of CH0 and CH1, the decode output control register (DEC_OUTON) can be set to "1". The decoder starts decode output the tDECON time after DEC_OUTON is set to "1"(*1).
(tWAIT = 2.0 ms, tDECON = 0 ms [initial value] ••• Can be set in the range of 0.0 ms to 32 ms in the internal data memory.)

WE_DC2 (CH0 & CH1)

The second valid write period will be 2.0 ms.

WE_DCn (CH0 & CH1) n = 3, 4, 5, ……

The third valid write period and succeeding ones will be 9 ms.

*1:
It is prohibited to make a transition to a single-channel operation (SC_CH0EN=0 & SC_CH1EN=1 or SC_CH0EN=1 & SC_CH1EN=0) before the decode output start offset time elapses after DEC_OUTON is set to "1".
Simultaneously with SC_CH0EN = SC_CH1EN="1" (which activates speech codec CH0 & CH1), DEC_OUTON can also be set to "1".
However, in this case, set in advance so that the internal data memory for controlling the decode output start offset time (DEC_ONTIM) is between 0010h (2.0 ms) and 0100h (32 ms).
Upon both completion of writing the first received data (CH0 & CH1) and elapse of the above offset time after starting a speech codec, the decoder starts decode output.

• Receive error processing

Finish writing CH0 receive data and CH1 receive data within the valid write period.
If a write from the MCU side does not finish within the valid write period, the receive error of the applicable channel (CH0: RXERR_CH0, CH1: RXERR_CH1) will be set to "1". The receive error will be held until immediately before the frame during which the receive data of the applicable channel has normally been written is terminated in the succeeding valid write periods. If an error occurs, generated data is output according to the PLC (Packet Loss Concealment) algorithm defined in G.711 Appendix I. However, the decoder outputs silence data if the G.711 PLC function is disabled. Also, if the receive data of the same channel is written within one frame, the invalid-write-on-the-receive-side error (RXBW_ERR) is set to "1". RXBW_ERR will be held until immediately before the frame during which invalid receive data has no longer been written is terminated in the succeeding valid write periods.

Note:
This operational description is pertaining to the case of the 10 ms mode; in the 20 ms mode, the valid read period and valid write period are as follows:

Valid read period RE_DCn (CH0 & CH1)

Finish reading the CH0 and CH1 transmit data within 18.0 ms after the CH0 transmit data read request (FR0_CH0=0) is generated.

Valid write period WE_DCn (CH0& CH1)

WE_DC1 (CH0 & CH1)
There is no time limit for the first valid write period after starting a speech codec (CH0 & CH1).
If only the tWAIT wait time has elapsed after completion of writing received data of CH0 and CH1, the decode output control register (DEC_OUTON) can be set to "1". The decoder starts decode output the tDECON time after DEC_OUTON is set to "1"(*1 above).
(tWAIT = 2.0 ms, tDECON = 0 ms [initial value] • • • Can be set in the range of 0.0 ms to 32 ms in the internal data memory.)

WE_DC2 (CH0 & CH1)
The second valid write period will be 12.0 ms.

WE_DCn (CH0 & CH1) n = 3, 4, 5, ……
The third valid write period and succeeding ones will be 18 ms.

3) 2-channel operation stop
To return from a 2-channel operating state to a stop state, set SC_CH0EN = 0 and SC_CH1EN = 0.
The encoder of a speech codec (CH0 & CH1) stops writing data within a maximum of 250 µs after SC_CH0EN = 0 and SC_CH1EN = 0 are set. The decoder outputs silence data after stopping.

Note:
1. After setting SC_CH0EN = 0 and SC_CH1EN = 0, RXFLAG is automatically cleared to 0b in a maximum of 250 µs.
2. A wait time of at least 10 ms is required to set SC_CH0EN = SC_EN = 1 again after setting SC_CH0EN = 0 and SC_CH1EN = 0.

(4) G.711 (u-law/A-law) 10ms mode: 2-channel processing in the midle of operation

Figure 25 G.711 (μ-law/A-law) 10 ms Mode: Control Timing of 2-Channel Processing in the Middle of Operation

Operational Description

1) single-channel operation in progress
Indicates a state in which only CH0 transmit data and receive data are being exchanged.

2) 2-channel operation activated
To also activate CH1 from the single-channel operation state at CH0, set SC_CH1EN=1 (and SC_CH0EN=1).
Encoder:
Starts encoding CH0 and CH1 signals a maximum of 1 frame after SC_CH1EN is set to “1”.
Decoder:
Makes two requests to write receive data in one frame a maximum of 1 frame after SC_CH1EN is set to “1”.

3) 2-channel operation in progress

■ Transmission

- 2-channel transmit request status notification register (TXREQ_DC)
  While a request to read transmit data is being made twice in one frame, the 2-channel transmit requesting notification register (TXREQ_DC) is set to “1”.

- Order of channels to read
  Two requests to read transmit data are made in the order of CH0 and then CH1 within one frame. However, if a read from the MCU side does not finish for a CH0 transmit data read request, a request to read CH1 transmit data will not be generated.

- Reading procedure
  Once the encoding processing for one frame of each of the CH0 and CH1 signals is finished, a CH0 transmit data read request will be made as FR0_CH0 = 1. Read CH0 transmit data (80 bytes) by a read request. Once the reading of the CH1 transmit data is finished, a CH1 transmit data read request will be made as FR0_CH1 = 1. Read CH1 transmit data (80 bytes) by a read request.

- Valid read period RE_DCn(CH0 & CH1)
  Complete the CH0 and CH1 transmit data read-out within 9.0 ms after a CH0 transmit data read request is generated (FR0_CH1=0).

- Transmit error processing
  If a read from the MCU side is not finished within the valid read period, the transmit error of the applicable channel (CH0: TXERR_CH0, CH1: TXERR_CH1) will be set to “1”. The transmit error will be held until immediately before the frame during which the transmit data of the applicable channel has normally been read is terminated in the succeeding valid read periods. Even if a data read-out has not been finished, the data in the transmit buffer will be updated as usual.

■ Reception

- 2-channel receive request status notification register (RXREQ_DC)
  In this operating state, the 2-channel receive requesting notification register (RXREQ_DC) is set to “1”, and two requests to write receive data in one frame are notified to the MCU side.

- Order of channels to write
  There is no specification as to the order of channles to write, so write receive data in either the order of CH0 to CH1, or CH1 to CH0 within one frame.

  Note:
  Do not write the receive data of the same channel within one frame, such as CH0 to CH0, or CH1 to CH1.
  In case the receive data of the same channel is written within one frame, the receive data written by the first receive request will be decoded, but the receive data written by the second receive requst will be discarded, setting the invalid-write-on-the-receive-side error (RXBW_ERR) to “1”.
- Writing procedure

The following describes the operation when receive data is written in the order of CH0 to CH1.
Write CH0 receive data (80 bytes) by the first receive data write request (FR1 = 1&RXREQ_First = 1).
Also, before starting to write CH0 receive data, by setting the receive data write channel notification register (RXFLAG) to "0b", notify this LSI that CH0 receive data will be written. Once the writing of the CH0 receive data is finished, the second receive data write request (FR1 = 1 & RXREQ_First = 0) will be made.
Write CH1 receive data (80 bytes) by the second write request. Also in this case, before starting to write CH1 receive data, by setting the receive data write channel notification register (RXFLAG) to "1b", notify this LSI that CH1 receive data will be written. Note that, regardless of the first or second time, FR1 is set to "1" when a receive data write request is made.

- Valid write period WE_DCn (CH10& CH1)
  The valid write period will be 9 ms.

- Receive error processing
  Finish writing CH0 receive data and CH1 receive data within the valid write period.
  If a write from the MCU side does not finish within the valid write period, the receive error of the applicable channel (CH0: RXERR_CH0, CH1: RXERR_CH1) will be set to "1". The receive error will be held until immediately before the frame during which the receive data of the applicable channel has normally been written is terminated in the succeeding valid write periods. If an error occurs, generated data is output according to the PLC (Packet Loss Concealment) algorithm defined in G.711 Appendix I. However, the decoder outputs silence data if the G.711 PLC function is disabled. Also, if the receive data of the same channel is written within one frame, the invalid-write-on-the-receive-side error (RXBW_ERR) is set to "1". RXBW_ERR will be held until immediately before the frame during which invalid receive data has no longer been written is terminated in the succeeding valid write periods.

Note:
This operational description is pertaining to the case of the 10 ms mode; in the 20 ms mode, the valid read period and valid write period are as follows:

Valid read period RE_DCn (CH0 & CH1)
Finish reading the CH0 and CH1 transmit data within 18.0 ms after the CH0 transmit data read request (FR0_CH0=1) is generated.

Valid write period WE_DCn (CH0& CH1)
The valid write period will be 18.0 ms.

4) 2-channel operation stop
Stop the speech codec of the channel to be stopped. (This example shows a case where the speech codec of CH1 is stopped.)

Note:
1. Even in a frame in which 2-channel operation stop is set, a transmit data read request and receive data write request of CH0/CH1 will be generated as usual. However, no error will be generated even if a read of transmit data or a write of receive data of the stopped channel is not perfomred.
2. Once RXREQ_DC is cleared to "0", it is no longer necessary to write to RXFLAG.
3. A wait time of at least 10 ms is required after TXREQ_DC = 0 and RXREQ_DC = 0 are set before starting a 2-channel operation again, following a stop of a channel operation.

5) Single-channel operation in progress
This is a state in which only CH0 transmit data and receive data are exchanged.

PCM Interface

(1) Overview

The PCM interface of this LSI consists of the following two interfaces, and SYNC and BCLK are common in each interface.

- I/O interface (PCMO_a, PCMI_a) for CH0a/CH1a PCM data transmission/reception
- I/O interface (PCMO_b, PCMI_b) for CH0b/CH1b PCM data transmission/reception

(2) PCM Time Slot Configuration

The bit width of one time slot of a PCM interface is fixed to 16 bits.
Therefore, in the case of BCLK = 2.048 MHz, up to 16 time slots (TS#1–TS#16) can be multiplexed on a PCM interface. However, because upper 8 bits (TSnU: n = 1 to 16) or lower 8 bits (TSnL: n = 1 to 16) can be selected for one time slot (TSn: n = 1 to 16), up to 32 time slots can be multiplexed on a PCM interface. Figure 26 shows the time slot structure of a PCM interface.

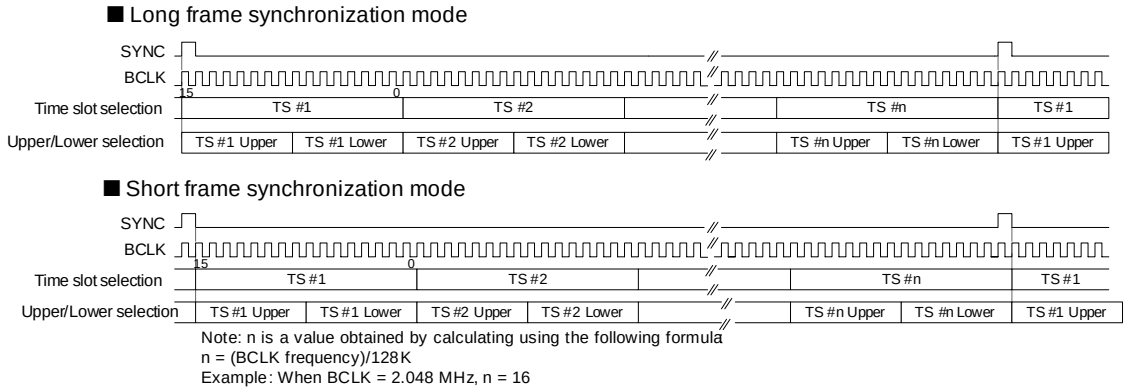


Figure 26 Structure of PCM Time Slot

(3) Input Time Slot Selection Method

• PCM Signal Input Pin for CH0a/CH1a (PCMI_a)

The PCM data to be input from PCMI_a can be used to capture a maximum of four time slots with the four buffers (16-bit width) PCMIa input buffer 0 (ITS0a), PCMIa input buffer 1 (ITS1a), PCMIa input buffer 2 (ITS2a) and PCMIa input buffer 3 (ITS3a). The four buffers are assigned to capture the following PCM input signals. (See also Block Diagram of this LSI.)

– PCMIa input buffer 0 (ITS0a):
This buffer captures the PCM input signal for CH0a if a PCM interface is selected as a front end interface.

– PCMIa input buffer 1 (ITS1a)
This buffer captures the PCM input signal for CH1a if a PCM interface is selected as a front end interface.

– PCMIa input buffer 2 (ITS2a)
This buffer captures the PCM input signal for CH0a if a PCM interface is selected as a speech CODEC interface.

– PCMIa input buffer 3 (ITS3a)
This buffer captures the PCM input signal for CH1a if a PCM interface is selected as a speech CODEC interface.

For each of the buffers, time slot and enable/disable settings can be made individually using the following setting method.

<Setting Method>

1) Select TS#1 to TS#16 with the PCMa input buffer n setting register (PCM_ITSn[3:0]_a: n = 0 to 3). Furthermore, specify either upper 8 bits or lower 8 bits of 16-bit width with the PCMa input buffer n upper/lower selection register (ITSn_SEL_a).
2) The capturing of the PCM data at the applicable time slot position will be started by setting the PCMa input buffer n enable control register (PCMIn_EN_a; n = 0 to 3) to “1”.

• PCM Signal Input Pin for CH0b/CH1b (PCMI_b)

The PCM data to be input from PCMI_b can be used to capture a maximum of four time slots with the the four buffers (16-bit width) PCMIb input buffer 0 (ITS0b), PCMIb input buffer 1 (ITS1b), PCMIb input buffer 2 (ITS2b) and PCMIb input buffer 3 (ITS3b). The four buffers are assigned to capture the following PCM input signals. (See also the Block Diagram of this LSI.)

– PCMIb input buffer 0 (ITS0b):
This buffer captures the PCM input signal for CH0b if a PCM interface is selected as a front end interface.

– PCMIb input buffer 1 (ITS1b)
This buffer captures the PCM input signal for CH1b if a PCM interface is selected as a front end interface.

– PCMIb input buffer 2 (ITS2b)
This buffer captures the PCM input signal for CH0b if a PCM interface is selected as a speech CODEC interface.

– PCMIb input buffer 3 (ITS3b)
This buffer captures the PCM input signal for CH1b if a PCM interface is selected as a speech CODEC interface.

For each of the buffers, time slot and enable/disable settings can be made individually using the following setting method.

<Setting Method>

1) Select TS#1 to TS#16 with the PCMb input buffer n setting register (PCM_ITSn[3:0]_b: n = 0 to 3). Furthermore, specify either upper 8 bits or lower 8 bits of 16-bit width with the PCMb input buffer n upper/lower selection register (ITSn_SEL_b).
2) The capturing of the PCM data at the applicable time slot position will be started by setting the PCMb input buffer n enable control register (PCMIn_EN_b; n = 0 to 3) to “1”.

Note: Using a PCM interface as a speech codec interface is not currently supported; therefore, ITS2a, ITS3a, ITS2b and ITS3b cannot be used. If it is necessary to use a PCM interface as a speech codec interface, contact our sales personnel.

(4) Output Time Slot Selection Method

- PCM Signal Output Pin for CH0a/CH1a (PCMO_a)

  The PCM data to be output from PCMO_a can be output to up to two time slots with the two buffers (16-bit width) PCMOa ouptut buffer 0 (OTS0a) and PCMOa output buffer 1 (OTS1a). These two buffers are assigned to output the PCM signals described below. (See also the Block Diagram of this LSI.)

  – PCMOa output buffer 0 (OTS0a) :
    If a PCM interface is selected as a front end interface, the PCM signal for CH0a is output. Additionally, if a PCM interface is selected as a speech codec interface, the PCM signal for CH0a is output.
  – PCMOa output buffer 1 (OTS1a) :
    If a PCM interface is selected as a front end interface, the PCM signal for CH1a is output. Additionally, if a PCM interface is selected as a speech codec interface, the PCM signal for CH1a is output.

Note:
Note that if a PCM interface is selected for both a front end interface and a speech codec interface, the PCM output signal of each interface will be output using to the upper 8 bits and lower 8 bits of one time slot.

For each of the buffers, time slot and enable/disable settings can be made individually using the following setting method.

<Setting Method>

1) Select TS#1 to TS#16 with the PCMa output buffer n setting register (PCM_OTSn[3:0]_a: n=0 to 3).
   Furthermore, specify either upper 8 bits or lower 8 bits of 16-bit width with the PCMa output buffer n upper/lower selection register (OTSn_SEL_a).
2) The output of the PCM data at the applicable time slot position will be started by setting the PCMa output buffer n enable control register (PCMOn_EN_a; n = 0 to 3) to “1”.
   Note that PCM data is output using the upper 8 bits or lower 8 bits selected by the PCMa output buffer n upper/lower selection register (OTSn_SEL_a), and the unselected 8 bits will be FFh (Hi-Z) output.

• PCM Signal Output Pin for CH0b/CH1b (PCMO_b)
The PCM data to be output from PCMO_b can be output to up to two time slots with the two buffers (16-bit width) PCMOb ouptut buffer 0 (OTS0b) and PCMOb output buffer 1 (OTS1b). These two buffers are assigned to output the PCM signals described below. (See also the Block Diagram of this LSI.)

– PCMOb output buffer 0 (OTS0b) :
If a PCM interface is selected as a front end interface, the PCM signal for CH0b is output. Additionally, if a PCM interface is selected as a speech codec interface, the PCM signal for CH0b is output.
– PCMOb output buffer 1 (OTS1b) :
If a PCM interface is selected as a front end interface, the PCM signal for CH1b is output. Additionally, if a PCM interface is selected as a speech codec interface, the PCM signal for CH1b is output.

Note:
Note that if a PCM interface is selected for both a front end interface and a speech codec interface, the PCM output signal of each interface will be output by multiplexing to the upper 8 bits and lower 8 bits of one time slot.

For each of the buffers, time slot and enable/disable settings can be Mbde individually using the following setting method.

<Setting Method>
1) Select TS#1 to TS#16 with the PCMb output buffer n setting register (PCM_OTSn[3:0]_b: n=0 to 3).
Furthermore, specify either upper 8 bits or lower 8 bits of 16-bit width with the PCMb output buffer n upper/lower selection register (OTSn_SEL_b).
2) The output of the PCM data at the applicable time slot position will be started by setting the PCMb output buffer n enable control register (PCMOn_EN_b; n = 0 to 3) to “1”.
Note that PCM data is output using the upper 8 bits or lower 8 bits selected by the PCMb output buffer n upper/lower selection register (OTSn_SEL_b), and the unselected 8 bits will be FFh (Hi-Z) output.

Note: Using a PCM interface as a speech codec interface is not currntly supported; therefore, OTS0a, OTS1a, OTS0b and OTS1b will be used for PCM signal output via a front end interface. If it is necessary to use a PCM interface as a speech codec interface, contact our sales personnel.

Serial Control Interface

(1) Overview

This LSI has two systems of serial control interfaces.

One serial control interface can control read and write operations to the control registers on the DSP_A side, and the other can control read and write opeations to the control registers on the DSP_B side.

Each of the serial control interfaces consists of four pins: SDENB pin, SCLK pin, SDI pin and SDO pin. The SDENB pin is a data enable signal input pin, the SCLK pin is a data shift clock signal input pin, the SDI pin is an address and data input pin, and the SDO pin is a data output pin. To use the serial control interfaces, it is necessary to set the SCNTEN pin to "1".

(2) Write and Read Control Timings

Figure 27 shows write and read control timings in the serial control interfaces.

Write and read operations are controlled in units of 16 bits consisting of 2 control bits (RW and CD), a 6-bit address (A[5:0]) and 8-bit data (D[7:0]).

- Control bit

  RW : "0" = At write control, "1" = At read control

  CD : "0" = Upon access to a control register, "1" = Upon access to the register for download/GPIO
- Address A[5:0]

  Specify the address of the control register or register for download/GPIO to which write/read control is to be performed.

  Note: Note that some of the addresses to be specified differs between parallel bus interface access and serial control interface access.
- Data D[7:0]

  Specify data to be written to the control register or register for download at the time of write control. The data of the control register at the address specified is output at read control.

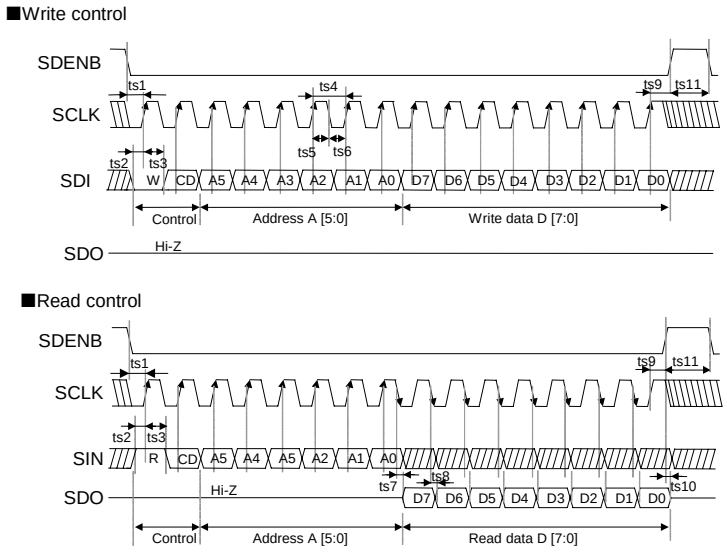


Figure 27 Serial Control Interface Timings

Note: To use serial control interfaces, it is necessary to set the SCNTEN pin to "1". However, note that the control registers cannot be accessed via a parallel bus interface in this case. Only the transmit and receive buffers can be accessed via a parallel bus interface.

List of Control Registers (DSP_A Side)

This LSI has CR0a–CR47a as control registers that perform various control and status notification on the DSP_A side, GPCR0a–GPCR8a as general-purpose input/output port control registers, and DLCR0a–DLCR5a as control registers for downloading DSP firmware.

Control Register Map (DSP_A Side) [page 1 of 6]

Reg Name	Address*1	Contents								R/W
	A7a-A0a	B7	B6	B5	B4	B3	B2	B1	B0	
CR0a	00h	DSP_RESET_a	AFE1_PDN_a	AFE0_PDN_a	#	#	#	SYNC_SEL_a	OPE_STAT_a	R/W
		/E,D	I/	I/	—	—	—	I/	I/	
CR1a	01h	XDMWR_a	XDMRD_a	#	#	XDMWR2_a	#	#	#	R/W
		I/E	I/E	—	—	I/E	—	—	—	
CR2a	02h	TGEN0_TX_a	TGEN0_RX_a	TGEN0_CNT5_a	TGEN0_CNT4_a	TGEN0_CNT3_a	TGEN0_CNT2_a	TGEN0_CNT1_a	TGEN0_CNT0_a	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
CR3a	03h	TGEN1_TX_a	TGEN1_RX_a	TGEN1_CNT5_a	TGEN1_CNT4_a	TGEN1_CNT3_a	TGEN1_CNT2_a	TGEN1_CNT1_a	TGEN1_CNT0_a	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
CR4a	04h	MGEN_TCEN_a	MGEN_TBEN_a	MGEN_TAEN_a	#	#	#	#	MGEN_FOUT_a	R/W
		MF	MF	MF	—	—	—	—	MF	
CR5a	05h	READY_a	DL_ST2_a	DL_ST1_a	DL_ST0_a	#	#	#	RX_FLAG_a	R/W
		—	—	—	—	—	—	—	/E	
CR6a	06h	Internal data memory access (higher address/higher data)								/W
		A15_a /D15_a	A14_a /D14_a	A13_a /D13_a	A12_a /D12_a	A11_a /D11_a	A10_a /D10_a	A9_a /D9_a	A8_a /D8_a	
		I/E								
CR7a	07h	Internal data memory access (lower address/lower data)								/W
		A7_a /D7_a	A6_a /D6_a	A5_a /D5_a	A4_a /D4_a	A3_a /D3_a	A2_a /D2_a	A1_a /D1_a	A0_a /D0_a	
		I/E								
CR8a	08h	Internal data memory access (higher data)								R/W
		D15_a	D14_a	D13_a	D12_a	D11_a	D10_a	D9_a	D8_a	
		I/E								
CR9a	09h	Internal data memory access (lower data)								R/W
		D7_a	D6_a	D5_a	D4_a	D3_a	D2_a	D1_a	D0_a	
		I/E								
CR10a	0Ah	CH1_IFSEL_a	CH0_IFSEL_a	#	#	#	VFRO1_SEL_a	VFRO0_SEL_a	#	R/W
		I/	I/	—	—	—	I/E	I/E	—	

Control Register Map (DSP_A Side) [page 2 of 6]

Reg Name	Address*1	Contents								R/W
	A7a-A0a	B7	B6	B5	B4	B3	B2	B1	B0	
CR11a	0Bh	#	#	PCMI3_EN_a	PCMI2_EN_a	PCMO1_EN_a	PCMI1_EN_a	PCMI0_EN_a	PCMO0_EN_a	R/W
		—	—	/E	/E	/E	/E	/E	/E	
CR12a	0Ch	$	$	$	$	$	$	$	$	/
CR13a	0Dh	FD_SEL_a	BW_SEL_a	TXSC_SEL1_a	TXSC_SEL0_a	TXBUF_TIM_a	RXSC_SEL1_a	RXSC_SEL0_a	RXBUF_TIM_a	R/W
		I/	I/	I/	I/	I/	I/	I/	I/	
CR14a	0Eh	PCM_SEL1_a	PCM_SEL0_a	#	#	#	#	#	#	R/W
		I/	I/	—	—	—	—	—	—	
CR15a to CR16a	0Fh to 10h	$	$	$	$	$	$	$	$	/
CR17a	11h	TONE_RXDET0_a	TONE_TXDET0_a	DP0_DET_a	DTMF0_DET_a	DTMF0_C3_a	DTMF0_C2_a	DTMF0_C1_a	DTMF0_C0_a	R/
		—	—	—	—	—	—	—	—	
CR18a	12h	TONE_RXDET1_a	TONE_TXDET1_a	DP1_DET_a	DTMF1_DET_a	DTMF1_C3_a	DTMF1_C2_a	DTMF1_C1_a	DTMF1_C0_a	R/
		—	—	—	—	—	—	—	—	
CR19a	13h	DSP_ERR_a	ANSPM_TXDET0_a	ANS_TXDET0_a	ANSPM_RXDET0_a	ANS_RXDET0_a	TGEN0_EXFLAG_a	MGEN_FRFLAG_a	MGEN_EXFLAG_a	R/
		—	—	—	—	—	—	—	—	
CR20a	14h	#	ANSPM_TXDET1_a	ANS_TXDET1_a	ANSPM_RXDET1_a	ANS_RXDET1_a	TGEN1_EXFLAG_a	#	#	R/
		—	—	—	—	—	—	—	—	
CR21a	15h	TX_SCFLAG_a	TX_BTFLAG_a	TXREQDC_a	TXREQFirst_a	TXERR_CH1_a	TXERR_CH0_a	FR0_CH1_a	FR0_CH0_a	R/
		—	—	—	—	—	—	—	—	
CR22a	16h	RX_SCFLAG_a	RX_BTFLAG_a	RXREQDC_a	RXREQFirst_a	RXERR_CH1_a	RXERR_CH0_a	RXBW_ERR_a	FR1_a	R/
		—	—	—	—	—	—	—	—	
CR23a	17h	$	$	$	$	$	$	$	$	/

Control Register Map (DSP_A Side) [page 3 of 6]

Reg Name	Address*1	Contents								R/W
	A7a-A0a	B7	B6	B5	B4	B3	B2	B1	B0	
CR24a	18h	SC_CH0EN_a	SC_CH1EN_a	DEC_OUTON_a	PLCEN_a	SCIF_SEL_a	#	#	MGEN_FREN_a	R/W
		I/E	I/E	/E	I/	I/	—	—	I/E	
CR25a	19h	TONE_RXDET0EN_a	TONE_TXDET0EN_a	FGEN0_EN_a	TD_RXDET0EN_a	TD_TXDET0EN_a	DTMF0_EN_a	EC0_EN_a	#	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	—	
CR26a	1Ah	TONE_RXDET1EN_a	TONE_TXDET1EN_a	FGEN1_EN_a	TD_RXDET1EN_a	TD_TXDET1EN_a	DTMF1_EN_a	EC1_EN_a	#	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	—	
CR27a	1Bh	#	DPGEN0_EN_a	DPGEN0_POL_a	DPGEN0_PPS_a	DPGEN0_D3_a	DPGEN0_D2_a	DPGEN0_D1_a	DPGEN0_D0_a	R/W
		—	I/E	I/	I/E	I/E	I/E	I/E	I/E	
CR28a	1Ch	#	DPGEN1_EN_a	DPGEN1_POL_a	DPGEN1_PPS_a	DPGEN1_D3_a	DPGEN1_D2_a	DPGEN1_D1_a	DPGEN1_D0_a	R/W
		—	I/E	I/	I/E	I/E	I/E	I/E	I/E	
CR29a	1Dh	#	#	#	#	#	#	#	FGEN0_FLAG_a	R/W
		—	—	—	—	—	—	—	I/E	
CR30a	1Eh	#	#	#	#	#	#	#	FGEN1_FLAG_a	R/W
		—	—	—	—	—	—	—	I/E	
CR31a	1Fh	DPDET0_D7_a	DPDET0_D6_a	DPDET0_D5_a	DPDET0_D4_a	DPDET0_D3_a	DPDET0_D2_a	DPDET0_D1_a	DPDET0_D0_a	R/
		—								
CR32a	20h	DPDET1_D7_a	DPDET1_D6_a	DPDET1_D5_a	DPDET1_D4_a	DPDET1_D3_a	DPDET1_D2_a	DPDET1_D1_a	DPDET1_D0_a	R/
		—								
CR33a	21h	ITS0_SEL_a	#	#	#	PCM_ITS0[3]_a	PCM_ITS0[2]_a	PCM_ITS0[1]_a	PCM_ITS0[0]_a	R/W
		I/E	—	—	—	I/E	I/E	I/E	I/E	
CR34a	22h	ITS1_SEL_a	#	#	#	PCM_ITS1[3]_a	PCM_ITS1[2]_a	PCM_ITS1[1]_a	PCM_ITS1[0]_a	R/W
		I/E	—	—	—	I/E	I/E	I/E	I/E	
CR35a	23h	OTS0_SEL_a	#	#	#	PCM_OTS0[3]_a	PCM_OTS0[2]_a	PCM_OTS0[1]_a	PCM_OTS0[0]_a	R/W
		I/E	—	—	—	I/E	I/E	I/E	I/E	

Control Register Map (DSP_A Side) [page 4 of 6]

Reg Name	Address*1 A7a-A0a	Contents B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR36a	24h	ITS2_SEL_a	#	#	#	PCM_ITS2[3]_a	PCM_ITS2[2]_a	PCM_ITS2[1]_a	PCM_ITS2[0]_a	R/W
		I/E	—	—	—	I/E	I/E	I/E	I/E	
CR37a	25h	ITS3_SEL_a	#	#	#	PCM_ITS3[3]_a	PCM_ITS3[2]_a	PCM_ITS3[1]_a	PCM_ITS3[0]_a	R/W
		I/E	—	—	—	I/E	I/E	I/E	I/E	
CR38a	26h	OTS1_SEL_a	#	#	#	PCM_OTS1[3]_a	PCM_OTS1[2]_a	PCM_OTS1[1]_a	PCM_OTS1[0]_a	R/W
		I/E	—	—	—	I/E	I/E	I/E	I/E	
CR39a to CR41a	27h to 29h	$	$	$	$	$	$	$	$	/
CR42a	2Ah	FGEN0_D7_a	FGEN0_D6_a	FGEN0_D5_a	FGEN0_D4_a	FGEN0_D3_a	FGEN0_D2_a	FGEN0_D1_a	FGEN0_D0_a	R/W
		I/E								
CR43a	2Bh	FGEN1_D7_a	FGEN1_D6_a	FGEN1_D5_a	FGEN1_D4_a	FGEN1_D3_a	FGEN1_D2_a	FGEN1_D1_a	FGEN1_D0_a	R/W
		I/E								
CR44a	2Ch	T1_TXON_a	T1_RXON_a	R1_TXON_a	R1_RXON_a	T0_TXON_a	T0_RXON_a	R0_TXON_a	R0_RXON_a	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
CR45a	2Dh	#	#	TIM_EN_a	#	DPDET1_POL_a	DPDET1_EN_a	DPDET0_POL_a	DPDET0_EN_a	R/W
		—	—	I/E	—	I/	I/E	I/	I/E	
CR46a to CR47a	2Eh to 2Fh	$	$	$	$	$	$	$	$	/
—	30h to 3Fh	$	$	$	$	$	$	$	$	/

Control Register Map (DSP_A Side) [page 5 of 6]

Reg Name	Address*1	Contents								R/W
	A7a-A0a	B7	B6	B5	B4	B3	B2	B1	B0	
GP CR0a	40h (S:00h)	#	#	#	#	#	#	GPMA [1]_a	GPMA [0]_a	R/W
		—	—	—	—	—	—	I/E	I/E	
GP CR1a	41h (S:01h)	#	#	#	#	#	#	GPDA [1]_a	GPDA [0]_a	R/W
		—	—	—	—	—	—	I/E	I/E	
GP CR2a	42h (S:02h)	#	#	#	#	#	#	GPFA [1] _a	GPFA [0] _a	R/W
		—	—	—	—	—	—	I/E	I/E	
GP CR3a	43h (S:03h)	#	#	#	#	GPMB [3]_a	GPMB [2]_a	GPMB [1]_a	GPMB [0]_a	R/W
		—	—	—	—	I/E	I/E	I/E	I/E	
GP CR4a	44h (S:04h)	#	#	#	#	GPDB [3]_a	GPDB [2]_a	GPDB [1]_a	GPDB [0]_a	R/W
		—	—	—	—	I/E	I/E	I/E	I/E	
GP CR5a	45h (S:05h)	$	$	$	$	$	$	$	$	/
GP CR6a	46h (S:06h)	GPMC [7]_a	GPMC [6]_a	GPMC [5]_a	GPMC [4]_a	GPMC [3]_a	GPMC [2]_a	GPMC [1]_a	GPMC [0]_a	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
GP CR7a	47h (S:07h)	GPDC [7]_a	GPDC [6]_a	GPDC [5]_a	GPDC [4]_a	GPDC [3]_a	GPDC [2]_a	GPDC [1]_a	GPDC [0]_a	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
GP CR8a	48h (S:08h)	$	$	$	$	$	$	$	$	/
—	49h to 7Fh	$	$	$	$	$	$	$	$	/
—	82h to 8Fh	$	$	$	$	$	$	$	$	/

Control Register Map (DSP_A Side) [page 6 of 6]

Reg Name	Address*1	Contents								R/W
	A7a-A0a	B7	B6	B5	B4	B3	B2	B1	B0	
DL CR0a	90h (S:10h)	#	#	#	#	#	#	DLa_ SEL	DLa_ EN	R/W
		—	—	—	—	—	—	D/	D/	
DL CR1a	91h (S:11h)	DLa_ A7	DLa_ A6	DLa_ A5	DLa_ A4	DLa_ A3	DLa_ A2	DLa_ A1	DLa_ A0	R/W
		D/	D/	D/	D/	D/	D/	D/	D/	
DL CR2a	92h (S:12h)	DLa_ A15	DLa_ A14	DLa_ A13	DLa_ A12	DLa_ A11	DLa_ A10	DLa_ A9	DLa_ A8	R/W
		D/	D/	D/	D/	D/	D/	D/	D/	
DL CR3a	93h (S:13h)	DLa_ BUF7	DLa_ BUF6	DLa_ BUF5	DLa_ BUF4	DLa_ BUF3	DLa_ BUF2	DLa_ BUF1	DLa_ BUF0	/W
		D/	D/	D/	D/	D/	D/	D/	D/	
DL CR4a	94h (S:14h)	DLa_ BUF15	DLa_ BUF14	DLa_ BUF13	DLa_ BUF12	DLa_ BUF11	DLa_ BUF10	DLa_ BUF9	DLa_ BUF8	/W
		D/	D/	D/	D/	D/	D/	D/	D/	
DL CR5a	95h (S:15H)	DLa_ BUF23	DLa_ BUF22	DLa_ BUF21	DLa_ BUF20	DLa_ BUF19	DLa_ BUF18	DLa_ BUF17	DLa_ BUF16	/W
		D/	D/	D/	D/	D/	D/	D/	D/	
—	96h to FFh	$	$	$	$	$	$	$	$	/

List of Control Registers (DSP_B Side)

This LSI has CR0b–CR47b as control registers that perform various control and status notification on the DSP_B side, GPCR0b–GPCR8b as general-purpose input/output port control registers, and DLCR0b–DLCR5ba as control registers for downloading DSP firmware.

Control Register Map (DSP_B Side) [page 1 of 6]

Reg Name	Address*1	Contents								R/W
	A7b-A0b	B7	B6	B5	B4	B3	B2	B1	B0	
CR0b	00h	DSP_RESET_b	AFE1_PDN_b	AFE0_PDN_b	#	#	#	SYNC_SEL_b	OPE_STAT_b	R/W
		/E,D	I/	I/	—	—	—	I/	I/	
CR1b	01h	XDMWR_b	XDMRD_b	#	#	XDMWR2_b	#	#	#	R/W
		I/E	I/E	—	—	I/E	—	—	—	
CR2b	02h	TGEN0_TX_b	TGEN0_RX_b	TGEN0_CNT5_b	TGEN0_CNT4_b	TGEN0_CNT3_b	TGEN0_CNT2_b	TGEN0_CNT1_b	TGEN0_CNT0_b	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
CR3b	03h	TGEN1_TX_b	TGEN1_RX_b	TGEN1_CNT5_b	TGEN1_CNT4_b	TGEN1_CNT3_b	TGEN1_CNT2_b	TGEN1_CNT1_b	TGEN1_CNT0_b	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
CR4b	04h	MGEN_TCEN_b	MGEN_TBEN_b	MGEN_TAEN_b	#	#	#	#	MGEN_FOUT_b	R/W
		MF	MF	MF	—	—	—	—	MF	
CR5b	05h	READY_b	DL_ST2_b	DL_ST1_b	DL_ST0_b	#	#	#	RX_FLAG_b	R/W
		—	—	—	—	—	—	—	/E	
CR6b	06h	Internal data memory access (higher address/higher data)								/W
		A15_b /D15_b	A14_b /D14_b	A13_b /D13_b	A12_b /D12_b	A11_b /D11_b	A10_b /D10_b	A9_b /D9_b	A8_b /D8_b	
		I/E								
CR7b	07h	Internal data memory access (lower address/lower data)								/W
		A7_b /D7_b	A6_b /D6_b	A5_b /D5_b	A4_b /D4_b	A3_b /D3_b	A2_b /D2_b	A1_b /D1_b	A0_b /D0_b	
		I/E								
CR8b	08h	Internal data memory access (higher data)								R/W
		D15_b	D14_b	D13_b	D12_b	D11_b	D10_b	D9_b	D8_b	
		I/E								
CR9b	09h	Internal data memory access (lower data)								R/W
		D7_b	D6_b	D5_b	D4_b	D3_b	D2_b	D1_b	D0_b	
		I/E								
CR10b	0Ah	CH1_IFSEL_b	CH0_IFSEL_b	#	#	#	VFRO1_SEL_b	VFRO0_SEL_b	#	R/W
		I/	I/	—	—	—	I/E	I/E	—	

Control Register Map (DSP_B Side) [page 2 of 6]

Reg Name	Address*1 A7b-A0b	Contents B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR11b	0Bh	#	#	PCMI3_EN_b	PCMI2_EN_b	PCMO1_EN_b	PCMI1_EN_b	PCMI0_EN_b	PCMO0_EN_b	R/W
		—	—	/E	/E	/E	/E	/E	/E	
CR12b	0Ch	$	$	$	$	$	$	$	$	/
CR13b	0Dh	FD_SEL_b	BW_SEL_b	TXSC_SEL1_b	TXSC_SEL0_b	TXBUF_TIM_b	RXSC_SEL1_b	RXSC_SEL0_b	RXBUF_TIM_b	R/W
		I/	I/	I/	I/	I/	I/	I/	I/	
CR14b	0Eh	PCM_SEL1_b	PCM_SEL0_b	#	#	#	#	#	#	R/W
		I/	I/	—	—	—	—	—	—	
CR15b to CR16b	0Fh to 10h	$	$	$	$	$	$	$	$	/
CR17b	11h	TONE_RXDET0_b	TONE_TXDET0_b	DP0_DET_b	DTMF0_DET_b	DTMF0_C3_b	DTMF0_C2_b	DTMF0_C1_b	DTMF0_C0_b	R/
		—	—	—	—	—	—	—	—	
CR18b	12h	TONE_RXDET1_b	TONE_TXDET1_b	DP1_DET_b	DTMF1_DET_b	DTMF1_C3_b	DTMF1_C2_b	DTMF1_C1_b	DTMF1_C0_b	R/
		—	—	—	—	—	—	—	—	
CR19b	13h	DSP_ERR_b	ANSPM_TXDET0_b	ANS_TXDET0_b	ANSPM_RXDET0_b	ANS_RXDET0_b	TGEN0_EXFLAG_b	MGEN_FRFLAG_b	MGEN_EXFLAG_b	R/
		—	—	—	—	—	—	—	—	
CR20b	14h	#	ANSPM_TXDET1_b	ANS_TXDET1_b	ANSPM_RXDET1_b	ANS_RXDET1_b	TGEN1_EXFLAG_b	#	#	R/
		—	—	—	—	—	—	—	—	
CR21b	15h	TX_SCFLAG_b	TX_BTFLAG_b	TXREQDC_b	TXREQFirst_b	TXERR_CH1_b	TXERR_CH0_b	FR0_CH1_b	FR0_CH0_b	R/
		—	—	—	—	—	—	—	—	
CR22b	16h	RX_SCFLAG_b	RX_BTFLAG_b	RXREQDC_b	RXREQFirst_b	RXERR_CH1_b	RXERR_CH0_b	RXBW_ERR_b	FR1_b	R/
		—	—	—	—	—	—	—	—	
CR23b	17h	$	$	$	$	$	$	$	$	/

Control Register Map (DSP_B Side) [page 3 of 6]

Reg Nbme	Address[*1] A7b-A0b	Contents B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR24b	18h	SC_CH 0EN_b	SC_CH 1EN_b	DEC_OU TON_b	PLCEN _b	SCIF _SEL_b	#	#	MGEN _FREN _b	R/W
		I/E	I/E	/E	I/	I/	—	—	I/E	
CR25b	19h	TONE_ RXDET 0EN_b	TONE_ TXDET 0EN_b	FGEN0 _EN_b	TD_RX DET0E N_b	TD_TX DET0E N_b	DTMF0 _EN_b	EC0 _EN_b	#	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	—	
CR26b	1Ah	TONE_ RXDET 1EN_b	TONE_ TXDET 1EN_b	FGEN1 _EN_b	TD_RX DET1E N_b	TD_TX DET1E N_b	DTMF1 _EN_b	EC1_E N_b	#	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	—	
CR27b	1Bh	#	DPGEN 0_EN_b	DPGEN0 _POL_b	DPGEN0 _PPS_b	DPGEN 0_D3_b	DPGEN 0_D2_b	DPGEN 0_D1_b	DPGEN 0_D0_b	R/W
		—	I/E	I/	I/E	I/E	I/E	I/E	I/E	
CR28b	1Ch	#	DPGEN 1_EN_b	DPGEN1 _POL_b	DPGEN1 _PPS_b	DPGEN 1_D3_b	DPGEN 1_D2_b	DPGEN 1_D1_b	DPGEN 1_D0_b	R/W
		—	I/E	I/	I/E	I/E	I/E	I/E	I/E	
CR29b	1Dh	#	#	#	#	#	#	#	FGEN0_ FLAG_b	R/W
		—	—	—	—	—	—	—	I/E	
CR30b	1Eh	#	#	#	#	#	#	#	FGEN1_F LAG_b	R/W
		—	—	—	—	—	—	—	I/E	
CR31b	1Fh	DPDET 0_D7_b	DPDET 0_D6_b	DPDET 0_D5_b	DPDET 0_D4_b	DPDET 0_D3_b	DPDET 0_D2_b	DPDET 0_D1_b	DPDET 0_D0_b	R/
		—								
CR32b	20h	DPDET 1_D7_b	DPDET 1_D6_b	DPDET 1_D5_b	DPDET 1_D4_b	DPDET 1_D3_b	DPDET 1_D2_b	DPDET 1_D1_b	DPDET 1_D0_b	R/
		—								
CR33b	21h	ITS0_ SEL_b	#	#	#	PCM_ ITS0[3]_b	PCM_ ITS0[2]_b	PCM_ ITS0[1]_b	PCM_ ITS0[0]_b	R/W
		I/E	—	—	—	I/E	I/E	I/E	I/E	
CR34b	22h	ITS1_ SEL_b	#	#	#	PCM_ ITS1[3] _b	PCM_ ITS1[2] _b	PCM_ ITS1[1] _b	PCM_ ITS1[0] _b	R/W
		I/E	—	—	—	I/E	I/E	I/E	I/E	
CR35b	23h	OTS0_ SEL_b	#	#	#	PCM_ OTS0[3]_b	PCM_ OTS0[2]_b	PCM_ OTS0[1]_b	PCM_ OTS0[0]_b	R/W
		I/E	—	—	—	I/E	I/E	I/E	I/E	

Control Register Map (DSP_B Side) [page 4 of 6]

Reg Nbme	Address*1	Contents								R/W
	A7b-A0b	B7	B6	B5	B4	B3	B2	B1	B0	
CR36b	24h	ITS2_ SEL_b	#	#	#	PCM_ ITS2[3]_b	PCM_ ITS2[2]_b	PCM_ ITS2[1]_b	PCM_ ITS2[0]_b	R/W
		I/E	—	—	—	I/E	I/E	I/E	I/E	
CR37b	25h	ITS3_ SEL_b	#	#	#	PCM_ ITS3[3]_b	PCM_ ITS3[2]_b	PCM_ ITS3[1]_b	PCM_ ITS3[0]_b	R/W
		I/E	—	—	—	I/E	I/E	I/E	I/E	
CR38b	26h	OTS1_ SEL_b	#	#	#	PCM_ OTS1 [3]_b	PCM_ OTS1 [2]_b	PCM_ OTS1 [1]_b	PCM_ OTS 1[0]_b	R/W
		I/E	—	—	—	I/E	I/E	I/E	I/E	
CR39b to CR41b	27h to 29h	$	$	$	$	$	$	$	$	/
CR42b	2Ah	FGEN0 _D7_b	FGEN0 _D6_b	FGEN0 _D5_b	FGEN0 _D4_b	FGEN0 _D3_b	FGEN0 _D2_b	FGEN0 _D1_b	FGEN0 _D0_b	R/W
		I/E								
CR43b	2Bh	FGEN1 _D7_b	FGEN1 _D6_b	FGEN1 _D5_b	FGEN1 _D4_b	FGEN1 _D3_b	FGEN1 _D2_b	FGEN1 _D1_b	FGEN1 _D0_b	R/W
		I/E								
CR44b	2Ch	T1_TX ON_b	T1_RX ON_b	R1_TX ON_b	R1_RX ON_b	T0_TX ON_b	T0_RX ON_b	R0_TX ON_b	R0_RX ON_b	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
CR45b	2Dh	#	#	TIM_EN _b	#	DPDET1_ POL_b	DPDET 1_EN_b	DPDET0 _POL_b	DPDET 0_EN_b	R/W
		—	—	I/E	—	I/	I/E	I/	I/E	
CR46b to CR47b	2Eh to 2Fh	$	$	$	$	$	$	$	$	/
—	30h to 3Fh	$	$	$	$	$	$	$	$	/

Control Register Map (DSP_B Side) [page 5 of 6]

Reg Nbme	Address[*1] A7b-A0b	Contents B7	B6	B5	B4	B3	B2	B1	B0	R/W
GP CR0b	40h (S:00h)	#	#	#	#	#	#	GPMA [1]_b	GPMA [0]_b	R/W
		—	—	—	—	—	—	I/E	I/E	
GP CR1b	41h (S:01h)	#	#	#	#	#	#	GPDA [1]_b	GPDA [0]_b	R/W
		—	—	—	—	—	—	I/E	I/E	
GP CR2b	42h (S:02h)	#	#	#	#	#	#	GPFA [1] _b	GPFA [0] _b	R/W
		—	—	—	—	—	—	I/E	I/E	
GP CR3b	43h (S:03h)	#	#	#	#	GPMB [3]_b	GPMB [2]_b	GPMB [1]_b	GPMB [0]_b	R/W
		—	—	—	—	I/E	I/E	I/E	I/E	
GP CR4b	44h (S:04h)	#	#	#	#	GPDB [3]_b	GPDB [2]_b	GPDB [1]_b	GPDB [0]_b	R/W
		—	—	—	—	I/E	I/E	I/E	I/E	
GP CR5b	45h (S:05h)	$	$	$	$	$	$	$	$	/
GP CR6b	46h (S:06h)	GPMC [7]_b	GPMC [6]_b	GPMC [5]_b	GPMC [4]_b	GPMC [3]_b	GPMC [2]_b	GPMC [1]_b	GPMC [0]_b	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
GP CR7b	47h (S:07h)	GPDC [7]_b	GPDC [6]_b	GPDC [5]_b	GPDC [4]_b	GPDC [3]_b	GPDC [2]_b	GPDC [1]_b	GPDC [0]_b	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
GP CR8b	48h (S:08h)	$	$	$	$	$	$	$	$	/
—	49h to 7Fh	$	$	$	$	$	$	$	$	/
—	82h to 8Fh	$	$	$	$	$	$	$	$	/

Control Register Map (DSP_B) [page 6 of 6]

Reg Name	Address*1 A7b-A0b	Contents B7	B6	B5	B4	B3	B2	B1	B0	R/W
DL CR0b	90h (S:10h)	#	#	#	#	#	#	DLb_ SEL	DLb_ EN	R/W
		—	—	—	—	—	—	D/	D/	
DL CR1b	91h (S:11h)	DLb_ A7	DLb_ A6	DLb_ A5	DLb_ A4	DLb_ A3	DLb_ A2	DLb_ A1	DLb_ A0	R/W
		D/	D/	D/	D/	D/	D/	D/	D/	
DL CR2b	92h (S:12h)	DLb_ A15	DLb_ A14	DLb_ A13	DLb_ A12	DLb_ A11	DLb_ A10	DLb_ A9	DLb_ A8	R/W
		D/	D/	D/	D/	D/	D/	D/	D/	
DL CR3b	93h (S:13h)	DLb_ BUF7	DLb_ BUF6	DLb_ BUF5	DLb_ BUF4	DLb_ BUF3	DLb_ BUF2	DLb_ BUF1	DLb_ BUF0	/W
		D/	D/	D/	D/	D/	D/	D/	D/	
DL CR4b	94h (S:14h)	DLb_ BUF15	DLb_ BUF14	DLb_ BUF13	DLb_ BUF12	DLb_ BUF11	DLb_ BUF10	DLb_ BUF9	DLb_ BUF8	/W
		D/	D/	D/	D/	D/	D/	D/	D/	
DL CR5b	95h (S:15H)	DLb_ BUF23	DLb_ BUF22	DLb_ BUF21	DLb_ BUF20	DLb_ BUF19	DLb_ BUF18	DLb_ BUF17	DLb_ BUF16	/W
		D/	D/	D/	D/	D/	D/	D/	D/	
—	96h to FFh	$	$	$	$	$	$	$	$	/

[Notation]
Bit symbols:

#	: Reserved bit. Do not change the initial value (“0”).
$	: Access-prohibited bit. Do not perfome any read or write operation to this bit.

Mode where setting can be changed:

I/E	: Can be changed either in the initial mode or during operation.
I/	: Can be changed only in the initial mode.
/E	: Can be changed only during operation.
/E,D	: Can be changed only during operation or in the download mode.
D	: Can be changed only in the download mode.
MF	: Can be changed only in the high-speed melody read mode.

R/W:

R/W	: Both read and write are possible.
/W	: Write only
R/	: Read only
/	: Access prohibited

*1:
Some registers have different addresses depending on whether access is made via a parallel bus interface or a serial control interface. Such registers are given an address for serial control interface access immediately below in parentheses “( )”.

Note:
Since reading is made in synchronization with the SYNC signal (8 kHz) if the following control registers are set during operation, maintain the condition for 250 μs or more.
CR1–CR5, CR10–CR11, CR13–CR14, CR24, CR25–CR30, CR33–CR38, CR42–CR45

For how to set the following control registers, see the method of accessing and controlling the internal data memory.
CR6, CR7, CR8, CR9

Description of Control Registers
The control registers are described from the next page. Since the control registers mounted on the DSP_A side and DSP_B side are functionally identical, the register description is given as a common explanation of the DSP_A side and DSP_B side.

(0) CR0

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR0	DSP_ RESET	AFE1_ PDN	AFE0_ PDN	#	#	#	SYNC_ SEL	OPE_ STAT	R/W
Mode where setting can be changed	/E, D	I/	I/	—	—	—	I/	I/	
Initial value	0(*1)	0	0	0	0	0	0	0	

*1: It is automatically set to "1" by the cancellation of hardware power down (PDNB = 0→1). Write "0" after the DSP firmware has been written.

B7 : DSP reset control register
0 : No reset
1 : Reset
The DSP can be placed in a reset state by setting this bit to "1" for at least 200 ns.
The contents of the control registers (excluding DLCR0–5) and internal data memories will automatically be cleared when reset. The reset state can be canceled by setting this bit to "0" after setting it to "1".

B6 : Analog front end CH1 power down control register
0 : Normally operating state
1 : Power down state (except AVREF)
The analog front end CH1 is powered down by setting this bit to "1".
It is recommended to set this bit to "1" if the analog front end CH1 is not used.
Also, when setting this bit to "1", set the output of VFRO1 to the AVREF side ("0") with the VFRO1 selection register (VFRO1_SEL).

B5 : Analog front end CH0 power down control register
0 : Normally operating state
1 : Power down state (except AVREF)
The analog front end CH0 is powered down by setting this bit to "1".
It is recommended to set this bit to "1" if the analog front end CH0 will not be used.
Also, when setting this bit to "1", set the output of VFRO0 to the AVREF side ("0") with the VFRO0 selection register (VFRO0_SEL).

Note:
In this code, selecting an analog interface as a front end interface is not allowed; therefore, be sure to set AFE1_PDN = 1 and AFE0_PDN = 1 while in the initial mode.

B4–B2 : Reserved bits. Do not change the initial values.

B1 : SYNC frame control register
0: Long frame synchronization signal
1: Short frame synchronization signal

Note:
The clocks of a PCM interface (SYNC and BCLK) are common on the DSP_A side and DSP_B side
Therefore, in the selection of long frame synchronization or short frame synchronization, short frame synchoronization will be selected if "1" is set in either the SYNC frame control register (SYNC_SEL_a) on the DSP_A side or the SYNC frame control register (SYNC_SEL_b) on the DSP_B side.

B0: Operation start control register
0: Operation hold
1: Operation start

The initial mode is entered when download of the DSP firmware is completed normally. In the initial mode, it becomes possible to modify the contents of the control registers and the internal data memory. Read out the initial mode display register (READY) repeatedly and start modifying the contents of the control registers and the internal data memory after detecting a “1” in this bit.
When this bit is set to “1” after completing the writing of data in the control registers and the internal data memory, READYis set to “0” and the normal operation mode is initiated.
Also, if modifying the control registers and the internal data memory again after setting this bit to “1”, do so after making a transition to the normal operation mode.

Note:
The wait time of the AVREF rise time (tAVREF) or longer is required until OPE_STAT can be set to “1” after the cancellation of a power down reset by PDNB. See Figure 1 for the AVREF rise time (tAVREF) or longer.

(1) CR1

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR1	XDMWR	XDMRD	#	#	XDMW R2	#	#	#	R/W
Mode where setting can be changed	I/E	I/E	—	—	I/E	—	—	—	
Initial value	0	0	0	0	0	0	0	0	

B7: Internal data memory 1-word write control register

0: Write stopped

1: Executes 1-word write

This register is used to write 1 words of data into the distributed address area in the internal data memory. The data set in CR8 and CR9 (D15 to D0) is written into the address set in CR6 and CR7 (A15 to A0). When this writing is completed, this bit is automatically cleared to "0". When writing data successively, do so after confirming that this bit is at "0".

For details of the method of controlling the internal memory, see the section on the method of accessing and controlling the internal data memory described later.

B6: Internal data memory read control register

0: Read stopped

1: Reads data

The data at the address set in CR6 and CR7 (A15 to A0) can be read out into CR8 and CR9 (D15 to D0). When this read-out is completed, this bit is cleared to "0" automatically. When reading out data successively, read the data after confirming that this bit is at "0".

For details of the method of controlling the internal memory, see the section on the method of accessing and controlling the internal data memory described later.

B5–B4 : Reserved bits. Do not change the initial values.

B3 : Internal data memory 2-word write control register

0: Write stopped

1: Executes 2-word write

This register is used to write multiple words of data into the continuous address area in the internal data memory.

For details of the method of controlling the internal memory, see the section on the method of accessing and controlling the internal data memory described later.

B2–B0 : Reserved bits. Do not change the initial values.

Note:

1-word write control, 2-word write control and read control cannot be performed simultaneously to the internal data memory. It is not allowed to set two or more bits of XDMWR, XDMRD and XDMWR2 to "1" simultaneously.

(2) CR2

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR2	TGEN0 _TX	TGEN0 _RX	TGEN0 _CNT5	TGEN0 _CNT4	TGEN0 _CNT3	TGEN0 _CNT2	TGEN0 _CNT1	TGEN0 _CNT0	R/W
Mode where setting can be changed	I/E								
Initial value	0	0	0	0	0	0	0	0	

B7: TGEN0 TX section output control register
0: Stops output.
1: Outputs tone at the TX section.

B6: TGEN0 RX section output control register
0: Stops output.
1: Outputs tone at the RX section.

B5: Register for controlling addition or multiplication of TONE A/B
0: Addition (The TONE A and TONE B outputs are added.)
1: Multiplication (The TONE A and TONE B outputs are multiplied.)

B4: TONE A/B output control register
0: Single-tone output
The signal is output for a duration equal to the sum of TIM_M0 and TIM_M1 and then stopped. After stopping, this register will be cleared automatically inside the LSI.
1: Continuous tone output
The signal is output repeatedly as controlled by the time duration equal to the sum of TIM_M0 and TIM_M1.
To stop the signal output, set this register to 00h.

Note:
It is prohibited to write any value into this register other than 00h when continuous output is being made.
In the case of single-tone output operation, make the next setting only after making sure that the content of this register has become 00h.
To output again after stopping continuous outputs, set by allocating at least “FADE OUT time + 250 μs.”

B3, B2: TONE A output control registers
00: No tone is output.
01: The tone is stopped during the M0 period and is output during the M1 period.
10: The tone is output during the M0 period and stopped during the M1 period.
11: The tone is output during both the M0 and M1 periods.

B1, B0: TONE B output control registers
00: No tone is output.
01: The tone is stopped during the M0 period and is output during the M1 period.
10: The tone is output during the M0 period and is stopped during the M1 period.
11: The tone is output during both the M0 and M1 periods.

Note:
Although it is possible to output TONE A and TONE B alternately when the output controls of TONE A and TONE B are set in a mutually exclusive manner and their outputs are summed, the waveform after addition will be discontinuous since the phases of the two signals will be independent of each other.

To activate TGEN0, be sure to place FSKGEN0 and DPGEN0 in a stop state. It is not allowed to use TGEN0, FSKGEN0 and DPGEN0 simultaneously.

(3) CR3

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR3	TGEN1 _TX	TGEN1 _RX	TGEN1 _CNT5	TGEN1 _CNT4	TGEN1 _CNT3	TGEN1 _CNT2	TGEN1 _CNT1	TGEN1 _CNT0	R/W
Mode where setting can be changed	I/E								
Initial value	0	0	0	0	0	0	0	0	

B7: TGEN1 TX section output control register
0: Stops output.
1: Outputs tone at the TX section.

B6: TGEN1 RX section output control register
0: Stops output.
1: Outputs tone at the RX section.

B5: Register for controlling addition or multiplication of TONE C/D
0: Addition (The TONE C and TONE D outputs are added.)
1: Multiplication (The TONE C and TONE D outputs are multiplied.)

B4: TONE C/D output control register
0: Single-tone output
The signal is output for a duration equal to the sum of TIM_M0 and TIM_M1 and then stopped.
After stopping, this register will be cleared automatically inside the LSI.
1: Continuous tone output
The signal is output repeatedly as controlled by the time duration equal to the sum of TIM_M0 and TIM_M1.
To stop the signal output, set this register to 00h.

Note:
It is prohibited to write any value into this register other than 00h when continuous output is being made.
In the case of single-tone output operation, make the next setting only after making sure that the content of this register has become 00h.
To output again after stopping continuous outputs, set by allocating at least “FADE OUT time + 250 μs.”

B3, B2: TONE C output control registers
00: No tone is output.
01: The tone is stopped during the M0 period and is output during the M1 period.
10: The tone is output during the M0 period and stopped during the M1 period.
11: The tone is output during both the M0 and M1 periods.

B1, B0: TONE D output control registers
00: No tone is output.
01: The tone is stopped during the M0 period and is output during the M1 period.
10: The tone is output during the M0 period and is stopped during the M1 period.
11: The tone is output during both the M0 and M1 periods.

Note:
Although it is possible to output TONE C and TONE D alternately when the output controls of TONE C and TONE D are set in a mutually exclusive manner and their outputs are summed, the waveform after addition will be discontinuous since the phases of the two signals will be independent of each other.

To activate TGEN1, be sure to place FSKGEN1 and DPGEN1 in a stop state. It is not allowed to use TGEN1, FSKGEN1 and DPGEN1 simultaneously.

Figure 28 shows block diagrams of the tone generation section (TGEN0 and TGEN1).
There is no differene in the tone generation method of TGEN0 and TGEN1. Figure 29 illustrates the tone output control method, and Figures 30 and 31 show the tone output control parameters, using TGEN0 as an example.

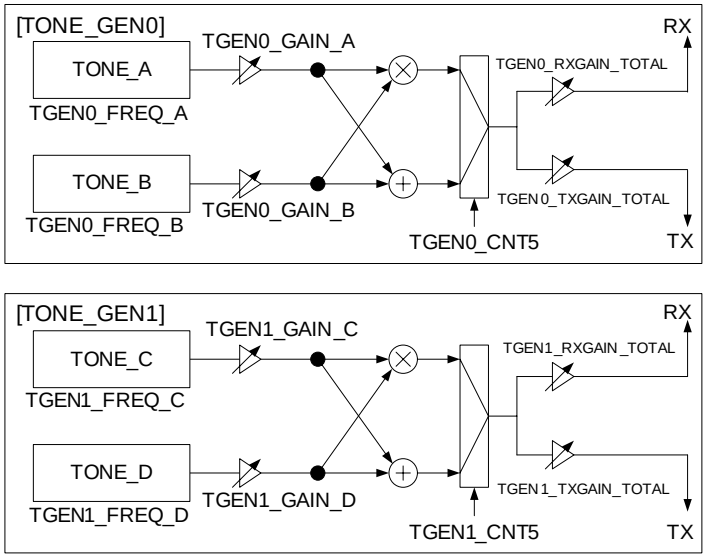


Figure 28 Block Diagram of Tone Generation Section

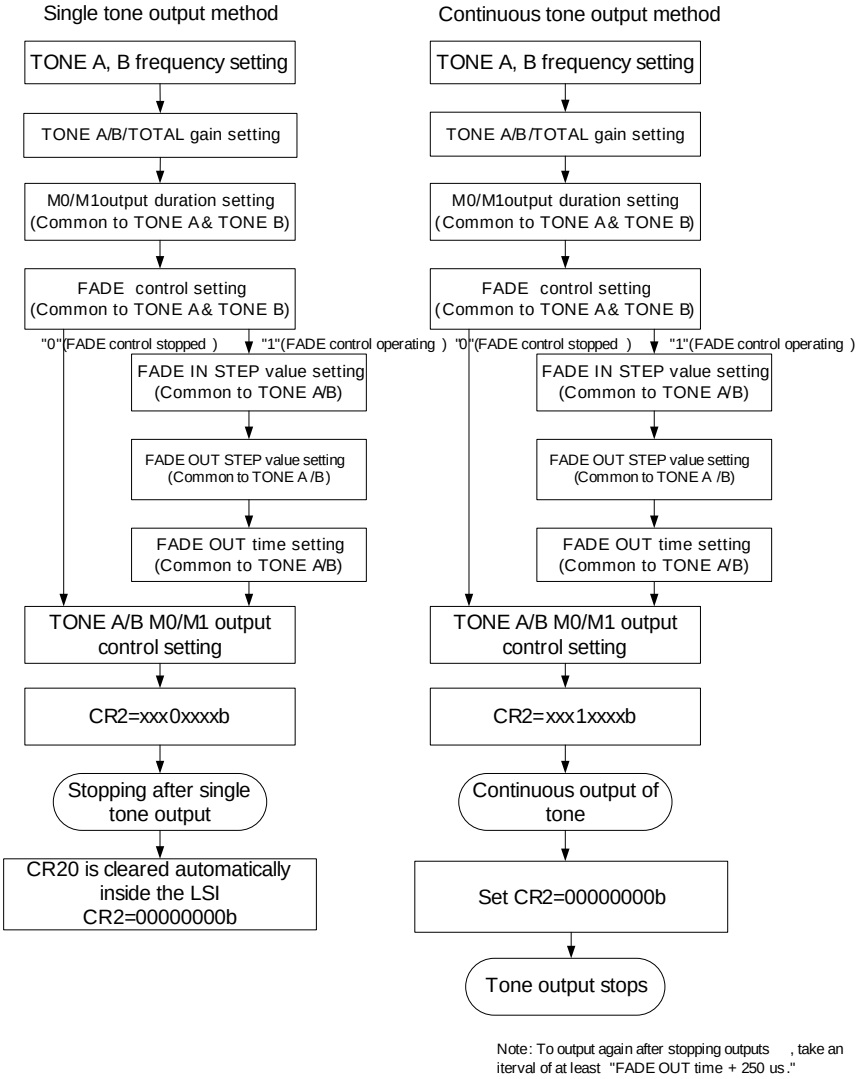


Figure 29 Tone Output Control Method (for TONE_GEN0)

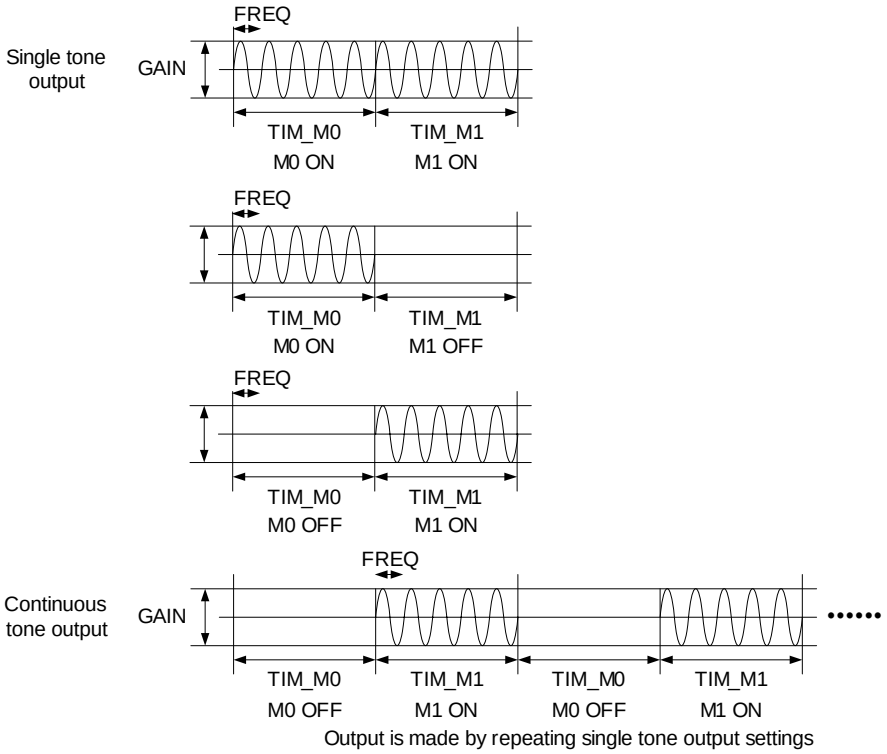


Figure 30 Tone Output Control Parameter (when TONE_GEN0 / TGEN0_FADE_CONT are set OFF)

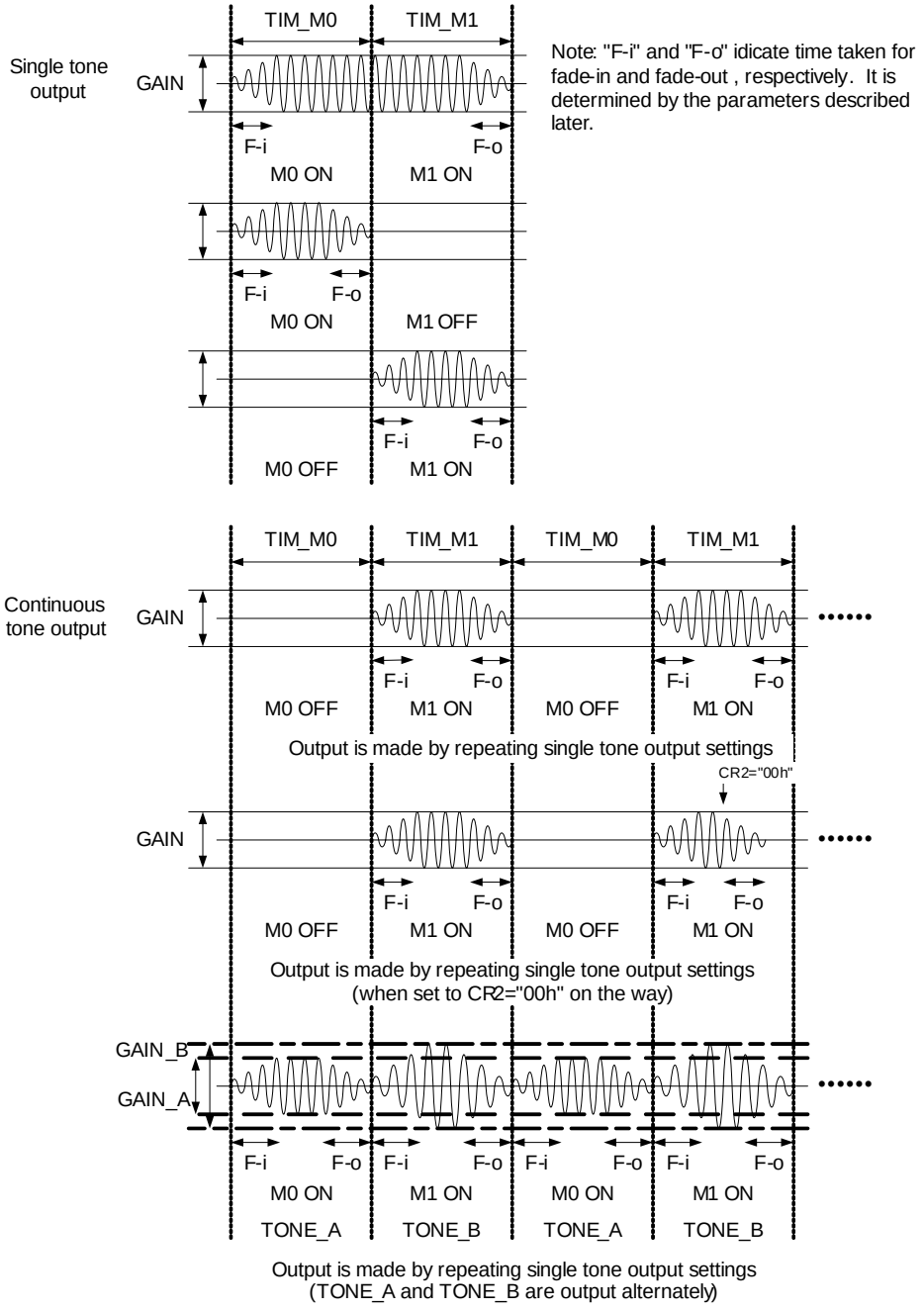


Figure 31 Tone Output Control Parameters (when TONE_GEN0 / TGEN0_FADE_CONT are set ON)

(4) CR4

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR4	MGEN_ TCEN	MGEN_ TBEN	MGEN_ TAEN	#	#	#	#	MGEN_ FOUT	R/W
Mode where setting can be changed	MF	MF	MF	—	—	—	—	MF	
Initial value	0	0	0	0	0	0	0	0	

B7 : TRACKC output contrl register
0 : Stop
1 : Output

B6 : TRACKB output contrl register
0 : Stop
1 : Output

B5 : TRACKA output contrl register
0 : Stop
1 : Output

B4–B1: Reserved bits. Do not change the initial values.

B0 : Output control register for MGEN high-speed read mode
0 : Stop
1 : Outputs melody to the encoder of a speech codec.

(5) CR5

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR5	READY	DL_ ST2	DL_ ST1	DL_ ST0	#	#	#	RX_ FLAG	R/W
Mode where setting can be changed	—	—	—	—	—	—	—	/E	
Initial value	0	0	0	0	0	0	0	0	

B7: Initial mode indication register
0: Other than the initial mode
1: Initialization in progress
Once the downloading of the DSP firmware is completed normally, the mode enters the initial mode. This bit will be set to "1" in the initial mode.

B6 : Download circuit status notification register 2
0 : PRAM write normally ended
1 : PRAM write error occurred
By reading this register when the download circuit status notification register 0 (DL_ST0) is "1", whether a write to PRAM has been compelted normally or not can be checked. Note that when the download circuit status notification register 0 (DL_ST0) is "0", the value of this register is invalid.

B5 : Download circuit status notification register 1
0 : DRAM write normally ended
1 : DRAM write error occurred
By reading this register when the download circuit status notification register 0 (DL_ST0) is "1", whether a write to DRAM has been compelted normally or not can be checked. Note that when the download circuit status notification register 0 (DL_ST0) is "0", the value of this register is invalid.

B4 : Download circuit status notification register 0
0 : Does not notify status.
1 : Notifies status.
This bit is set to "1" when notifying whether or not the writing of data to PRAM/DRAM has been completed normally. Read the download circuit status notification register 1 (DL_ST1) or the download circuit status notification register 2 (DL_ST2) while this bit is "1".

Note:
Write error check performed by this LSI never can detect all write errors.

B3–B1 : Reserved bits. Do not change the initial values.

B0 : Receive data write channel notification register
While requesting 2-channel reception (RXREQ_DC=1), two reception requests will be made within one frame. Write the receive data of channel 0 or 1 for every reception request. There is no specification as to the order of writing. Notify the channel of receive data to the LSI by setting RXFLAG to one of the following before writing receive data:
"0" : Notifies the writing of receive data of channel 0.
"1" : Notifies the writing of receive data of channel 1.

(6) CR6

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR6	A15 /D15	A14 /D14	A13 /D13	A12 /D12	A11 /D11	A10 /D10	A9 /D9	A8 /D8	/W
Mode where setting can be changed	I/E								
Initial value	0(*1)	0(*1)	0(*1)	0(*1)	0(*1)	0(*1)	0(*1)	0(*1)	

B7–B0 : Registers for setting the high-order address/high-order data of the internal data memory.
For details on the method of writing, see the section on the method of accessing and controlling the internal data memory.

*1: Although the initial value of CR6 is 00h, it is automatically set to 72h before starting the initial mode.

(7) CR7

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR7	A7 /D7	A6 /D6	A5 /D5	A4 /D4	A3 /D3	A2 /D2	A1 /D1	A0 /D0	/W
Mode where setting can be changed	I/E								
Initial value	0(*1)	0(*1)	0(*1)	0(*1)	0(*1)	0(*1)	0(*1)	0(*1)	

B7–B0 : Registers for setting the low-order address/low-order data of the internal data memory.
For details on the method of writing, see the section on the method of accessing and controlling the internal data memory.

*1: Although the initial value of CR7 is 00h, it is automatically set to 24h before starting the initial mode. By reading the values of CR6 and CR7 before starting the initial mode, the LSI type (ML7224) can be checked.

(8) CR8

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR8	D15	D14	D13	D12	D11	D10	D9	D8	R/W
Mode where setting can be changed	I/E								
Initial value	0(*1)	0(*1)	0(*1)	0(*1)	0(*1)	0(*1)	0(*1)	0(*1)	

B7–B0 : Registers for setting the high-order data of the internal data memory.
For details on the method of writing and reading, see the section on the method of accessing and controlling the internal data memory.

*1: Although the initial value of CR8 is 00h, it is automatically set to 01h before starting the initial mode. By reading the values of CR8 before starting the initial mode, CODE (-001) can be checked.

(9) CR9

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR9	D7	D6	D5	D4	D3	D2	D1	D0	R/W
Mode where setting can be changed	I/E								
Initial value	0(*1)	0(*1)	0(*1)	0(*1)	0(*1)	0(*1)	0(*1)	0(*1)	

B7–B0 : Registers for setting the low-order data of the internal data memory.
For details on the method of writing and reading, see the section on the method of accessing and controlling the internal data memory.

*1: Although the initial value of CR9 is 00h, it is automatically set to xxh (dependent on DSP firmware version) before starting the initial mode. By reading the value of CR9 before starting the initial mode, the DSP firmware version can be checked.

(10) CR10

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR10	CH1_ IFSEL	CH0_ IFSEL	#	#	#	VFRO1 _SEL	VFRO0 _SEL	#	R/W
Mode where setting can be changed	I/	I/	—	—	—	I/E	I/E	—	
Initial value	0	0	0	0	0	0	0	0	

B7 : CH1 front-end interface selection register
0 : Analog interface
1 : PCM interface

B6 : CH0 front-end interface selection register
0 : Analog interface
1 : PCM interface

Note:
This code does not allow selecting of an analog interface as a front end interface; therefore, be sure to set CH1_IFSEL = 1 and CH0_IFSEL = 1 while in the initial mode.

B5–B3 : Reserved bits. Do not change the initial values.

B2 : VFRO1 selection register
0 : AVREF (Outputs approx. 1.4 V.)
1 : Voice output on the receiving side

B1 : VFRO0 selection register
0 : AVREF (Outputs approx. 1.4 V.)
1 : Voice output on the receiving side

Note:
This code does not allow selecting of an analog interface as a front end interface; therefore, do not change the initial values of VFRO0_SEL and VFRO1_SEL.

B0 : Reserved bits. Do not change the initial values.

(11) CR11

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR11	#	#	PCMI3_EN	PCMI2_EN	PCMO1_EN	PCMI1_EN	PCMI0_EN	PCMO0_EN	R/W
Mode where setting can be changed	—	—	/E	/E	/E	/E	/E	/E	
Initial value	0	0	0	0	0	0	0	0	

B7, B6 : Reserved bits. Do not change the initial values.

B5 : PCM input buffer 3 enable control register
0 : Stop
1 : Activate
By setting this bit to “1”, the PCM data at the time slot position set by the PCM input buffer 3 time slot selection register (PCM_ITS3[3:0]) is captured. The capturing of PCM data will start from the next frame in which the setting of this bit to “1” has been detected. Figure 32 shows the PCM input timing.

B4 : PCM input buffer 2 enable control register
0 : Stop
1 : Activate
By setting this bit to “1”, the PCM data at the time slot position set by the PCM input buffer 2 time slot selection register (PCM_ITS2[3:0]) is captured. The capturing of PCM data will start from the next frame in which the setting of this bit to “1” has been detected. Figure 32 shows the PCM input timing.

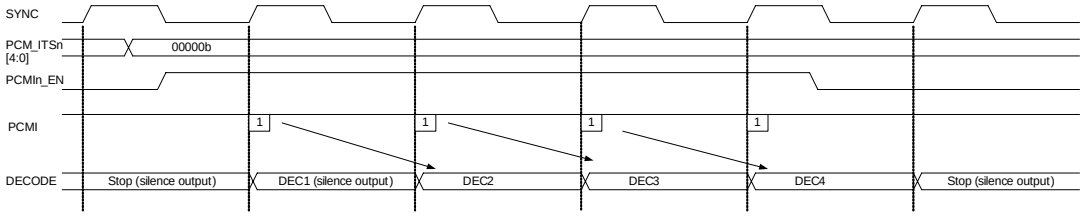
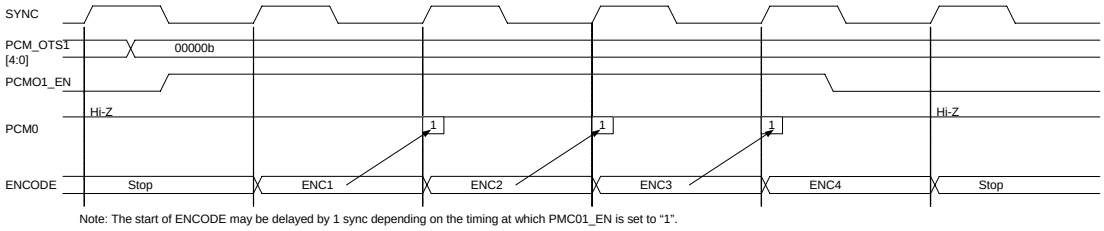


Figure 32 PCM Input Timing

B3 : PCM output buffer 1 enable control register
0 : Stop
1 : Activate
By setting this bit to “1”, PCM data is output at the time slot position set by the PCM output buffer 1 time slot selection register (PCM_OTS1[3:0]). The outputting of PCM data will start from the next frame in which this bit has been set to “1”. Figure 33 shows the PCM output timing.



Note: The start of ENCODE may be delayed by 1 sync depending on the timing at which PMC01_EN is set to “1”.

Figure 33 PCM Output Timing

B2 : PCM input buffer 1 enable control register
0 :Stop
1 : Activate
By setting this bit to “1”, the PCM data at the time slot position set by the PCM input buffer 1 time slot selection register (PCM_ITS1[3:0]) is captured. The capturing of PCM data will start from the next frame in which the setting of this bit to “1” has been detected. Figure 32 shows the PCM input timing.

B1 : PCM input buffer 0 enable control register
0 :Stop
1 : Activate
By setting this bit to “1”, the PCM data at the time slot position set by the PCM input buffer 0 time slot selection register (PCM_ITS0[3:0]) is captured. The capturing of PCM data will start from the next frame in which the setting of this bit to “1” has been detected. Figure 32 shows the PCM input timing.

B0 : PCM output buffer 0 enable control register
0 :Stop
1 : Activate
By setting this bit to “1”, PCM data is output at the time slot position set by the PCM output buffer 0 time slot selection register (PCM_OTS0[3:0]). The outputting of PCM data will start from the next frame in which this bit has been set to “1”. Figure 33 shows the PCM output timing.

Note:
Using a PCM interface as a speech codec interface is not currently supported; therefore, do not change the initial values of PCMI3_EN and PCMI2_EN.

(12) CR12

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR12	$	$	$	$	$	$	$	$	
Mode where setting can be changed	—	—	—	—	—	—	—	—	/
Initial value	—	—	—	—	—	—	—	—	

B7–B0 : Reserved bits. Access prohibited.

(13) CR13

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR13	FD_ SEL	BW_ SEL	TXSC _SEL1	TXSC _SEL0	TXBUF _TIM	RXSC _SEL1	RXSC _SEL0	RXBUF _TIM	
Mode where setting can be changed	I/	I/	I/	I/	I/	I/	I/	I/	R/W
Initial value	0	0	0	0	0	0	0	0	

B7 : FRAME/DMA selection register
0 : FRAME access
1 : DMA slave interface access
Select the method of accessing the transmit buffers and receive buffers. The initial value is frame access.

B6 : MCU iterface data width selection register
0 : 16-bit data width
1 : 8-bit data width
Select the data bus width for the transmit buffers and receive buffers. The initial value is the 16-bit data width. If the 8-bit data width is used, fix D15 to D8 at either “1” or “0”.

B5, B4 : Transmitting side speech codec selection register
(0 , 0) : Setting not allowed
(0 , 1) : G.711 (μ-law)
(1 , 0) : Setting not allowed
(1 , 1) : G.711 (A-law)

Note:
It is not allowed to use the initial value of this register; therefore, be sure to set either (0,1) or (1,1) while in the initial mode.

B3 : Transmit buffering time selection register
0 : 10 ms
1 : 20 ms

B2, B1 : Receiving side speech codec selection register
(0 , 0) : Setting not allowed
(0 , 1) : G.711(μ-law)
(1 , 0) : Setting not allowed
(1 , 1) : G.711(A-law)

Note:
Using the initial value of this register is not allowed; therefore, be sure to set either (0,1) or (1,1) while in the initial mode.

B0 : Receive buffering time selection register
0 : 10 ms
1 : 20 ms

(14) CR14

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR14	PCM_ SEL1	PCM_ SEL0	#	#	#	#	#	#	R/W
Mode where setting can be changed	I/	I/	—	—	—	—	—	—	
Initial value	0	0	0	0	0	0	0	0	

B7, B6 : PCM interface coding format selection register
These bits select the PCM interface coding format.
(0 , 0) : Setting not allowed
(0 , 1) : G.711 (μ-law)
(1 , 0) : Setting not allowed
(1 , 1) : G.711 (A-law)

Note:
It is not allowed to use the initial value of this register; therefore, be sure to set either (0,1) or (1,1) while in the initial mode.

B5–B0 : Reserved bits. Do not change the initial values.

(15) CR15

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR15	$	$	$	$	$	$	$	$	/
Mode where setting can be changed	—	—	—	—	—	—	—	—	
Initial value	—	—	—	—	—	—	—	—	

B7–B0 : Reserved bits. Access prohibited.

(16) CR16

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR16	$	$	$	$	$	$	$	$	/
Mode where setting can be changed	—	—	—	—	—	—	—	—	
Initial value	—	—	—	—	—	—	—	—	

B7–B0 : Reserved bits. Access prohibited.

(17) CR17

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR17	TONE_RXDET0	TONE_TXDET0	DP0_DET	DTMF0_DET	DTMF0_C3	DTMF0_C2	DTMF0_C1	DTMF0_C0	R/
Mode where setting can be changed	—	—	—	—	—	—	—	—	
Initial value	0	0	0	0	0	0	0	0	

B7 : TONE_RXDET0 detection status register
"1" is set in a segment where tone is detected by TONE_RXDET0. "0" is set for any other segments.
0: Not detected
1: Detected

B6 : TONE_TXDET0 detection status register
"1" is set in a segment where tone is detected by TONE_TXDET0. "0" is set for any other segments.
0: Not detected
1: Detected

B5 : DPDET0 detection status register
"1" is set in a segment where dial pulse is detected by DPDET0. "0" is set for any other segments.
0: Not detected
1: Detected

B4 : DTMF0 detection status register
"1" is set in a segment where the DTMF signal is detected by DTMFDET0. "0" is set for any other segments.
0: Not detected
1: Detected

B3–B0 : DTMF0 detection code display register
An valid code is stored in a segment where the DTMF signal is detected (DTMF0_DET = "1") by DTMFDET0. When the DTMF signal is not detected (DTMF0_DET = "0"), "0000" is output. Table 4 shows each code.

(18) CR18

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR18	TONE_RXDET1	TONE_TXDET1	DP1_DET	DTMF1_DET	DTMF1_C3	DTMF1_C2	DTMF1_C1	DTMF1_C0	
Mode where setting can be changed	—	—	—	—	—	—	—	—	R/
Initial value	0	0	0	0	0	0	0	0	

B7 : TONE_RXDET1 detection status register
"1" is set in a segment where tone is detected by TONE_RXDET1. "0" is set for any other segment.
0: Not detected
1: Detected

B6 : TONE_TXDET1 detection status register
"1" is set in a segment where tone is detected by TONE_TXDET1. "0" is set for any other segment.
0: Not detected
1: Detected

B5 : DPDET1 detection status register
"1" is set in a segment where dial pulse is detected by DPDET1. "0" is set for any other segments.
0: Not detected
1: Detected

B4 : DTMFDET1 detection status register
"1" is set in a segment where the DTMF signal is detected by DTMFDET1. "0" is set for any other segments.
0: Not detected
1: Detected

B3–B0 : DTMF1 detection code display register
An valid code is stored in a segment where the DTMF signal is detected (DTMF1_DET = "1") by DTMFDET1. When the DTMF signal is not detected (DTMF1_DET = "0"), "0000" is output. Table 4 shows each code.

Table 4 DTMF Detection Codes

DTMF_3	DTMF_2	DTMF_1	DTMF_0	Low group [Hz]	High group [Hz]	Dial No.
0	0	0	0	697	1209	1
0	0	0	1	770	1209	4
0	0	1	0	852	1209	7
0	0	1	1	941	1209	*
0	1	0	0	697	1336	2
0	1	0	1	770	1336	5
0	1	1	0	852	1336	8
0	1	1	1	941	1336	0
1	0	0	0	697	1477	3
1	0	0	1	770	1477	6
1	0	1	0	852	1477	9
1	0	1	1	941	1477	#
1	1	0	0	697	1633	A
1	1	0	1	770	1633	B
1	1	1	0	852	1633	C
1	1	1	1	941	1633	D

(19) CR19

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR19	DSP_ERR	ANSPM_TXDET0	ANS_TXDET0	ANSPM_RXDET0	ANS_RXDET0	TGEN0_EXFLAG	MGEN_FRFLAG	MGEN_EXFLAG	
Mode where setting can be changed	—	—	—	—	—	—	—	—	R/
Initial value	0	0	0	0	0	0	0	0	

B7: DSP status register
0: Normal operation state
1: Abnormal operation state
This LSI has a built-in watchdog timer, and when the program of the DSP section goes into uncontrollable execution state due to external disturbances around this LSI or due to power supply abnormalities, etc., the DSP status register (DSP_ERR) will be set to "1". When this bit becomes "1", carry out a power down reset using either PDNB or the DSP reset control register (DSP_RESET). This bit is cleared by a power down reset operation.

Note:
The DSP status register (DSP_ERR) cannot detect all abnormal operation conditions. The abnormality will not be detected even when the DSP goes into uncontrolled program execution if the watchdog timer gets cleared during that program execution.

B6 : TD_TXDET0—2100 Hz phase inversion detection status register
0: Not detected
1: Detected

B5 : TD_TXDET0—2100 Hz single-tone detection status register
0: Not detected
1: Detected

B4 : TD_RXDET0—2100 Hz phase inversion detection status register
0: Not detected
1: Detected

B3 : TD_RXDET0—2100 Hz single-tone detection status register
0: Not detected
1: Detected

B2 : TGEN0 execution status flag indication register
0 : Being stopped
1 : Operating

B1 : MGEN high-speed read mode notification flag
0 : Other than during high-speed melody read mode
1 : During high-speed melody read mode

B0 : MGEN execution status indication flag
0 : Being stopped
1 : Operating

(20) CR20

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR20	#	ANSPM_TXDET1	ANS_TXDET1	ANSPM_RXDET1	ANS_RXDET1	TGEN1_EXFLAG	#	#	R/
Mode where setting can be changed	—	—	—	—	—	—	—	—	
Initial value	0	0	0	0	0	0	0	0	

B7 : Reserved bits. Do not change the initial values.

B6 : TD_TXDET1—2100 Hz phase inversion detection status register
0: Not detected
1: Detected

B5 : TD_TXDET1—2100 Hz single-tone detection status register
0: Not detected
1: Detected

B4 : TD_RXDET1—2100 Hz phase inversion detection status register
0: Not detected
1: Detected

B3 : TD_RXDET1—2100 Hz single-tone detection status register
0: Not detected
1: Detected

B2 : TGEN1 execution status flag indication register
0 : Being stopped
1 : Operating

B1, B0 : Reserved bits. Do not change the initial values.

(21) CR21

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR21	TX_SC FLAG	TX_BT FLAG	TXREQ DC	TXREQ First	TXERR _CH1	TXERR _CH0	FR0 _CH1	FR0 _CH0	
Mode where setting can be changed	—	—	—	—	—	—	—	—	R/
Initial value	0	0	0	0	0	0	0	0	

B7 : Transmitting side speech codec operation mode notification flag
0 : Other than G.711 (μ-law / A-law)
1 : G.711 (μ-law / A-law)

B6 : Transmitting side buffering time operation mode notification flag
0 : 10 ms
1 : 20 ms
By referencing this bit, the operating mode of the buffering time on the transmitting side can be checked. If this bit is “0” when a transmission request is made by a fall of FR0B, it indicates that the transmit buffer is buffering encode data for 10 ms. If this bit is “1” when a transmission request is made by a fall of FR0B, it indicates that the transmit buffer is buffering encode data for 20 ms.

B5 : 2-channel transmission requesting status notification register
0 : Other than the state where 2-channel transmission is being requested
1 : 2-channel transmission is being requested
While requesting 2-channel transmission (TXREQ_DC=1), two transmission requests will be made within one frame.
Read the transmit data of channel 0 by a CH0 transmission request (FR0_CH0 = 1), and the transmission data of channel 1 by a CH1 transmission request (FR0_CH1)

B4 : Transmission frame start notification register
While requesting 2-channel transmission (TXREQ_DC = 1), two transmission requests will be made within one frame. With this bit, the start timing of each transmission frame can be checked.
While requesting 2-channel transmission (TXREQ_DC = 1), this bit is set to “1” immediately before a CH0 transmission request (FR0_CH0 = 1), and cleared to “0” immediately before a CH1 transmission request (FR0_CH1 = 1).

B3 : CH1 transmission error status retgister
0 : No CH1 transmission error occurred
1 : CH1 transmission error occurred
This register is set to “1” if the reading of CH1 transmit data does not complete within the valid read period, and set to “0” for other cases.

B2 : CH0 transmission error status retgister
0 : No CH0 transmission error occurred
1 : CH0 transmission error occurred
This register is set to “1” if the reading of CH0 transmit data does not complete within the valid read period, and set to “0” for other cases.

B1 : CH1 transmission request notification register
0 : No CH1 transmission request generated
1 : CH1 transmission request generated
This register is set to “1” if the transmit buffer storing CH1 transmit data becomes full, and set to “0” if the reading of data in the transmit buffer is complete or the specified time is exceeded.

B0 : CH0 transmission request notification register
0 : No CH0 transmission request generated
1 : CH0 transmission request generated
This register is set to “1” if the transmit buffer storing CH0 transmit data becomes full, and set to “0” if the reading of data in the transmit buffer is complete or the specified time is exceeded.

When in the frame mode (FD_SEL = 0), a signal generated by a NOR of bit B1 and bit B0 is output to the FR0B pin[*1].

*1: Note that the status of bits B1 and B0 does not match the status of the FR0B (DMARQ0B) when in the DMA mode (FD_SEL = 1).

(22) CR22

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR22	RX_SC FLAG	RX_BT FLAG	RXREQ DC	RXREQ First	RXERR _CH1	RXERR _CH0	RXBW _ERR	FR1	R/
Mode where setting can be changed	—	—	—	—	—	—	—	—	
Initial value	0	0	0	0	0	0	0	0	

B7 : Receiving side speech codec operation mode notification flag
0 : Other than G.711 (μ-law / A-law)
1 : G.711 (μ-law / A-law)

B6 : Receiving side buffering time operation mode notification flag
0 : 10 ms
1 : 20 ms
By referencing this bit, the operating mode of the buffering time on the receiving side can be checked. If this bit is “0” when a reception request is made by a fall of FR1B, it indicates that the receive buffer is requesting writing of data for 10 ms. If this bit is “1” when a reception request is made by a fall of FR1B, it indicates that the receive buffer is requesting writing of data for 20 ms.

B5 : 2-channel reception requesting status notification register
0 : Other than the state where 2-channel reception is being requested
1 : 2-channel reception is being requested
While requesting 2-channel reception (RXREQ_DC = 1), two reception requests will be made within one frame.
Write the receive data of channel 1 or channel 2 for each reception request (FR1 = 1)

B4 : Reception frame start notification register
While requesting 2-channel reception (RXREQ_DC = 1), two reception requests will be made within one frame. With this bit, whether it is the first reception request or not can be checked.
If this bit is “1” when a reception request (FR1 = 1) is generated, it indicates that it is the first reception request, and if “0”, it indicates that it is the second reception request.

B3 : CH1 reception error status retgister
0 : No CH1 reception error occurred
1 : CH1 reception error occurred
This register is set to “1” if the writing of CH1 receive data does not complete within the valid write period, and set to “0” for other cases.

B2 : CH0 reception error status retgister
0 : No CH0 reception error occurred
1 : CH0 reception error occurred
This register is set to “1” if the writing of CH0 receive data does not complete within the valid read period, and set to “0” for other cases.

B1 : Invalid-write-of-receive-data error notification register
0 : Invalid write of receive data did not occurred
1 : Invalid write of receive data occurred
This register is set to “1” if the channel of receive data is notified from the MCU side without observing the following prohibited item while requesting 2-channel reception (RXREQ_DC = 1), and set to “0” for other cases.

♦ Prohibited Item 1: Do not write the receive data of the same channel in succession within one frame.
If the receive data of the same channel is written in succession within one frame, RXBW_ERR is set to “1”.
In this case, the data written by the first reception request (FR1=1 & RXREQ_First = 1) will be decoded; however, the data written by the second reception request (FR1=1 & RXREQ_First = 0) will be discarded.

B0 : Reception request notification register
0 : Reception request absent
1 : Reception request present
This register is set to “1” if the receive buffer storing receive data becomes empty, and set to “0” if the receive buffer becomes full or the specified time is exceeded.

When in the frame mode (FD_SEL = 0), a signal generated by inverting the logic of bit B0 is output to the FR1B pin[*1].

*1: Note that the status of bit B0 does not match that of FR1B (DMARQ1B) when in the DMA mode (FD_SEL = 1).

(23) CR23

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR23	$	$	$	$	$	$	$	$	
Mode where setting can be changed	—	—	—	—	—	—	—	—	/
Initial value	—	—	—	—	—	—	—	—	

B7–B0 : Reserved bits. Access prohibited.

(24) CR24

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR24	SC_CH 0EN	SC_CH 1EN	DEC_ OUTON	PLCEN	SCIF _SEL	#	#	MGEN_ FREN	
Mode where setting can be changed	I/E	I/E	/E	I/	I/	—	—	I/E	R/W
Initial value	0	0	0	0	0	0	0	0	

B7 : Speech codec-CH0 control register
0 : Stops speech codec-CH0
1 : Operates speech codec-CH0

B6 : Speech codec-CH1 control register
0 : Stops speech codec-CH1
1 : Operates speech codec-CH1

B5 : Decode output control register
This bit controls the first decode output timing after starting a speech codec.
If the first received data has been written and the tWAIT wait time has elapsed after starting a speech codec, this bit can be set to “1”. Decode output will start as shown below, once this bit is set to “1”.
When G.711 (μ-law/A-law) is selected:
If the PLC function is enabled, silence data for approximately 3.75 ms is output after this bit is set to “1”, and then the decoder starts decode output.
If the PLC function is disabled, the decoder starts decode output after setting this bit to “1”.

Note that by making a setting in the internal data memory for controlling the decode output start offset time (DEC_ONTIM), the time until the start of the decode output descrirved above can be delayed in 0.125 ms. (DEC_ONTIM settable range: 0.0 ms to 32 ms)
Additionally, when stopping a speech codec, also clear this bit to “0”.

Note:
As the tWAIT wait time, at least 2.0 ms is required after starting a speech codec.

Simultaneously with the start of a speech codec, DEC_OUTON can also be set to “1”.
However, in this case, set in advance so that the internal data memory for controlling the decode output start offset time (DEC_ONTIM) is between 0010h (2.0 ms) and 0100h (32 ms).
Both upon completion of writing the first received data and upon elapse of the above offset time after starting a speech codec, the decoder starts decode output.

B4 : G.711 PLC funtion enable control register
Enable the G.711 PLC function by setting this bit to “1”.
0 : Disabled
1 : Enabled
Note: When setting G711_PLCEN to “1”, be sure to do so when a speech codec is in a stop state.

B3 : Speech codec interface selection register
0 : FIFO interface
1 : PCM interface

Note: Do not change the initial value (“0”) of this bit in this code. If it is necessary to use a PCM interface as a speech codec interface, contact our sales personnel.

B2, B1 : Reserved bits. Do not change the initial values.

B0 : MGEN high-speed read mode control register
0 : Stops high-speed read mode.
1 : Activates high-speed read mode.

(25) CR25

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR25	TONE_RXDET0EN	TONE_TXDET0EN	FGEN0_EN	TD_RXDET0EN	TD_TXDET0EN	DTMF0_EN	EC0_EN	#	R/W
Mode where setting can be changed	I/E	I/E	I/E	I/E	I/E	I/E	I/E	—	
Initial value	0	0	0	0	0	0	0	0	

B7 : TONE_RXDET0 enable control register
0 : Stop
1 : Operate
Setting this bit to “1” makes TONE_RXDET0 start operating.

B6 : TONE_TXDET0 enable control register
0 : Stop
1 : Operate
Setting this bit to “1” makes TONE_TXDET0 start operating.

B5 : FSKGEN0 enable control register
0 : Stop
1 : Operate
Setting this bit to “1” makes the FSK generator 0 (FSKGEN0) start operating.

Note:
To activate FSKGEN0, be sure to do so when TGEN0 and DPGEN0 are in a stop state. It is not allowed to use TGEN0, FSKGEN0 and DPGEN0 simultaneously.

B4 : TD_RXDET0 enable control register
0 : Stop
1 : Operate
Setting this bit to “1” makes TD_RXDET0 start operating.

B3 : TD_TXDET0 enable control register
0 : Stop
1 : Operate
Setting this bit to “1” makes TD_TXDET0 start operating.

B2 : DTMF0 enable control register
0 : Stop
1 : Operate
Setting this bit to “1” makes DTMFDET0 start operating.

B1 : EC0 enable control register
0 : Stop (The echo canceller will be bypassed.)
1 : Operate
Setting this bit to “1” makes EC0 start operating.
Remarks: At the time of operation start of EC0, the echo canceller's internal coefficients are cleared and then activated.

B0 : Reserved bit. Do not change the initial values.

Note:
If either TD_RXDET0 or TD_TXDET0 is activated, using TONE_RXDET0 is not allowed, nor is TONE_TXDET0.

(26) CR26

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR26	TONE_RXDET1EN	TONE_TXDET1EN	FGEN1_EN	TD_RXDET1EN	TD_TXDET1EN	DTMF1_EN	EC1_EN	#	R/W
Mode where setting can be changed	I/E	I/E	I/E	I/E	I/E	I/E	I/E	—	
Initial value	0	0	0	0	0	0	0	0	

B7 : TONE_RXDET1 enable control register
0 : Stop
1 : Operate
Setting this bit to “1” makes TONE_RXDET1 start operating.

B6 : TONE_TXDET1 enable control register
0 : Stop
1 : Operate
Setting this bit to “1” makes TONE_TXDET1 start operating.

B5 : FGEN1 enable control register
0 : Stop
1 : Operate
Setting this bit to “1” makes the FSK generator 1 (FSKGEN1) start operating.

Note:
To activate FSKGEN1, be sure to do so with TGEN1 and DPGEN1 placed in a stop state. Using TGEN1, FSKGEN1 and DPGEN1 simultaneously is not allowed.

B4 : TD_RXDET1 enable control register
0 : Stop
1 : Operate
Setting this bit to “1” makes TD_RXDET1 start operating.

B3 : TD_TXDET1 enable control register
0 : Stop
1 : Operate
Setting this bit to “1” makes TD_TXDET1 start operating.

B2 : DTMFDET1 enable control register
0 : Stop
1 : Operate
Setting this bit to “1” makes DTMFDET1 start operating.

B1 : EC1 enable control register
0 : Stop (The echo canceller will be bypassed.)
1 : Operate
Setting this bit to “1” makes EC1 start operating.
Remarks: At the time of operation start of EC1, the echo canceller's internal coefficients are cleared and then activated.

B0 : Reserved bit. Do not change the initial values.

Note:
If either TD_RXDET1 or TD_TXDET1 is activated, using TONE_RXDET1 is not allowed, nor is TONE_TXDET1.

(27) CR27

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR27	#	DPGEN 0_EN	DPGEN 0_POL	DPGEN 0_PPS	DPGEN 0_D3	DPGEN 0_D2	DPGEN 0_D1	DPGEN 0_D0	R/W
Mode where setting can be changed	—	I/E	I/	I/E	I/E	I/E	I/E	I/E	
Initial value	0	0	0	0	0	0	0	0	

B7 : Reserved bits. Do not change the initial values.

B6 : DPGEN0 transmission control register
0 : Stops transmission
1 : Output operation

B5 : DPGEN0 output polarity control register
0 : Positive logic (Low: Break interval; High: Make interval)
1 : Negative logic (Low:Make interval; High: Break interval)

B4 : DPGEN0 speed control register
0 : 10 pps
1 : 20 pps

B3–B0 : DPGEN0 dial pulse count setting register
Set the number of dial pulses to be transmitted.
Upper limit : 10 (Data: Ah)
Lower limit : 1 (Data: 1h)

Note: Before activating DPGEN0 (DPGEN0_EN = 1), be sure to set the following:
- Set the DPGEN0 output polarity control register (DPGEN0_POL).

By this setting, the output level (initial value) of the dial pulse output pin will be as follows:
When DPGEN0_POL = 0 (positive logic) : DPO0 = “0”
When DPGEN0_POL = 1 (negative logic) : DPO0 = “1”

- After the above setting, set the primary/secondary function selection register (GPFA[0]) of GPIOA[0] to “1”, and set to the secondary function (dial pulse output pin).

Note:
To activate DPGEN0, be sure to do so with TGEN0 and FSKGEN0 placed in a stop state. Using TGEN0, FSKGEN0 and DPGEN0 concurrently is not allowed.

(28) CR28

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR28	#	DPGEN 1_EN	DPGEN 1_POL	DPGEN 1_PPS	DPGEN 1_D3	DPGEN 1_D2	DPGEN 1_D1	DPGEN 1_D0	R/W
Mode where setting can be changed	—	I/E	I/	I/E	I/E	I/E	I/E	I/E	
Initial value	0	0	0	0	0	0	0	0	

B7 : Reserved bits. Do not change the initial values.

B6 : DPGEN1 output control register
0 : Stops output
1 : Output operation

B5 : DPGEN1 output polarity control register
0 : Positive logic (Low: Break interval; High: Make interval)
1 : Negative logic (Low:Make interval; High: Break interval)

B4 : DPGEN1 speed control register
0 : 10 pps
1 : 20 pps

B3–B0 : DPGEN1 dial pulse count setting register
Set the number of dial pulses to be transmitted.
Upper limit : 10 (Data: Ah)
Lower limit : 1 (Data: 1h)

Note: Before activating DPGEN1 (DPGEN1_EN = 1), be sure to set the following:
- Set the DPGEN1 output polarity control register (DPGEN1_POL).

By this setting, the output level (initial value) of the dial pulse output pin will be as follows:
When DPGEN1_POL = 0 (positive logic) : DPO1 = “0”
When DPGEN1_POL = 1 (negative logic) : DPO1 = “1”

- After the above setting, set the primary/secondary function selection register (GPFA[1]) of GPIOA[1] to “1”, and set to the secondary function (dial pulse output pin).

Note:
To activate DPGEN1, be sure to do so with TGEN1 and FSKGEN1 placed in a stop state. Using TGEN1, FSKGEN1 and DPGEN1 concurrently is not allowed.

(29) CR29

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR29	#	#	#	#	#	#	#	FGEN0_FLAG	R/W
Mode where setting can be changed	—	—	—	—	—	—	—	I/E	
Initial value	0	0	0	0	0	0	0	0	

B7–B1 : Reserved bits. Do not change the initial values.

B0 : FGEN0 output data setting completion flag
After writing data to the FGEN0 output data setting register (FGEN0_D[7:0]), set this bit to “1”. Once the loading of data into the internal buffer of the FSK signal generation section is complete, this bit is automatically cleared to “0”.
Do not write to this register while this bit is “1”.

(30) CR30

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR30	#	#	#	#	#	#	#	FGEN1_FLAG	R/W
Mode where setting can be changed	—	—	—	—	—	—	—	I/E	
Initial value	0	0	0	0	0	0	0	0	

B7–B1 : Reserved bits. Do not change the initial values.

B0 : FGEN1 output data setting completion flag
After writing data to the FGEN1 output data setting register (FGEN1_D[7:0]), set this bit to “1”. Once the loading of data into the internal buffer of the FSK signal generation section is complete, this bit is automatically cleared to “0”.
Do not write to this register while this bit is “1”.

(31) CR31

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR31	DPDET 0_D7	DPDET 0_D6	DPDET 0_D5	DPDET 0_D4	DPDET 0_D3	DPDET 0_D2	DPDET 0_D1	DPDET 0_D0	
Mode where setting can be changed	—								R/
Initial value	0	0	0	0	0	0	0	0	

B7–B0 : DPDET0 detection dial pulse count display register
Displays the number of detection dial pulses of DPDET0.

Note:
Read the DPDET0 detection dial pulse count display register (DPDET0-D[7:0]) at the timing when the value of the DPDET0 detection status register (DP0_DET) chagnes from “1” to “0”.

(32) CR32

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR32	DPDET 1_D7	DPDET 1_D6	DPDET 1_D5	DPDET 1_D4	DPDET 1_D3	DPDET 1_D2	DPDET 1_D1	DPDET 1_D0	
Mode where setting can be changed	—								R/
Initial value	0	0	0	0	0	0	0	0	

B7–B0 : DPDET1 detection dial pulse count display register
Displays the number of detection dial pulses of DPDET1.

Note:
Read the DPDET1 detection dial pulse count display register (DPDET1-D[7:0]) at the timing when the value of the DPDET1 detection status register (DP1_DET) chagnes from “1” to “0”.

(33) CR33

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR33	ITS0_ SEL	#	#	#	PCM_ ITS0[3]	PCM_ ITS0[2]	PCM_ ITS0[1]	PCM_ ITS0[0]	R/W
Mode where setting can be changed	I/E	—	—	—	I/E	I/E	I/E	I/E	
Initial value	0	0	0	0	0	0	0	0	

B7 : PCM input buffer 0 high order/low order selection register
0 : Selects low-order 8 bits
1 : Selects high-order 8 bits

B6–B4 : Reserved bits. Do not change the initial values.

B3–B0 : PCM input buffer 0 time slot selection register
Set the number of the time slot into which PCM data will be loaded according to the selection chart shown in Table 5.
To receive the PCM data at the specified time slot position, it is necessary to set the PCM input buffer 0 enable control register (PCMI0_EN) to “1”.

Table 5 PCM Input Buffer 0 Time Slot Selections

B3	B2	B1	B0	Time Slot
0	0	0	0	Slot1
0	0	0	1	Slot2
0	0	1	0	Slot3
0	0	1	1	Slot4
0	1	0	0	Slot5
0	1	0	1	Slot6
0	1	1	0	Slot7
0	1	1	1	Slot8
1	0	0	0	Slot9
1	0	0	1	Slot10
1	0	1	0	Slot11
1	0	1	1	Slot12
1	1	0	0	Slot13
1	1	0	1	Slot14
1	1	1	0	Slot15
1	1	1	1	Slot16

Note:
When making settings in this register, make sure that the value of the PCM input buffer 0 enable control register (PCMI0_EN) is “0”.

The maximum settable time slot number will be n[n = (BCLK frequency) ÷ 128K]. Setting any time slot number larger than the maximum time slot number above is not allowed.

(34) CR34

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR34	ITS1_ SEL	#	#	#	PCM_ ITS1[3]	PCM_ ITS1[2]	PCM_ ITS1[1]	PCM_ ITS1[0]	R/W
Mode where setting can be changed	I/E	—	—	—	I/E	I/E	I/E	I/E	
Initial value	0	0	0	0	0	0	0	0	

B7 : PCM input buffer 1 high order/low order selection register
0 : Selects low-order 8 bits
1 : Selects high-order 8 bits

B6–B4 : Reserved bits. Do not change the initial values.

B3–B0 : PCM input buffer 1 time slot selection register
Set the number of the time slot to which PCM data will be loaded according to the selection chart shown in Table 6.
To receive the PCM data at the specified time slot position, it is necessary to set the PCM input buffer 1 enable control register (PCMI1_EN) to “1”.

Table 6 PCM Input Buffer 1 Time Slot Selections

B3	B2	B1	B0	Time Slot
0	0	0	0	Slot1
0	0	0	1	Slot2
0	0	1	0	Slot3
0	0	1	1	Slot4
0	1	0	0	Slot5
0	1	0	1	Slot6
0	1	1	0	Slot7
0	1	1	1	Slot8
1	0	0	0	Slot9
1	0	0	1	Slot10
1	0	1	0	Slot11
1	0	1	1	Slot12
1	1	0	0	Slot13
1	1	0	1	Slot14
1	1	1	0	Slot15
1	1	1	1	Slot16

Note:
When making settings in this register, make sure that the value of the PCM input buffer 1 enable control register (PCMI1_EN) is “0”.

The maximum settable time slot number will be n[n = (BCLK frequency) ÷ 128K]. Setting any time slot number larger than the maximum time slot number above is not allowed.

(35) CR35

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR35	OTS0_ SEL	#	#	#	PCM_ OTS0[3]	PCM_ OTS0[2]	PCM_ OTS0[1]	PCM_ OTS0[0]	R/W
Mode where setting can be changed	I/E	—	—	—	I/E	I/E	I/E	I/E	
Initial value	0	0	0	0	0	0	0	0	

B7 : PCM output buffer 0 high order/low order selection register
0 : Selects low-order 8 bits
1 : Selects high-order 8 bits

B6–B4 : Reserved bits. Do not change the initial values.

B3–B0 : PCM output buffer 0 time slot selection register
Set the number of the time slot at which PCM data will be output according to the selection chart shown in Table 7.
To transmit PCM data at the specified time slot position, it is necessary to set the PCM output buffer 0 enable control register (PCMO0_EN) to “1”.

Table 7 PCM Output Buffer 0 Time Slot Selections

B3	B2	B1	B0	Time Slot
0	0	0	0	Slot1
0	0	0	1	Slot2
0	0	1	0	Slot3
0	0	1	1	Slot4
0	1	0	0	Slot5
0	1	0	1	Slot6
0	1	1	0	Slot7
0	1	1	1	Slot8
1	0	0	0	Slot9
1	0	0	1	Slot10
1	0	1	0	Slot11
1	0	1	1	Slot12
1	1	0	0	Slot13
1	1	0	1	Slot14
1	1	1	0	Slot15
1	1	1	1	Slot16

Note:
When making settings in this register, make sure that the value of the PCM output buffer 0 enable control register (PCMO0_EN) is “0”.

The maximum settable time slot number will be n[n = (BCLK frequency) ÷ 128K]. Setting any time slot number larger than the maximum time slot number above is not allowed.

(36) CR36

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR36	ITS2_ SEL	#	#	#	PCM_ ITS2[3]	PCM_ ITS2[2]	PCM_ ITS2[1]	PCM_ ITS2[0]	R/W
Mode where setting can be changed	I/E	—	—	—	I/E	I/E	I/E	I/E	
Initial value	0	0	0	0	0	0	0	0	

B7 : PCM input buffer 2 high order/low order selection register
0 : Selects low-order 8 bits
1 : Selects high-order 8 bits

B6–B4 : Reserved bits. Do not change the initial values.

B3–B0 : PCM input buffer 2 time slot selection register
Set the number of the time slot to which PCM data will be loaded according to the selection chart shown in Table 8.
To receive the PCM data at the specified time slot position, it is necessary to set the PCM input buffer 2 enable control register (PCMI2_EN) to “1”.

Table 8 PCM Input Buffer 2 Time Slot Selections

B3	B2	B1	B0	Time Slot
0	0	0	0	Slot1
0	0	0	1	Slot2
0	0	1	0	Slot3
0	0	1	1	Slot4
0	1	0	0	Slot5
0	1	0	1	Slot6
0	1	1	0	Slot7
0	1	1	1	Slot8
1	0	0	0	Slot9
1	0	0	1	Slot10
1	0	1	0	Slot11
1	0	1	1	Slot12
1	1	0	0	Slot13
1	1	0	1	Slot14
1	1	1	0	Slot15
1	1	1	1	Slot16

Note:
When making settings in this register, make sure that the value of the PCM input buffer 2 enable control register (PCMI2_EN) is “0”.

The maximum settable time slot number will be n[n = (BCLK frequency) ÷ 128K]. Setting any time slot number larger than the maximum time slot number above is not allowed.

Using a PCM interface as a speech codec interface is not currently supported; therefore, do not change the initial value of the register described above.

(37) CR37

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR37	ITS3_ SEL	#	#	#	PCM_ ITS3[3]	PCM_ ITS3[2]	PCM_ ITS3[1]	PCM_ ITS3[0]	R/W
Mode where setting can be changed	I/E	—	—	—	I/E	I/E	I/E	I/E	
Initial value	0	0	0	0	0	0	0	0	

B7 : PCM input buffer 3 high order/low order selection register
0 : Selects low-order 8 bits
1 : Selects high-order 8 bits

B6–B4 : Reserved bits. Do not change the initial values.

B3–B0 : PCM input buffer 3 time slot selection register
Set the number of the time slot to which PCM data will be loaded according to the selection chart shown in Table 9.
To receive the PCM data at the specified time slot position, it is necessary to set the PCM input buffer 3 enable control register (PCMI3_EN) to “1”.

Table 9 PCM Input Buffer 3 Time Slot Selections

B3	B2	B1	B0	Time Slot
0	0	0	0	Slot1
0	0	0	1	Slot2
0	0	1	0	Slot3
0	0	1	1	Slot4
0	1	0	0	Slot5
0	1	0	1	Slot6
0	1	1	0	Slot7
0	1	1	1	Slot8
1	0	0	0	Slot9
1	0	0	1	Slot10
1	0	1	0	Slot11
1	0	1	1	Slot12
1	1	0	0	Slot13
1	1	0	1	Slot14
1	1	1	0	Slot15
1	1	1	1	Slot16

Note:
When making settings in this register, make sure that the value of the PCM input buffer 3 enable control register (PCMI3_EN) is “0”.

The maximum settable time slot number will be n[n = (BCLK frequency) ÷ 128K]. Setting any time slot number larger than the maximum time slot number above is not allowed.

Using a PCM interface as a speech codec interface is not currently supported; therefore, do not change the initial value of the register described above.

(38) CR38

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR38	OTS1_ SEL	#	#	#	PCM_ OTS1[3]	PCM_ OTS1[2]	PCM_ OTS1[1]	PCM_ OTS1[0]	R/W
Mode where setting can be changed	I/E	—	—	—	I/E	I/E	I/E	I/E	
Initial value	0	0	0	0	0	0	0	0	

B7 : PCM output buffer 1 high order/low order selection register
0 : Selects low-order 8 bits
1 : Selects high-order 8 bits

B6–B4 : Reserved bits. Do not change the initial values.

B3–B0 : PCM output buffer 1 time slot selection register
Set the number of the time slot at which PCM data will be output according to the selection chart shown in Table 10.
To transmit PCM data at the specified time slot position, it is necessary to set the PCM output buffer 1 enable control register (PCMO1_EN) to “1”.

Table 10 PCM Output Buffer 1 Time Slot Selections

B4	B3	B2	B1	B0	Time Slot
0	0	0	0	0	Slot1
0	0	0	0	1	Slot2
0	0	0	1	0	Slot3
0	0	0	1	1	Slot4
0	0	1	0	0	Slot5
0	0	1	0	1	Slot6
0	0	1	1	0	Slot7
0	0	1	1	1	Slot8
0	1	0	0	0	Slot9
0	1	0	0	1	Slot10
0	1	0	1	0	Slot11
0	1	0	1	1	Slot12
0	1	1	0	0	Slot13
0	1	1	0	1	Slot14
0	1	1	1	0	Slot15
0	1	1	1	1	Slot16

Note:
When making settings in this register, make sure that the value of the PCM output buffer 1 enable control register (PCMO1_EN) is “0”.

The maximum settable time slot number will be n[n = (BCLK frequency) ÷ 128K]. Setting any time slot number larger than the maximum time slot number above is not allowed.

(39) CR39

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR39	$	$	$	$	$	$	$	$	
Mode where setting can be changed	—	—	—	—	—	—	—	—	/
Initial value	—	—	—	—	—	—	—	—	

B7–B0 : Reserved bits. Access prohibited.

(40) CR40

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR40	$	$	$	$	$	$	$	$	
Mode where setting can be changed	—	—	—	—	—	—	—	—	/
Initial value	—	—	—	—	—	—	—	—	

B7–B0 : Reserved bits. Access prohibited.

(41) CR41

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR41	$	$	$	$	$	$	$	$	
Mode where setting can be changed	—	—	—	—	—	—	—	—	/
Initial value	—	—	—	—	—	—	—	—	

B7–B0 : Reserved bits. Access prohibited.

(42) CR42

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR42	FGEN0_D7	FGEN0_D6	FGEN0_D5	FGEN0_D4	FGEN0_D3	FGEN0_D2	FGEN0_D1	FGEN0_D0	R/W
Mode where setting can be changed	I/E								
Initial value	0	0	0	0	0	0	0	0	

B7–B0 : FGEN0 output data setting register

For more information, see the description of the FSK generator 0 (FSKGEN0) in the section of “INTERNAL MEMORY ACCESS AND VARIOUS CONTROL METHODS” described later.

(43) CR43

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR43	FGEN1_D7	FGEN1_D6	FGEN1_D5	FGEN1_D4	FGEN1_D3	FGEN1_D2	FGEN1_D1	FGEN1_D0	R/W
Mode where setting can be changed	I/E								
Initial value	0	0	0	0	0	0	0	0	

B7–B0 : FGEN1 output data setting register

For more information, see the description of the FSK generator 1 (FSKGEN1) in the section of “INTERNAL MEMORY ACCESS AND VARIOUS CONTROL METHODS” described later.

(44) CR44

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR44	T1_ TXON	T1_ RXON	R1_ TXON	R1_ RXON	T0_ TXON	T0_ RXON	R0_ TXON	R0_ RXON	R/W
Mode where setting can be changed	I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
Initial value	0	0	0	0	0	0	0	0	

B7 : T1_TXON switch control register
0 : No connect
1 : Connect

B6 : T1_RXON switch control register
0 : No connect
1 : Connect

B5 : R1_TXON switch control register
0 : No connect
1 : Connect

B4 : R1_RXON switch control register
0 : No connect
1 : Connect

B3 : T0_TXON switch control register
0 : No connect
1 : Connect

B2 : T0_RXON switch control register
0 : No connect
1 : Connect

B1 : R0_TXON switch control register
0 : No connect
1 : Connect

B0 : R0_RXON switch control register
0 : No connect
1 : Connect

Make a setting of either connect or no connect for the speech path switch described above if three-way calling is implemented. For the configuration for implementing three-way calling, see the application configuration examples described later.

(45) CR45

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR45	#	#	TIM_EN	#	DPDET 1_POL	DPDET 1_EN	DPDET 0_POL	DPDET 0_EN	R/W
Mode where setting can be changed	—	—	I/E	—	I/	I/E	I/	I/E	
Initial value	0	0	0	0	0	0	0	0	

B7, B6 : Reserved bits. Do not change the initial values.

B5 : Timer control register
0 : Stops counting.
1 : Starts counting.

B4 : Reserved bits. Do not change the initial values.

B3 : DPDET1 polarity control register
Controls the polarity to be input from the GPIOB[1] pin.
0 : Does not invert polarity.
1 : Inverts polarity.

B2 : DPDET1 activation control register
0 : Stop
1 : Operate

B1 : DPDET0 polarity control register
Controls the polarity to be input from the GPIOB[0] pin.
0 : Does not invert polarity.
1 : Inverts polarity.

B0 : DPDET0 control register
0 : Stop
1 : Operate

(46) CR46

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR46	$	$	$	$	$	$	$	$	
Mode where setting can be changed	—	—	—	—	—	—	—	—	/
Initial value	—	—	—	—	—	—	—	—	

B7–B0 : Reserved bits. Access prohibited.

(47) CR47

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR47	$	$	$	$	$	$	$	$	
Mode where setting can be changed	—	—	—	—	—	—	—	—	/
Initial value	—	—	—	—	—	—	—	—	

B7–B0 : Reserved bits. Access prohibited.

(48) GPCR0

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
GPCR0	#	#	#	#	#	#	GPMA[1]	GPMA[0]	R/W
Mode where setting can be changed	—	—	—	—	—	—	I/E	I/E	
Initial value	0	0	0	0	0	0	0	0	

With this register (GPMA[1:0]), the direction (input or output) of general-purpose input/output port A[1:0] (GPIOA[1:0]) can be set for each bit.

B7–B2 : Reserved bits. Do not change the initial values.

B1 : GPIOA[1] input/output setting register
0 : Input
1 : Output
If GPFA[1] is set to the secondary function (DPO1), the pin is always placed in an output state.

B0 : GPIOA[0] input/output setting register
0 : Input
1 : Output
If GPFA[0] is set to the secondary function (DPO0), the pin is always placed in an output state.

(49) GPCR1

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
GPCR1	#	#	#	#	#	#	GPDA[1]	GPDA[0]	R/W
Mode where setting can be changed	—	—	—	—	—	—	I/E	I/E	
Initial value	0	0	0	0	0	0	(*1)	(*1)	

*1: Depends on the pin status.

This register (GPDA[1:0]) stores the input/output data of general-purpose input/output port A[1:0] (GPIOA[1:0]).
When it is set as a general-purpose output port, if a value is written to any bit of this register, the written value is output from the corresponding pin. Also in this case, if any bit of this register is read, the value of the corresponding bit is read.
When it is set as a general-purpose input port, if any bit of this register is read, the status of the corresponding pin can be read. Also in this case, if a value is written to any bit of this register, the register value is updated but the status of the pin does not change.
If the port is configured as its secondary function by the primary/secondary function selection register, the register value is updated by writing to any bit of this register, but the status of the corresponding pin does not change. Furthermore, if GPMA[1:0] is configured as input, the status of the corresponding pin is read; if configured as output, the value of the corresponding bit is read.

B7–B2 : Reserved bits. Do not change the initial values.

B1 : Data register for GPIOA[1]

GPFA[1]	GPMA[1]	At read	At write
0: GPIOA[1]	0: Input	Pin status	No change in pin status
	1: Output	Value of GPDA[1]	Written vaule is output from the corresponding pin.
1: DPO1	0: Input	Pin status	No change in pin status
	1: Output	Value of GPDA[1]	No change in pin status

B0 : Data register for GPIOA[0]

GPFA[0]	GPMA[0]	At read	At write
0: GPIOA[0]	0: Input	Pin status	No change in pin status
	1: Output	Value of GPDA[0]	Written vaule is output from the corresponding pin.
1: DPO0	0: Input	Pin status	No change in pin status
	1: Output	Value of GPDA[0]	No change in pin status

(50) GPCR2

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
GPCR2	#	#	#	#	#	#	GPFA[1]	GPFA[0]	R/W
Mode where setting can be changed	—	—	—	—	—	—	I/E	I/E	
Initial value	0	0	0	1	1	1	0	0	

With this register (GPFA[1:0]), the primary/secondary function of general-purpose input/output port A[1:0] (GPIOA[1:0]) can be selected.

B7–B2 : Reserved bits. Do not change the initial values.

B1 : GPIOA[1] primary function/secondary function selection register
0 : General-purpose input/output port A[1] (Initial value)
1 : DPO1 (dial pulse output pin)

B0 : GPIOA[0] primary function/secondary function selection register
0 : General-purpose input/output port A[0] (Initial value)
1 : DPO0 (dial pulse output pin)

(51) GPCR3

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
GPCR3	#	#	#	#	GPMB[3]	GPMB[2]	GPMB[1]	GPMB[0]	R/W
Mode where setting can be changed	—	—	—	—	I/E	I/E	I/E	I/E	
Initial value	0	0	0	0	0	0	0	0	

With this register (GPMB[3:0]), the direction (input or output) of general-purpose input/output port B[3:0] (GPIOB[3:0]) can be set for each bit.

B7–B4 : Reserved bits. Do not change the initial values.

B3 : GPIOB[3] input/output setting register
0 : Input
1 : Output

B2 : GPIOB[2] input/output setting register
0 : Input
1 : Output

B1 : GPIOB[1] input/output setting register
0 : Input
1 : Output

B0 : GPIOB[0] input/output setting register
0 : Input
1 : Output

(52) GPCR4

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
GPCR4	#	#	#	#	GPDB[3]	GPDB[2]	GPDB[1]	GPDB[0]	R/W
Mode where setting can be changed	—	—	—	—	I/E	I/E	I/E	I/E	
Initial value	0	0	0	0	(*1)	(*1)	(*1)	(*1)	

*1: Depends on the pin status.

This register (GPDB[3:0]) stores the input/output data of general-purpose input/output port B[3:0] (GPIOB[3:0]). When it is set as a general-purpose output port, if a value is written to any bit of this register, the written value is output from the corresponding pin. Also in this case, if any bit of this register is read, the value of the corresponding bit is read.
When it is set as a general-purpose input port, if any bit of this register is read, the status of the corresponding pin can be read. Also in this case, if a value is written to any bit of this register, the register value is updated but the status of the pin does not change.

B7–B4 : Reserved bits. Do not change the initial values.

B3 : Data register for GPIOB[3]

GPMB[3]	At read	At write
0: Input	Pin status	No change in pin status
1: Output	Value of GPDB[3]	Written vaule is output from the corresponding pin.

B2 : Data register for GPIOB[2]

GPMB[2]	At read	At write
0: Input	Pin status	No change in pin status
1: Output	Value of GPDB[2]	Written vaule is output from the corresponding pin.

B1 : Data register for GPIOB[1]

GPMB[1]	At read	At write
0: Input	Pin status	No change in pin status
1: Output	Value of GPDB[1]	Written vaule is output from the corresponding pin.

B0 : Data register for GPIOB[0]

GPMB[0]	At read	At write
0: Input	Pin status	No change in pin status
1: Output	Value of GPDB[0]	Written vaule is output from the corresponding pin.

(53) GPCR5

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
GPCR5a	$	$	$	$	$	$	$	$	/
Mode where setting can be changed	—	—	—	—	—	—	—	—	
Initial value	0	0	0	0	1	1	1	1	

B7–B0 : Reserved bits. Access prohibited.

(54) GPCR6

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
GPCR6	GPMC[7]	GPMC[6]	GPMC[5]	GPMC[4]	GPMC[3]	GPMC[2]	GPMC[1]	GPMC[0]	R/W
Mode where setting can be changed	I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
Initial value	0	0	0	0	0	0	0	0	

With this register (GPMC[7:0]), the direction (input or output) of general-purpose input/output port C[7:0] (GPIOC[7:0]) can be set for each bit.

B7 : GPIOC[7] input/output setting register
0 : Input
1 : Output

B6 : GPIOC[6] input/output setting register
0 : Input
1 : Output

B5 : GPIOC[5] input/output setting register
0 : Input
1 : Output

B4 : GPIOC[4] input/output setting register
0 : Input
1 : Output

B3 : GPIOC[3] input/output setting register
0 : Input
1 : Output

B2 : GPIOC[2] input/output setting register
0 : Input
1 : Output

B1 : GPIOC[1] input/output setting register
0 : Input
1 : Output

B0 : GPIOC[0] input/output setting register
0 : Input
1 : Output

(55) GPCR7

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
GPCR7	GPDC[7]	GPDC[6]	GPDC[5]	GPDC[4]	GPDC[3]	GPDC[2]	GPDC[1]	GPDC[0]	R/W
Mode where setting can be changed	I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
Initial value	(*1)	(*1)	(*1)	(*1)	(*1)	(*1)	(*1)	(*1)	

*1: Depends on the pin status.

This register (GPDC[7:0]) stores the input/output data of general-purpose input/output port C[7:0] (GPIOC[7:0]). When it is set as a general-purpose output port, if a value is written to any bit of this register, the written value is output from the corresponding pin. Also in this case, if any bit of this register is read, the value of the corresponding bit is read.
When it is set as a general-purpose input port, if any bit of this register is read, the status of the corresponding pin can be read. Also in this case, if a value is written to any bit of this register, the register value is updated but the status of the pin does not change.

B7 : Data register for GPIOC[7]

GPMB[7]	At read	At write
0: Input	Pin status	No change in pin status
1: Output	Value of GPDC[7]	Written vaule is output from the corresponding pin.

B6 : Data register for GPIOC[6]

GPMB[6]	At read	At write
0: Input	Pin status	No change in pin status
1: Output	Value of GPDC[6]	Written vaule is output from the corresponding pin.

B5 : Data register forGPIOC[5]

GPMB[5]	At read	At write
0: Input	Pin status	No change in pin status
1: Output	Value of GPDC[5]	Written vaule is output from the corresponding pin.

B4 : Data register forGPIOC[4]

GPMB[4]	At read	At write
0: Input	Pin status	No change in pin status
1: Output	Value of GPDC[4]	Written vaule is output from the corresponding pin.

B3 : Data register for GPIOC[3]

GPMB[3]	At read	At write
0: Input	Pin status	No change in pin status
1: Output	Value of GPDC[3]	Written vaule is output from the corresponding pin.

B2 : Data register for GPIOC[2]

GPMB[2]	At read	At write
0: Input	Pin status	No change in pin status
1: Output	Value of GPDC[2]	Written vaule is output from the corresponding pin.

B1 : Data register for GPIOC[1]

GPMB[1]	At read	At write
0: Input	Pin status	No change in pin status
1: Output	Value of GPDC[1]	Written vaule is output from the corresponding pin.

B0 : Data register for GPIOC[0]

GPMB[0]	At read	At write
0: Input	Pin status	No change in pin status
1: Output	Value of GPDC[0]	Written vaule is output from the corresponding pin.

(56) CRCR8

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
GPCR8	$	$	$	$	$	$	$	$	
Mode where setting can be changed	—	—	—	—	—	—	—	—	/
Initial value	1	1	1	1	1	1	1	1	

B7–B0 : Reserved bits. Access prohibited.

(57)DLCR0

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
DLCR0	#	#	#	#	#	#	DL_ SEL	DL_ EN	R/W
Mode where setting can be changed	—	—	—	—	—	—	D/	D/	
Initial value	0	0	0	0	0	0	0	0	

B7–B2 : Reserved bits. Do not change the initial values.

B1 : Download circuit access control register
0 : PRAM access mode
1 : DRAM access mode

B0 : Download circuit activation control register
0 : Stop
1 : Activate

(58) DLCR1

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
DLCR1	DL_ A7	DL_ A6	DL_ A5	DL_ A4	DL_ A3	DL_ A2	DL_ A1	DL_ A0	R/W
Mode where setting can be changed	D/	D/	D/	D/	D/	D/	D/	D/	
Initial value	0	0	0	0	0	0	0	0	

B7–B0 : Download address setting register 0
When writing data to PRAM/DRAM, set the start address of PRAM/DRAM (lower 8 bits: A7–A0) into this register.

(59) DLCR2

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
DLCR2	DL_ A15	DL_ A14	DL_ A13	DL_ A12	DL_ A11	DL_ A10	DL_ A9	DL_ A8	R/W
Mode where setting can be changed	D/	D/	D/	D/	D/	D/	D/	D/	
Initial value	0	0	0	0	0	0	0	0	

B7–B0 : Download address setting register 1
When writing data to PRAM/DRAM, set the start address of PRAM/DRAM (upper 8 bits: A15–A8) into this register.

Also, when in the PRAM access mode, the address (DL_A[15:0]) is automatically incremented each time data is written to the download data buffer register 2 (DL_BUF[23:16])
Furthermore, when in the DRAM access mode, the address (DL_A[15:0]) is automatically incremented each time data is written to the download data buffer register 1 (DL_BUF[15:8]).

(60) DLCR3

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
DLCR3	DL_ BUF7	DL_ BUF6	DL_ BUF5	DL_ BUF4	DL_ BUF3	DL_ BUF2	DL_ BUF1	DL_ BUF0	
Mode where setting can be changed	D/	D/	D/	D/	D/	D/	D/	D/	/W
Initial value	(*1)	(*1)	(*1)	(*1)	(*1)	(*1)	(*1)	(*1)	

*1: The initial value of this register is undefined.

B7–B0 : Download data buffer register 0

When writing data to PRAM/DRAM, write data (D7-D0) via this register.

(61) DLCR4

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
DLCR4	DL_ BUF15	DL_ BUF14	DL_ BUF13	DL_ BUF12	DL_ BUF11	DL_ BUF10	DL_ BUF9	DL_ BUF8	
Mode where setting can be changed	D/	D/	D/	D/	D/	D/	D/	D/	/W
Initial value	(*1)	(*1)	(*1)	(*1)	(*1)	(*1)	(*1)	(*1)	

*1: The initial value of this register is undefined.

B7–B0 : Download data buffer register 1

When writing data to PRAM/DRAM, write data (D15–D8) via this register.

In the DRAM access mode, the 16-bit data of DL_BUF[15:0] is stored in the DRAM's address (DL_A[15:0]) by writing data to this register. Furthermore, the address (DL_A[15:0]) is automatically incremented each time data is written to this register.

(62) DLCR5

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
DLCR5	DL_ BUF23	DL_ BUF22	DL_ BUF21	DL_ BUF20	DL_ BUF19	DL_ BUF18	DL_ BUF17	DL_ BUF16	
Mode where setting can be changed	D/	D/	D/	D/	D/	D/	D/	D/	/W
Initial value	(*1)	(*1)	(*1)	(*1)	(*1)	(*1)	(*1)	(*1)	

*1: The initial value of this register is undefined.

B7–B0 : Download data buffer register 2

When writing data to PRAM, write data (D23-D16) via this register.

In the PRAM access mode, the 24-bit data of DL_BUF[23:0] is stored in the PRAM's address (DL_A[15:0]) by writing data to this register. Furthermore, the address (DL_A[15:0]) is automatically incremented each time data is written to this register.

INTERNAL MEMORY ACCESS AND VARIOUS CONTROL METHODS

Various controls can be performed by accessing the internal data memories of this LSI. This LSI has two built-in DSPs (DSP_A and DSP_B), each of which is embedded with separate internal data memories.
The 8-bit registers CR6a–CR9a, which are mapped inside the control registers on the DSP_A side, are assigned to the following for the purpose of accessing the internal data memory on the DSP_A side.

16-bit address of internal data memory (A15–A0)
16-bit data for reading and writing (D15–D0)

Similarly, the 8-bit registers CR6b–CR9b, which are mapped inside the control registers on the DSP_B side, are assigned to the following for the purpose of accessing the internal data memories on the DSP_B side.

16-bit address of internal data memory (A15–A0)
16-bit data for reading and writing (D15–D0)

The following shows the methods of writing to and reading from the internal data memories. Moreover, Table 11 shows internal data memory lists.

Note that the following descriptions are given as common explanations of the DSP_A and DSP_B sides. To change the internal data memories on the DSP_A side, acceess the control registers (CR0a–CR47a) on the DSP_A side, and to change the internal data memories on the DSP_B side, access the control registers (CR0b–CR47b) on the DSP_B side.

Write Method (1 Word)

By setting the internal data memory 1-word write control register (XDMWR) to "1" after setting an internal data memory address and write data in CR6–CR9, the writing of internal data memory for one word will be completed. XDMWR will automaticlly be cleared to "0" upon completion of a write operation. Figure 34 shows the method of writing one word to an internal data memory.
To rewrite a multiple number of memories with distributed addresses, repeat the write operation described above. After all writes are finished, a normal operation will start by setting the operation start control register (OPE_STAT) to "1".

The internal data memories are write enabled even in the normal operation mode. Also in such a case, use the same method as described above.

Note:
When data is set in the internal data memory during normal operaiton mode, since in that case the reading is done in synchronization with the SYNC signal (8 kHz), maintain the state for 250 μs or more.

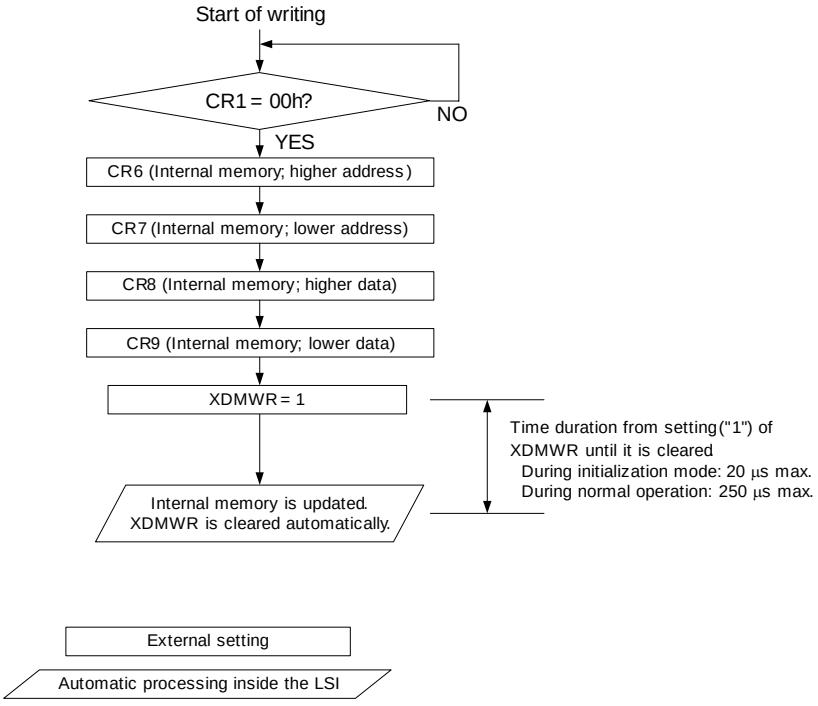


Figure 34 Internal Data Memory Write Method (1 Word)

Write Method (Multiple Words)

When writing to contiguous address spaces in an internal data memory, multiple words (2N words) can be written consecutively without setting addresses individually, as described below.

1) Setting the Start Address

Set the starting address according to the write method (1 word) shown in Figure 34.

Set the address of the internal data memory for setting the start address for writing multiple words in CR6–CR7, and set the start address of the internal data memory to which multiple words will actually be written (START_ADDRESS) in CR8–CR9.

Next, by setting the internal data memory 1-word write control register (XDMWR) to "1", START_ADDRESS will be written to the internal data memory. Note that XDMWR will automatically be cleared to "0" upon completion of a write operation.

2) Writing Data

After the writing of START_ADDRESS finishes, data can be written in succession for every two words without setting addresses individually, according to the procedure below.

By setting the internal data memory 2-word write control register (XDMWR_2) to "1" after setting write data (first word) in CR6–CR7 and write data (second word) in CR8–CR9, the first word data is written to START_ADDRESS + 0 and the second word data to START_ADDRESS + 1, and after write operations finish, XDMWR_2 is automatically cleared to "0".

Thereafter, repeat the writing of data for every two words according to the procedure described in "2) Writing Data" until a write of 2N words finishes. (The write destination address will automatically be updated.)

Figure 35 shows the method of writing (multiple words) to an internal data memory.

The internal data memories are write enabled even in the normal operation mode. Also in such a case, use the same method as described above.

Note:

When data is set in the internal data memory during normal operaiton mode, since in that case the reading is done in synchronization with the SYNC signal (8 kHz), maintain the state for 250 μs or more.

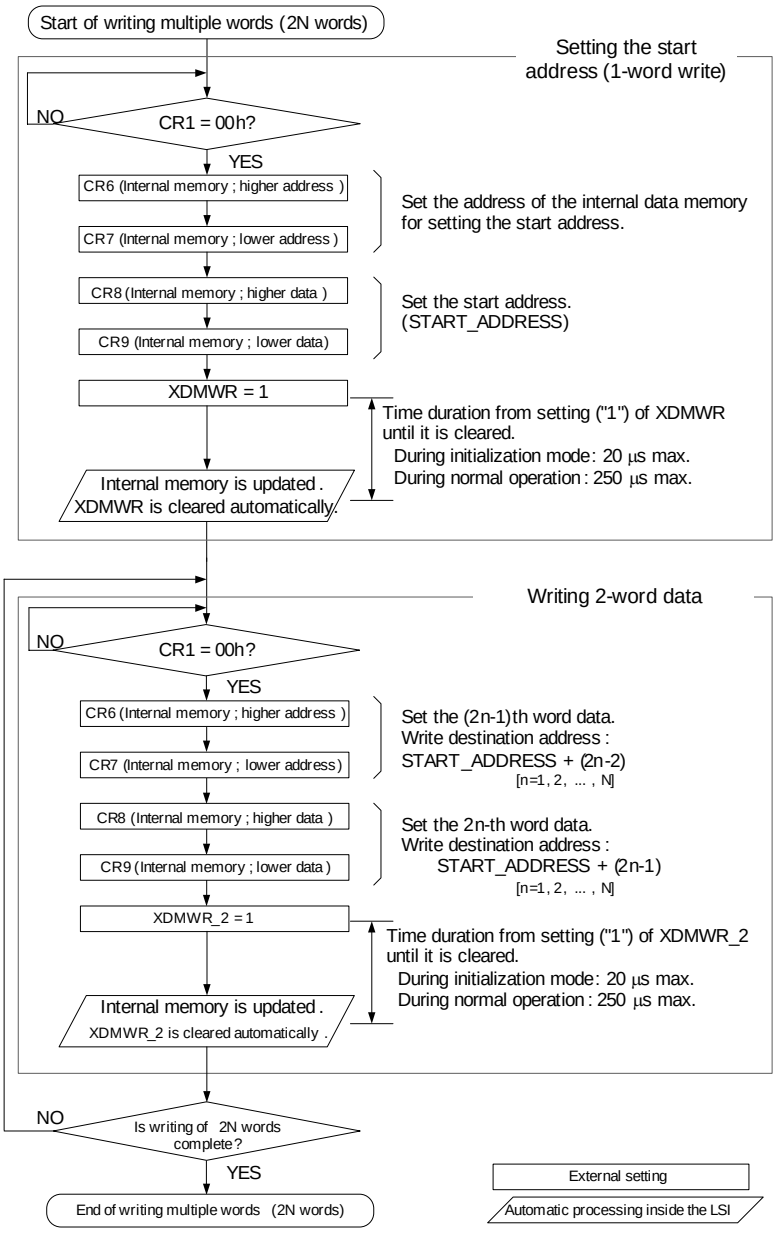


Figure 35 Internal Data Memory Write Method (Multiple Words)

Read Method

After setting the internal data memory address in CR6 and CR7, one word of data from the internal data memory is stored in CR8 and CR9 setting the internal data memory read control register (XDMRD) to "1". After reading the data, XDMRD will be cleared to "0" automatically. The method of reading the internal data memory is shown in Figure 36.
Reading the internal data memory is only available for the internal data memories and the read only data memories within the related registers listed in Table 11.

The internal data memories are write enabled even in the normal operation mode. Also in such a case, use the same method as described above.

Note:
When an internal data memory is read during normal operaiton mode, since in that case the reading is done in synchronization with the SYNC signal (8 kHz), maintain the set address in the same state for 250 µs or more.

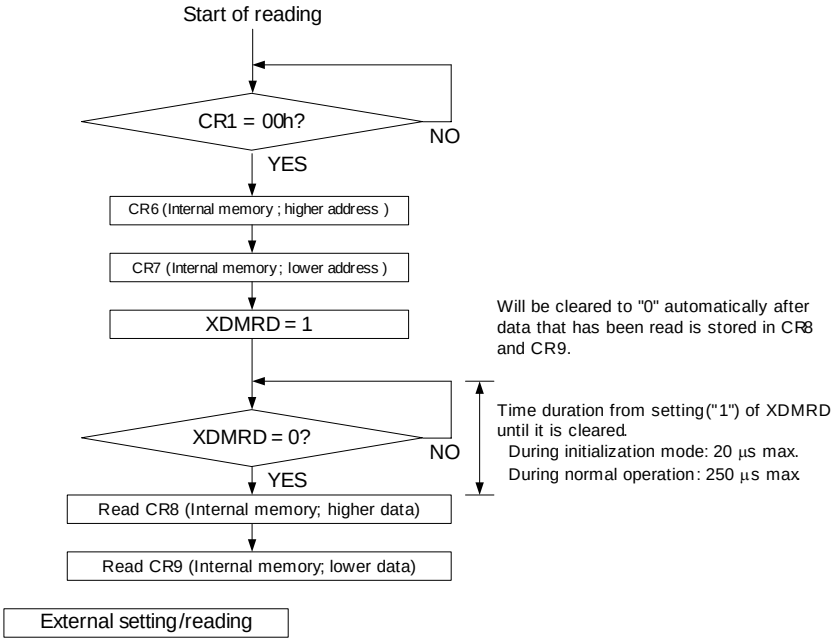


Figure 36 Internal Data Memory Read Method

In tables that follow, note the following terms/symbols and their meaning:
Initial mode: Indicates the state after completion of downloading of the DSP firmware, and in which the initial values of control registers and internal data memories can be changed.
During idle state: Indicates the state in which the function given in the function name column is being stopped.
During operation: Indicates the state in which the function given in the function name column is operating.
○: Supported
×: Not supported
[ ] : Related control register

Table 11 List of Internal Data Memories and Related Control Registers (Page 1 of 12)

Function name	Internal data memory name / related control register name	Address	Initial value		Mode that allows change of setting and reading		
			Data	Data value	During initial mode	During idle state	During operation
Gain control	Transmit path related						
	Internal data memory for adjusting CH0 transmit gain 0 (TXGAIN0_CH0)	0081h	0080h	0 dB	○	○	○
	Internal data memory for adjusting CH0 transmit gain 1 (TXGAIN1_CH0)	0083h	0080h	0 dB	○	○	○
	Internal data memory for adjusting CH1 transmit gain 0 (TXGAIN0_CH1)	0082h	0080h	0 dB	○	○	○
	Internal data memory for adjusting CH1 transmit gain 1 (TXGAIN1_CH1)	0084h	0080h	0 dB	○	○	○
	Receive path related						
	Internal data memory for adjusting CH0 receive gain 0 (RXGAIN0_CH0)	0085h	0080h	0 dB	○	○	○
	Internal data memory for adjusting CH0 receive gain 1 (RXGAIN1_CH0)	0087h	0080h	0 dB	○	○	○
	Internal data memory for adjusting CH1 receive gain 0 (RXGAIN0_CH1)	0086h	0080h	0 dB	○	○	○
	Internal data memory for adjusting CH1 receive gain 1 (RXGAIN1_CH1)	0088h	0080h	0 dB	○	○	○
	Side tone						
	Internal data memory for adjusting CH0 side tone gain (STGAIN_CH0)	007Dh	0000h	MUTE	○	○	○
	Internal data memory for adjusting CH1 side tone gain (STGAIN_CH1)	007Eh	0000h	MUTE	○	○	○
	Fade control related						
	Internal data memory for gain fade control (GAIN_FADE_CONT)	0089h	0000h	Stop	○	○	×
	Internal data memory for gain fade-in step value control (GAIN_FADE_IN_ST)	008Ah	4C10h	+1.5 dB	○	○ (*1)	×
	Internal data memory for gain fade-out step value control (GAIN_FADE_OUT_ST)	008Bh	35D9h	−1.5 dB	○	○ (*1)	×

*1: Applies when the gain fade control is stopped.

Table 11 List of Internal Data Memories and Related Control Registers (Page 2 of 12)

Function name	Internal data memory name / related control register name	Address	Initial value		Mode that allows change of setting and reading		
			Data	Data value	During initial mode	During idle state	During operation
Tone generation 0 TGEN0	TGEN0 transmission control register	CR2	00h	Transmission stop	○	○	○
	TONE A frequency control (TGEN0_FREQ_A)	0BC5h	0CCDh	400 Hz	○	○	×
	TONE B frequency control (TGEN0_FREQ_B)	0BC7h	007Bh	15 Hz	○	○	×
	TONE A gain control (TGEN0_GAIN_A)	0BC9h	0080h	−13.3 dBm0	○	○	○
	TONE B gain control (TGEN0_GAIN_B)	0BCAh	0080h	−13.3 dBm0	○	○	○
	TGEN0 output time control 0 (TGEN0_TIM_M0)	0BCBh	0FA0h	500 ms	○	○	×
	TGEN0 output time control 1 (TGEN0_TIM_M1)	0BCEh	0FA0h	500 ms	○	○	×
	TGEN0 RX side tone total gain control (TGEN0_RXGAIN_TOTAL)	0BD2h	0080h	0 dB	○	○	○
	TGEN0 TX side tone total gain control (TGEN0_TXGAIN_TOTAL)	0BD3h	0080h	0 dB	○	○	○
	Internal data memory for TGEN0 fade control (TGEN0_FADE_CONT)	0BBDh	0000h	Stop	○	○	×
	Internal data memory for TGEN0 fade-in step value control (TGEN0_FADE_IN_ST)	0BBEh	47CFh	+1 dB	○	○	×
	Internal data memory for TGEN0 fade-out step value control (TGEN0_FADE_OUT_ST)	0BBFh	390Ah	−1 dB	○	○	×
	Internal data memory for TGEN0 fade-out time control (TGEN0_FADE_OUT_TIM)	0BC0h	002Bh	43 Sync	○	○	×
	Internal data memory for TGEN0 total gain fade control (TGEN0_GAIN_TOTAL_FADE_CONT)	0BCFh	0000h	Stop	○	○	×
	Internal data memory for TGEN0 total gain fade-in step value control (TGEN0_GAIN_TOTAL_FADE_IN_ST)	0BD0h	4C10h	+1.5 dB	○	○	×
	Internal data memory for TGEN0 total gain fade-out step value control (TGEN0_GAIN_TOTAL_FADE_OUT_ST)	0BD1h	35D9h	−1.5 dB	○	○	×
	TGEN0 execution status flag indication register (TGEN0_EXFLAG)	CR19-B2	0b	Being stopped	○	○	○

Table 11 List of Internal Data Memories and Related Control Registers (Page 3 of 12)

Function name	Internal data memory name / related control register name	Address	Initial value		Mode that allows change of setting and reading		
			Data	Data value	During initial mode	During idle state	During operation
Tone generation 1 TGEN1	TGEN1 transmission control register	CR3	00h	Transmission stop	○	○	○
	TONE C frequency control (TGEN1_FREQ_C)	0BDCh	0CCDh	400 Hz	○	○	×
	TONE D frequency control (TGEN1_FREQ_D)	0BDEh	007Bh	15 Hz	○	○	×
	TONE C gain control (TGEN1_GAIN_C)	0BE0h	0080h	–13.3 dBm0	○	○	○
	TONE D gain control (TGEN1_GAIN_D)	0BE1h	0080h	–13.3 dBm0	○	○	○
	TGEN1 output time control 0 (TGEN1_TIM_M0)	0BE2h	0FA0h	500 ms	○	○	×
	TGEN1 output time control 1 (TGEN1_TIM_M1)	0BE5h	0FA0h	500 ms	○	○	×
	TGEN1 RX side tone total gain control (TGEN1_RXGAIN_TOTAL)	0BE9h	0080h	0 dB	○	○	○
	TGEN1 TX side tone total gain control (TGEN1_TXGAIN_TOTAL)	0BEAh	0080h	0 dB	○	○	○
	Internal data memory for TGEN1 fade control (TGEN1_FADE_CONT)	0BD4h	0000h	Stop	○	○	×
	Internal data memory for TGEN1 fade-in step value control (TGEN1_FADE_IN_ST)	0BD5h	47CFh	+1 dB	○	○	×
	Internal data memory for TGEN1 fade-out step value control (TGEN1_FADE_OUT_ST)	0BD6h	390Ah	–1 dB	○	○	×
	Internal data memory for TGEN1 fade-out time control (TGEN1_FADE_OUT_TIM)	0BD7h	002Bh	43 Sync	○	○	×
	Internal data memory for TGEN1 total gain fade control (TGEN1_GAIN_TOTAL_FADE_CONT)	0BE6h	0000h	Stop	○	○	×
	Internal data memory for TGEN1 total gain fade-in step value control (TGEN1_GAIN_TOTAL_FADE_IN_ST)	0BE7h	4C10h	+1.5 dB	○	○	×
	Internal data memory for TGEN1 total gain fade-out step value control (TGEN1_GAIN_TOTAL_FADE_OUT_ST)	0BE8h	35D9h	–1.5 dB	○	○	×
	TGEN1 execution status flag indication register (TGEN1_EXFLAG)	CR20-B2	0b	Being stopped	○	○	○

Table 11 List of Internal Data Memories and Related Control Registers (Page 4 of 12)

Function name	Internal data memory name / related control register name	Address	Initial value		Mode that allows change of setting and reading		
			Data	Data value	During initial mode	During idle state	During operation
FSK0 generator FSK GEN0	FGEN0 enable control register (FGEN0_EN)	CR25-B5	0b	Stop	○	○	○
	FGEN0 output data setup completion flag (FGEN0_FLAG)	CR29-B0	0b	Write enable	○	○	○
	FGEN0 output data setup register (FGEN0_D[7:0])	CR42	00h	00h	○	○	○
	Internal data memory for FGEN0 gain control (FGEN0_GAIN)	0362h	0080h	−13.3 dBm0	○	○	×
FSK1 generator FSK GEN1	FGEN1 enable control register (FGEN1_EN)	CR26-B5	0b	Stop	○	○	○
	FGEN1 output data setup completion flag (FGEN1_FLAG)	CR30-B0	0b	Write enable	○	○	○
	FGEN1 output data setup register (FGEN1_D[7:0])	CR43	00h	00h	○	○	○
	Internal data memory for FGEN1 gain control (FGEN1_GAIN)	0370h	0080h	−13.3 dBm0	○	○	×

Table 11 List of Internal Data Memories and Related Control Registers (Page 5 of 12)

Function name	Internal data memory name / related control register name	Address	Initial value		Mode that allows change of setting and reading		
			Data	Data value	During initial mode	During idle state	During operation
TONE detector RX0 TONE_RX DET0	TONE_RXDET0 enable control register (TONE_RXDET0EN)	CR25-B7	0b	Stop	○	○	○
	TONE_RXDET0 detection status register (TONE_RXDET0)	CR17-B7	0b	Not detected	○	○	○
	Internal data memory for TONE_RXDET0 main signal detection level control (TONE_RXDET0_S_TH)	218Ah	1EBBh	–5.3 dBm0	○	○	×
	Internal data memory for TONE_RXDET0 noise detection level control (TONE_RXDET0_N_TH)	219Fh	1EBBh	–5.3 dBm0	○	○	×
	Internal data memory for TONE_RXDET0 detection ON guard timer (TONE_RXDET0_ON_TM)	21A0h	0028h	5 ms	○	○	×
	Internal data memory for TONE_RXDET0 detection OFF guard timer (TONE_RXDET0_OFF_TM)	21A1h	0028h	5 ms	○	○	×
	Internal data memory for TONE_RXDET0 detection frequency control (TONE_RXDET0_FREQ)	----h	—	400 Hz	○	○	×
TONE detector TX0 TONE_TX DET0	TONE_TXDET0 enable control register (TONE_TXDET0EN)	CR25-B6	0b	Stop	○	○	○
	TONE_TXDET0 detection status register (TONE_TXDET0)	CR17-B6	0b	Not detected	○	○	○
	Internal data memory for TONE_TXDET0 main signal detection level control (TONE_TXDET0_S_TH)	215Eh	1EBBh	–5.3 dBm0	○	○	×
	Internal data memory for TONE_TXDET0 noise detection level control (TONE_TXDET0_N_TH)	2173h	1EBBh	–5.3 dBm0	○	○	×
	Internal data memory for TONE_TXDET0 detection ON guard timer (TONE_TXDET0_ON_TM)	2174h	0028h	5 ms	○	○	×
	Internal data memory for TONE_TXDET0 detection OFF guard timer (TONE_TXDET0_OFF_TM)	2175h	0028h	5 ms	○	○	×
	Internal data memory for TONE_TXDET0 detection frequency control(TONE_TXDET0_FREQ)	----h	—	400 Hz	○	○	×

Table 11 List of Internal Data Memories and Related Control Registers (Page 6 of 12)

Function name	Internal data memory name / related control register name	Address	Initial value		Mode that allows change of setting and reading		
			Data	Data value	During initial mode	During idle state	During operation
TONE detector RX1 TONE_RX DET1	TONE_RXDET1 enable control register (TONE_RXDET1EN)	CR26-B7	0b	Stop	○	○	○
	TONE_RXDET1 detection status register (TONE_RXDET1)	CR18-B7	0b	Not detected	○	○	○
	Internal data memory for TONE_RXDET1 main signal detection level control (TONE_RXDET1_S_TH)	21E2h	1EBBh	–5.3 dBm0	○	○	×
	Internal data memory for TONE_RXDET1 noise detection level control (TONE_RXDET1_N_TH)	21F7h	1EBBh	–5.3 dBm0	○	○	×
	Internal data memory for TONE_RXDET1 detection ON guard timer (TONE_RXDET1_ON_TM)	21F8h	0028h	5 ms	○	○	×
	Internal data memory for TONE_RXDET1 detection OFF guard timer (TONE_RXDET1_OFF_TM)	21F9h	0028h	5 ms	○	○	×
	Internal data memory for TONE_RXDET1 detection frequency control (TONE_RXDET1_FREQ)	----h	—	400 Hz	○	○	×
TONE detector TX1 TONE_TX DET1	TONE_TXDET1 enable control register (TONE_TXDET1EN)	CR26-B6	0b	Stop	○	○	○
	TONE_TXDET1 detection status register (TONE_TXDET1)	CR18-B6	0b	Not detected	○	○	○
	Internal data memory for TONE_TXDET1 main signal detection level control (TONE_TXDET1_S_TH)	21B6h	1EBBh	–5.3 dBm0	○	○	×
	Internal data memory for TONE_TXDET1 noise detection level control (TONE_TXDET1_N_TH)	21CBh	1EBBh	–5.3 dBm0	○	○	×
	Internal data memory for TONE_TXDET1 detection ON guard timer (TONE_TXDET1_ON_TM)	21CCh	0028h	5 ms	○	○	×
	Internal data memory for TONE_TXDET1 detection OFF guard timer (TONE_TXDET1_OFF_TM)	21CDh	0028h	5 ms	○	○	×
	Internal data memory for TONE_TXDET1 detection frequency control (TONE_TXDET1_FREQ)	----h	—	400 Hz	○	○	×

Table 11 List of Internal Data Memories and Related Control Registers (Page 7 of 12)

Function name	Internal data memory name / related control register name	Address	Initial value		Mode that allows change of setting and reading		
			Data	Data value	During initial mode	During idle state	During operation
Tone disabler TD0	TD_RXDET0 enable control register (TD_RXDET0_EN)	CR25-B4	0b	Stop	○	○	○
	TD_RXDET0 2100 Hz single-tone detection status register (ANS_RXDET0)	CR19-B3	0b	Not detected	○	○	○
	TD_RXDET0 2100 Hz phase inversion detection status register (ANSPM_RXDET0)	CR19-B4	0b	Not detected	○	○	○
	Internal data memory for TD_RXDET0 detection level control (TD_RXDET0_TH)	2387h	241Fh	–34 dBm0	○	○	×
	Internal data memory for TD_RXDET0 ON guard timer (TD_RXDET0_ON_TM)	07E9h	0028h	5 ms	○	○	×
	Internal data memory for TD_RXDET0 OFF guard timer (TD_RXDET0_OFF_TM)	07EAh	0028h	5 ms	○	○	×
	Internal data memory for TD_RXDET0 noise detection function control (TD_RXDET0_NDET_CONT)	2398h	313Fh	Enabled	○	○	×
	TD_TXDET0 enable control register (TD_TXDET0_EN)	CR25-B3	0b	Stop	○	○	○
	TD_TXDET0 2100 Hz single-tone detection status register (ANS_TXDET0)	CR19-B5	0b	Not detected	○	○	○
	TD_TXDET0 2100 Hz phase inversion detection status register (ANSPM_TXDET0)	CR19-B6	0b	Not detected	○	○	○
	Internal data memory for TD_TXDET0 detection level control (TD_TXDET0_TH)	235Ah	241Fh	–34 dBm0	○	○	×
	Internal data memory for TD_TXDET0-ON guard timer (TD_TXDET0_ON_TM)	07E7h	0028h	5 ms	○	○	×
	Internal data memory for TD_TXDET0-OFF guard timer (TD_TXDET0_OFF_TM)	07E8h	0028h	5 ms	○	○	×
	Internal data memory for TD_TXDET0 noise detection function control (TD_TXDET0_NDET_CONT)	236Bh	313Fh	Enabled	○	○	×

Table 11 List of Internal Data Memories and Related Control Registers (Page 8 of 12)

Function name	Internal data memory name / related control register name	Address	Initial value		Mode that allows change of setting and reading		
			Data	Data value	During initial mode	During idle state	During operation
Tone disabler TD1	TD_RXDET1 enable control register (TD_RXDET1_EN)	CR26-B4	0b	Stop	○	○	○
	TD_RXDET1 2100 Hz single-tone detection status register (ANS_RXDET1)	CR20-B3	0b	Not detected	○	○	○
	TD_RXDET1 2100 Hz phase inversion detection status register (ANSPM_RXDET1)	CR20-B4	0b	Not detected	○	○	○
	Internal data memory for TD_RXDET1 detection level control (TD_RXDET1_TH)	23E1h	241Fh	–34 dBm0	○	○	×
	Internal data memory for TD_RXDET1 ON guard timer (TD_RXDET1_ON_TM)	07EDh	0028h	5 ms	○	○	×
	Internal data memory for TD_RXDET1 OFF guard timer (TD_RXDET1_OFF_TM)	07EEh	0028h	5 ms	○	○	×
	Internal data memory for TD_RXDET1 noise detection function control (TD_RXDET1_NDET_CONT)	23F2h	313Fh	Enabled	○	○	×
	TD_TXDET1 enable control register (TD_TXDET1_EN)	CR26-B3	0b	Stop	○	○	○
	TD_TXDET1 2100 Hz single-tone detection status register (ANS_TXDET1)	CR20-B5	0b	Not detected	○	○	○
	TD_TXDET1 2100 Hz phase inversion detection status register (ANSPM_TXDET1)	CR20-B6	0b	Not detected	○	○	○
	Internal data memory for TD_TXDET1 detection level control (TD_TXDET1_TH)	23B4h	241Fh	–34 dBm0	○	○	×
	Internal data memory for TD_TXDET1 ON guard timer (TD_TXDET1_ON_TM)	07EBh	0028h	5 ms	○	○	×
	Internal data memory forTD_TXDET1 OFF guard timer (TD_TXDET1_OFF_TM)	07ECh	0028h	5 ms	○	○	×
	Internal data memory for TD_TXDET1 noise detection function control (TD_TXDET1_NDET_CONT)	23C5h	313Fh	Enabled	○	○	×

Table 11 List of Internal Data Memories and Related Control Registers (Page 9 of 12)

Function name	Internal data memory name / related control register name	Address	Initial value		Mode that allows change of setting and reading		
			Data	Data value	During initial mode	During idle state	During operation
DTMF detector DTMF DET0	DTMF0 enable control register (DTMF0_EN)	CR25-B2	0b	Stop	○	○	○
	DTMF0 detection code indication register (DTMF0_C[3:0])	CR17-B[3:0]	0000b	0000b	○	○	○
	DTMF0 detection status register (DTMF0_DET)	CR17-B4	0b	Not detected	○	○	○
	Internal data memory for DTMF0 detection level control (DTMF0_TH)	25B4h	1000h	–37.0 dBm0	○	○	×
	Internal data memory for DTMF0 detection ON guard timer (DTMF0_ON_TM)	263Ch	00A0h	20 ms	○	○	×
	Internal data memory for DTMF0 detection OFF guard timer (DTMF0_OFF_TM)	263Eh	00A0h	20 ms	○	○	×
	Internal data memory for DTMF0 noise detection function control (DTMF0_NDET_CONT)	2616h	0002h	Noise detection enabled	○	○	×
DTMF detector DTMF DET1	DTMF1 enable control register (DTMF1_EN)	CR26-B2	0b	Stop	○	○	○
	DTMF1 detection code indication register (DTMF1_C[3:0])	CR18-B[3:0]	0000b	0000b	○	○	○
	DTMF1 detection status register (DTMF1_DET)	CR18-B4	0b	Not detected	○	○	○
	Internal data memory for DTMF1 detection level control (DTMF1_TH)	2640h	1000h	–37.0 dBm0	○	○	×
	Internal data memory for DTMF1 detection ON guard timer (DTMF1_ON_TM)	26C8h	00A0h	20 ms	○	○	×
	Internal data memory for DTMF1 detection OFF guard timer (DTMF1_OFF_TM)	26CAh	00A0h	20 ms	○	○	×
	Internal data memory for DTMF1 noise detection function control (DTMF1_NDET_CONT)	26A2h	0002h	Noise detection enabled	○	○	×
EC0	EC0 control register (EC0_EN)	CR25-B1	0b	Stop	○	○	○
	Internal data memory for EC0 control (EC0_CR)	0238h	0012h	HD ATT OFF	○	○	○
	Internal data memory for EC0 GLPAD control (EC0_GLPAD_CR)	0239h	000Fh	+6/–6 dB	○	○	×
	Internal data memory for controlling EC0 Comfort Noise generation function (EC0_CN_CONT)	023Ch	0003h	Enabled	○	○	○
EC1	EC1 control register (EC1_EN)	CR26-B1	0b	Stop	○	○	○
	Internal data memory for EC1 control (EC1_CR)	023Ah	0012h	HD ATT OFF	○	○	○
	Internal data memory for EC1 GLPAD control (EC1_GLPAD_CR)	023Bh	000Fh	+6/–6 dB	○	○	×
	Internal data memory for controlling EC1 Comfort Noise generation function (EC1_CN_CONT)	023Dh	0003h	Enabled	○	○	○

Table 11 List of Internal Data Memories and Related Control Registers (Page 10 of 12)

Function name	Internal data memory name / related control register name	Address	Initial value		Mode that allows change of setting and reading		
			Data	Data value	During initial mode	During idle state	During operation
DP detector DP DET0	DPDET0 activation control register (DPDET0_EN)	CR45-B0	0b	Stop	○	○	○
	DPDET0 detection status register (DP0_DET)	CR17-B5	0b	Not detected	○	○	○
	DPDET0 polarity control register (DPDET0_POL)	CR45-B1	0b	Positive logic	○	×	×
	DPDET0 dial pulse count indication register (DPDET0_D[7:0])	CR31-B[7:0]	00h	Not detected	○	○	○
	Internal data memory for setting DPDET0 ON guard timer (DPDET0_ON_TIM)	033Ch	0014h	5 ms	○	○	×
	DPDET0 OFF guard timer control (DPDET0_OFF_TIM)	033Dh	0014h	5 ms	○	○	×
	Internal data memory for setting DPDET0 detection end timer (DPDET0_DETOFF_TIM)	033Eh	01F4h	125 ms	○	○	×
DP detector DP DET1	DPDET1 activation control register (DPDET1_EN)	CR45-B2	0b	Stop	○	○	○
	DPDET1 detection status register (DP1_DET)	CR18-B5	0b	Not detected	○	○	○
	DPDET1 polarity control register (DPDET1_POL)	CR45-B3	0b	Positive logic	○	×	×
	DPDET1 dial pulse count indication register (DPDET1_D[7:0])	CR32-B[7:0]	00h	Not detected	○	○	○
	Internal data memory for setting DPDET1 ON guard timer (DPDET1_ON_TIM)	0344h	0014h	5 ms	○	○	×
	DPDET1 OFF guard timer control (DPDET1_OFF_TIM)	0345h	0014h	5 ms	○	○	×
	Internal data memory for setting DPDET1 detection end timer (DPDET1_DETOFF_TIM)	0346h	01F4h	125 ms	○	○	×

Table 11 List of Internal Data Memories and Related Control Registers (Page 11 of 12)

Function name	Internal data memory name / related control register name	Address	Initial value		Mode that allows change of setting and reading		
			Data	Data value	During initial mode	During idle state	During operation
DP transmitter DP GEN0	DPGEN0 transmit control register (DPGEN0_EN)	CR27-B6	0b	Stop	○	○	○
	DPGEN0 dial pulse count setup register (DPGEN0_D[3:0])	CR27-B[3:0]	0000b	Stop	○	○	×
	DPGEN0 speed control register (DPGEN0_PPS)	CR27-B4	0b	10 pps	○	○	×
	DPGEN0 output polarity control register (DPGEN0_POL)	CR27-B5	0b	Positive logic	○	×	×
	Internal data memory for DPGEN0 make ratio control (DPGEN0_DUTY)	0379h	0108h	33ms	○	○	×
	Internal data memory for DPGEN0 output termination control (DPGEN0_OFF_TIM)	037Bh	03E8h	125 ms	○	○	×
DP transmitter DP GEN1	DPGEN1 transmit control register (DPGEN1_EN)	CR28-B6	0b	Stop	○	○	○
	DPGEN1 dial pulse count setup register (DPGEN1_D[3:0])	CR28-B[3:0]	0000b	Stop	○	○	×
	DPGEN1 speed control register (DPGEN1_ PPS)	CR28-B4	0b	10 pps	○	○	×
	DPGEN1 output polarity control register (DPGEN1_POL)	CR28-B5	0b	Positive logic	○	×	×
	Internal data memory for DPGEN1 make ratio control (DPGEN1_DUTY)	0380h	0108h	33 ms	○	○	×
	Internal data memory for DPGEN1 output termination control (DPGEN1_OFF_TIM)	0382h	03E8h	125 ms	○	○	×
Outband control	Outband control 0 (OUTBAND_CONTROL0)	0336h	0000h	Stop	○	×	×
	Outband control 1 (OUTBAND_CONTROL1)	0337h	0000h	Stop	○	×	×
TIMER	Timer control register (TIM_EN)	CR45-B5	0b	Stop	○	○	○
	Timer counter value indication (TIM_COUNT) (Read-only data memory)	0350h	0000h	Count value	○	○	○
	Timer data setting (TIM_DATA)	0351h	FFFFh	MAX FFFFh	○	○	×

Table 11 List of Internal Data Memories and Related Control Registers (Page 12 of 12)

Function name	Internal data memory name / related control register name	Address	Initial value		Mode that allows change of setting and reading		
			Data	Data value	During initial mode	During idle state	During operation
Melody generator MGEN	MGEN high-speed read mode control register (MGEN_FREN)	CR24-B0	0b	Stop	○	○	○
	MGEN high-speed read mode notification flag (MGEN_FRFLAG)	CR19-B1	0b	Other than during high-speed read mode	○	○	○
	MGEN execution status flag indication register (MGEN_EXFLAG)	CR19-B0	0b	Being stopped	○	○	○
	TRACKm output control register (MGEN_TmEN: m = A, B, C)	CR4-B[7:5]	000b	Stop	○	○	×
	Output control register for MGEN high-speed read mode (MGEN_FOUT)	CR4-B0	0b	Stop	○	○	×
	Internal data memory for setting MGEN music data						
	MGEN_TRACKA_TIM	00B0 to 012E	xxxxh	Undefined	○	○	×
	MGEN_TRACKB_TIM	0130 to 01AE	xxxxh	Undefined	○	○	×
	MGEN_TRACKC_TIM	01B0 to 022E	xxxxh	Undefined	○	○	×
	MGEN_TRACKA_FREQ	00B1 to 012F	xxxxh	Undefined	○	○	×
	MGEN_TRACKB_FREQ	0131 to 01AF	xxxxh	Undefined	○	○	×
	MGEN_TRACKC_FREQ	01B1 to 022F	xxxxh	Undefined	○	○	×
	Internal data memory for MGEN melody gain control						
	MGEN_GAINA	0096h	0080h	0 dB	○	○	×
	MGEN_GAINB	009Bh	0080h	0 dB	○	○	×
	MGEN_GAINC	00A0h	0080h	0 dB	○	○	×
	Internal data memory for MGEN total gain control						
	MGEN_GAIN_TOTAL_FR	00ABh	0080h	0 dB	○	○	×
	Internal data memory for MGEN fade control						
	MGEN_FADE_CONT_STEP	00A7h	0056h	86sync	○	○	×
	MGEN_FADE_CONT_PL	00A9h	43CBh	+0.5 dB	○	○	×
	MGEN_FADE_CONT_MI	00AAh	3C6Bh	–0.5 dB	○	○	×
Decode control	Decode output start offset time control (DEC_ONTIM)	039Ah	0000h	0 ms	○	○	×
Internal RAM write	For setting the start address for writing multiple words (START_ADDRESS)	0030h	0000h	0000h	○	○	○

Gain Control

A. Gain related to the transmit path

A-1 : Internal data memory for adjusting CH0 transmit gain 0 (TXGAIN0_CH0)

Initial value : 0080h (0.0 dB)

When changing the gain value, compute it using the following equation:

Equation: 0080h × GAIN

Example: Making the gain +6 dB (× 2):

0080h × 2 = 0100h

Upper limit :	Approx. +40 dB	(data: 3200h)
	: 0 dB	(data: 0080h)
Lower limit :	Approx. –42 dB	(data: 0001h)
	: MUTE	(data: 0000h)

A-2 : Internal data memory for adjusting CH0 transmit gain 1 (TXGAIN1_CH0)

Initial value : 0080h (0.0 dB)

When changing the gain value, compute it using the following equation:

Equation: 0080h × GAIN

Example: Making the gain +6 dB (× 2):

0080h × 2 = 0100h

Upper limit :	Approx. +40 dB	(data: 3200h)
	: 0 dB	(data: 0080h)
Lower limit :	Approx. –42 dB	(data: 0001h)
	: MUTE	(data: 0000h)

A-3 : Internal data memory for adjusting CH1 transmit gain 0 (TXGAIN0_CH1)

Initial value : 0080h (0.0 dB)

When changing the gain value, compute it using the following equation:

Equation: 0080h × GAIN

Example: Making the gain +6 dB (× 2):

0080h× 2 = 0100h

Upper limit :	Approx. +40 dB	(data: 3200h)
	: 0 dB	(data: 0080h)
Lower limit :	Approx. –42 dB	(data: 0001h)
	: MUTE	(data: 0000h)

A-4 : Internal data memory for adjusting CH1 transmit gain 1 (TXGAIN1_CH1)

Initial value : 0080h (0.0 dB)

When changing the gain value, compute it using the following equation:

Equation: 0080h × GAIN

Example: Making the gain +6 dB (× 2):

0080h × 2 = 0100h

Upper limit :	Approx. +40 dB	(data: 3200h)
	: 0 dB	(data: 0080h)
Lower limit :	Approx. –42 dB	(data: 0001h)
	: MUTE	(data: 0000h)

B. Gain related to the receive path

B-1 : Internal data memory for adjusting CH0 receive gain 0 (RXGAIN0_CH0)
Initial value : 0080h (0.0 dB)
When changing the gain value, compute it using the following equation:
Equation: 0080h × GAIN
Example: Making the gain +6 dB (× 2):
0080h × 2 = 0100h

Upper limit	: Approx. +40 dB	(data: 3200h)
	: 0 dB	(data: 0080h)
Lower limit	: Approx. –42 dB	(data: 0001h)
	: MUTE	(data: 0000h)

B-2 : Internal data memory for adjusting CH0 receive gain 1 (RXGAIN1_CH0)
Initial value : 0080h (0.0 dB)
When changing the gain value, compute it using the following equation:
Equation: 0080h × GAIN
Example: Making the gain +6 dB (× 2):
0080h × 2 = 0100h

Upper limit	: Approx. +40 dB	(data: 3200h)
	: 0 dB	(data: 0080h)
Lower limit	: Approx. –42 dB	(data: 0001h)
	: MUTE	(data: 0000h)

B-3 : Internal data memory for adjusting CH1 receive gain 0 (RXGAIN0_CH1)
Initial value : 0080h (0.0 dB)
When changing the gain value, compute it using the following equation:
Equation: 0080h × GAIN
Example: Making the gain +6 dB (×2):
0080h × 2 = 0100h

Upper limit	: Approx. +40 dB	(data: 3200h)
	: 0 dB	(data: 0080h)
Lower limit	: Approx. –42 dB	(data: 0001h)
	: MUTE	(data: 0000h)

B-4 : Internal data memory for adjusting CH1 receive gain 1 (RXGAIN1_CH1)
Initial value : 0080h (0.0 dB)
When changing the gain value, compute it using the following equation:
Equation: 0080h × GAIN
Example: Making the gain +6 dB (× 2):
0080h × 2 = 0100h

Upper limit	: Approx. +40 dB	(data: 3200h)
	: 0 dB	(data: 0080h)
Lower limit	: Approx. –42 dB	(data: 0001h)
	: MUTE	(data: 0000h)

C. Side tone gain

C-1 : Internal data memory for adjusting CH0 side tone gain (STGAIN_CH0)

Initial value : 0000h (MUTE)

When changing the side tone gain value, compute it using the following equation:

Equation: 1000h × GAIN

Example: Making the gain –20 dB (× 0.1):

1000h × 0.1 = 019Ah

Upper limit :	0 dB	(data: 1000h)
Lower limit :	Approx. –72 dB	(data: 0001h)
	: MUTE	(data: 0000h)

C-2 : Internal data memory for adjusting CH1 side tone gain (STGAIN_CH1)

Initial value : 0000h (MUTE)

When changing the side tone gain value, compute it using the following equation:

Equation: 1000h × GAIN

Example: Making the gain –20 dB (× 0.1):

1000h × 0.1 = 019Ah

Upper limit :	0 dB	(data: 1000h)
Lower limit :	Approx. –72 dB	(data: 0001h)
	: MUTE	(data: 0000h)

D. Internal Data Memory for Gain Fade Control (GAIN_FADE_CONT)

The function for attenuating or amplifying to the gain after change at the specified step (gain fade-in/fade-out function) is provided for cases where the amount of gain has been changed except for the side tone gain.

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	—	—	—	—	—	—	—	OUT BAND_FC
Initial value	0	0	0	0	0	0	0	0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	RXGAIN 1_CH1	RXGAIN 0_CH1	RXGAIN 1_CH0	RXGAIN 0_CH0	TXGAIN 1_CH1	TXGAIN 0_CH1	TXGAIN 1_CH0	TXGAIN 0_CH0
Initial value	0	0	0	0	0	0	0	0

B15–B9 : Reserved bits. Do not change the initial values.

B8 : OUTBAND_FADE_CONT control
1 : ON (Performs fade-in/out processing when transitioning to, or returning from, mute processing.)
0 : OFF

B7 : RXGAIN1_CH1_FADECONT control
1 : ON (Performs fade-in/out processing when changing RXGAIN1_CH1.)
0 : OFF

B6 : RXGAIN0_CH1_FADECONT control
1 : ON (Performs fade-in/out processing when changing RXGAIN0_CH1.)
0 : OFF

B5 : RXGAIN1_CH0_FADECONT control
1 : ON (Performs fade-in/out processing when changing RXGAIN1_CH0.)
0 : OFF

B4 : RXGAIN0_CH0_FADECONT control
1 : ON (Performs fade-in/out processing when changing RXGAIN0_CH0.)
0 : OFF

B3 : TXGAIN1_CH1_FADECONT control
1 : ON (Performs fade-in/out processing when changing TXGAIN1_CH1.)
0 : OFF

B2 : TXGAIN0_CH1_FADECONT control
1 : ON (Performs fade-in/out processing when changing TXGAIN0_CH1.)
0 : OFF

B1 : TXGAIN1_CH0_FADECONT control
1 : ON (Performs fade-in/out processing when changing TXGAIN1_CH0.)
0 : OFF

B0 : TXGAIN0_CH0_FADECONT control
1 : ON (Performs fade-in/out processing when changing TXGAIN0_CH0.)
0 : OFF

E. Internal data memory for gain fade-in step value control (GAIN_FADE_IN_ST)

Initial value: 4C10h (+1.5dB)
When changing the step amount X, compute it using the following equation:
Equation: 10^ (X/20)*16384
Example: Making the step value +3 dB:
10^ (3/20)*16384 = 23143d = 5A67h
Maximum step value: +6.0 dB (data: 7FB2h)
Minimum step value: +0.1 dB (data: 40BEh)

F. Internal data memory for gain fade-out step value control (GAIN_FADE_OUT_ST)

Initial value : 35D9h (–1.5 dB)
When changing the step amount X, compute it using the following equation:
Equation: 10^ (X/20)*16384
Example: Making the step value –3 dB:
10^ (–3/20)*16384 = 11599d = 2D4Fh
Maximum step value: –6.0 dB (data: 2013h)
Minimum step value: –0.1 dB (data: 3F44h)

(Remarks) The step values of fade-in and fade-out can be set individually, but parameters that have been set will become common among all gain controllers that enable fade-in/fad-out processing.

Tone Generator 0 (TGEN0)

This generator can generate various tones on both the transmit and receive sides of CH0. The following describes various parameters that can be set for this generator.

A. Internal data memory for tone frequency control

TONE A frequency control (TGEN0_FREQ_A)

Initial value: 0CCDh (400 Hz)

TONE B frequency control (TGEN0_FREQ_B)

Initial value: 007Bh (15 Hz)

As the defaults, a tone of 400 Hz is output for TONE A and a tone of 15 Hz is output for TONE B. Use the following equation to compute the value of the setting when changing the frequency.

Equation: $f \times 8.192$ (f is the frequency to be set)

Example: To set a frequency of 2100 Hz:

$2100 \times 8.192 \neq 4333h$

Upper limit : 3 kHz (data: 6000h)

Lower limit : 15 Hz (data: 007Bh)

B. Internal data memory for tone gain control

TONE A gain control (TGEN0_GAIN_A)

Initial value: 0080h

TONE B gain control (TGEN0_GAIN_B)

Initial value: 0080h

The output level as the default will be –13.3 dBm0. Use the following equation to compute the value of the setting when changing the output level.

Equation: 0080h×GAIN

Example: For reducing the gain by 6 dB (×0.5):

$0080h \times 0.5 = 0040h$

Upper limit : +12 dB (data: 01FEh)

Lower limit : –12 dB (data: 0020h)

Note:

Make sure that the maximum amplitude does not exceed 3.17 dBm0 when the tones are multiplied or added.

C. Internal data memory for tone output time control (TGEN0_TIM_M0/TGEN0_TIM_M1)

TGEN0 output time control 0 (TGEN0_TIM_M0)

Initial value: 0FA0h (500ms)

TGEN0 output time control 1 (TGEN0_TIM_M1)

Initial value: 0FA0h (500ms)

Compute the value using the following equation when changing the time durations:
Equation: T/0.125 (T is the time duration in milliseconds)
Example: When setting a time duration of 200 ms:
200/0.125 = 1600d = 0640h
Upper limit: 4095.875 ms (data: 7FFFh)
Lower limit: 0.125 ms (data: 0001h)

Note:
Setting a time duration of 0000h (0 ms) is prohibited.

D. Internal data memory for tone total gain control (TGEN0_RXGAIN_TOTAL/TGEN0_TXGAIN_TOTAL)

TGEN0 RX-side tone total gain control (TGEN0_RXGAIN_TOTAL)

Initial value: 0080h

TGEN0 TX-side tone total gain control (TGEN0_TXGAIN_TOTAL)

Initial value: 0080h

The initial values will be 0 dB. Compute using the following equation when changing the output level.
Equation: 0080h × GAIN
Example: Decreasing the output level by 6 dB:
0080h × 0.5 = 0040h
Upper limit: +40 dB (data: 3200h)
Lower limit: –40 dB (data: 0001h)
: MUTE (data: 0000h)

Note:
The maximum amplitude should never exceed 3.17 dBm0.

E. Internal data memory for TGEN0 fade control (TGEN0_FADE_CONT)

Initial value: 0000h (stop)
Setting “0001h” in this data memory operates the fade-in/fade-out function of TGEN0 gain control.

0000h: Stops fade-in/fade-out
0001h: Operates fade-in/fade-out

Note:
When using this control function, set the fade-out time correctly.

F. Internal data memory for TGEN0 fade-in step value control (TGEN0_FADE_IN_ST)
Initial value: 47CFh (+1.0 dB)
When changing the step amount X, compute it using the following equation:
Equation: 10^ (X/20)*16384
Example: Making the step value +3 dB:
10^ (3/20)*16384 = 23143d = 5A67h
Maximum step value: +6.0 dB (data: 7FB2h)
Minimum step value: +0.1 dB (data: 40BEh)

G. Internal data memory for TGEN0 fade-out step value control (TGEN0_FADE_OUT_ST)
Initial value: 390Ah (–1.0 dB)
When changing the step amount X, compute it using the following equation:
Equation: 10^ (X/20)*16384
Example: Making the step value –3 dB:
10^ (–3/20)*16384 = 11599d = 2D4Fh
Maximum step value: –6.0 dB (data: 2013h)
Minimum step value: –0.1 dB (data: 3F44h)

H. Internal data memory for TGEN0 fade-out time control (TGEN0_FADE_OUT_TIM)
Initial value : 002Bh (43Sync)
When changing the fade-out time, compute it using the following equation:
Equation: 43 dB/"fade-out step value"dB
Example: When the step value is 2 dB:
43/2 = 22d =16h
Upper limit : 430 Sync (data: 01AEh)
Lower limit : 8 Sync (data: 0008h)

Notes:
Setting 0000h is prohibited.
Be sure to observe the following:
Fade-out time < TIM_M0, TIM_M1

(Remarks) The step values can be set individually, but parameters set will become common to TONE_A and TONE_B. Also, the operation control and stop time parameters will become common to TONE_A and TONE_B.

I. Internal data memory for TGEN0 total gain fade control (TGEN0_GAIN_TOTAL_FADE_CONT)
Initial value : 0000h (stop)
Setting "0001h" in this data memory operates the fade-in/fade-out function of TX side/RX side total gain control.

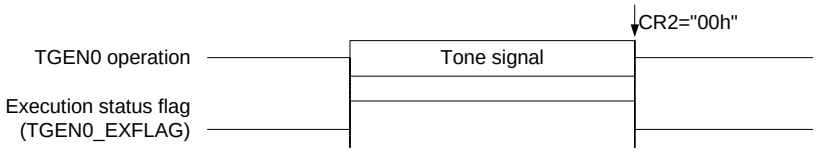
0000h : Stops fade-in/fade-out
0001h : Operates fade-in/fade-out

J. Internal data memory for TGEN0 total gain fade-in step value control (TGEN0_GAIN_TOTAL_FADE_IN_ST)
Initial value: 4C10h (+1.5 dB)
When changing the step amount X, compute it using the following equation:
Equation: 10^ (X/20)*16384
Example: Making the step value +3 dB:
10^ (3/20)*16384 = 23143d = 5A67h
Maximum step value: +6.0 dB (data: 7FB2h)
Minimum step value: +0.1 dB (data: 40BEh)

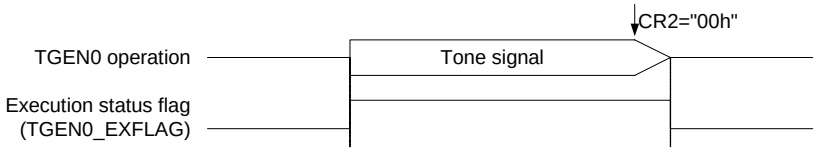
K. Internal data memory for TGEN0 total gain fade-out step value control
(TGEN0_GAIN_TOTAL_FADE_OUT_ST)
Initial value: 35D9h (–1.5 dB)
When changing the step amount X, compute it using the following equation:
Equation: 10^ (X/20)*16384
Example: Making the step value –3 dB:
10^ (–3/20)*16384 = 11599d = 2D4Fh
Maximum step value: –6.0 dB (data: 2013h)
Minimum step value: –0.1 dB (data: 3F44h)

(Remarks) The step values can be set individually, but parameters set will become common to TGEN0_RXGAIN_TOTAL and TGEN0_TXGAIN_TOTAL Also, the operation control and stop time parameters will become common to TGEN0_RXGAIN_TOTAL and TGEN0_TXGAIN_TOTAL.

L. TGEN0 execution status flag indication register (TGEN0_EXFLAG)
TGEN0_EXFLAG is set to “1” while the tone generator 0 is operating. (Initial value = “0”: Generator stopped)



When TGEN0_FADE_CONT is OFF



When TGEN0_FADE_CONT is ON

Tone Generator 1 (TGEN1)

This generator can generate various tones on both the transmit and receive sides of CH1. The following describes various parameters that can be set for this generator.

A. Internal data memory for tone frequency control

TONE C frequency control (TGEN1_FREQ_C)
Initial value: 0CCDh (400 Hz)
TONE D frequency control (TGEN1_FREQ_D)
Initial value: 007Bh (15 Hz)

As the defaults, a tone of 400 Hz is output for TONE C and a tone of 15 Hz is output for TONE D. Use the following equation to compute the value of the setting when changing the frequency.
Equation: $f \times 8.192$ (f is the frequency to be set)
Example: To set a frequency of 2100 Hz:
$2100 \times 8.192 \neq 4333h$
Upper limit : 3 kHz (data: 6000h)
Lower limit : 15 Hz (data: 007Bh)

B. Internal data memory for tone gain control

TONE C gain control (TGEN1_GAIN_C)
Initial value: 0080h
TONE D gain control (TGEN1_GAIN_D)
Initial value: 0080h

The output level as the default will be –13.3 dBm0. Use the following equation to compute the value of the setting when changing the output level.
Equation: 0080h×GAIN
Example: For reducing the gain by 6 dB (×0.5):
$0080h \times 0.5 = 0040h$
Upper limit : +12 dB (data: 01FEh)
Lower limit : –12 dB (data: 0020h)

Note:
Make sure that the maximum amplitude does not exceed 3.17 dBm0 when the tones are multiplied or added.

C. Internal data memory for tone output time control (TGEN1_TIM_M0/TGEN1_TIM_M1)

TGEN1 output time control 0 (TGEN1_TIM_M0)

Initial value: 0FA0h (500 ms)

TGEN1 output time control 1 (TGEN1_TIM_M1)

Initial value: 0FA0h (500 ms)

Compute the value using the following equation when changing the time durations:
Equation: T/0.125 (T is the time duration in milliseconds)
Example: When setting a time duration of 200 ms:
200/0.125 = 1600d = 0640h
Upper limit: 4095.875 ms (data: 7FFFh)
Lower limit: 0.125 ms (data: 0001h)

Note:
Setting a time duration of 0000h (0 ms) is prohibited.

D. Internal data memory for tone total gain control (TGEN1_RXGAIN_TOTAL/TGEN1_TXGAIN_TOTAL)

TGEN1 RX-side tone total gain control (TGEN1_RXGAIN_TOTAL)

Initial value: 0080h

TGEN1 TX-side tone total gain control (TGEN1_TXGAIN_TOTAL)

Initial value: 0080h

The initial values will be 0 dB. Compute using the following equation when changing the output level.
Equation: 0080h × GAIN
Example: Decreasing the output level by 6 dB:
0080h × 0.5 = 0040h
Upper limit: +40 dB (data: 3200h)
Lower limit: –40 dB (data: 0001h)
: MUTE (data: 0000h)

Note:
The maximum amplitude should never exceed 3.17 dBm0.

E. Internal data memory for TGEN1 fade control (TGEN1_FADE_CONT)

Initial value : 0000h (stop)
Setting “0001h” in this data memory operates the fade-in/fade-out function of TGEN1 gain control.

0000h : Stops fade-in/fade-out
0001h : Operates fade-in/fade-out

Note:
When using this control function, set the fade-out time correctly.

F. Internal data memory for TGEN1 fade-in step value control (TGEN1_FADE_IN_ST)
Initial value: 47CFh (+1.0 dB)
When changing the step amount X, compute it using the following equation:
Equation: 10^ (X/20)*16384
Example: Making the step value +3 dB:
10^ (3/20)*16384 = 23143d = 5A67h
Maximum step value: +6.0 dB (data: 7FB2h)
Minimum step value: +0.1 dB (data: 40BEh)

G. Internal data memory for TGEN1 fade-out step value control (TGEN1_FADE_OUT_ST)
Initial value: 390Ah (–1.0 dB)
When changing the step amount X, compute it using the following equation:
Equation: 10^ (X/20)*16384
Example: Making the step value –3 dB:
10^ (–3/20)*16384 = 11599d = 2D4Fh
Maximum step value: –6.0 dB (data: 2013h)
Minimum step value: –0.1 dB (data: 3F44h)

H. Internal data memory for TGEN1 fade-out time control (TGEN1_FADE_OUT_TIM)
Initial value: 002Bh (43Sync)
When changing the fade-out time, compute it using the following equation:
Equation: 43 dB/"fade-out step value"dB
Example: When the step value is 2 dB:
43/2 = 22d =16h
Upper limit : 430 Sync (data: 01AEh)
Lower limit : 8 Sync (data: 0008h)

Notes:
Setting 0000h is prohibited.
Be sure to observe the following:
Fade-out time < TIM_M0, TIM_M1

(Remarks) The step values can be set individually, but parameters set will become common to TONE_C and TONE_D. Also, the operation control and stop time parameters will become common to TONE_C and TONE_D.

I. Internal data memory for TGEN1 total gain fade control (TGEN1_GAIN_TOTAL_FADE_CONT)
Initial value: 0000h (stop)
Setting "0001h" in this data memory operates the fade-in/fade-out function of RX side/TX side total gain control.

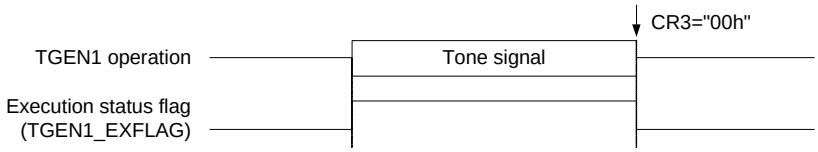
0000h: Stops fade-in/fade-out
0001h: Operates fade-in/fade-out

J. Internal data memory for TGEN1 total gain fade-in step value control (TGEN1_GAIN_TOTAL_FADE_IN_ST)
Initial value: 4C10h (+1.5 dB)
When changing the step amount X, compute it using the following equation:
Equation: 10^ (X/20)*16384
Example: Making the step value +3 dB:
10^ (3/20)*16384 = 23143d = 5A67h
Maximum step value: +6.0 dB (data: 7FB2h)
Minimum step value: +0.1 dB (data: 40BEh)

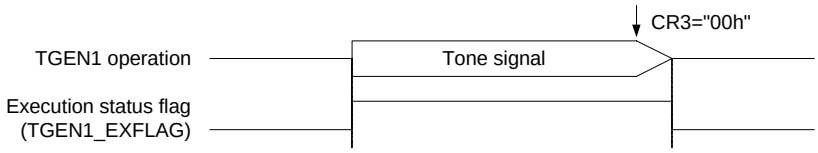
K. Internal data memory for TGEN1 total gain fade-out step value control
(TGEN1_GAIN_TOTAL_FADE_OUT_ST)
Initial value: 35D9h (–1.5 dB)
When changing the step amount X, compute it using the following equation:
Equation: 10^ (X/20)*16384
Example: Making the step value –3 dB:
10^ (–3/20)*16384 = 11599d = 2D4Fh
Maximum step value: –6.0 dB (data: 2013h)
Minimum step value: –0.1 dB (data: 3F44h)

(Remarks) The step values can be set individually, but parameters set will become common to TGEN1_RXGAIN_TOTAL and TGEN1_TXGAIN_TOTAL. Also, the operation control parameters will become common to TGEN1_RXGAIN_TOTAL and TGEN1_TXGAIN_TOTAL.

L. TGEN1 execution status flag indication register (TGEN1_EXFLAG)
TGEN1_EXFLAG is set to “1” while the tone generator 1 is operating. (Initial value = “0”: Generator stopped)



When TGEN1_FADE_CONT is OFF



When TGEN1_FADE_CONT is ON

FSK Generator 0 (FSKGEN0)

The FSK generator 0 (FSKGEN0) can generate the FSK signal on the receive side of CH0.
This generator modulates the data set in a control register with frequency modulation and outputs it to VFRO0. Table 12 shows the specifications of the FSK generator 0, and Figure 37 shows its block diagram.
The FSK generator 0 consists of an FSK signal generation section that can buffer up to 3 words, a data setting register and a gain adjustment section. The FSK generator 0 will start operating when FGEN0_EN is set to "1", and continuously output a mark bit ("1"). To start transmitting data, set the first transmit data in FGEN0_D[7:0], and set FGEN0_FLAG to "1". When FGEN0_FLGA is set to "1", the transmit data in FGEN0_D[7:0] is transferred to the internal buffer if it has a free space, and clears FGEN0_FLAG to "0". ST (Start Bit "0") and SP (Stop Bit "1") are added to the data transferred to the internal buffer, and then that data is output in the transmission order shown in Figure 38. To set the next data to be transmitted, do so when FGEN0_FLAG is "0". While there is no data waiting to be transmitted in the internal buffer of the FGEN signal generation section, a mark bit ("1") is continuously output. Note that the internal buffer of the FSK signal generation section has a 3-stage structure, and thus it can buffer up to 4 words including the FSK output data setting register FGEN0_D[7:0]. To end transmission, set FGEN0_EN to "0" while FGEN0_FLAG is "0". When the transmission of data set in FGEN0_D[7:0] is completed before FGEN0_EN is set to "0", the FSK generator 0 stops. Note that if FGEN0_EN is set to "0" while continuously transmitting a mark bit ("1") and there is no data waiting to be transmitted, the FSK generator 0 stops after outputting a mark bit ("1") for a maximum period of 1 bit. Figure 39 shows the transmission and stop timings, and Figure 40 shows a control example. Also, the output level of the FSK generator 0 can be changed with the internal data memory (FGEN0_GAIN).

Table 12 Specifications of FSK Generator

Modulation method	Frequency modulation
Synchronization method	Start-stop synchronization
Transfer speed	1200 bps
Output frequencies	1300 Hz (Data "1" Mark)
	2100 Hz (Data "0" Space)
Output data setup register	8 bits (FGEN_D[7:0])
Output level	–13.3 dBm0 (Initial value, gain adjustment possible)

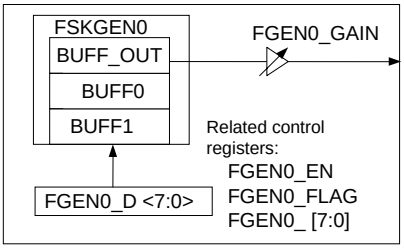


Figure 37 FSK Generation Block

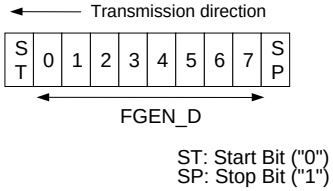


Figure 38 Data Transmission Sequence

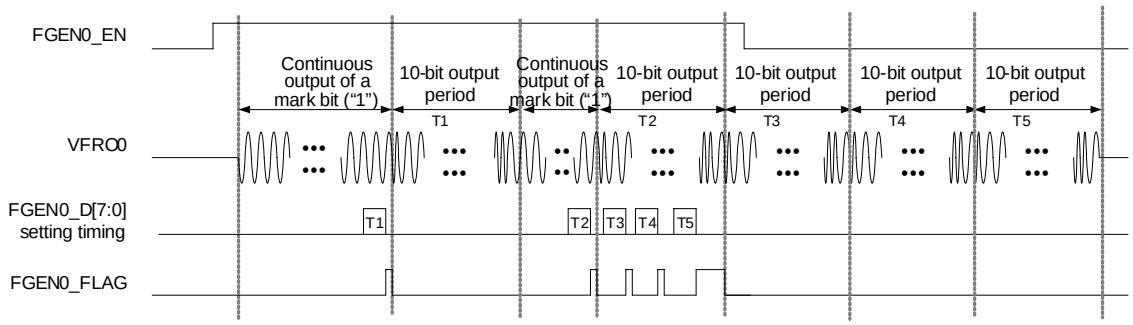


Figure 39 FSK Data Transmission and Stop Timings (When Transmitting 50 Bits)

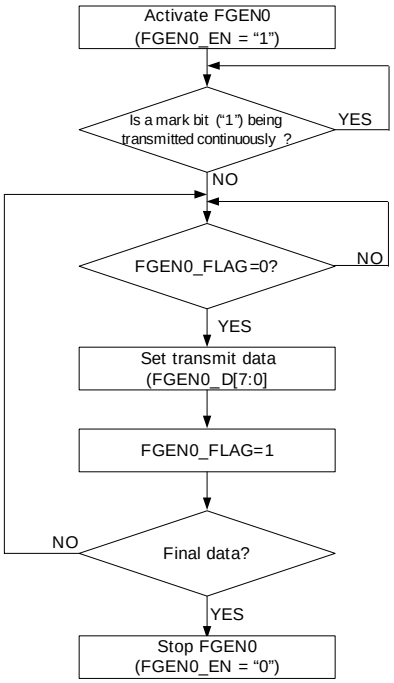


Figure 40 FSK Output Control Method

A. FGEN0 enable control register (FGEN0_EN)
0: Stops FGEN0 (initial value)
1: Operates FGEN0

B. FGEN0 output data setting completion flag (FGEN0_FLAG)
After writing data to the FGEN0 output data setting register (FGEN0_D[7:0]), set this bit to "1". Once the loading of data into the internal buffer of the FSK signal generation section is complete, this bit is automatically cleared to "0". Do not write to this register while this bit is "1", however.

C. FGEN0 output data setting register (FGEN0_D[7:0])
Initial value: 00h

D. Internal data memory for FGEN0 gain control (FGEN0_GAIN)
Initial value: 0080h
The output level as the default will be –13.3 dBm0. Use the following equation to compute the value of the setting when changing the output level.
Equation: 0080h×GAIN
Example: For reducing the output level by 6 dB:
0080h × 0.5 = 0040h
Upper limit : +40 dB (data: 3200h)
Lower limit : –40 dB (data: 0001h)

Note:
Make sure that the maximum amplitude does not exceed 3.17 dBm0.

FSK generator 1 (FSKGEN1)

The FSK generator 1 (FSKGEN1) can generate the FSK signal on the receive side of CH1.
This generator modulates the data set in a control register with frequency modulation and outputs it to VFRO1. Table 13 shows the specifications of the FSK generator 1, and Figure 41 shows its section diagram.
The FSK generator 1 consists of an FSK signal generation section that can buffer up to 3 words, a data setting register and a gain adjustment section. The FSK generator 1 will start operating when FGEN1_EN is set to "1", and continuously output a mark bit ("1"). To start transmitting data, set the first transmit data in FGEN1_D[7:0], and set FGEN1_FLAG to "1". When FGEN1_FLGA is set to "1", the transmit data in FGEN1_D[7:0] is transferred to the internal buffer if it has a free space, and clears FGEN1_FLAG to "0". ST (Start Bit "0") and SP (Stop Bit "1") are added to the data transferred to the internal buffer, and then that data is output in the transmission order shown in Figure 42. To set the next data to be transmitted, do so when FGEN1_FLAG is "0". While there is no data waiting to be transmitted in the internal buffer of the FGEN signal generation section, a mark bit ("1") is continuously output. Note that the internal buffer of the FSK signal generation section has a 3-stage structure, and thus it can buffer up to 4 words including the FSK output data setting register FGEN1_D[7:0]. To end transmission, set FGEN1_EN to "0" while FGEN1_FLAG is "0". When the transmission of data set in FGEN1_D[7:0] is completed before FGEN1_EN is set to "0", the FSK generator 1 stops. Note that if FGEN1_EN is set to "0" while continuously transmitting a mark bit ("1") and there is no data waiting to be transmitted, the FSK generator 1 stops after outputting a mark bit ("1") for a maximum period of 1 bit. Figure 43 shows the transmission and stop timings, and Figure 44 shows a control example. Also, the output level of the FSK generator 1 can be changed with the internal data memory (FGEN1_GAIN).

Table 13 Specifications of FSK Generator

Modulation method	Frequency modulation
Synchronization method	Start-stop synchronization
Transfer speed	1200 bps
Output frequencies	1300 Hz (Data "1" Mark)
	2100 Hz (Data "0" Space)
Output data setup register	8 bits (FGEN_D[7:0])
Output level	–13.3 dBm0 (Initial value, gain adjustment possible)

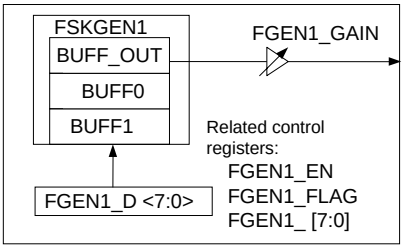


Figure 41 FSK Generation Block

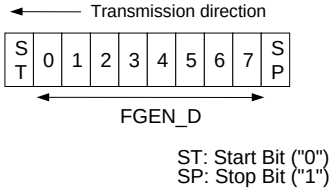


Figure 42 Data Transmission Sequence

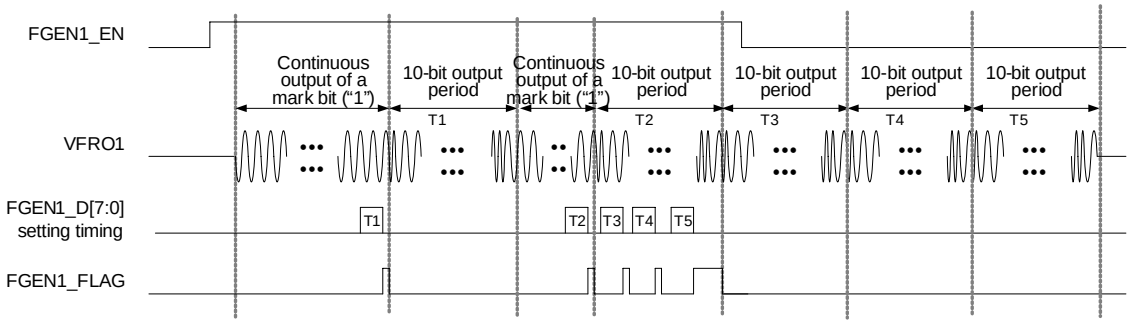


Figure 43 FSK Data Transmission and Stop Timings (When Transmitting 50 Bits)

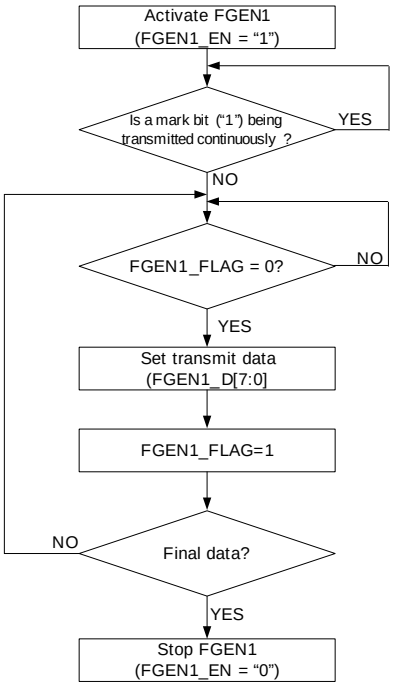


Figure 44 FSK Output Control Method

A. FGEN1 enable control register (FGEN1_EN)
0: Stops FGEN1 (initial value)
1: Operates FGEN1

B. FGEN1 output data setting completion flag (FGEN1_FLAG)
After writing data to the FGEN1 output data setting register (FGEN1_D[7:0]), set this bit to "1". Once the loading of data into the internal buffer of the FSK signal generation block is complete, this bit is automatically cleared to "0". Do not write to this register while this bit is "1", however.

C. FGEN1 output data setting register (FGEN1_D[7:0])
Initial value: 00h

D. Internal data memory for FGEN1 gain control (FGEN1_GAIN)
Initial value: 0080h
The output level as the default will be –13.3 dBm0. Use the following equation to compute the value of the setting when changing the output level.
Equation: 0080h×GAIN
Example: For reducing the output level by 6 dB:
0080h × 0.5 = 0040h
Upper limit : +40 dB (data: 3200h)
Lower limit : –40 dB (data: 0001h)

Note:
Make sure that the maximum amplitude does not exceed 3.17 dBm0.

TONE Detector RX0 (TONE_RXDET0)

The tone detector RX0 is a 400 Hz tone detector mounted on the receive side of CH0.
TONE_RXDET0 consists of a main signal detection section that detects signals having the applicable frequency, a noise detection section that detects signals having other than the applicable frequency, a ON guard timer and a OFF guard timer, and detects input 400 Hz single tone signals.
TONE_RXDET0 is enabled when the control register TONE_RXDET0EN is "1". When a tone is detected (a main signal is detected and in a state where no noise detected), the control register TONE_RXDET0 is set to "1". When no tone is detected or TONE_RXDET0EN is "0", TONE_RXDET0 is set to "0".
Also, it can adjust the detection time with the ON and OFF guard timers, as well as the noise detection level for main signal detection and noise detection. The initial values of both guard timers are 5 ms. The initial value of the detection level is –5.3 dBm0 for both main signal detection level and noise detection level. Figure 45 shows the tone detection timing.

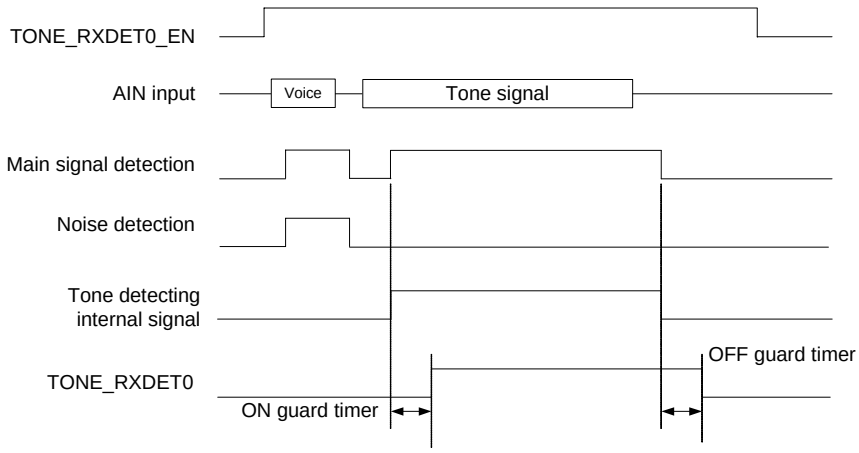


Figure 45 Tone Detection Timing

A. TONE_RXDET0 enable control register (TONE_RXDET0EN)
0 : Stop (Initial value)
1 : Operate

B. TONE_RXDET0 detection status register (TONE_RXDET0)
0 : No tone detected (Initial value)
1 : Tone detected

C. Internal data memory for TONE_RXDET0 main signal detection level control (TONE_RXDET0_S_TH)
Initial value : 1EBBh (–5.3 dBm0)
Compute the setting value using the following equation when changing the detection level X.
Equation: 10^((X–3.17)/20)*2/PI*32768
Example: Detect level of –5.3 dBm0
10^((–5.3 – 3.17)/20)*2/PI*32768 = 7867d = 1EBBh
Upper limit: 3.17 dBm0 (data: 517Dh)
: –5.3 dBm0 (data: 1EBBh)
Lower limit: –35 dBm0 (data: 0102h)

D. Internal data memory for TONE_RXDET0 noise detection level control (TONE_RXDET0_N_TH)
Initial value: 1EBBh (–5.3 dBm0)
Compute the setting value using the following equation when changing the detection level X.
Equation: 10^((X – 3.17)/20)*2/PI*32768
Example: Detect level of –5.3 dBm0
10^((–5.3 – 3.17)/20)*2/PI*32768 = 7867d = 1EBBh
Upper limit: 3.17 dBm0 (data: 517Dh)
: –5.3 dBm0 (data: 1EBBh)
Lower limit: –30 dBm0 (data: 01CAh)

To stop the noise detection function, write 7FFFh to the above described internal data memory (TONE_RXDET0_N_TH).

E. Internal data memory for TONE_RXDET0 detection ON guard timer (TONE_RXDET0_ON_TM)
Initial value: 0028h (5 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 5 ms
5/0.125 = 40d = 0028h
Upper limit : 4095.875 ms (data: 7FFFh)
: 5 ms (data: 0028h)
Lower limit : 0.125 ms (data: 0001h)

F. Internal data memory for TONE_RXDET0 detection OFF guard timer (TONE_RXDET0_OFF_TM)
Initial value: 0028h (5 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 5 ms
5/0.125 = 40d = 0028h
Upper limit : 4095.875 ms (data: 7FFFh)
: 5 ms (data: 0028h)
Lower limit : 0.125 ms (data: 0001h)

G. Internal data memory for TONE_RXDET0 detection frequency control (TONE_RXDET0_FREQ)
Initial value : -
The detection frequency can be changed. Contact our sales personnel if it is desired to change the detection frequency.

TONE Detector TX0 (TONE_TXDET0)

The tone detector TX0 is a 400 Hz tone detector mounted on the transmit side of CH0.
TONE_TXDET0 consists of a main signal detection section that detects signals having the applicable frequency, a noise detection section that detects signals having other than the applicable frequency, a ON guard timer and a OFF guard timer, and detects input 400 Hz single tone signals.
TONE_TXDET0 is enabled when the control register TONE_TXDET0EN is "1". When a tone is detected (a main signal is detected and in a state where no noise detected), the control register TONE_TXDET0 is set to "1". When no tone is detected or TONE_TXDET0EN is "0", TONE_TXDET0 is set to "0".
Also, it can adjust the detection time with the ON and OFF guard timers, as well as the noise detection level for main signal detection and noise detection. The initial values of both guard timers are 5 ms. The initial value of the detection level is –5.3 dBm0 for both main signal detection level and noise detection level. Figure 46 shows the tone detection timing.

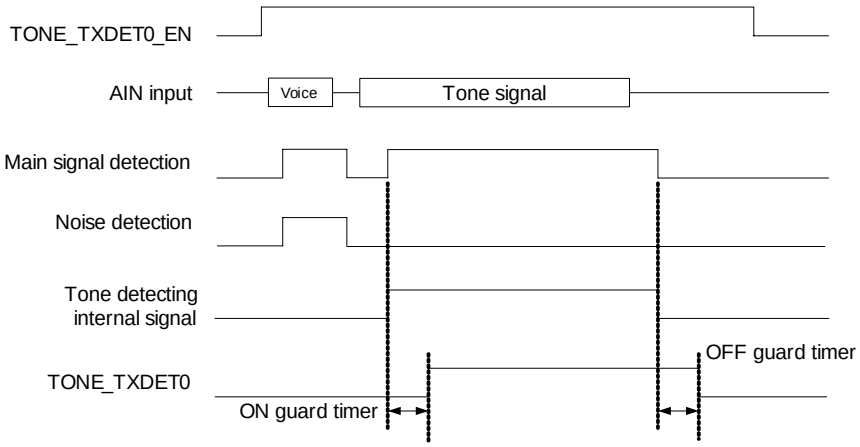


Figure 46 Tone Detection Timing

A. TONE_TXDET0 enable control register (TONE_TXDET0EN)
0 : Stop (Initial value)
1 : Operate

B. TONE_TXDET0 detection status register (TONE_TXDET0)
0 : No tone detected (Initial value)
1 : Tone detected

C. Internal data memory for TONE_TXDET0 main signal detection level control (TONE_TXDET0_S_TH)
Initial value : 1EBBh (–5.3 dBm0)
Compute the setting value using the following equation when changing the detection level X.
Equation: 10^((X–3.17)/20)*2/PI*32768
Example: Detect level of –5.3 dBm0
10^((–5.3 – 3.17)/20)*2/PI*32768 = 7867d = 1EBBh
Upper limit: 3.17 dBm0 (data: 517Dh)
: –5.3 dBm0 (data: 1EBBh)
Lower limit: –35 dBm0 (data: 0102h)

D. Internal data memory for TONE_TXDET0 noise detection level control (TONE_TXDET0_N_TH)
Initial value: 1EBBh (–5.3 dBm0)
Compute the setting value using the following equation when changing the detection level X.
Equation: 10^((X – 3.17)/20)*2/PI*32768
Example: Detect level of –5.3 dBm0
10^((–5.3 – 3.17)/20)*2/PI*32768 = 7867d = 1EBBh
Upper limit: 3.17 dBm0 (data: 517Dh)
: –5.3 dBm0 (data: 1EBBh)
Lower limit: –30 dBm0 (data: 01CAh)

To stop the noise detection function, write 7FFFh to the above described internal data memory (TONE_TXDET0_N_TH).

E. Internal data memory for TONE_TXDET0 detection ON guard timer (TONE_TXDET0_ON_TM)
Initial value: 0028h (5 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 5 ms
5/0.125 = 40d = 0028h
Upper limit : 4095.875 ms (data: 7FFFh)
: 5 ms (data: 0028h)
Lower limit : 0.125 ms (data: 0001h)

F. Internal data memory for TONE_TXDET0 detection OFF guard timer (TONE_TXDET0_OFF_TM)
Initial value: 0028h (5 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 5 ms
5/0.125 = 40d = 0028h
Upper limit : 4095.875 ms (data: 7FFFh)
: 5 ms (data: 0028h)
Lower limit : 0.125 ms (data: 0001h)

G. Internal data memory for TONE_TXDET0 detection frequency control (TONE_TXDET0_FREQ)
Initial value : -
The detection frequency can be changed. Contact our sales personnel if it is desired to change the detection frequency.

TONE Detector RX1 (TONE_RXDET1)

The tone detector RX1 is a 400 Hz tone detector mounted on the receive side of CH0.
TONE_RXDET1 consists of a main signal detection section that detects signals having the applicable frequency, a noise detection section that detects signals having other than the applicable frequency, a ON guard timer and a OFF guard timer, and detects input 400 Hz single tone signals.
TONE_RXDET1 is enabled when the control register TONE_RXDET1EN is "1". When a tone is detected (a main signal is detected and in a state where no noise detected), the control register TONE_RXDET1 is set to "1". When no tone is detected or TONE_RXDET1EN is "0", TONE_RXDET1 is set to "0".
Also, it can adjust the detection time with the ON and OFF guard timers, as well as the noise detection level for main signal detection and noise detection. The initial values of both guard timers are 5 ms. The initial value of the detection level is –5.3 dBm0 for both main signal detection level and noise detection level. Figure 47 shows the tone detection timing.

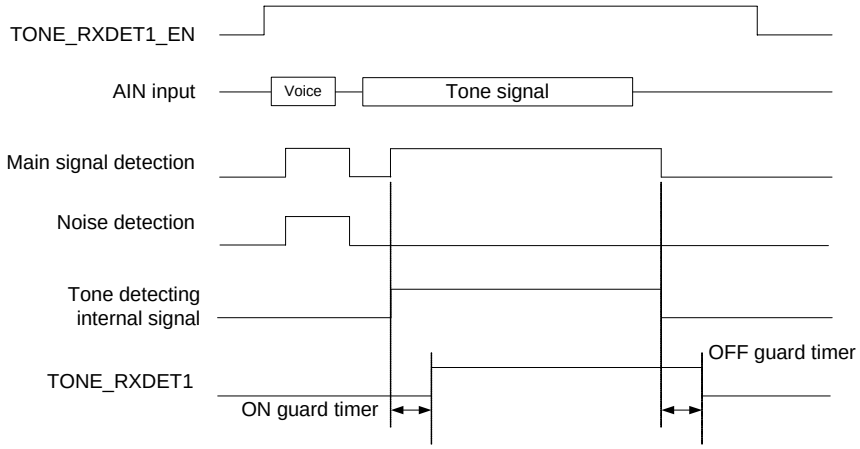


Figure 47 Tone Detection Timing

A. TONE_RXDET1 enable control register (TONE_RXDET1EN)
0 : Stop (Initial value)
1 : Operate

B. TONE_RXDET1 detection status register (TONE_RXDET1)
0 : No tone detected (Initial value)
1 : Tone detected

C. Internal data memory for TONE_RXDET1 main signal detection level control (TONE_RXDET1_S_TH)
Initial value : 1EBBh (–5.3 dBm0)
Compute the setting value using the following equation when changing the detection level X.
Equation: 10^((X–3.17)/20)*2/PI*32768
Example: Detect level of –5.3 dBm0
10^((–5.3 – 3.17)/20)*2/PI*32768 = 7867d = 1EBBh
Upper limit: 3.17 dBm0 (data: 517Dh)
: –5.3 dBm0 (data: 1EBBh)
Lower limit: –35 dBm0 (data: 0102h)

D. Internal data memory for TONE_RXDET1 noise detection level control (TONE_RXDET1_N_TH)
Initial value: 1EBBh (–5.3 dBm0)
Compute the setting value using the following equation when changing the detection level X.
Equation: 10^((X – 3.17)/20)*2/PI*32768
Example: Detect level of –5.3 dBm0
10^((–5.3 – 3.17)/20)*2/PI*32768 = 7867d = 1EBBh
Upper limit: 3.17 dBm0 (data: 517Dh)
: –5.3 dBm0 (data: 1EBBh)
Lower limit: –30 dBm0 (data: 01CAh)

To stop the noise detection function, write 7FFFh to the above described internal data memory (TONE_RXDET1_N_TH).

E. Internal data memory for TONE_RXDET1 detection ON guard timer (TONE_RXDET1_ON_TM)
Initial value: 0028h (5 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 5 ms
5/0.125 = 40d = 0028h
Upper limit : 4095.875 ms (data: 7FFFh)
: 5 ms (data: 0028h)
Lower limit : 0.125 ms (data: 0001h)

F. Internal data memory for TONE_RXDET1 detection OFF guard timer (TONE_RXDET1_OFF_TM)
Initial value: 0028h (5 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 5 ms
5/0.125 = 40d = 0028h
Upper limit : 4095.875 ms (data: 7FFFh)
: 5 ms (data: 0028h)
Lower limit : 0.125 ms (data: 0001h)

G. Internal data memory for TONE_RXDET1 detection frequency control (TONE_RXDET1_FREQ)
Initial value : -
The detection frequency can be changed. Contact our sales personnel if it is desired to change the detection frequency.

TONE Detector TX1 (TONE_TXDET1)

The tone detector TX1 is a 400 Hz tone detector mounted on the transmit side of CH0.

TONE_TXDET1 consists of a main signal detection section that detects signals having the applicable frequency, a noise detection section that detects signals having other than the applicable frequency, a ON guard timer and a OFF guard timer, and detects input 400 Hz single tone signals.

TONE_TXDET1 is enabled when the control register TONE_TXDET1EN is "1". When a tone is detected (a main signal is detected and in a state where no noise detected), the control register TONE_TXDET1 is set to "1". When no tone is detected or TONE_TXDET1EN is "0", TONE_TXDET1 is set to "0".

Also, it can adjust the detection time with the ON and OFF guard timers, as well as the noise detection level for main signal detection and noise detection. The initial values of both guard timers are 5 ms. The initial value of the detection level is –5.3 dBm0 for both main signal detection level and noise detection level. Figure 48 shows the tone detection timing.

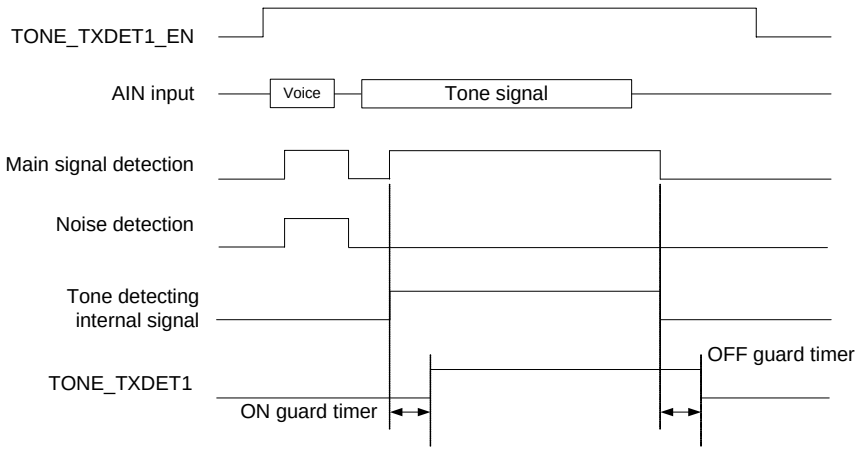


Figure 48 Tone Detection Timing

A. TONE_TXDET1 enable control register (TONE_TXDET1EN)
- 0 : Stop (Initial value)
- 1 : Operate

B. TONE_TXDET1 detection status register (TONE_TXDET1)
- 0 : No tone detected (Initial value)
- 1 : Tone detected

C. Internal data memory for TONE_TXDET1 main signal detection level control (TONE_TXDET1_S_TH)

Initial value : 1EBBh (–5.3 dBm0)

Compute the setting value using the following equation when changing the detection level X.

Equation: 10^((X–3.17)/20)*2/PI*32768

Example: Detect level of –5.3 dBm0

10^((–5.3 – 3.17)/20)*2/PI*32768 = 7867d = 1EBBh

Upper limit: 3.17 dBm0 (data: 517Dh)

: –5.3 dBm0 (data: 1EBBh)

Lower limit: –35 dBm0 (data: 0102h)

D. Internal data memory for TONE_TXDET1 noise detection level control (TONE_TXDET1_N_TH)
Initial value: 1EBBh (–5.3 dBm0)
Compute the setting value using the following equation when changing the detection level X.
Equation: 10^((X – 3.17)/20)*2/PI*32768
Example: Detect level of –5.3 dBm0
10^((–5.3 – 3.17)/20)*2/PI*32768 = 7867d = 1EBBh
Upper limit: 3.17 dBm0 (data: 517Dh)
: –5.3 dBm0 (data: 1EBBh)
Lower limit: –30 dBm0 (data: 01CAh)

To stop the noise detection function, write 7FFFh to the above described internal data memory (TONE_TXDET1_N_TH).

E. Internal data memory for TONE_TXDET1 detection ON guard timer (TONE_TXDET1_ON_TM)
Initial value: 0028h (5 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 5 ms
5/0.125 = 40d = 0028h
Upper limit : 4095.875 ms (data: 7FFFh)
: 5 ms (data: 0028h)
Lower limit : 0.125 ms (data: 0001h)

F. Internal data memory for TONE_TXDET1 detection OFF guard timer (TONE_TXDET1_OFF_TM)
Initial value: 0028h (5 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 5 ms
5/0.125 = 40d = 0028h
Upper limit : 4095.875 ms (data: 7FFFh)
: 5 ms (data: 0028h)
Lower limit : 0.125 ms (data: 0001h)

G. Internal data memory for TONE_TXDET1 detection frequency control (TONE_TXDET1_FREQ)
Initial value : -
The detection frequency can be changed. Contact our sales personnel if it is desired to change the detection frequency.

Tone Disabler 0 (TD_RXDET0/TD_TXDET0)

The tone disabler 0 detects the phase inverted signal (ANSPM) of a 2100 Hz single tone signal input to the receive and transmit sides of CH0, and also detectes the single tone signal (ANS). The tone disabler 0 can be activated individually for reception and transmission using the control registers TD_RXDET0_EN and TD_TXDET0_EN. When the phase inversion of an input signal is detected, "1" is set in the applicable control register at the time of tone detection.

Also, if a silent state continues after detection, the tone disabler releases the signal (clears the applicable control register to "0"). Figure 49 shows the detection timing of the tone disabler, using the transmit side as an example. The following shows the various detection characteristics of this detector:

(Tone detection characteristics)

- Detection frequency : 2100 Hz
- Detection level : –34 dBm0 or more

(Phase inversion detection characteristics)

- Detecting conditions : Detects phase inversion once for each timing before and after a tone of 2100 Hz , for approx. 450±25 ms.
- Phase inversion characteristics:180 degrees

(Release characteristics)

- Detection level –33.5 dBm0 or less
- Release time 100 ms

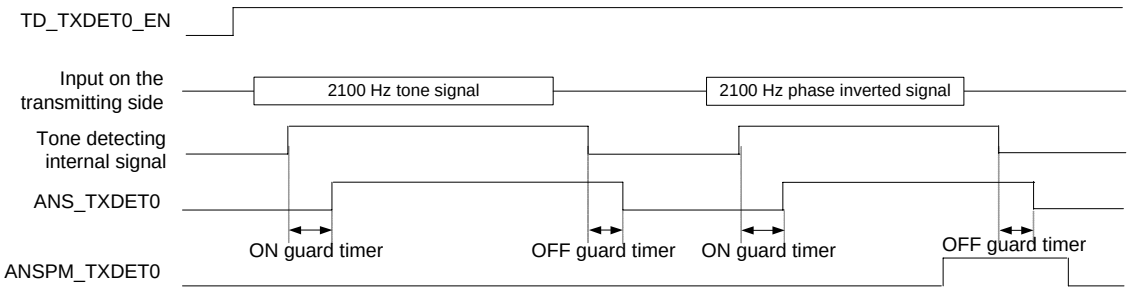


Figure 49 Tone Disabler 0 Transmit Side Detection Timing

A. : TD_RXDET0 related

A-1. : TD_RXDET0 enable control register (TD_RXDET0_EN)
0 : Stop (Initial value)
1 : Operate

A-2. : TD_RXDET0 2100 Hz single tone detection status register (ANS_RXDET0)
0 : Not detected (Initial value)
1 : Detected

A-3. : TD_RXDET0 2100 Hz phase inversion detection status register (ANSPM_RXDET0)
0 : Not detected (Initial value)
1 : Detected

A-4. : Internal data memory for TD_RXDET0 detection level control (TD_RXDET0_TH)
Initial value : 241Fh (–34 dBm0)
Compute the setting value using the following equation when changing the detection level X.
Equation: 10^((X–3.17)/20)*(2^21)/PI
Example: Detection level of –34 dBm0
10^((–34–3.17)/20)*(2^21)/PI = 9247d = 241Fh
Upper limit: –28 dBm0 (data: 4811h)
Lower limit: –34 dBm0 (data: 241Fh)

A-5. : Internal data memory for TD_RXDET0 ON guard timer (TD_RXDET0_ON_TM)
Initial value : 0028h (5 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 5 ms
5/0.125 = 40d = 0028h
Upper limit : 4095.875 ms (data: 7FFFh)
: 5 ms (data: 0028h)
Lower limit : 0.125 ms (data: 0001h)

A-6. : Internal data memory for TD_RXDET0 OFF guard timer (TD_RXDET0_OFF_TM)
Initial value : 0028h (5 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 5 ms
5/0.125 = 40d = 0028h
Upper limit : 4095.875 ms (data: 7FFFh)
: 5 ms (data: 0028h)
Lower limit : 0.125 ms (data: 0001h)

A-7. : Internal data memory for TD_RXDET0 noise detection function control (TD_RXDET0_NDET_CONT)
Initial value : 313Fh (Noise detection function enabled)
By writing 0000h to this internal data memory, the noise detection function of TD_RXDET0 will be disabled.
In the initial state, the noise detection function is enabled, and if a signal other than 2100 Hz is detected, ANS_RXDET0 will be set to “0” (Not detected) even when a 2100 Hz signal is detected.

B. : TD_TXDET0 related

B-1. : TD_TXDET0 enable control register (TD_TXDET0_EN)
0 : Stop (Initial value)
1 : Operate

B-2. : TD_TXDET0 2100 Hz single tone detection status register (ANS_TXDET0)
0 : Not detected (Initial value)
1 : Detected

B-3. : TD_TXDET0 2100 Hz phase inversion detection status register (ANSPM_TXDET0)
0 : Not detected (Initial value)
1 : Detected

B-4. : Internal data memory for TD_TXDET0 detection level control (TD_TXDET0_TH)
Initial value : 241Fh (–34 dBm0)
Compute the setting value using the following equation when changing the detection level X.
Equation: 10^((X–3.17)/20)*(2^21)/PI
Example: Detection level of –34 dBm0
10^((–34–3.17)/20)*(2^21)/PI = 9247d = 241Fh
Upper limit: –28 dBm0 (data: 4811h)
Lower limit: –34 dBm0 (data: 241Fh)

B-5. : Internal data memory for TD_TXDET0 ON guard timer (TD_TXDET0_ON_TM)
Initial value : 0028h (5 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 5 ms
5/0.125 = 40d = 0028h
Upper limit : 4095.875 ms (data: 7FFFh)
: 5 ms (data: 0028h)
Lower limit : 0.125 ms (data: 0001h)

B-6. : Internal data memory for TD_TXDET0 OFF guard timer (TD_TXDET0_OFF_TM)
Initial value : 0028h (5 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 5 ms
5/0.125 = 40d = 0028h
Upper limit : 4095.875 ms (data: 7FFFh)
: 5 ms (data: 0028h)
Lower limit : 0.125 ms (data: 0001h)

B-7. : Internal data memory for TD_TXDET0 noise detection function control (TD_TXDET0_NDET_CONT)
Initial value : 313Fh (Noise detection function enabled)
By writing 0000h to this internal data memory, the noise detection function of TD_TXDET0 will be disabled.
In the initial state, the noise detection function is enabled, and if a signal other than 2100 Hz is detected, ANS_TXDET0 will be set to “0” (Not detected) even when a 2100 Hz signal is detected.

Tone Disabler 1 (TD_RXDET1/TD_TXDET1)

The tone disabler 1 detects the phase inverted signal (ANSPM) of a 2100 Hz single tone signal input to the receive and transmit sides of CH1, and also detectes the single tone signal (ANS). The tone disabler 1 can be activated individually for reception and transmission using the control registers TD_RXDET1_EN and TD_TXDET1_EN. When the phase inversion of an input signal is detected, "1" is set in the applicable control register at the time of tone detection.

Also, if a silent state continues after detection, the tone disabler releases the signal (clears the applicable control register to "0"). Figure 50 shows the detection timing of the tone disabler, using the transmit side as an example. The following shows the various detection characteristics of this detector:

(Tone detection characteristics)

- Detection frequency : 2100 Hz
- Detection level : –34 dBm0 or more

(Phase inversion detection characteristics)

- Detecting conditions : Detects phase inversion once for each timing before and after a tone of 2100 Hz , for approx. 450±25 ms.
- Phase inversion characteristics:180 degrees

(Release characteristics)

- Detection level –33.5 dBm0 or less
- Release time 100 ms

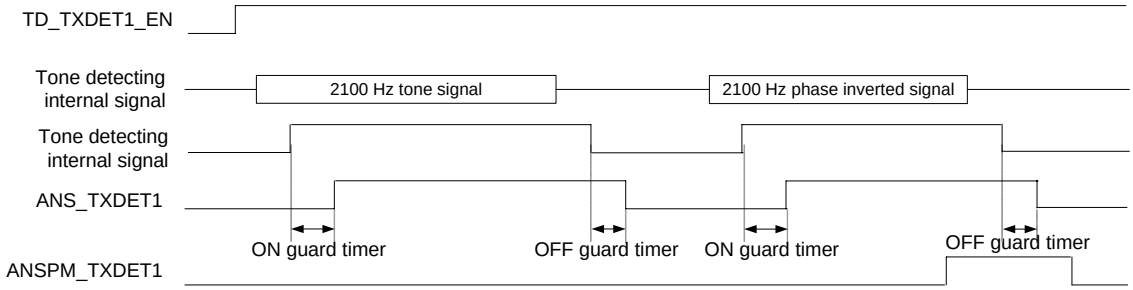


Figure 50 Tone disabler 1 Transmit Side Detection Timing

A. : TD_RXDET1 related

A-1. : TD_RXDET1 enable control register (TD_RXDET1_EN)
0 : Stop (Initial value)
1 : Operate

A-2. : TD_RXDET1 2100 Hz single tone detection status register (ANS_RXDET1)
0 : Not detected (Initial value)
1 : Detected

A-3. : TD_RXDET1 2100 Hz phase inversion detection status register (ANSPM_RXDET1)
0 : Not detected (Initial value)
1 : Detected

A-4. : Internal data memory for TD_RXDET1 detection level control (TD_RXDET1_TH)
Initial value : 241Fh (–34 dBm0)
Compute the setting value using the following equation when changing the detection level X.
Equation: 10^((X–3.17)/20)*(2^21)/PI
Example: Detection level of –34 dBm0
10^((–34–3.17)/20)*(2^21)/PI = 9247d = 241Fh
Upper limit: –28 dBm0 (data: 4811h)
Lower limit: –34 dBm0 (data: 241Fh)

A-5. : Internal data memory for TD_RXDET1 ON guard timer (TD_RXDET1_ON_TM)
Initial value : 0028h (5 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 5 ms
5/0.125 = 40d = 0028h
Upper limit : 4095.875 ms (data: 7FFFh)
: 5 ms (data: 0028h)
Lower limit : 0.125 ms (data: 0001h)

A-6. : Internal data memory for TD_RXDET1 OFF guard timer (TD_RXDET1_OFF_TM)
Initial value : 0028h (5 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 5 ms
5/0.125 = 40d = 0028h
Upper limit : 4095.875 ms (data: 7FFFh)
: 5 ms (data: 0028h)
Lower limit : 0.125 ms (data: 0001h)

A-7. : Internal data memory for TD_RXDET1 noise detection function control (TD_RXDET1_NDET_CONT)
Initial value : 313Fh (Noise detection function enabled)
By writing 0000h to this internal data memory, the noise detection function of TD_RXDET1 will be disabled.
In the initial state, the noise detection function is enabled, and if a signal other than 2100 Hz is detected, ANS_RXDET1 will be set to “0” (Not detected) even when a 2100 Hz signal is detected.

B. : TD_TXDET1 related

B-1. : TD_TXDET1 enable control register (TD_TXDET1_EN)
0 : Stop (Initial value)
1 : Operate

B-2. : TD_TXDET1 2100 Hz single tone detection status register (ANS_TXDET1)
0 : Not detected (Initial value)
1 : Detected

B-3. : TD_TXDET1 2100 Hz phase inversion detection status register (ANSPM_TXDET1)
0 : Not detected (Initial value)
1 : Detected

B-4. : Internal data memory for TD_TXDET1 detection level control (TD_TXDET1_TH)
Initial value : 241Fh (–34 dBm0)
Compute the setting value using the following equation when changing the detection level X.
Equation: 10^((X–3.17)/20)*(2^21)/PI
Example: Detection level of –34 dBm0
10^((–34–3.17)/20)*(2^21)/PI = 9247d = 241Fh
Upper limit: –28 dBm0 (data: 4811h)
Lower limit: –34 dBm0 (data: 241Fh)

B-5. : Internal data memory for TD_TXDET1 ON guard timer (TD_TXDET1_ON_TM)
Initial value : 0028h (5 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 5 ms
5/0.125 = 40d = 0028h
Upper limit : 4095.875 ms (data: 7FFFh)
: 5 ms (data: 0028h)
Lower limit : 0.125 ms (data: 0001h)

B-6. : Internal data memory for TD_TXDET1 OFF guard timer (TD_TXDET1_OFF_TM)
Initial value : 0028h (5 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 5 ms
5/0.125 = 40d = 0028h
Upper limit : 4095.875 ms (data: 7FFFh)
: 5 ms (data: 0028h)
Lower limit : 0.125 ms (data: 0001h)

B-7. : Internal data memory for TD_TXDET1 noise detection function control (TD_TXDET1_NDET_CONT)
Initial value : 313Fh (Noise detection function enabled)
By writing 0000h to this internal data memory, the noise detection function of TD_TXDET1 will be disabled.
In the initial state, the noise detection function is enabled, and if a signal other than 2100 Hz is detected, ANS_TXDET1 will be set to “0” (Not detected) even when a 2100 Hz signal is detected.

DTMF Detector 0 (DTMFDET0)

This detector can detect the DTMF signal on the transmit side of CH0.

The DTMF detector 0 consists of a DTMF detection section that detects the DTMF signal, a noise detection section that detects signals other than the DTMF signal, a ON guard timer and a OFF guard timer.

The DTMF detector 0 is enabled when the control register DTMF0_EN is "1". If it detects a valid DTMF signal (a DTMF signal is detected and in a state where no noise detected), DTMF0_DET is set to "1", and the receive code is stored in DTMF0_C[3:0]. If a DTMF signal is not detected, or DTMF0_EN is "0", DTMF0_DET will be "0" and DTMF0_C[3:0] will be "0000." Figure 51 shows the DTMF detection timing. This detector can adjust the detection time with the ON and OFF guard timers, and also can adjust the detection level. The initial values of both guard timers are 20 ms. And the initial value of the detection level is –37.0 dBm0.

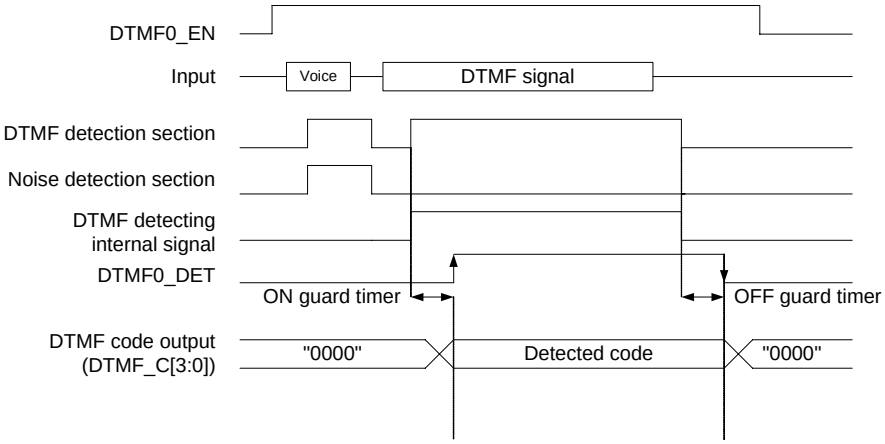


Figure 51 DTMF Detection Timing

A. : DTMF0 enable control register (DTMF0_EN)
0 : Stop (Initial value)
1 : Operate

B. : DTMF0 detection code indication register (DTMF0_C[3:0])
While the DTMF0 enable control register (DTMF0_EN) is set to "1", a detected code is stored during the period where the DTMF is being detected (DTMF0 detection status register DTMF0_DET = "1").
If the DTMF signal is not detected (DTMF0_DET = "0"), "0000" will be output. (Initial value :0000b)

C. : DTMF0 detection status register (DTMF0_DET)
0 : No DTMF signal detected (Initial value)
1 : DTMF signal detected

D. Internal data memory for DTMF0 detection level control (DTMF0_TH)
Initial value : 1000h (–37.0 dBm0)
Compute the setting value using the following equation when changing the detect level.
Equation: 1000h×1/GAIN
Example: Increasing the detect level by 6 dB.
1000h × 0.5 = 0800h
Upper limit: +12 dB (data: 0405h)
Lower limit: –12 dB (data: 3FB2h)

(Note)
The level set in the data memory (DTMF0_TH) described above is used as the common detection level in the DTMF detection block and the noise detection block.

E. Internal data memory for DTMF0 detection ON guard timer (DTMF0_ON_TM)
Initial value : 00A0h (20 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 5 ms
5/0.125 = 40d = 0028h

Upper limit	: 4095.875 ms	(data: 7FFFh)
	: 5 ms	(data: 0028h)
Lower limit	: 0.125 ms	(data: 0001h)

F. Internal data memory for DTMF0 detection OFF guard timer (DTMF0_OFF_TM)
Initial value : 00A0h (20 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 5 ms
5/0.125 = 40d = 0028h

Upper limit	: 4095.875 ms	(data: 7FFFh)
	: 5 ms	(data: 0028h)
Lower limit	: 0.125 ms	(data: 0001h)

G. Internal data memory for DTMF0 noise detection funciton control (DTMF0_NDET_CONT)
Initial value : 0002h (Noise detection funciton enabled)
By writing 0000h to this internal data memory, the noise detection function of the DTMF detector 1 will be disabled.

DTMF Detector 1 (DTMFDET1)

This detector can detect the DTMF signal on the transmit side of CH1.

The DTMF detector 1 consists of a DTMF detection section that detects the DTMF signal, a noise detection section that detects signals other than the DTMF signal, a ON guard timer and a OFF guard timer.

The DTMF detector 1 is enabled when the control register DTMF1_EN is "1". If it detects a valid DTMF signal (a DTMF signal is detected and in a state where no noise detected), DTMF1_DET is set to "1", and the receive code is stored in DTMF1_C[3:0]. If a DTMF signal is not detected, or DTMF1_EN is "0", DTMF1_DET will be "0" and DTMF1_C[3:0] will be "0000." Figure 52 shows the DTMF detection timing. This detector can adjust the detection time with the ON and OFF guard timers, and also can adjust the detection level. The initial values of both guard timers are 20 ms. And the initial value of the detection level is –37.0 dBm0.

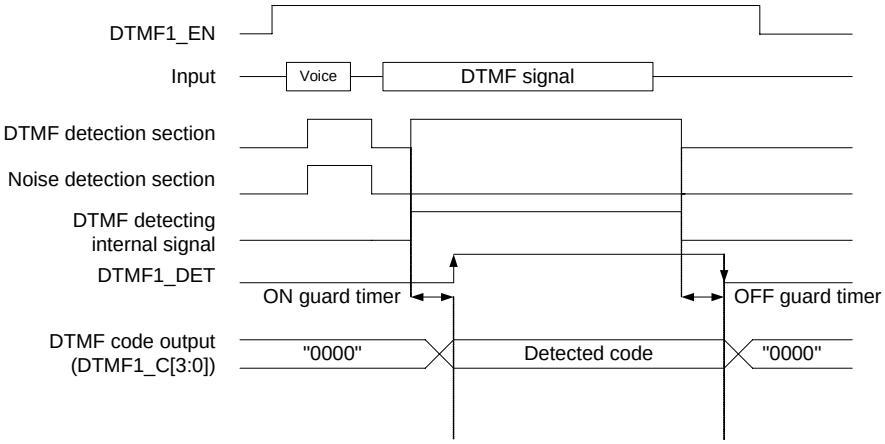


Figure 52 DTMF Detection Timing

A. : DTMF1 enable control register (DTMF1_EN)
0 : Stop (Initial value)
1 : Operate

B. : DTMF1 detection code indication register (DTMF1_C[3:0])
While the DTMF1 enable control register (DTMF1_EN) is set to "1", a detected code is stored during the period where the DTMF is being detected (DTMF1 detection status register DTMF1_DET = "1").
If the DTMF signal is not detected (DTMF1_DET = "0"), "0000" will be output. (Initial value :0000b)

C. : DTMF1 detection status register (DTMF1_DET)
0 : No DTMF signal detected (Initial value)
1 : DTMF signal detected

D. Internal data memory for DTMF1 detection level control (DTMF1_TH)
Initial value : 1000h (–37.0 dBm0)
Compute the setting value using the following equation when changing the detect level.
Equation: 1000h×1/GAIN
Example: Increasing the detect level by 6 dB.
1000h × 0.5 = 0800h
Upper limit: +12 dB (data: 0405h)
Lower limit: –12 dB (data: 3FB2h)

(Note)
The level set in the data memory (DTMF1_TH) described above is used as the common detection level in the DTMF detection block and the noise detection block.

E. Internal data memory for DTMF1 detection ON guard timer (DTMF1_ON_TM)
Initial value : 00A0h (20 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 5 ms
5/0.125 = 40d = 0028h

Upper limit	: 4095.875 ms	(data: 7FFFh)
	: 5 ms	(data: 0028h)
Lower limit	: 0.125 ms	(data: 0001h)

F. Internal data memory for DTMF1 detection OFF guard timer (DTMF1_OFF_TM)
Initial value : 00A0h (20 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 5 ms
5/0.125 = 40d = 0028h

Upper limit	: 4095.875 ms	(data: 7FFFh)
	: 5 ms	(data: 0028h)
Lower limit	: 0.125 ms	(data: 0001h)

G. Internal data memory for DTMF1 noise detection funciton control (DTMF1_NDET_CONT)
Initial value : 0002h (Noise detection funciton enabled)
By writing 0000h to this internal data memory, the noise detection function of the DTMF detector 1 will be disabled.

Echo Canceller 0

Echo canceller 0 is an echo canceller for CH0. The block diagram of echo canceller 0 is shown in Figure 53.

The echo canceller 0 has a delay time of 32 ms and is activated by setting the echo canceller 0 control register (EC0_EN) to "1". The operation setting of the echo canceller 0 is done mainly using internal data memories EC0_CR and EC0_GLPAD_CR.

The echo canceller 0 is also equipped with the Comfort Noise generation function that adds generated noise to Sout, according to the background noise amount of a signal input from Sin.

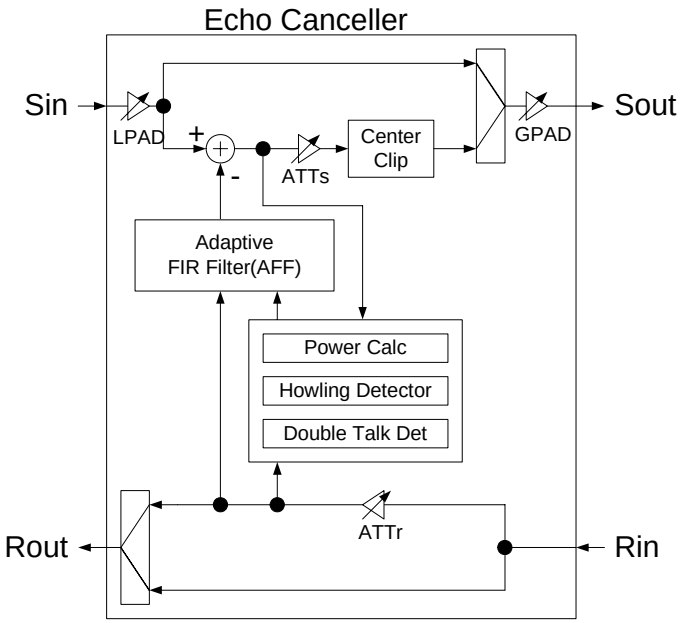


Figure 53 Block Diagram of Echo Canceller

A. EC0 control register (EC0_EN)

0 : Stops. The echo canceller is bypassed. (Initial value)

1 : Operates.

B. Internal data memory for EC0 control (EC0_CR)

Initial value : 0012h

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	THR	—	HLD	H DB	CLP	—	ATTB	—
Initial value	0	0	0	1	0	0	1	0

B15–B8 : Reserved bits. Do not change the initial values.

B7: Through mode control
1: Through mode
0: Normal mode (echo cancelling operation)
The data of Rin and Sin is output directly to Rout and Sout while retaining their respective echo coefficients. Further, during the through mode, the HLD, HDB, CLP, and ATTB functions are disabled.

B6: Reserved bit. Do not change the initial value.

B5: Coefficient update control
1: Coefficient is fixed
0: Coefficient is updated
This bit specifies whether the adaptive FIR filter (AFF) coefficient of the echo canceller will be updated or not. This function is enabled when THR is in the normal mode.

B4: Howling detector control
1: OFF
0: ON
This bit controls the function of detecting and removing howling which is generated in a hands-free acoustic system, etc. This function is enabled when THR is in the normal mode.

B3: Center clip control
1: ON
0: OFF
This bit controls the center clip function in which the Sout output is forcibly fixed to the minimum positive value when the Sout output of the echo canceller is –57 dBm0 or less and in the single talk state. This function is enabled when THR is in the normal mode.

B2: Reserved bit. Do not change the initial value.

B1: Attenuator control
1: ATT OFF
0: ATT ON
This bit selects the switching ON/OFF of the ATT function which prevents howling using the attenuators ATTs and ATTr provided at the Rin input and Sout output of the echo canceller. When only the Rin input is present, the attenuator (ATTs) of Sout will be inserted. When only the Sin input is present or when both the Sin and Rin inputs are present, the attenuator (ATTr) of Rin will be inserted. The respective attenuation values are 6 dB. This function becomes valid when THR is in the normal mode.

B0: Reserved bit. Do not change the initial value.

C. Internal data memory for EC0 GLPAD control (EC0_GLPAD_CR)
Initial value: 000Fh
This data memory controls the GLPAD within the echo canceller 0.

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	—	—	—	—	GPAD2	GPAD1	LPAD2	LPAD1
Initial value	0	0	0	0	1	1	1	1

B15–B4: Reserved bits. Do not change the initial values.

B3, B2: Output level control
These bits control the GPAD level for the echo canceller output gain.
(0, 1): +18 dB
(0, 0): +12 dB
(1, 1): +6 dB
(1, 0): 0 dB

B1, B0: Input level control
These bits control the LPAD level for the echo canceller input loss.
(0, 1): –18 dB
(0, 0): –12 dB
(1, 1): –6 dB
(1, 0): 0 dB

D. Internal data memory for controlling EC0 Comfort Noise generation function (EC0_CN_CONT)
Initial value: 0003h (Comfort Noise generation function enabled)
By writing 0000h to this internal data memory, the comfort noise generation function of EC0 will be disabled. If center clip control and attenuator control are enabled, write 0003h to this internal data memory in order to enable the comfort noise generation function. On the other hand, if center clip control and attenuator control are disabled, write 0000h to this internal data memory in order to disable the comfort noise generation function. The initial values of both center clip control and attenuator control are set to disable. If center clip control and attenuator control will not be used, write 0000h to this internal data memory.

E. Precautions in using the echo canceller

E-1
In the echo path, make sure that the echo signal does not cause saturation, waveform distortion, etc., in the external amplifier, etc. The echo attenuation becomes poor if any saturation or waveform distortion occurs.

E-2
Make the settings so that the echo return loss (E.R.L.) is attenuating. Further, it is recommended to use the GLPAD function if the E.R.L. is set to be amplified. The echo attenuation gets deteriorated seriously if the E.R.L. is set to be amplified.
The E.R.L. is the attenuation (loss) of echo amount from the echo canceller output (Rout) to the echo canceller input (Sin).

E-3
When the echo path can change (such as during a reconnected call), it is recommended to carry out a reset using EC0_EN, PDNB, or DSP_RESET.

Echo Canceller 1

Echo canceller 1 is an echo canceller for CH1. The block diagram of echo canceller 1 is shown in Figure 54.

The echo canceller 1 has a delay time of 32 ms and is activated by setting the echo canceller 1 control register (EC1_EN) to "1". The operation setting of the echo canceller 1 is done mainly using internal data memories EC1_CR and EC1_GLPAD_CR.

The echo canceller 1 is also equipped with the Comfort Noise generation function that adds generated noise to Sout, according to the background noise amount of a signal input from Sin.

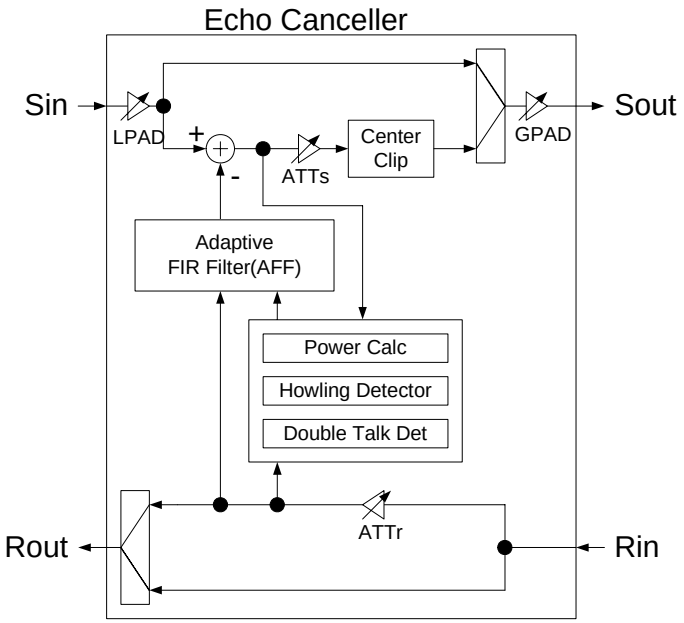


Figure 54 Block Diagram of Echo Canceller

A. EC1 control register (EC1_EN)

0 : Stops. The echo canceller is bypassed. (Initial value)

1 : Operates.

B. Internal data memory for EC1 control (EC1_CR)

Initial value : 0012h

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	THR	—	HLD	H DB	CLP	—	ATTB	—
Initial value	0	0	0	1	0	0	1	0

B15–B8 : Reserved bits. Do not change the initial values.

B7: Through mode control
1: Through mode
0: Normal mode (echo cancelling operation)
The data of Rin and Sin is output directly to Rout and Sout while retaining their respective echo coefficients. Further, during the through mode, the HLD, HDB, CLP, and ATTB functions are disabled.

B6: Reserved bit. Do not change the initial value.

B5: Coefficient update control
1: Coefficient is fixed
0: Coefficient is updated
This bit specifies whether the adaptive FIR filter (AFF) coefficient of the echo canceller will be updated or not. This function is enabled when THR is in the normal mode.

B4: Howling detector control
1: OFF
0: ON
This bit controls the function of detecting and removing howling which is generated in a hands-free acoustic system, etc. This function is enabled when THR is in the normal mode.

B3: Center clip control
1: ON
0: OFF
This bit controls the center clip function in which the Sout output is forcibly fixed to the minimum positive value when the Sout output of the echo canceller is –57 dBm0 or less and in the double talk state. This function is enabled when THR is in the normal mode.

B2: Reserved bit. Do not change the initial value.

B1: Attenuator control
1: ATT OFF
0: ATT ON
This bit selects the switching ON/OFF of the ATT function which prevents howling using the attenuators ATTs and ATTr provided at the Rin input and Sout output of the echo canceller. When only the Rin input is present, the attenuator (ATTs) of Sout will be inserted. When only the Sin input is present or when both the Sin and Rin inputs are present, the attenuator (ATTr) of Rin will be inserted. The respective attenuation values are 6 dB. This function becomes valid when THR is in the normal mode.

B0: Reserved bit. Do not change the initial value.

C. Internal data memory for EC1 GLPAD control (EC1_GLPAD_CR)
Initial value: 000Fh
This data memory controls the GLPAD within the echo canceller 1.

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	—	—	—	—	GPAD2	GPAD1	LPAD2	LPAD1
Initial value	0	0	0	0	1	1	1	1

B15–B4: Reserved bits. Do not change the initial values.

B3, B2: Output level control
These bits control the GPAD level for the echo canceller output gain.
(0, 1): +18 dB
(0, 0): +12 dB
(1, 1): +6 dB
(1, 0): 0 dB

B1, B0: Input level control
These bits control the LPAD level for the echo canceller input loss.
(0, 1): –18 dB
(0, 0): –12 dB
(1, 1): –6 dB
(1, 0): 0 dB

D. Internal data memory for controlling EC1 Comfort Noise generation function (EC1_CN_CONT)
Initial value: 0003h (Comfort Noise generation function enabled)
By writing 0000h to this internal data memory, the comfort noise generation function of EC1 will be disabled. If center clip control and attenuator control are enabled, write 0003h to this internal data memory in order to enable the comfort noise generation function. On the other hand, if center clip control and attenuator control are disabled, write 0000h to this internal data memory in order to disable the comfort noise generation function. The initial values of both center clip control and attenuator control are set to disable. If center clip control and attenuator control will not be used, write 0000h to this internal data memory.

E. Precautions in using the echo canceller

E-1
In the echo path, make sure that the echo signal does not cause saturation, waveform distortion, etc., in the external amplifier, etc. The echo attenuation becomes poor if any saturation or waveform distortion occurs.

E-2
Make the settings so that the echo return loss (E.R.L.) is attenuating. Further, it is recommended to use the GLPAD function if the E.R.L. is set to be amplified. The echo attenuation gets deteriorated seriously if the E.R.L. is set to be amplified.
The E.R.L. is the attenuation (loss) of echo amount from the echo canceller output (Rout) to the echo canceller input (Sin).

E-3
When the echo path can change (such as during a reconnected call), it is recommended to carry out a reset using EC1_EN, PDNB, or DSP_RESET.

Dial Pulse Detector 0 (DPDET0)

The dial pulse detector 0 can detect dial pulse signals input from the general-purpose input/output port GPIOB[0]. The dial pulse detector 0 is enabled when the DPDET0 activation control register (DPDET0_EN) is "1", the DPDET0 detection status register (DP0_DET) is set to "1" when a dial pulse signal is detected, and it is stored in the DPDET0 detection dial pulse count display register (DPDET0_D[7:0]). Read the dial pulse count detected when DP0_DET changes from "1" to "0" from DPDET0_D[7:0]. If a dial pulse signal is not detected, or DPDET0_EN is "0", DP0_DET is set to "0".

Figure 55 shows the dial pulse detection timing.

The dial pulse detector samples dial pulse signals input from GPIOB[0] at every 4 kHz, and detects dial pulses according to the setting values of the ON guard timer (DPDET0_ON_TIM) and the OFF guard timer (DPDET0_OFF_TIM). It can adjust the detection end time by setting the detection end timer (DPDET0_DETOFF_TIM).

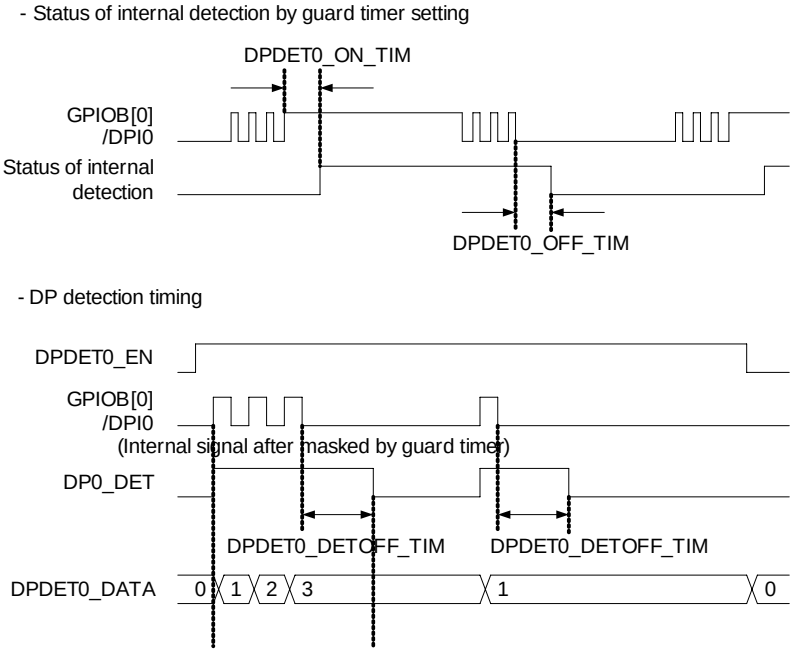


Figure 55 Dial Pulse Detection Timing

A. DPDET0 activation control register (DPDET0_EN)
- 0 : Stop (Initial value)
- 1 : Operate

B. DPDET0 detection status register (DP0_DET)
- 0 : No dial pulse signal detected (Initial value)
- 1 : Dial pulse signal detected

This bit is set to "1" after DPDET0_EN has been set when an edge of a signal input from the GPIOB[0] pin is detected. Further, if no edge is detected for a period set in DPDET0_DETOFF_TIM after an edge detection, this bit will be cleared automatically to "0".

C. DPDET0 polarity control register (DPDET0_POL)
Controls the polarity input from the GPIOB[0] pin.
0 : Does not invert polarity. (Initial value)
1 : Inverts polarity.

D. DPDET0 detected dial pulse count display register (DPDET0_D[7:0])
Initial value : 00h (State where no dial pulse detected)
Displays the number of detected dial pulses. This register is updated when an edge is detected.

E. Internal data memory for setting DPDET0 ON guard timer (DPDET0_ON_TIM)
Initial value : 0014h (5 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.250 ms
Example: 5 ms
5/0.250 = 20d = 0014h

Upper limit	: 8191.75 ms	(data: 7FFFh)
	: 5 ms	(data: 0014h)
Lower limit	: 0.250 ms	(data: 0001h)

F. Internal data memory for setting DPDET0 OFF guard timer (DPDET0_OFF_TIM)
Initial value : 0014h (5 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.250 ms
Example: 5 ms
5/0.250 = 20d = 0014h

Upper limit	: 8191.75 ms	(data: 7FFFh)
	: 5 ms	(data: 0014h)
Lower limit	: 0.250 ms	(data: 0001h)

G. Internal data memory for setting DPDET0 detection end timer (DPDET0_DETOFF_TIM)
Initial value : 01F4h (125 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 125 ms
125/0.250 = 0500d = 01F4h

Upper limit	: 8191.75 ms	(data: 7FFFh)
	: 125 ms	(data: 01F4h)
Lower limit	: 0.250 ms	(data: 0001h)

(Note)
To activate DPDET0, set GPIOB[0] to input in advance. Also, activate it after setting the level of input to GPIOB[0] to meet the following conditions by setting value(s) in the DPDET0 polarity control register (DPDET0_POL).

- DPDET0_POL = “0”, GPIOB[0] = “0”
- DPDET0_POL = “1”, GPIOB[0] = “1”

Dial Pulse Detector 1 (DPDET1)

The dial pulse detector 1 can detect dial pulse signals input from the general-purpose input/output port GPIOB[1]. The dial pulse detector 1 is enabled when the DPDET1 activation control register (DPDET1_EN) is "1", the DPDET1 detection status register (DP1_DET) is set to "1" when a dial pulse signal is detected, and it is stored in the DPDET1 detection dial pulse count display register (DPDET1_D[7:0]). Read the dial pulse count detected when DP1_DET changes from "1" to "0" from DPDET1_D[7:0]. If a dial pulse signal is not detected, or DPDET1_EN is "0", DP1_DET is set to "0".

Figure 56 shows the dial pulse detection timing.

The dial pulse detector samples dial pulse signals input from GPIOB[1] at every 4 kHz, and detects dial pulses according to the setting values of the ON guard timer (DPDET1_ON_TIM) and the OFF guard timer (DPDET1_OFF_TIM). It can adjust the detection end time by setting the detection end timer (DPDET1_DETOFF_TIM).

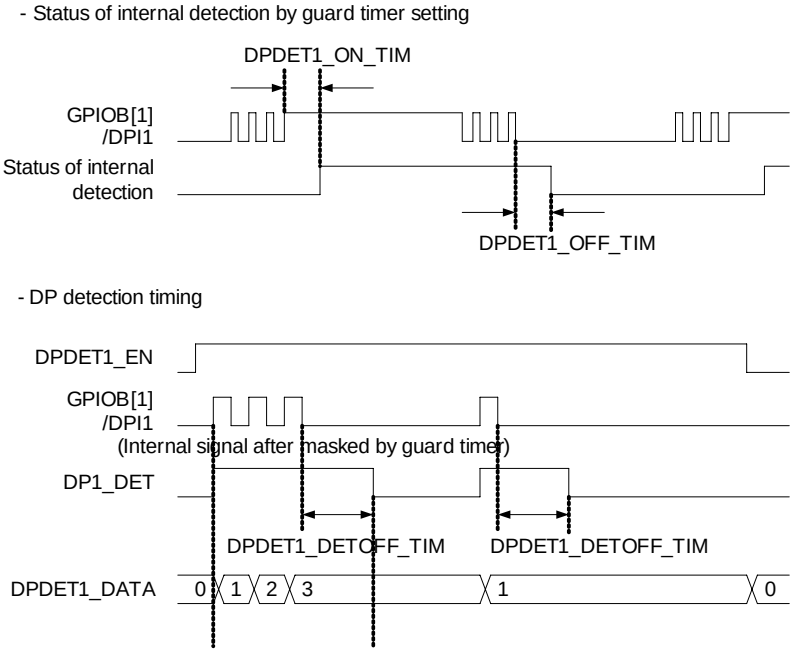


Figure 56 Dial Pulse Detection Timing

A. DPDET1 activation control register (DPDET1_EN)
- 0 :Stop (Initial value)
- 1 : Operate

B. DPDET1 detection status register (DP1_DET)
- 0 : No dial pulse signal detected (Initial value)
- 1 : Dial pulse signal detected

This bit is set to "1" after DPDET1_EN has been set when an edge of a signal input from the GPIOB[1] pin is detected. Further, if no edge is detected for a period set in DPDET1_DETOFF_TIM after an edge detection, this bit will be cleared automatically to "0".

C. DPDET1 polarity control register (DPDET1_POL)
Controls the polarity input from the GPIOB[1] pin.
0 : Does not invert polarity. (Initial value)
1 : Inverts polarity.

D. DPDET1 detected dial pulse count display register (DPDET1_D[7:0])
Initial value : 00h (State where no dial pulse detected)
Displays the number of detected dial pulses. This register is updated when an edge is detected.

E. Internal data memory for setting DPDET1 ON guard timer (DPDET1_ON_TIM)
Initial value : 0014h (5 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.250 ms
Example: 5 ms
5/0.250 = 20d = 0014h

Upper limit	: 8191.75 ms	(data: 7FFFh)
	: 5 ms	(data: 0014h)
Lower limit	: 0.250 ms	(data: 0001h)

F. Internal data memory for setting DPDET1 OFF guard timer (DPDET1_OFF_TIM)
Initial value : 0014h (5 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.250 ms
Example: 5 ms
5/0.250 = 20d = 0014h

Upper limit	: 8191.75 ms	(data: 7FFFh)
	: 5 ms	(data: 0014h)
Lower limit	: 0.250 ms	(data: 0001h)

G. Internal data memory for setting DPDET1 detection end timer (DPDET1_DETOFF_TIM)
Initial value : 01F4h (125 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 125 ms
125/0.250 = 0500d = 01F4h

Upper limit	: 8191.75 ms	(data: 7FFFh)
	: 125 ms	(data: 01F4h)
Lower limit	: 0.250 ms	(data: 0001h)

(Note)
To activate DPDET1, set GPIOB[1] to input in advance. Also, activate it after setting the level of input to GPIOB[1] to meet the following conditions by setting value(s) in the DPDET1 polarity control register (DPDET1_POL).

- DPDET1_POL = “0”, GPIOB[1] = “0”
- DPDET1_POL = “1”, GPIOB[1] = “1”

Dial Pulse Transmitter 0 (DPGEN0)

If the general-purpose input/output port GPIOA[0] is configured as its secondary function (DPO0: dial pulse output pin), the dial pulse transmitter 0 can output dial pulse signals.

The dial pulse transmitter 0 is enabled when the DPGEN0 transmission control register (DPGEN0_EN) is "1", and outputs dial pulse signals for the number of pulses set in the DPGEN0 dial pulse count setting register (DPGEN0_D[3:0]). Figure 57 shows the dial pulse output timing.

The speed of dial pulses can be chosen between 10 pps and 20 pps with the DPGEN0 speed control register (DPGEN0_PPS). The make ratio can also be adjusted by setting the duration of the break interval by DPGEN0_DUTY. Additionally, the output polarity of dial pulse signals can be changed by the DPGEN0 output polarity control register (DPGEN0_POL).

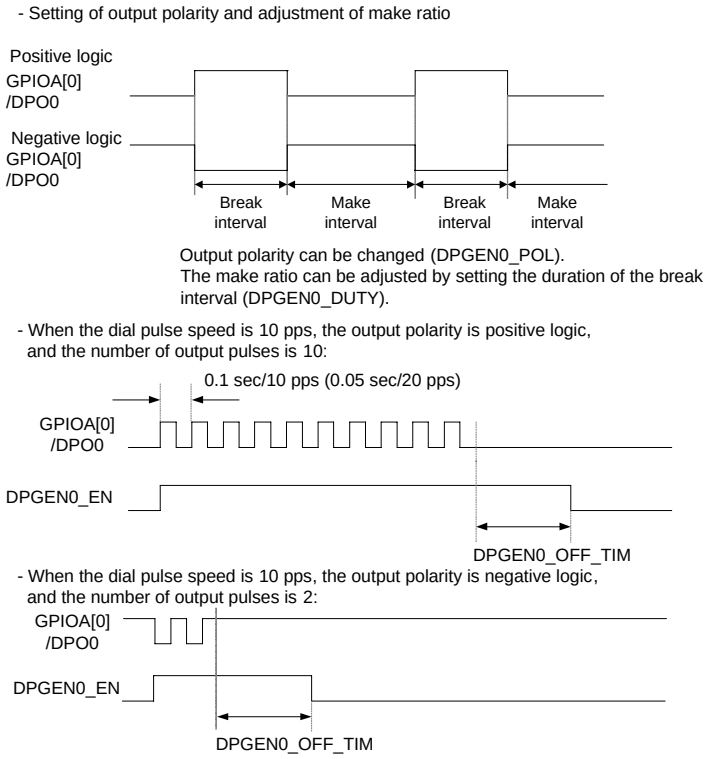


Figure 57 Dial Pulse Output Timing

A. DPGEN0 transmission control register (DPGEN0_EN)
- 0 : Stops transmission (Initial value)
- 1 : Carries out transmission

B. DPGEN0 dial pulse count setting register (DPGEN0_D[3:0])

Initial value : 0h
- Upper limit: 10 (data: Ah)
- Lower limit: 1 (data: 1h)

C. DPGEN0 speed control register (DPGEN0_PPS)
0 : 10 pps (Initial value)
1 : 20 pps

D. DPGEN0 output polarity control register (DPGEN0_POL)
0 Positive logic (Low: Make interval, High: Break interval), Initial value
1 Negative logic (Low: Break interval, High: Make interval)

E. Internal data memory for DPGEN0 make ratio control (DPGEN0_DUTY)
Initial value : 0108h(33ms/10 pps, 16.5 ms/20 pps)
To set the time of the break interval, use the following formula:
For 20 pps, the time is a half of this setting value.

Equation: Break interval output time in ms/0.125 ms
Example: 33 ms
33/0.125 = 264d = 0108h

Upper limit	: 100 ms	(data: 0320h)
	: 33 ms	(data: 0108h)
Lower limit	: 0.125 ms	(data: 0001h)

F. Internal data memory for DPGEN0 output end control (DPGEN0_OFF_TIM)
Initial value : 03E8h(125 ms)
Use the following equation when controlling the end of output.
Equation: Output end time in ms/0.125 ms
Example: 125 ms
125/0.125 = 1000d = 03E8h

Upper limit	: 4095.875 ms	(data: 7FFFh)
	: 125 ms	(data: 03E8h)
Lower limit	: 0 ms	(data: 0000h)

(Note) Before activating DPGEN0 (DPGEN0_EN=1), be sure to set the following:

- Set the DPGEN0 output polarity control register (DPGEN0_POL).
  By this setting, the output level (initial value) of the dial pulse output pin will be as follows:
  When DPGEN0_POL = 0 (positive logic) : GPOA[0]/DPO0 = “0”
  When DPGEN0_POL = 1 (negative logic) : GPOA[0]/DPO0 = “1”
- After the above setting, set the primary/secondary function selection register of GPIOA[0] (GPFA[0]) to “1” to select the secondary function (dial pulse output pin).

Dial Pulse Transmitter 1 (DPGEN1)

If the general-purpose input/output port GPIOA[1] is configured as its secondary function (DPO1: dial pulse output pin), the dial pulse transmitter 1 can output dial pulse signals.

The dial pulse transmitter 1 is enabled when the DPGEN1 transmission control register (DPGEN1_EN) is "1", and outputs dial pulse signals for the number of pulses set in the DPGEN1 dial pulse count setting register (DPGEN1_D[3:0]). Figure 58 shows the dial pulse output timing.

The speed of dial pulses can be chosen between 10 pps and 20 pps with the DPGEN1 speed control register (DPGEN1_PPS). The make ratio can also be adjusted by setting the duration of the break interval by DPGEN1_DUTY. Additionally, the output polarity of dial pulse signals can be changed by the DPGEN1 output polarity control register (DPGEN1_POL).

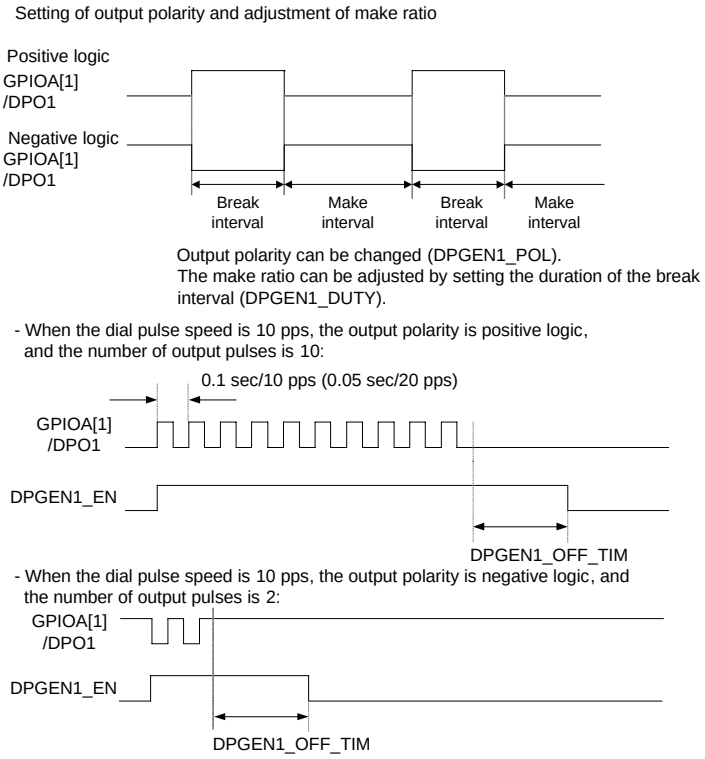


Figure 58 Dial Pulse Output Timing

A. DPGEN1 transmission control register (DPGEN1_EN)
- 0 : Stops transmission (Initial value)
- 1 : Carries out transmission

B. DPGEN1 dial pulse count setting register (DPGEN1_D[3:0])

Initial value : 0h
- Upper limit: 10 (data: Ah)
- Lower limit: 1 (data: 1h)

C. DPGEN1 speed control register (DPGEN1_PPS)
0 : 10 pps (Initial value)
1 : 20 pps

D. DPGEN1 output polarity control register (DPGEN1_POL)
0 Positive logic (Low: Make interval, High: Break interval), Initial value
1 Negative logic (Low: Break interval, High: Make interval)

E. Internal data memory for DPGEN1 make ratio control (DPGEN1_DUTY)
Initial value : 0108h(33ms/10 pps, 16.5 ms/20 pps)
To set the time of the break interval, use the following formula:
For 20 pps, the time is a half of this setting value.

Equation: Break interval output time in ms/0.125 ms
Example: 33 ms
33/0.125 = 264d = 0108h

Upper limit	: 100 ms	(data: 0320h)
	: 33 ms	(data: 0108h)
Lower limit	: 0.125 ms	(data: 0001h)

F. Internal data memory for DPGEN1 output end control (DPGEN1_OFF_TIM)
Initial value : 03E8h (125 ms)
Use the following equation when controlling the end of output.
Equation: Output end time in ms/0.125 ms
Example: 125 ms
125/0.125 = 1000d = 03E8h

Upper limit	: 4095.875 ms	(data: 7FFFh)
	: 125 ms	(data: 03E8h)
Lower limit	: 0 ms	(data: 0000h)

(Note) Before activating DPGEN1 (DPGEN1_EN=1), be sure to set the following:

- Set the DPGEN1 output polarity control register (DPGEN1_POL).
  By this setting, the output level (initial value) of the dial pulse output pin will be as follows:
  When DPGEN1_POL = 0 (positive logic) : GPOA[1]/DPO1 = “0”
  When DPGEN1_POL = 1 (negative logic) : GPOA[1]/DPO1 = “1”
- After the above setting, set the primary/secondary function selection register of GPIOA[1] (GPFA[1]) to “1” to select the secondary function (dial pulse output pin).

Outband Control 0 (OUTBAND_CONTROL0)

At the time of tone detection, mute processing is automatically performed inside the LSI when a DTMF signal is detected. The following describes the processing contents in speech codecs.

G.711 (μ-law): Mute processing is performed for the input data of a speech codec.
G.711 (A-law): Mute processing is performed for the input data of a speech codec.

Initial value : 0000h

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	—	—	—	—	—	TONE_TXDET0_OB_EN	ANS_TXDET0_OB_EN	DTMF0_DET_OB_EN
Initial value	0	0	0	0	0	0	0	0

B15–B3 : Reserved bits. Do not change the initial values.
B2 : TONE_TXDET0_OUTBAND_EN control
1 : ON (Mute processing is performed while TONE_TXDET0 is “1”.)
0 : OFF
B1 : ANS_TXDET0_OUTBAND_EN control
1 : ON (Mute processing is performed while ANS_TXDET0 is “1”.)
0 : OFF
B0 : DTMF0_DET_OUTBAND_EN control
1 : ON (Mute processing is performed while DTMF0_DET is “1”.)
0 : OFF

• Tone Leakage Time to the Transmit Buffer

The following shows the reference formula of the tone leakage time to the transmit buffer in each speech codec.

G.711: 0 ms + A + B
A: Detection delay time of each detector (ms)
Detection delay time A of each detector depends on conditions such as the input level frequency.
B: ON guard timer time of each detector (ms)

Example:
The leakage time to the transmit buffer when the detection delay time of the detector is set to approximately 30 ms and the ON guard timer is set to 20 ms is as follows:

G.711: 30 ms (A) + 20 ms (B) = Approx. 50 ms

Outband Control 1 (OUTBAND_CONTROL1)

At the time of tone detection, mute processing is automatically performed inside the LSI when a DTMF signal is detected. The following describes the processing contents in speech codecs.

G.711 (μ-law): Mute processing is performed for the input data of a speech codec.
G.711 (A-law): Mute processing is performed for the input data of a speech codec.

Initial value : 0000h

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	—	—	—	—	—	TONE_TXDET1_OB_EN	ANS_TXDET1_OB_EN	DTMF1_DET_OB_EN
Initial value	0	0	0	0	0	0	0	0

B15–B3 : Reserved bits. Do not change the initial values.
B2 : TONE_TXDET1_OUTBAND_EN control
1 : ON (Mute processing is performed while TONE_TXDET1 is “1”.)
0 : OFF
B1 : ANS_TXDET1_OUTBAND_EN control
1 : ON (Mute processing is performed while ANS_TXDET1 is “1”.)
0 : OFF
B0 : DTMF1_DET_OUTBAND_EN control
1 : ON (Mute processing is performed while DTMF1_DET is “1”.)
0 : OFF

• Tone Leakage Time to the Transmit Buffer

The following shows the reference formula of the tone leakage time to the transmit buffer in each speech codec.

G.711: 0 ms + A + B
A: Detection delay time of each detector (ms)
Detection delay time A of each detector depends on conditions such as the input level frequency.
B: ON guard timer time of each detector (ms)

Example:
The leakage time to the transmit buffer when the detection delay time of the detector is set to approximately 30 ms and the ON guard timer is set to 20 ms is as follows:

G.711: 30 ms (A) + 20 ms (B) = Approx. 50 ms

Timer (TIMER)

This is a 16-bit up-counter timer. When the timer control register (TIM_EN) is set to "1", the timer counter starts incrementing at every 125 μs. When the timer count value (TIM_COUNT) matches the timer data set value (TIM_DATA), the timer counter value will be reset to "0000h" and the timer starts incrementing again.

A. Timer control register (TIM_EN)
The timer starts incrementing when this bit is set to "1".
When set to "0", it stops incrementing and the counter value will be cleared.
0: Stops counting (Initial value)
0: Starts counting

B. Internal data memory for timer count indication (TIM_COUNT)
Initial value: 0000h

C. Internal data memory for setting the timer data (TIM_DATA)
Initial value: FFFFh
Upper limit : 8192 ms (data: FFFFh)
Lower limit : 0.250 ms (data: 0001h)

Melody Generator (MGEN)

A block diagram of the melody generator is shown in Figure 59, and its operation is described below.

The MCU has a ROM embedded with tunes data (such as tempo, musical notes and musical scale), and can generate melodies by making various settings for, and performing various controls of, the internal data memories and control registers of this LSI. This LSI incorporates into it with an internal data memory for setting frequency data of 64 words and time data of 64 words at every three tracks. The MCU must convert musical scale to frequency (16 bits), convert tempo and musical notes to time (16 bits), and set them in internal data memories.

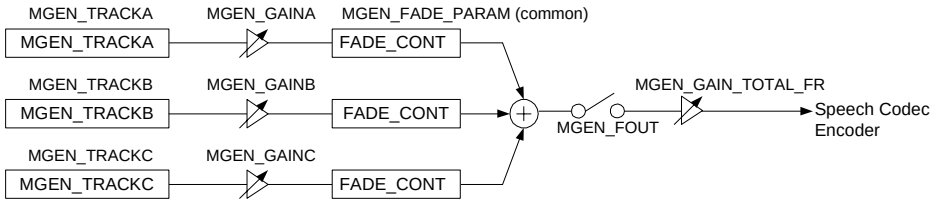


Figure 59 Block Diagram of Melody Generator

(Note) Restrictions While in the High-Speed Melody Read Mode

If the melody generation function is used, stop all the functions described below on the DSP side that generates melodies.

When activating a speech codec, do not activate it on the channel 1 side (SC_CH1EN=1).

- Tone generation function (TGEN0/TGEN1)
- Tone detection function (TONE_RXDET0/TONE_TXDET0, TONE_RXDET1/TONE_TXDET1)
- FSK generation function (FSKGEN0/FSKGEN1)
- Tone disabler detection function (TD_RXDET0/TD_TXDET0, TD_RXDET1/TD_TXDET1)
- DTMF detection function (DTMF_DET0/DTMF_DET1)
- Echo cancellers (EC0/EC1)
- Dial pulse detection function (DPDET0/DPDET1)
- Dial pulse transmission function (DPGEN0/DPGEN1)
- Timer (TIMER)

Perform melody regeneration control with this melody generator only after making a transition to the high-speed read mode shown below.

- High-Speed Melody Read Mode

  The mode transitions to the high-speed melody read mode (MGEN_FRFLAG = 1) when the melody generator high-speed read mode control register (MGEN_FREN) is set to “1”.

  In this high-speed melody read mode, melody data regenerated by the melody generator is encoded in the selected coding format, and a read request is issued to the MCU side. Because this read request is issued at a higher speed compared to a read request of speech data, melody data can be transferred to RAM or other storage on the MCU side in short time. Figure 60 shows a control flow of the high-speed melody read mode, and Figure 61 shows its control timing.

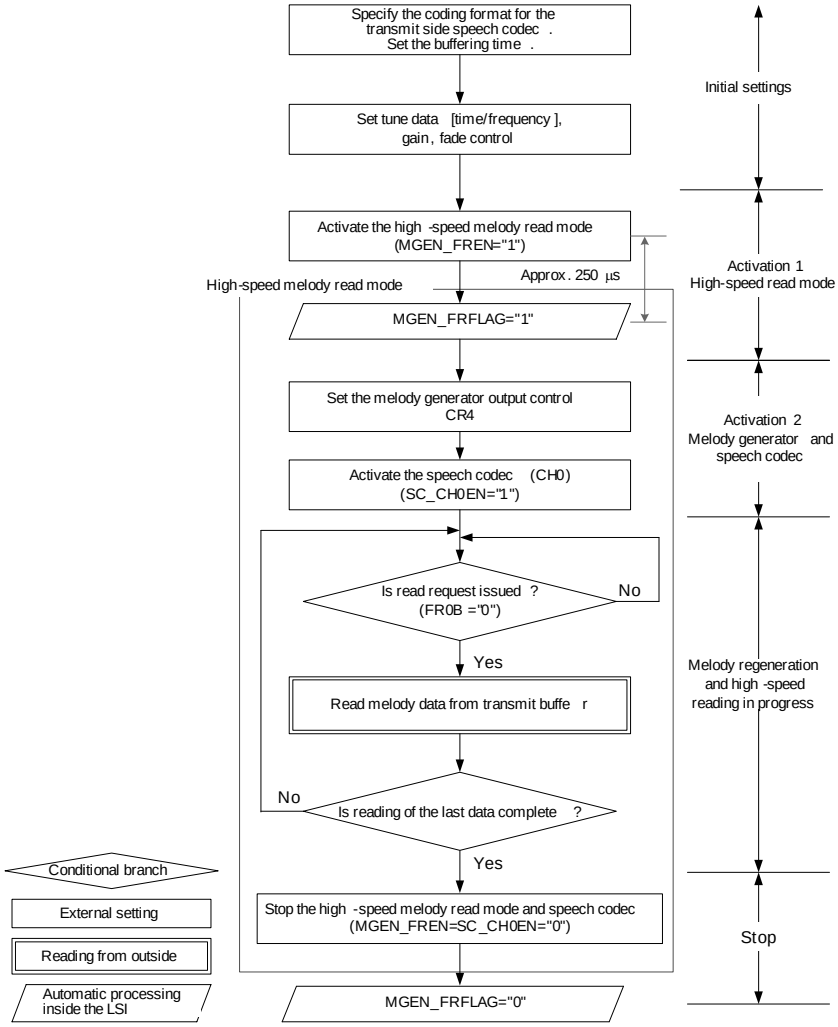


Figure 60 Control Flow in High-Speed Melody Read Mode

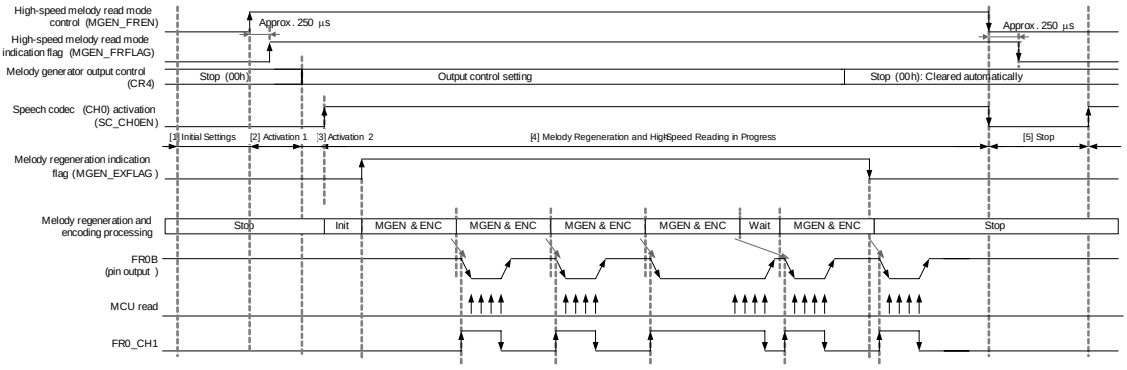


Figure 61 Control Timing in High-Speed Melody Read Mode

- Operational Description

[1] Initial Settings

- Make the following initial settings:
  - Initial settings to the melody generator, transmit side speech codec coding format TXSC_SEL[1:0] (G.711 µ-law/A-law), and transmit side buffering time TXBUF_TIM (10 ms/20 ms)

[2] Activation 1—Activate the High-Speed Melody Read Mode

- If the MGEN high-speed read mode control register (MGEN_FREN) is set to "1", the MGEN high-speed read mode display flag (MGEN_FRFLAG) will be set to "1" approximately 250 µs later, entering the high-speed melody read mode.

[3] Activation 2—Activate the Melody Generator and the Speech Codec

- Once MGEN_FRFLAG is set to "1", set the melody generator output control (CR4), and then activate (SC_CH0EN = "1") the speech codec (CH0).

[4] Melody Regeneration and High-Speed Reading in Progress

- With the start of melody regeneration, the MGEN execution flag indication register (MGEN_EXFLAG) is set to "1".
- Upon completion of regenerating melody data for 10 ms/20 ms and encode processing, a read request (FR0B = "1"→"0") is issued to the MCU side.
  Read melody data for 10 ms/20 ms from the transmit buffer for every read request.
  Read requests are repeated to the MCU side until the regeneration of tune data set on the melody generator is completed.
- Upon completion of the regeneration of tune data set on the melody generator, the melody generator output control setting (CR4) will automatically be cleared to 00h.
  Additionally, the MGEN execution flag indication register (MGEN_EXFLAG) will be set to "0" before issuing a read request for the last melody data upon completion of the regeneration and encode processing of tune data set on the melody generator.

(Notes)

- A read request (FR0B = 0) will not be cleared until a read by the MCU is completed.
- Also, in the high-speed melody read mode, a request to write receive data (FR1B = "1"→"0") will not be issued to the MCU side.
- Depending on set tune data, melody data to be regenerated may not be divided into 10 ms/20 ms units.
  In this case, the last melody data will be data for 10 ms/20 ms, which is made up of melody data regenerated by the melody generator added with silence data.

[5] Stop

- After the reading of the last melody data is completed, stop the speech codec (CH0) (SC_CH0EN = 0) and also stop the high-speed melody read mode (MGEN_FREN = 0). MGEN_FRFLAG is set to “0” by the stopping of the high-speed melody read mode.

- Reference Data—Estimated Time of Melody Data Regeneration for 20 ms and Speech Codec Encode Processing
  When speech cocec G.711 is selected: Approximately 1 ms

A. MGEN high-speed read mode control register (MGEN_FREN)
0 : Stops high-speed read mode
1 : Activates high-speed read mode

B. MGEN high-speed read mode notification flag (MGEN_FRFLAG)
0 : Other than during high-speed melody read mode
1 : During high-speed melody read mode

C. MGEN execution flag indication register (MGEN_EXFLAG)
0 : Being stopped
1 : Operating

D. TRACKm [m = A, B, C] output control register (MGEN_TmEN: m = A, B, C)
0 : Stop
1 : Output

E. Output control register for MGEN high-speed read mode (MGEN_FOUT)
0 : Stop
1 : Outputs melody to the encoder of the speech codec.

F. Internal memory for setting MGEN tune data

Tempo and musical notes (time)	64 Words × 3 Tracks =192 Words (including the END command)
Musical scale (frequency)	64 Words × 3 Tracks =192 Words (including the END command)

- Formats

MGEN_TRACKA_TIM = {T0}{T1}……{T62}{END}
MGEN_TRACKA_FREQ = {F0}{F1}……{F62}{END}

MGEN_TRACKB_TIM = {T0}{T1}……{T62}{END}
MGEN_TRACKB_FREQ = {F0}{F1}……{F62}{END}

MGEN_TRACKC_TIM = {T0}{T1}……{T62}{END}
MGEN_TRACKC_FREQ = {F0}{F1}……{F62}{END}

Internal data memory name	MGEN_TRACKn_TIM (n = A, B, C)
Initial value	xxxxh
Upper limit	7FFFh (4095.875 ms)
Lower limit	0001h (0.125 ms)
END command	FF00h: End (Single output)
Equation	T/0.125 (T is the time duration in ms)

Internal data memory name	MGEN_TRACKn_FREQ (n = A, B, C)
Initial value	xxxxh
Upper limit	6000h (3 kHz)
Lower limit	007Bh (15 Hz)
END command, silence frequency	0000h
Equation	Freq × 8.192 (Freq: desired frequency)

G. Internal data memory for MGEN gain control

Each output level of MGEN_TRACKm is –13.3 dBm0 at 0 dB with the initial value.
Use the following equation when changing the output level.

Internal data memory name	MGEN_GAINm (m = A, B, C)
Initial value	0080h (0 dB)
Upper limit	01FEh (Approx. +12 dB)
Lower limit	0020h (Approx. –12 dB)
Equation	128 × 10^ (X/20)
Example (–6 dB)	128 × 10^ (–6/20) = 64 = 0040h

H. Internal data memory for MGEN total gain control

Use the following equation when changing the output level.

Internal data memory name	MGEN_GAIN_TOTAL_FR
Initial value	0080h (0 dB)
Upper limit	3200h (Approx. +40 dB)
Lower limit	0001h (Approx. –40 dB)
MUTE	0000h (MUTE)
Equation	128 × 10^ (X/20)
Example (–6 dB)	128 × 10^ (–6/20) = 64 = 0040h

(Note)
Set the above output level so that the amplitude value and level after each track synthesis do not exceed the maximum amplitude of 1.3 Vp-p and the maximum level of 3.17 dBm0.

I. Internal data memory for MGEN fade control

Internal data memory name	MGEN_FADE_CONT_STEP (Fade-out starting time setting)
Initial value	0056h (86 sync= 10.75 ms)
Upper limit	01AEh (430 sync = 53.75 ms)
Lower limit	0008h (8 sync = 1ms)
Equation	43/–MI (MI: MGEN_FADE_CONT_MI)
Example (MI = –3 dB)	43/3 = 15 = 000Fh

Internal data memory name	MGEN_FADE_CONT_PL
Initial value	43CBh (+0.5 dB)
Upper limit	7FB2h (Approx. +6.0 dB)
Lower limit	40BEh (Approx. +0.1 dB)
Equation	16384 × 10^(X/20)
Example (+3 dB)	10^ (3/20) × 16384 = 23143d = 5A67h

Internal data memory name	MGEN_FADE_CONT_MI
Initial value	3C6Bh (–0.5 dB)
Upper limit	2013h (Approx. –6.0 dB)
Lower limit	3F44h (Approx. –0.1 dB)
Equation	16384 × 10^ (X/20)
Example (–3 dB)	10^ (–3/20) × 16384 = 11599d = 2D4Fh

(Note) To regenerate multiple tracks, it is necessary to make the time for each track identical.

Decode Output Start Offset Time Control (DEC_ONTIM)
Initial value : 0000h(0 ms)
Use the following equation when changing the decode output start offset time (tDECON).

Equation: “Decode output start offset time”ms/0.125 ms
Example: 5 ms
5/0.125 = 0040d = 0028h
Upper limit: 32 ms (data: 0100h)
Lower limit: 0.0 ms (data: 0000h)

(Note)
With G.711 (when the PLC function is enabled), silence data of approximately 3.75 ms is output and then decode output starts, after setting the decode output control register (DEC_OUTON) to “1”, regardless of the decode output start offset time. (Because of G.711 PLC algorithm delay)
In other words, note that the time until the actual decode output is started will be the time obtained by adding approximately 3.75 ms to the set value of the decode output start offset time in the internal data memory described above. Moreover, with G.711 (when the PLC function is disabled), decode output will start after the decode output start offset time set in the data memory described above.

Internal Data Memory for Setting the Start Address for Writing Multiple Words (START_ADDRESS)

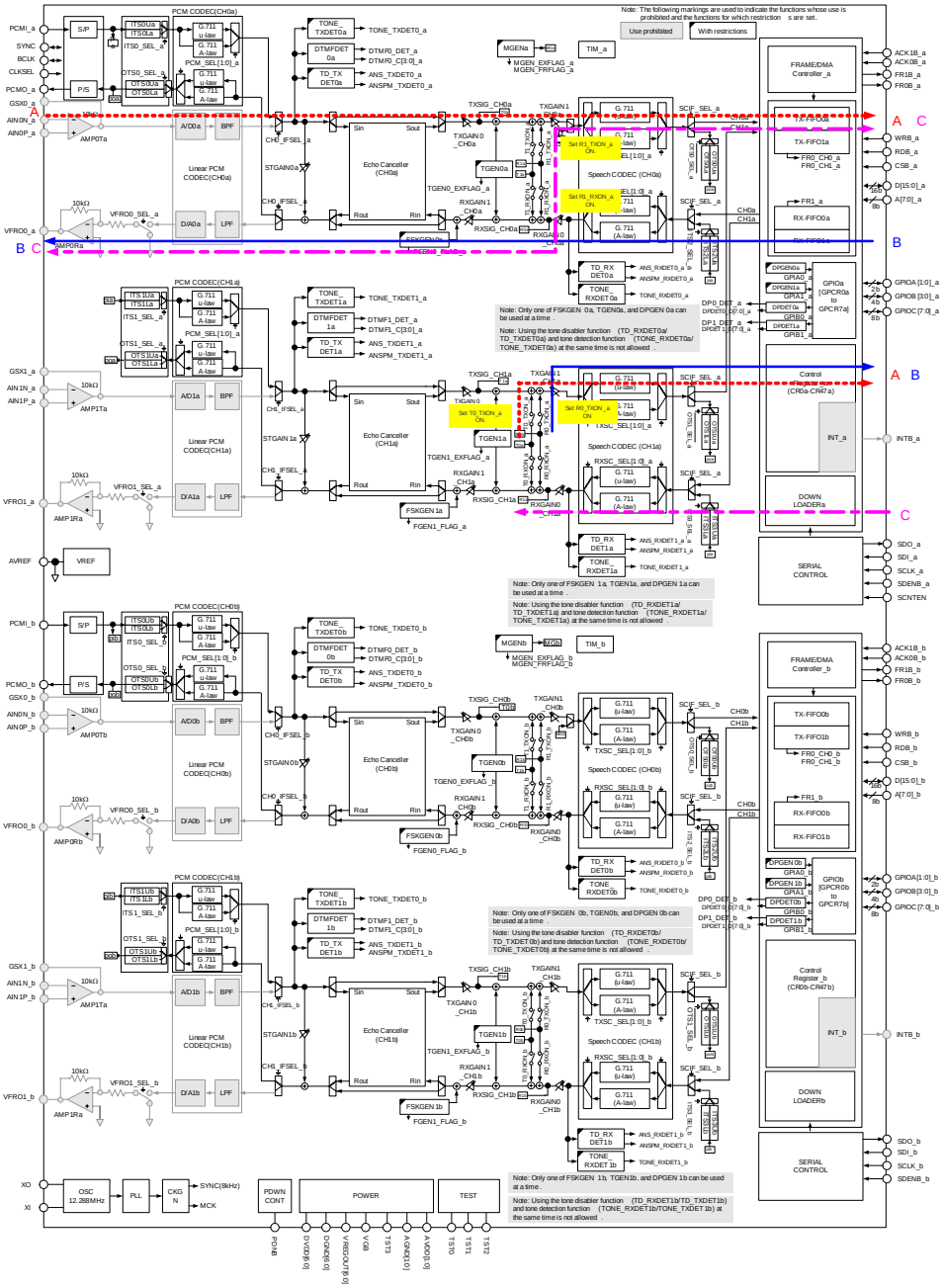
Set the start address of an internal data memory when a write to consecutive address spaces of the internal data memory will be performed according to the procedure shown in Figure 35. (Initial value: 0000h)

EXAMPLES OF APPLIED CONFIGURATIONS

This LSI can support three-way calls by control of an internal speech path switch. Configuration examples of three-way calls implementation are given on the next and succeeding pages.

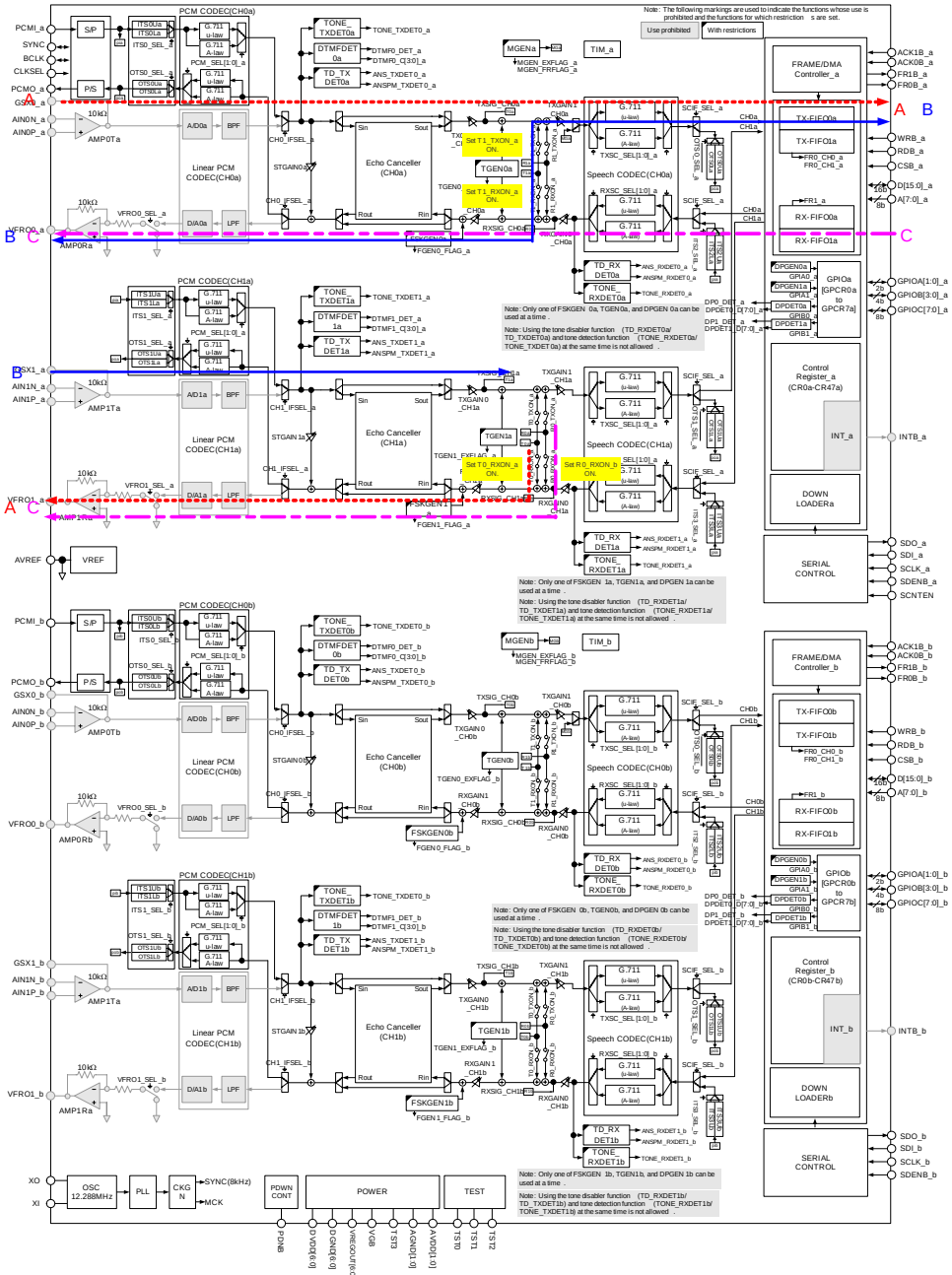
Configuration Example 1 (three-way calling: one person on the terminal side, two persons on the network side)

This configuration example shows a case of calling made by three persons: one person (Mr. A) on the terminal side, two persons (Mr. B and Mr. C) on the network side.
To make a three-way calling in this configuration, control the speech path switch using the following settings:
R1_TXON_a (CR44a-B5) = 1, R1_RXON_a (CR44a-B4) = 1
R0_TXON_a (CR44a-B1) = 1, T0_TXON_a (CR44a-B3) = 1



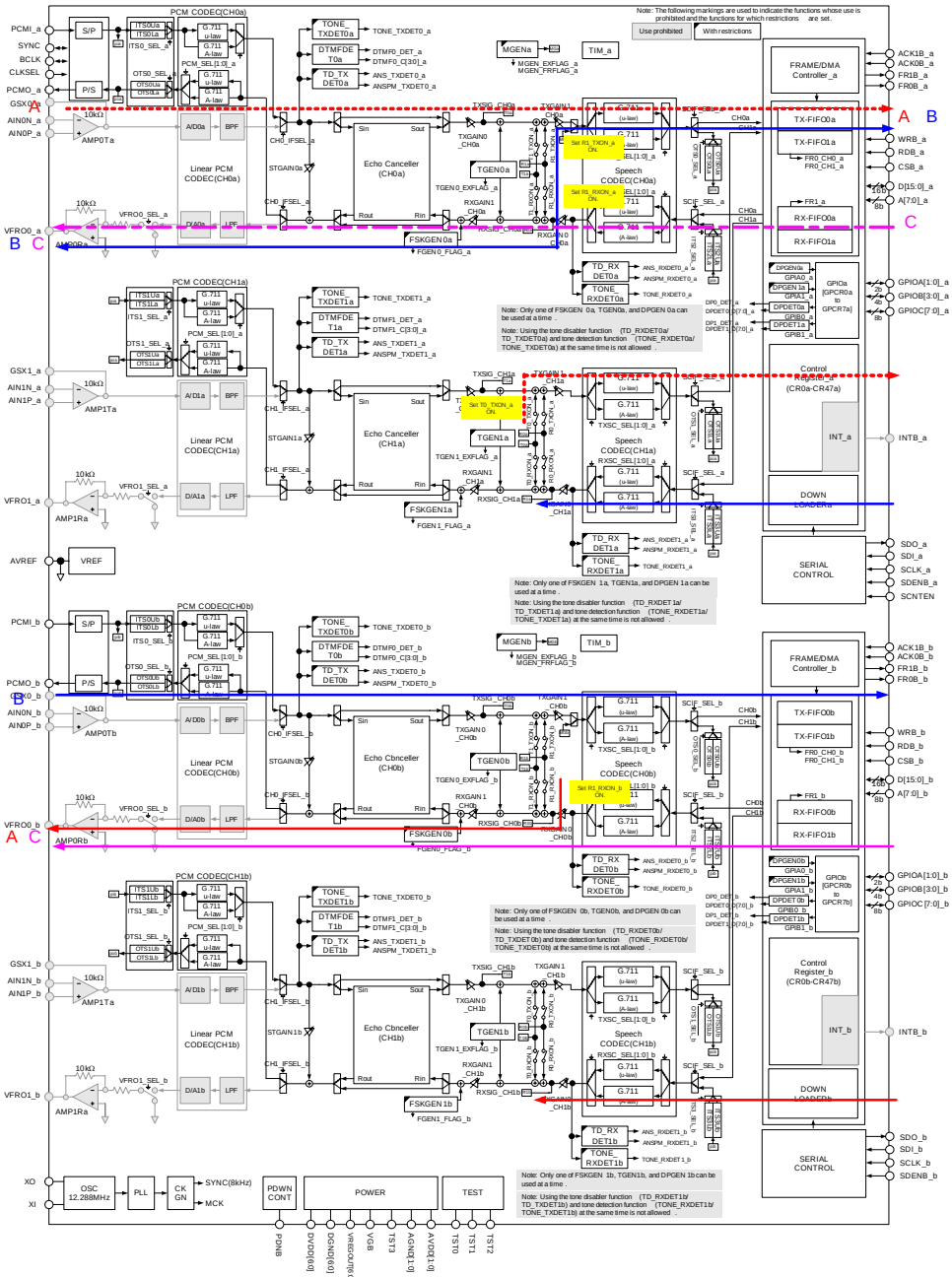
Configuration Example 2 (three-way calling: two persons on the terminal side [CH0a–CH1a], one person on the network side)

This configuration example shows a case of calling made by three persons: two persons (Mr. A and Mr. B) on the terminal side, one person (Mr. C) on the network side.
This configuration example shows a case where two persons on the terminal side are connected to CH0a and CH1a.
To make a three-way calling in this configuration, control the speech path switch using the following settings:
T1_TXON_a (CR44a-B7) = 1, T1_RXON_a (CR44a-B6) = 1
R0_RXON_b (CR44b-B0) = 1, T0_RXON_a (CR44a-B2) = 1



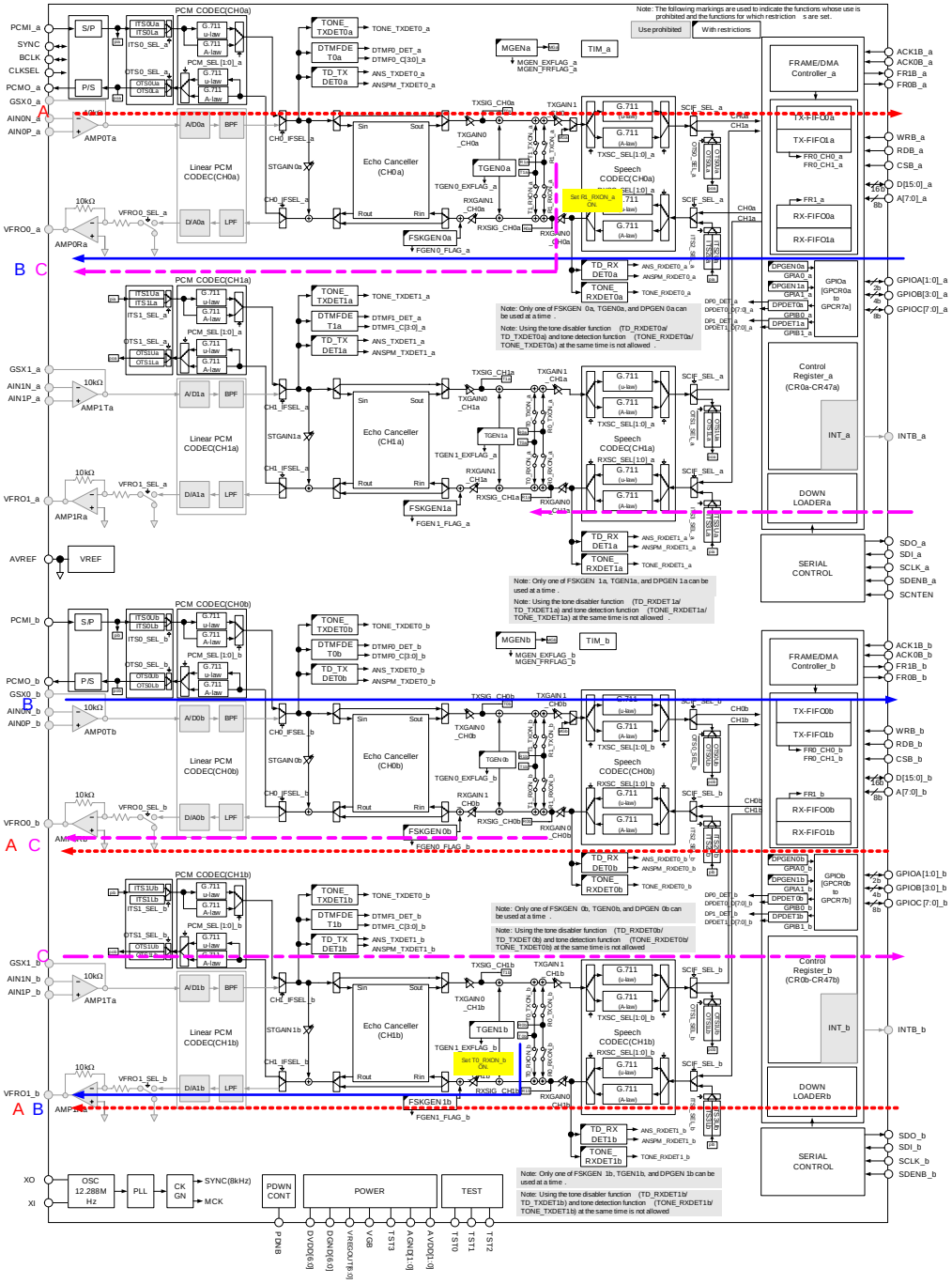
Configuration Example 3 (three-way calling: two persons on the terminal side [CHa–CHb], one person on the network side)

This configuration example shows a case of calling made by three persons: two persons (Mr. A and Mr. B) on the terminal side, one person (Mr. C) on the network side.
This configuration example shows a case where two persons on the terminal side are connected to CH0a and CH0b.
To make a three-way calling in this configuration, control the speech path switch using the following settings:
R1_TXON_a (CR44a-B5) = 1, R1_RXON_a (CR44a-B4) = 1
R1_RXON_b (CR44b-B4) = 1, T0_TXON_a (CR44a-B3) = 1



Configuration Example 4 (three-way calling: three persons on the terminal side)

This configuration example shows a case of calling made by three persons (Mr. A, Mr. B and Mr. C) on the terminal side.
To make a three-way calling in this configuration, control the speech path switch using the following settings:
R1_RXON_a (CR44a-B4) = 1, T0_RXON_b (CR44b-B2) = 1



NOTES ON USE

1. Only one of the FSK generation function, tone generation function (DTMF generation function) and dial pulse transmission function can be used at a time per channel. Note that using more than one generation function at the same time is not allowed. For activation control corresponding to each function described above, see the following table.

	DSP_A side		DSP_B side	
	CH0a	CH1a	CH0b	CH1b
Activation of FSK generation function	FGEN0_EN_a=1 (CR25a-B5)	FGEN1_EN_a=1 (CR26a-B5)	FGEN0_EN_b=1 (CR25b-B5)	FGEN1_EN_b=1 (CR26b-B5)
Activation of tone generation function	CR2a = xxh (Other than 00h: Depends on the output tone)	CR3a = xxh (Other than 00h: Depends on the output tone)	CR2b = xxh (Other than 00h: Depends on the output tone)	CR3b = xxh (Other than 00h: Depends on the output tone)
Activation of dial pulse transmission function	DPGEN0_EN_a=1 (CR27a-B6)	DPGEN1_EN_a=1 (CR28a-B6)	DPGEN0_EN_b=1 (CR27b-B6)	DPGEN1_EN_b=1 (CR28b-B6)

2. Using the 2100 Hz single tone/phase inversion detection function and the tone detection function for each channel at the same time is not allowed.
   For activation control corresponding to each function described above, see the following table.

	DSP_A side		DSP_B side	
	CH0a	CH1a	CH0b	CH1b
Activation of 2100 Hz single tone/ phase inversion detection function	TD_TXDET0EN_a=1 (CR25a-B3) TD_RXDET0EN_a=1 (CR25a-B4)	TD_TXDET1EN_a=1 (CR26a-B3) TD_RXDET1EN_a=1 (CR26a-B4)	TD_TXDET0EN_b=1 (CR25b-B3) TD_RXDET0EN_b=1 (CR25b-B4)	TD_TXDET1EN_b=1 (CR26b-B3) TD_RXDET1EN_b=1 (CR26b-B4)
Activation of tone detection function	TONE_TXDET0EN_a=1 (CR25a-B6) TONE_RXDET0EN_a=1 (CR25a-B7)	TONE_TXDET1EN_a=1 (CR26a-B6) TONE_RXDET1EN_a=1 (CR26a-B7)	TONE_TXDET0EN_b=1 (CR25b-B6) TONE_RXDET0EN_b=1 (CR25b-B7)	TONE_TXDET1EN_b=1 (CR26b-B6) TONE_RXDET1EN_b=1 (CR26b-B7)

3. If the melody generation function is used, stop all the functions described below on the DSP side that generates melodies. When activating a speech codec, do not activate it on the channel 1 side (SC_CH1EN=1).

- Tone generation function (TGEN0/TGEN1)
- Tone detection function (TONE_RXDET0/TONE_TXDET0, TONE_RXDET1/TONE_TXDET1)
- FSK generation function (FSKGEN0/FSKGEN1)
- Tone disabler detection function (TD_RXDET0/TD_TXDET0, TD_RXDET1/TD_TXDET1)
- DTMF detection function (DTMF_DET0/DTMF_DET1)
- Echo cancellers (EC0/EC1)
- Dial pulse detection function (DPDET0/DPDET1)
- Dial pulse transmission function (DPGEN0/DPGEN1)
- Timer (TIMER)

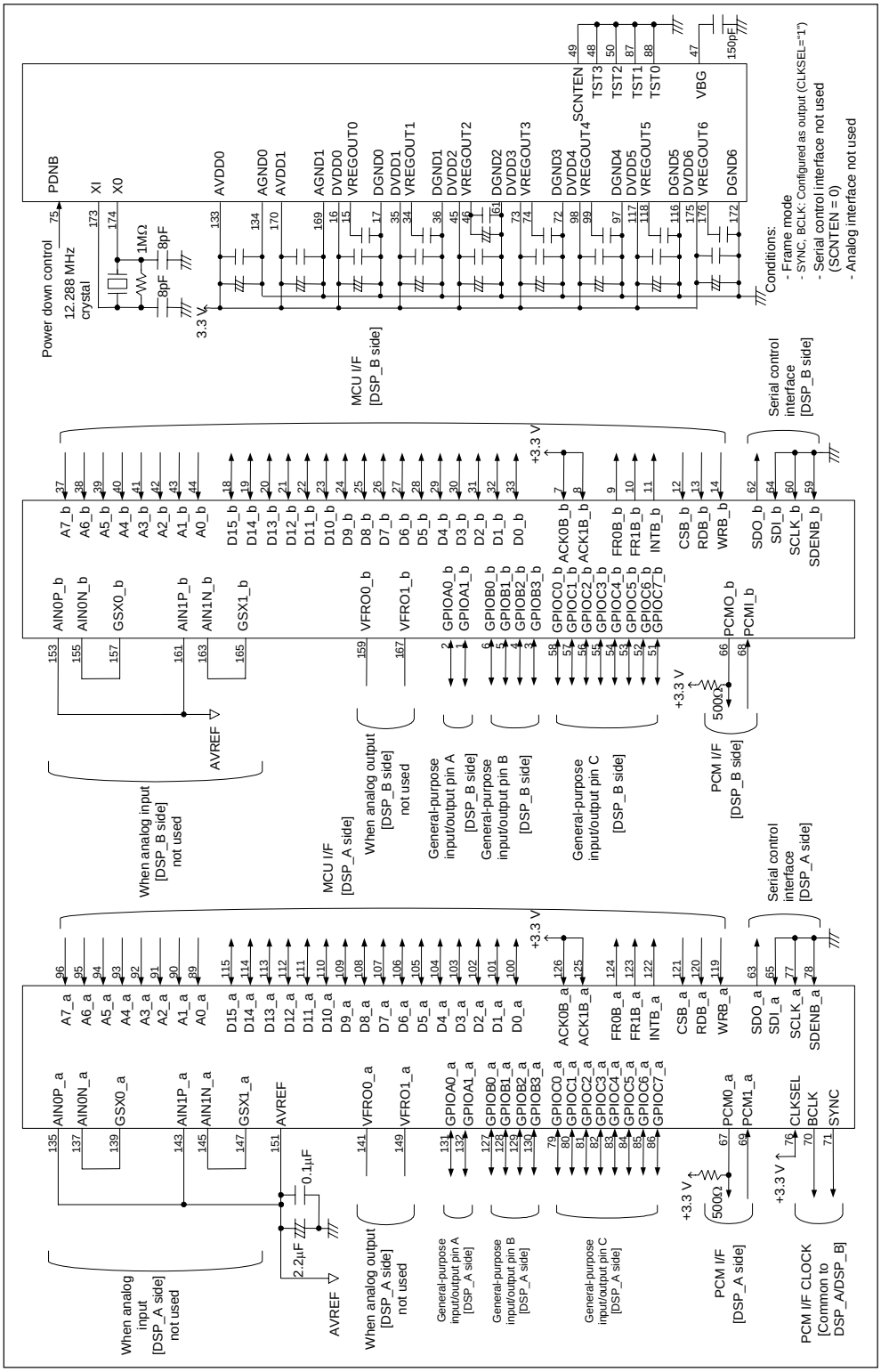
For activation control corresponding to each function described above, see the following table.

	DSP_A side		DSP_B side	
	CH0a	CH1a	CH0b	CH1b
Activation of tone generation function	CR2a=xxh (Other than 00h: Depends on the output tone)	CR3a=xxh (Other than 00h: Depends on the output tone)	CR2b=xxh (Other than 00h: Depends on the output tone)	CR3b=xxh (Other than 00h: Depends on the output tone)
Activation of tone detection function	TONE_TXDET0EN_a=1 (CR25a-B6) TONE_RXDET0EN_a=1 (CR25a-B7)	TONE_TXDET1EN_a=1 (CR26a-B6) TONE_RXDET1EN_a=1 (CR26a-B7)	TONE_TXDET0EN_b=1 (CR25b-B6) TONE_RXDET0EN_b=1 (CR25b-B7)	TONE_TXDET1EN_b=1 (CR26b-B6) TONE_RXDET1EN_b=1 (CR26b-B7)
Activation of FSK generation function	FGEN0_EN_a=1 (CR25a-B5)	FGEN1_EN_a=1 (CR26a-B5)	FGEN0_EN_b=1 (CR25b-B5)	FGEN1_EN_b=1 (CR26b-B5)
Activation of tone disabler function	TD_TXDET0EN_a=1 (CR25a-B3) TD_RXDET0EN_a=1 (CR25a-B4)	TD_TXDET1EN_a=1 (CR26a-B3) TD_RXDET1EN_a=1 (CR26a-B4)	TD_TXDET0EN_b=1 (CR25b-B3) TD_RXDET0EN_b=1 (CR25b-B4)	TD_TXDET1EN_b=1 (CR26b-B3) TD_RXDET1EN_b=1 (CR26b-B4)
Activation of DTMF detection function	DTMF0_EN_a (CR25a-B2)	DTMF1_EN_a (CR26a-B2)	DTMF0_EN_b (CR25b-B2)	DTMF1_EN_b (CR26b-B2)
Activation of echo canceller	EC0_EN_a (CR25a-B1)	EC1_EN_a (CR26a-B1)	EC0_EN_b (CR25b-B1)	EC1_EN_b (CR26b-B1)
Activation of dial pulse detection function	DPDET0_EN_a (CR45a-B0)	DPDET1_EN_a (CR45a-B2)	DPDET0_EN_b (CR45b-B0)	DPDET1_EN_b (CR45b-B2)
Activation of dial pulse transmission function	DPGEN0_EN_a=1 (CR27a-B6)	DPGEN1_EN_a=1 (CR28a-B6)	DPGEN0_EN_b=1 (CR27b-B6)	DPGEN1_EN_b=1 (CR28b-B6)
Activation of timer	TIM_EN_a=1 (CR45a-B5)		TIM_EN_b=1 (CR45b-B5)	
Activation of speech codec (CH1)	—	SC_CH1EN_a=1 (CR24a-B6)	—	SC_CH1EN_b=1 (CR24b-B6)

4. Selecting an analog interface is not allowed in this code. Also, selecting a PCM interface as a speech codec interface is not supported.
   Because of the functional restriction described above, be sure to set the following while in the initial mode.

	DSP_A side		DSP_B side	
	CH0a	CH1a	CH0b	CH1b
Selection of front end interface	CH0_IFSEL_a=1 (CR10a-B6)	CH1_IFSEL_a=1 (CR10a-B7)	CH0_IFSEL_b=1 (CR10b-B6)	CH1_IFSEL_b=1 (CR10b-B7)
Analog front end power down control	AFE0_PDN_a=1 (CR0a-B5)	AFE1_PDN_a=1 (CR0a-B6)	AFE0_PDN_b=1 (CR0b-B5)	AFE1_PDN_b=1 (CR0b-B6)

APPLICATION CIRCUIT

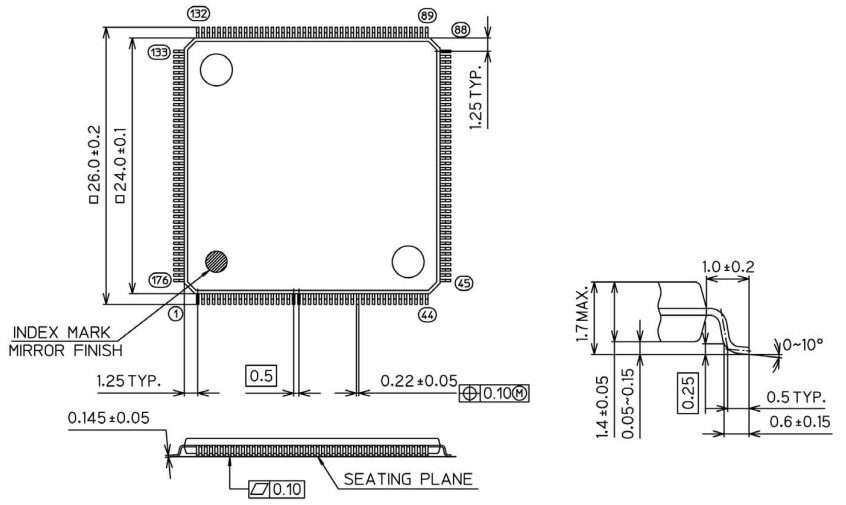


PACKAGE DIMENSIONS

176-Pin Plastic LQFP

(Unit: mm)

LQFP176-P-2424-0.50-ZK



Package material	Epoxy resin
Lead frame material	Cu alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	1.86 TYP.
Rev. No./Last Revised	1/Jan. 6, 2000

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL7224-001FULL-01	Sep. 28, 2005	–	–	Final edition 1

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1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

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